ISL6410, ISL6410A

Single Synchronous Buck Regulators with Integrated FET

FN9149
Rev 3.00
September 17, 2004

The ISL6410, ISL6410A are synchronous current-mode PWM regulators designed to provide a total DC-DC solution for microcontrollers, microprocessors, CPLDs, FPGAs, core processors/BBP/MAC, and ASICs. The ISL6410 should be selected for applications using 3.3V ±10% as an input voltage and the ISL6410A in applications requiring 5.0V ±10%.

These synchronous current mode PWM regulators have integrated N- and P-Channel power MOSFETs and provide pre-set pin programmable outputs. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and a reduced external component count. The operating frequency of 750kHz typical allows the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. A power good signal “PG” is generated when the output voltage falls outside the regulation limits. Other features include overcurrent protection and thermal overload shutdown. The ISL6410, ISL6410A are available in an MSOP 10 lead package.

Ordering Information

PART NUMBER*	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6410IR	-40 to 85	16 Ld 4x4 QFN	L16.4x4
ISL6410IRZ (Note)	-40 to 85	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6410IU	-40 to 85	10 Ld MSOP	M10.118
ISL6410IUZ (Note)	-40 to 85	10 Ld MSOP (Pb-free)	M10.118
ISL6410AIR	-40 to 85	16 Ld 4x4 QFN	L16.4x4
ISL6410AIRZ (Note)	-40 to 85	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6410AIU	-40 to 85	10 Ld MSOP	M10.118
ISL6410AIUZ (Note)	-40 to 85	10 Ld MSOP (Pb-free)	M10.118

*For tape and reel, add “-T”, “-TK” or “-T5K” suffix.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

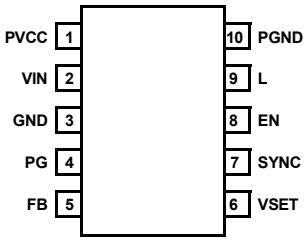
- Fully Integrated Synchronous Buck Regulator
- PWM Fixed Output Voltage Options
  - 1.8V, 1.5V or 1.2V with ISL6410 (VIN = 3.3V)
  - 3.3V, 1.8V or 1.2V with ISL6410A (VIN = 5.0V)
- Continuous Output Current 600mA
- Ultra-Compact DC-DC Converter Design
- Stable with Small Ceramic Output Capacitors
- High Conversion Efficiency
- Extensive Circuit Protection and Monitoring features
  - Overvoltage, UVLO
  - Overcurrent
  - Thermal Shutdown
- Available in MSOP and QFN packages
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Packaging Available

Applications

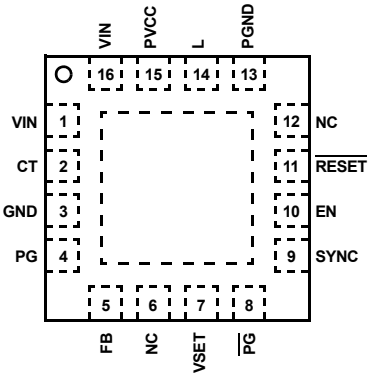
- CPUs, DSP, CPLDs, FPGAs
- ASICs
- DVD and DSL applications
- WLAN Cards
- Generic 5V to 3.3V Conversion

Pinouts

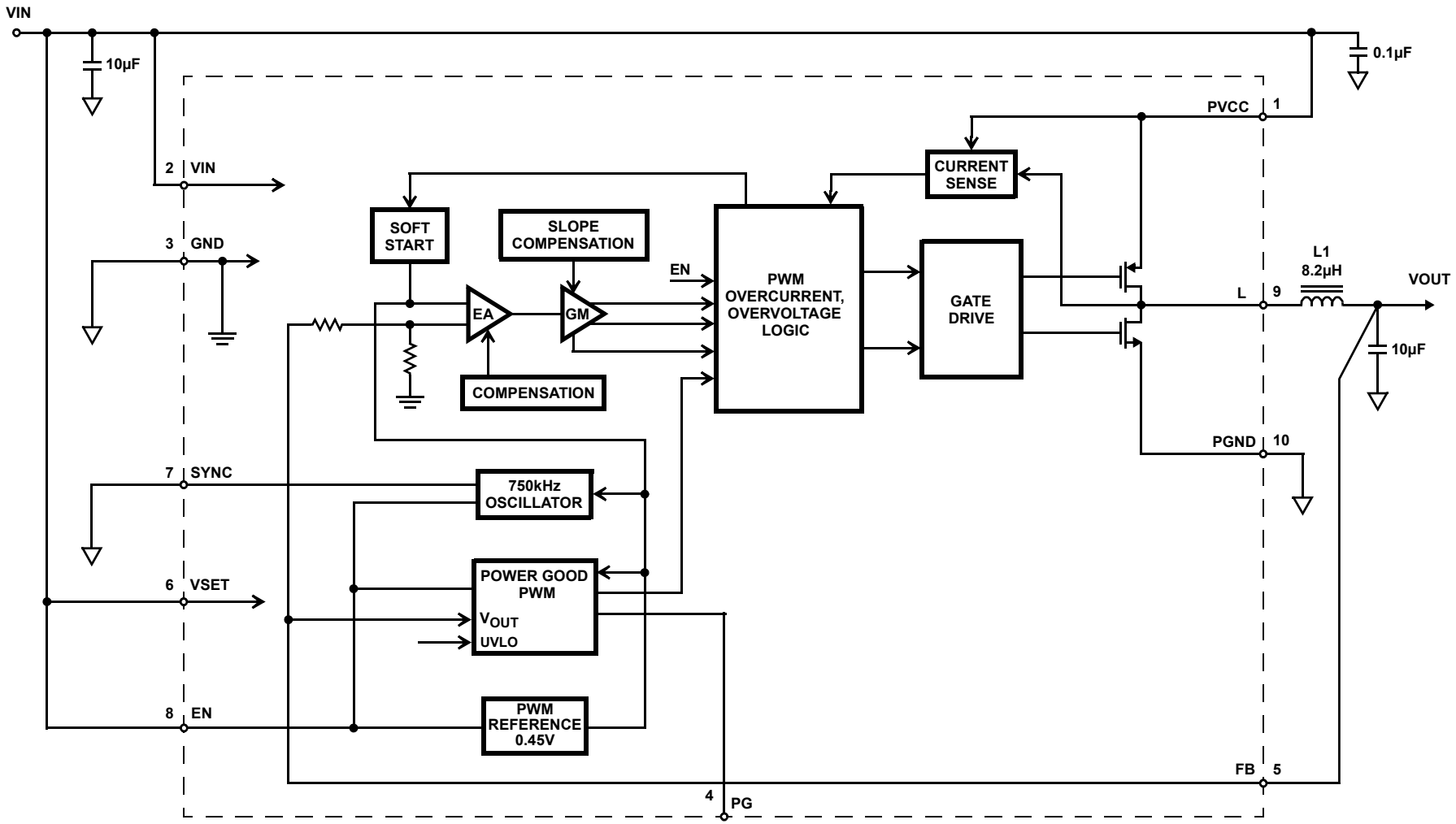
ISL6410 (MSOP)
TOP VIEW



ISL6410 (QFN)
TOP VIEW



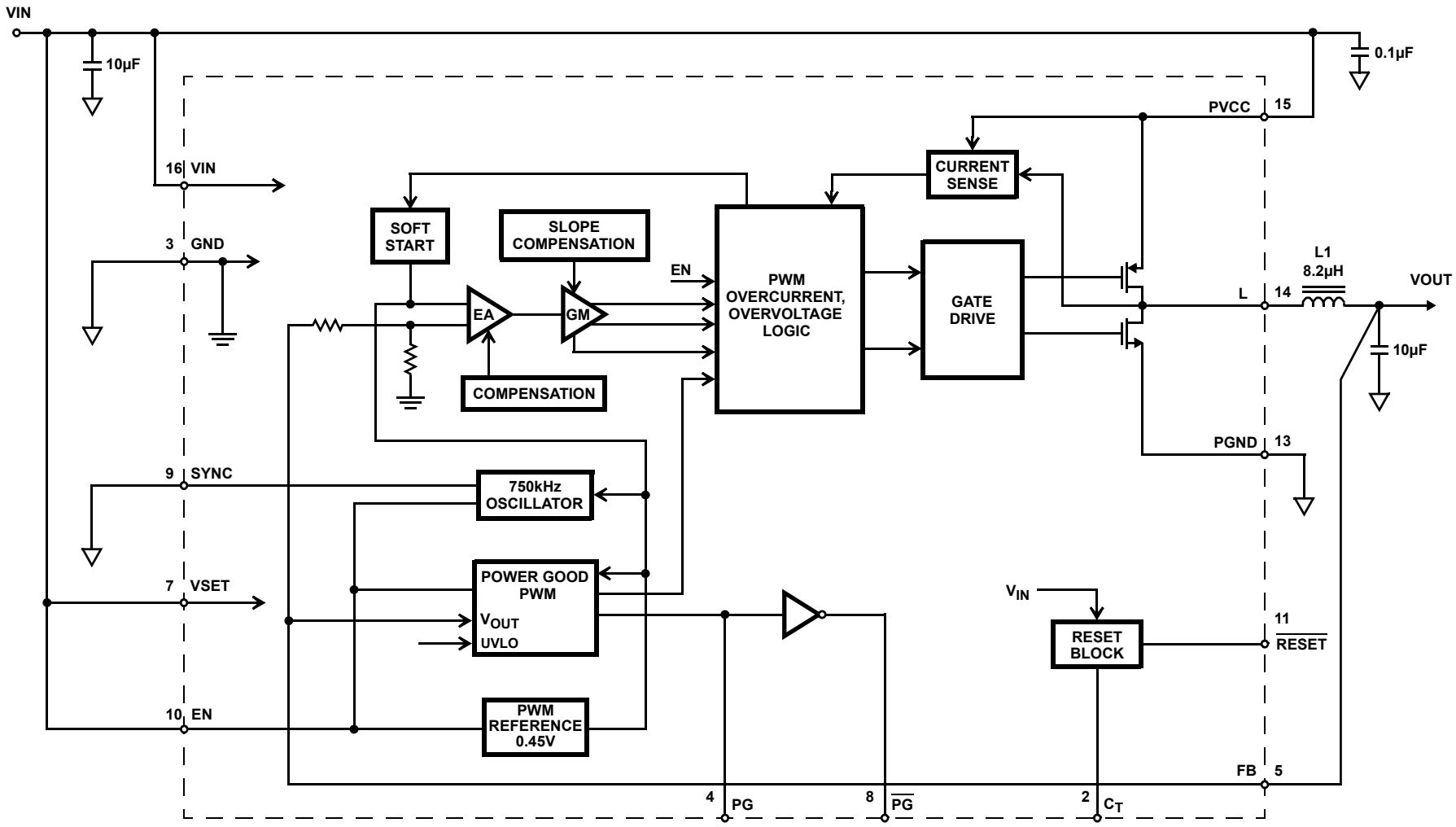
Functional Block Diagram for MSOP Version



NOTES:

1. VIN is 3.3V for ISL6410 and 5.0V for ISL6410A.
2. VSET in the above schematic is connected to VIN, so the VOUT is 1.8V for ISL6410 and 3.3V for ISL6410A.

Functional Block Diagram for QFN Version



NOTES:

1. VIN is 3.3V for ISL6410 and 5.0V for ISL6410A.
2. VSET in the above schematic is connected to VIN, so the VOUT is 1.8V for ISL6410 and 3.3V for ISL6410A.

Typical Application Schematics

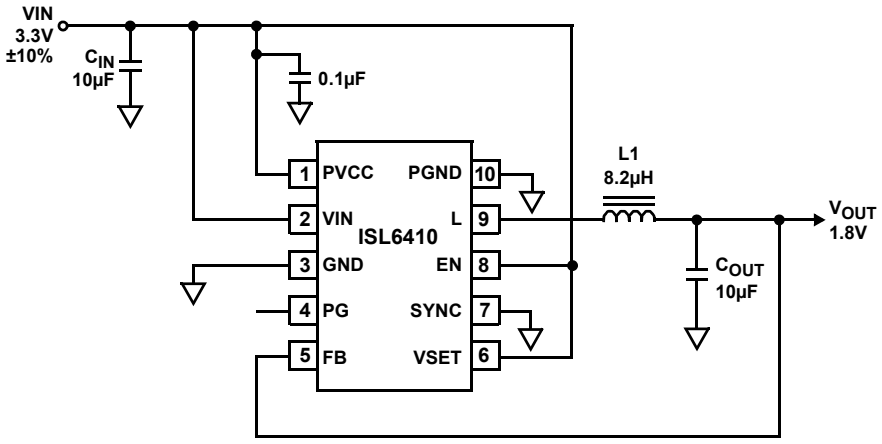


FIGURE 1. SCHEMATIC USING THE ISL6410 MSOP

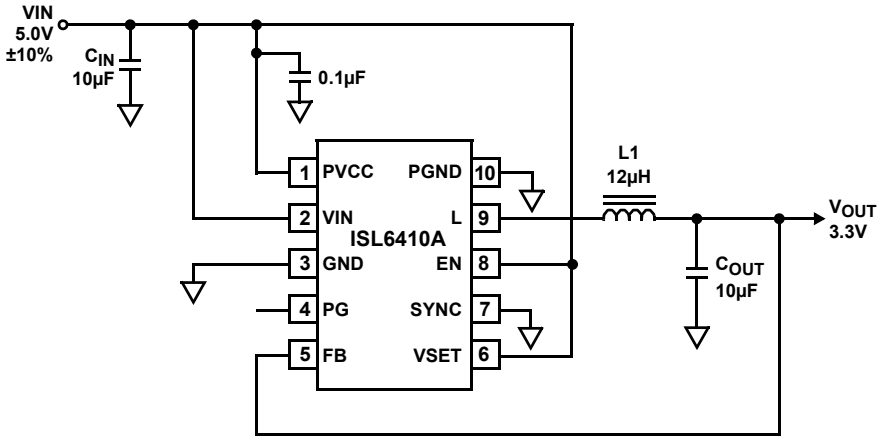


FIGURE 2. SCHEMATIC USING THE ISL6410A MSOP

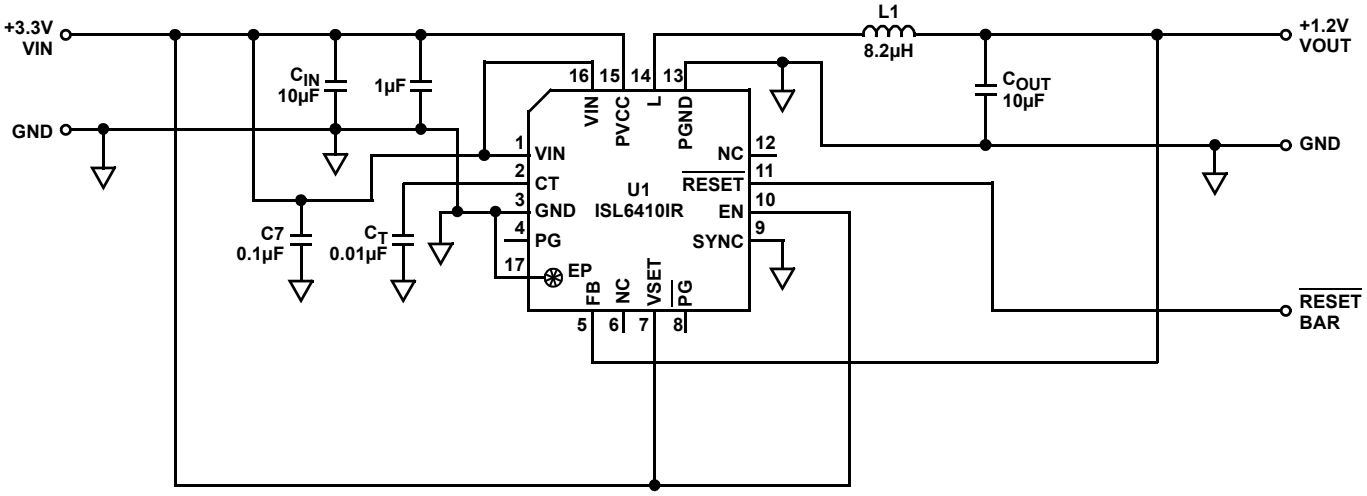


FIGURE 3. SCHEMATIC USING THE ISL6410 QFN

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . -0.3V to +6.0V
SYNC, FB, VSET & Enable Input (Note 3) . . . . -0.3V to VCC+0.3V
ESD Classification (Human Body Model) . . . . . Class 2

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
MSOP Package (Note 4)	128	NA
QFN Package (Notes 4, 5).	45	7.5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (10s, soldering . . . . . 260°C
Ambient Temperature Range. . . . . -40°C to 85°C
Junction Temperature Range. . . . . -40°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. All voltages are with respect to GND.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{IN} = 3.3V ±10% (ISL6410) or 5V ±10% (ISL6410A), T_A = 25°C (Note 6).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY					
Supply Voltage Range	VIN (ISL6410)	3.0	3.3	3.6	V
	VIN (ISL6410A)	4.5	5.0	5.5	V
Input UVLO Threshold	V_{TR} (ISL6410) Rising	2.62	2.68	2.73	V
	V_{TF} (ISL6410) Falling	2.53	2.59	2.64	V
	V_{TR} (ISL6410A) Rising	4.27	4.37	4.45	V
	V_{TF} (ISL6410A) Falling	4.1	4.22	4.32	V
Quiescent Supply Current	I_{OUT} = 0mA	-	2.3	-	mA
Shutdown Supply Current	EN = GND, T_A = 25°C	-	5	10	µA
	EN = GND, T_A = 85°C	-	10	15	µA
Thermal Shutdown Temperature (Note 7)	Rising Threshold	-	150	-	°C
Thermal Shutdown Hysteresis (Note 7)		-	20	25	°C
SYNCHRONOUS BUCK PWM REGULATOR					
Output Voltage	ISL6410, VSET = L	-	1.2	-	V
	ISL6410, VSET = H	-	1.8	-	V
	ISL6410, VSET = OPEN	-	1.5	-	V
	ISL6410A, VSET = L	-	1.2	-	V
	ISL6410A, VSET = H	-	3.3	-	V
	ISL6410A, VSET = OPEN	-	1.8	-	V
Output Voltage Accuracy	I_{OUT} = 3mA, T_A = -40°C to 85°C	-1.5	-	+1.5	%
Line Regulation	I_{OUT} = 3mA	-0.5	-	+0.5	%
Load Regulation	I_{OUT} = 3mA to 600mA	-1.5	-	+1.5	%
Maximum Output Current		-	-	600	mA
Peak Output Current Limit		700	-	1300	mA
PMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	230	-	mΩ
NMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	230	-	mΩ
Efficiency	I_{OUT} = 200mA, V_{IN} = 3.3V, V_O = 1.8V (ISL6410)	-	92	-	%

Electrical Specifications Recommended operating conditions unless otherwise noted. V_{IN} = 3.3V ±10% (ISL6410) or 5V ±10% (ISL6410A), T_A = 25°C (Note 6). **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Efficiency	I_{OUT} = 200mA, V_{IN} = 5.0V, V_O = 3.3V (ISL6410A)	-	93	-	%
Efficiency	I_{OUT} = 600mA, V_{IN} = 5.0V, V_O = 3.3V (ISL6410A)	-	91	-	%
Soft-Start Time	4096 Clock Cycles @ 750kHz	-	5.5	-	ms
OSCILLATOR					
Oscillator Frequency		620	750	860	kHz
Frequency Synchronization Range (f_{SYNC})	Clock signal on SYNC pin	500	-	1000	kHz
SYNC High Level Input Voltage	As % of VIN	70	-	-	%
SYNC Low Level Input Voltage	As % of VIN	-	-	30	%
Sync Input Leakage Current	SYNC = GND or V_{IN}	-1	-	1	µA
Duty Cycle of External Clock Signal (Note 7)		20	-	60	%
PGOOD (ISL6410 interfaces to 3.3V Logic, ISL6410A interfaces to 5.0V Logic)					
Rising Threshold	1mA minimum source/sink	+5.0	8.0	+10.5	%
Falling Threshold		-10.5	-8.0	-5.0	%
Rising/Falling Hysteresis		-	1	-	%
ENABLE					
EN High Level Input Voltage	As % of VIN	70	-	-	%
EN Low Level Input Voltage	As % of VIN	-	-	30	%
EN Input Leakage Current	EN = GND or V_{IN}	-1		1	µA
OVERVOLTAGE					
Overvoltage Threshold		27	30	33	%
RESET BLOCK SPECIFICATIONS					
RESET (reset released)	ISL6410, ISOURCE = 500µA, VIN = 2.90V	$0.8V_{IN}$	-	-	V
RESET (reset asserted)	ISL6410, ISINK = 1.2mA, VIN = 2.50V	-	-	0.3	V
RESET Rising Threshold	ISL6410	2.74	2.78	2.81	V
RESET Falling Threshold	ISL6410	2.72	2.77	2.79	V
RESET (reset released)	ISL6410A, ISOURCE = 800µA, VIN = 4.70V	$0.8V_{IN}$	-	-	V
RESET (reset asserted)	ISL6410A, ISINK = 3.2mA, VIN = 4.10V	-	-	0.4	V
RESET Rising Threshold	ISL6410A	4.5	4.58	4.64	V
RESET Falling Threshold	ISL6410A	4.47	4.55	4.61	V
RESET Threshold Hysteresis	ISL6410	-	20	-	mV
RESET Threshold Hysteresis	ISL6410A	-	30	-	mV
RESET Active Timeout Period (Note 8)	CT = 0.01mF	-	25	-	ms
V_{SET}					
V_{SET} High Level Input		V_{IN}-0.4V	-	-	V
V_{SET} Low Level Input		-	-	0.4	V
V_{SET} Open Level Input		-	$V_{IN}/2$	-	V

NOTES:

6. Specifications at -40°C and +85°C are guaranteed by design, not production tested.
7. Guaranteed by design, not production tested.
8. The RESET Timeout period is linear with C_T at a slope of 2.5ms/nF, thus a 10nF capacitor provides for 25ms.

Pin Description

VIN - Supply voltage for the IC. It is recommended to place a 1µF decoupling capacitor as close as possible to the IC.

GND - Small signal ground for the PWM controller stage. All internal control circuits are referenced to this pin.

PG - The Power good is an open-drain output. A pull-up resistor should be connected between PG and VIN. It is asserted active high when the output voltage reaches 94.5% of the nominal value.

FB - The Feedback pin is used to sense the output voltage, and should be connected to VOUT for normal operation.

VSET - This pin is used to program the output voltages. Refer to Table 1 below for details.

TABLE 1.

VSET	ISL6410 Vo	ISL6410A Vo
High	1.8V	3.3V
Open (NC)	1.5V	1.8V
Low	1.2V	1.2V

SYNC - This pin is used for synchronization. The converter switching frequency can be synchronized to an external CMOS clock signal in the range of (500kHz to 1MHz).

EN - A logic high enables the converter, logic low forces the device into shutdown mode reducing the supply current to less than 10µA at 25°C. This pin should be pulled up to VCC via a 10K resistor.

L - This pin is the drain junction of the internal power MOSFETs and is to be connected to the external inductor.

PGND - Power ground. Connect all power grounds to this pin.

PVCC - This pin provides the Input supply for the internal MOSFETs. It is recommended to place a 1µF decoupling capacitor as close as possible to the IC.

CT - Timing capacitor connection to set the 25ms minimum pulse width for the $\overline{\text{RESET}}$ signal.

$\overline{\text{RESET}}$ - The outputs of the reset supervisory circuit, which monitors VIN. The IC asserts these $\overline{\text{RESET}}$ signals whenever the supply voltage drops below a preset threshold and keeps it asserted for at least 25ms after VCC (VIN) has risen above the reset threshold. These outputs are push-pull. $\overline{\text{RESET}}$ is LOW when re-setting the microprocessor. The PWM will continue to operate until VIN drops below the UVLO threshold.

Functional Description

The ISL6410, ISL6410A is a synchronous buck regulator with integrated N- and P-channel power MOSFET and provides pre-set pin programmable outputs. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency of 750kHz typical allows the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG output indicates loss of regulation on PWM output.

The PWM is based on the peak current mode control topology with internal slope compensation. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. On exceeding a preset limit the high side switch is turned off causing the PWM comparator to trip. This occurs whenever the output voltage is in regulation or when the inductor current reaches the current limit. After a minimum dead time to prevent shoot through current, the low side N-channel MOSFET turns on and the current ramps down. As the clock cycle is completed, the low side switch turns off and the next clock cycle is initiated.

The control loop is internally compensated thus reducing the amount of external components.

The switch current is internally sensed and the maximum current limit is 1300mA peak.

Synchronization

The typical operating frequency for the converter is 750kHz. It is possible to synchronize the converter to an external clock frequency in the range of 500kHz to 1000kHz when an external signal is applied to SYNC pin. The device will automatically detect and synchronize to the rising edge of the first clock pulse. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues its operation without interruption. The switch over will be initiated if no rising edge triggers are present on the SYNC pin for a duration of four clock cycles.

Soft-Start

As the EN (Enable) pin goes high, the soft-start function will generate an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typically 5.5ms with 750kHz switching frequency. When the soft-start is completed, the error amplifier will be connected directly to the internal voltage reference.

Enable

Logic low on EN pin forces the PWM section into shutdown. In the shutdown mode all the major blocks of the PWM including power switches, drivers, voltage reference, and oscillator are turned off.

Undervoltage Lockout

An undervoltage lockout circuit prevents the converter from turning on when the voltage on VIN is less than the values specified in the Input UVLO Threshold section of the electrical specification.

Power Good

This output is asserted high when the PWM is enabled, and Vout is within 8.0% typical of its final value, and is active low outside this range. When disabled, the output turns active low. It is recommended to leave the PG pin unconnected when not used.

PWM Overvoltage and Overcurrent Protection

The PWM output current is sampled at the end of each PWM cycle, exceeding the overcurrent limit, causes a 4 bit up/down counter to increment by one LSB. A normal current state causes the counter to decrement by one LSB (the counter will not however “rollover” or count below 0000). When the PWM goes into overcurrent, the counter rapidly reaches count 1111 and the PWM output is shut down and the soft-start counter is reset. After 16 clocks the PWM output is enabled and the soft-start cycle is started.

If Vout exceeds the overvoltage limit for 32 consecutive clock cycles the PWM output is shut off and the soft-start cycle is initiated.

No Load Operation

If there is no load connected to the output, the converter will regulate the output voltage by allowing the inductor current to reverse for a short period of time.

Output Capacitor Selection

For best performance, a low ESR output capacitor is needed. Output voltages below 1.8V require a larger output capacitor and ESR value to improve the performance and stability of the converter. For 1.8V output applications, a ceramic capacitor of 10µF or higher value with ESR ≤50mΩ is recommended.

The RMS ripple current is calculated as:

$$I_{RMS(Co)} = Vo \times \frac{1 - \frac{Vo}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

L = the inductor value

f = the switching frequency

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR and the voltage ripple caused by charge and discharge of the output capacitor:

$$\Delta Vo = Vo \times \frac{1 - \frac{Vo}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Co \times f} + ESR \right)$$

Where the highest output voltage ripple occurs at the highest input voltage VIN.

TABLE 2. RECOMMENDED OUTPUT CAPACITORS

CAPACITOR VALUE	ESR (mΩ)	COMPONENT SUPPLIER	COMMENTS
10µF	<50	AVX 08056D106KAT2A	Ceramic

Input Capacitor Selection

The input current to the buck converter is pulsed, and therefore a low ESR input capacitor is required. This results in good input voltage filtering and minimizes the interference it causes to other circuits. The input capacitor should have a minimum value of 10µF and a higher value can be selected for improving input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = Io(max) \times \sqrt{\frac{Vo}{Vin} \times \left(1 - \frac{Vo}{Vin}\right)}$$

The worst case RMS ripple current occurs at D = 0.5 and is calculated as: Irms = Io/2.

D = Duty Cycle

Ceramic capacitors are preferred because of their low ESR value. They are also less sensitive to voltage transients when compared to tantalum capacitors. It is good practice to place the input capacitor as close as possible to the input pin of the IC for optimum performance.

Inductor Selection

The ISL6410 is an internally compensated device and hence a minimum of 8.2µH must be used for the ISL6410 and a minimum of 12µH for the ISL6410A. The selected inductor must have a low DC resistance and a saturation current greater than the maximum inductor current value can be calculated from the equations below

$$dIL = Vo \times \frac{1 - \frac{Vo}{Vin}}{L \times f}$$

$$IL\ max = Io\ max + \frac{dIL}{2}$$

where

dIL = the peak to peak inductor current
L = the inductor value
f = the switching frequency

ILmax = the max inductor current

TABLE 3. RECOMMENDED INDUCTORS

INDUCTOR VALUE	DCR (mΩ)	COMPONENT SUPPLIER
8.2µH	75	Coilcraft MSS6122-822MX
12µH	100	Coilcraft MSS6122-123MX

Layout Considerations

As in all switching power supplies, the layout is an important step in the design process, more so at high peak currents and switching frequencies. Improper layout practice will give rise to Stability and EMI issues. It is recommended that wide and short traces are used for the main current paths. The input capacitor should be placed as close as possible to the IC pins. This applies to the output inductor and capacitor as well. The analog ground, GND, and the power ground, PGND, need to be separated. Use a common ground node to minimize the effects of ground noise.

Performance Curves and Waveforms

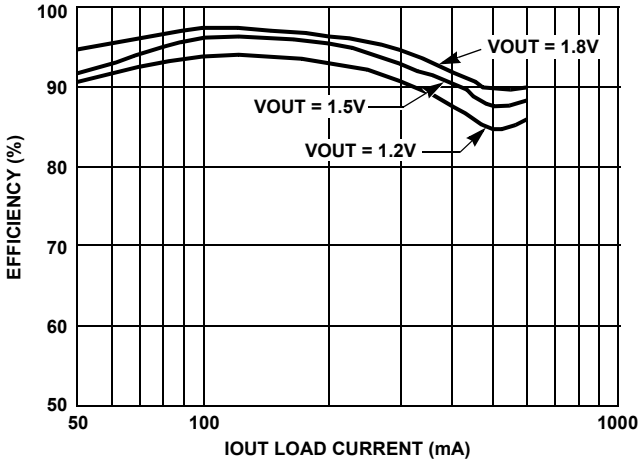


FIGURE 4. ISL6410 EFFICIENCY vs LOAD CURRENT

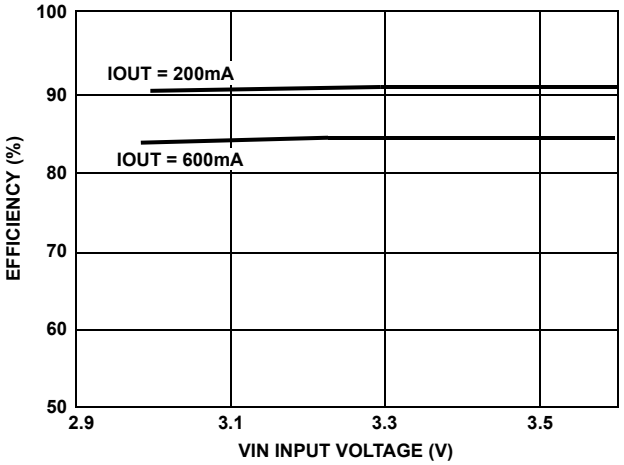


FIGURE 5. ISL6410 VIN vs EFFICIENCY

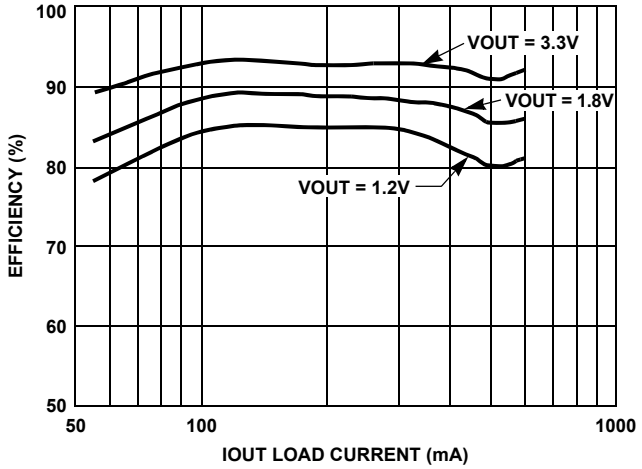


FIGURE 6. ISL6410A EFFICIENCY vs LOAD CURRENT

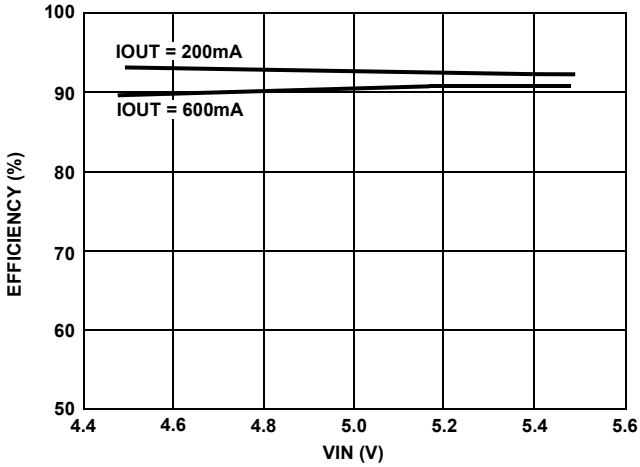


FIGURE 7. ISL6410A EFFICIENCY vs VIN

Performance Curves and Waveforms (Continued)

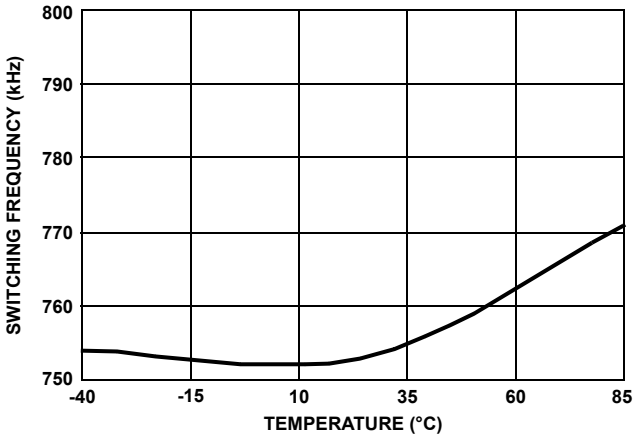


FIGURE 8. ISL6410 OSCILLATOR FREQUENCY vs TEMPERATURE

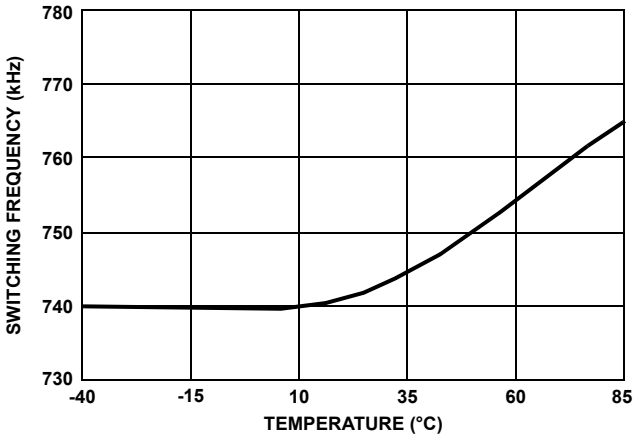


FIGURE 9. ISL6410A OSCILLATOR FREQUENCY vs TEMPERATURE

CH1 = Top, CH2 = Middle, CH4 = Bottom, where applicable

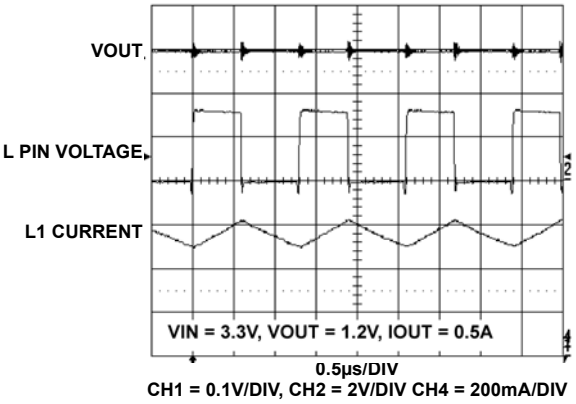


FIGURE 10. SWITCHING WAVEFORM FOR ISL6410

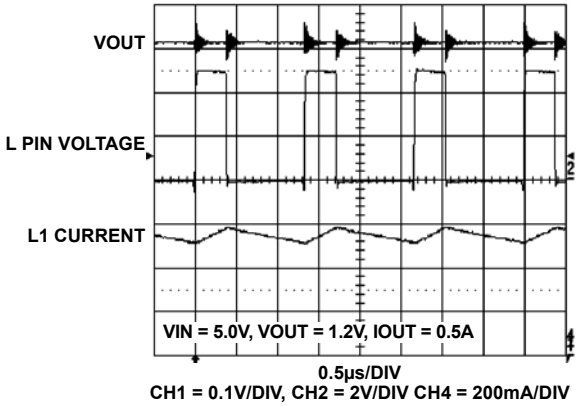


FIGURE 11. SWITCHING WAVEFORM FOR ISL6410A

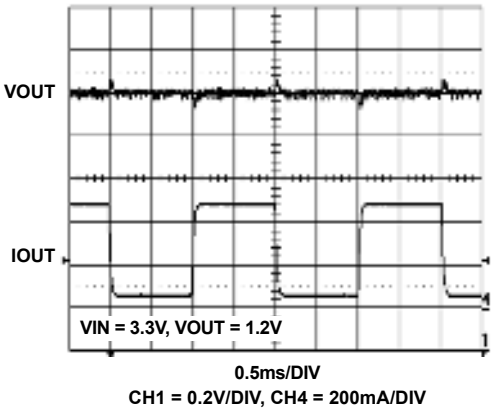


FIGURE 12. TRANSIENT LOAD WAVEFORM FOR ISL6410

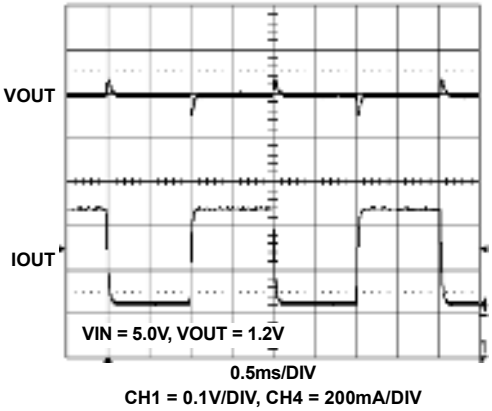


FIGURE 13. TRANSIENT LOAD WAVEFORM FOR ISL6410A

Performance Curves and Waveforms (Continued)

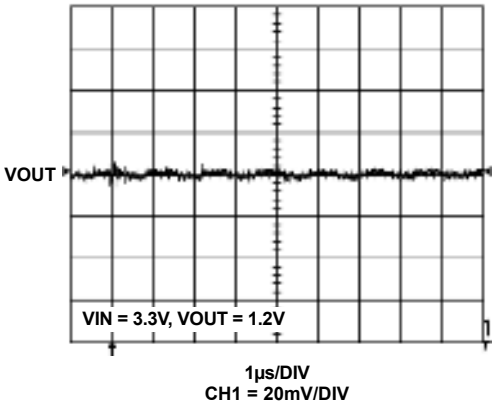


FIGURE 14. RIPPLE WAVEFORM FOR ISL6410

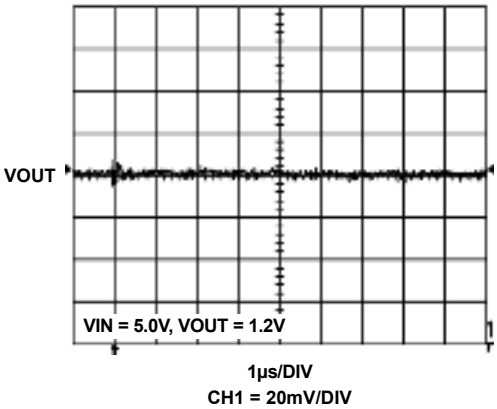


FIGURE 15. RIPPLE WAVEFORM FOR ISL6410A

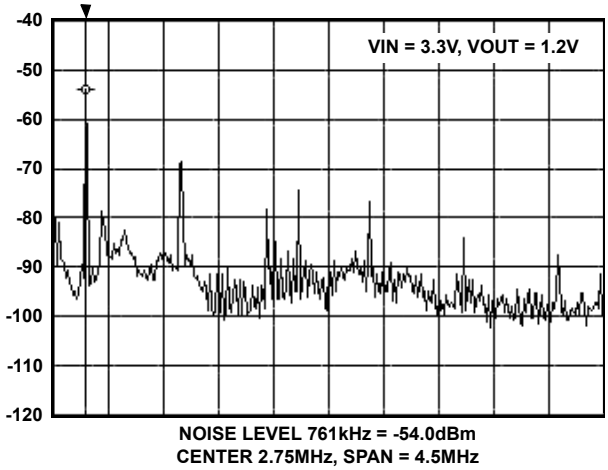


FIGURE 16. SWITCHING HARMONICS AND NOISE FOR ISL6410

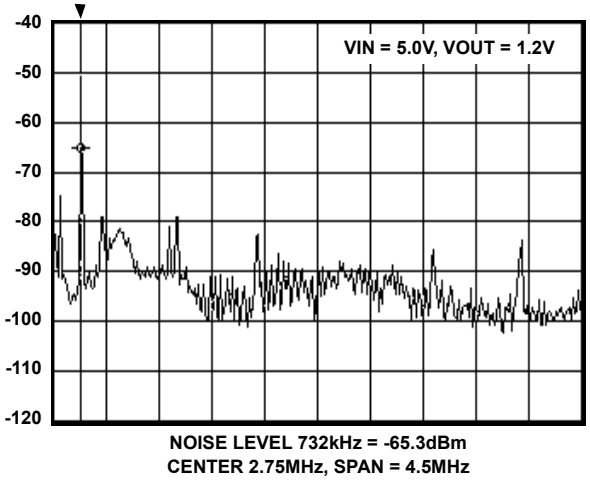


FIGURE 17. SWITCHING HARMONICS AND NOISE FOR ISL6410A

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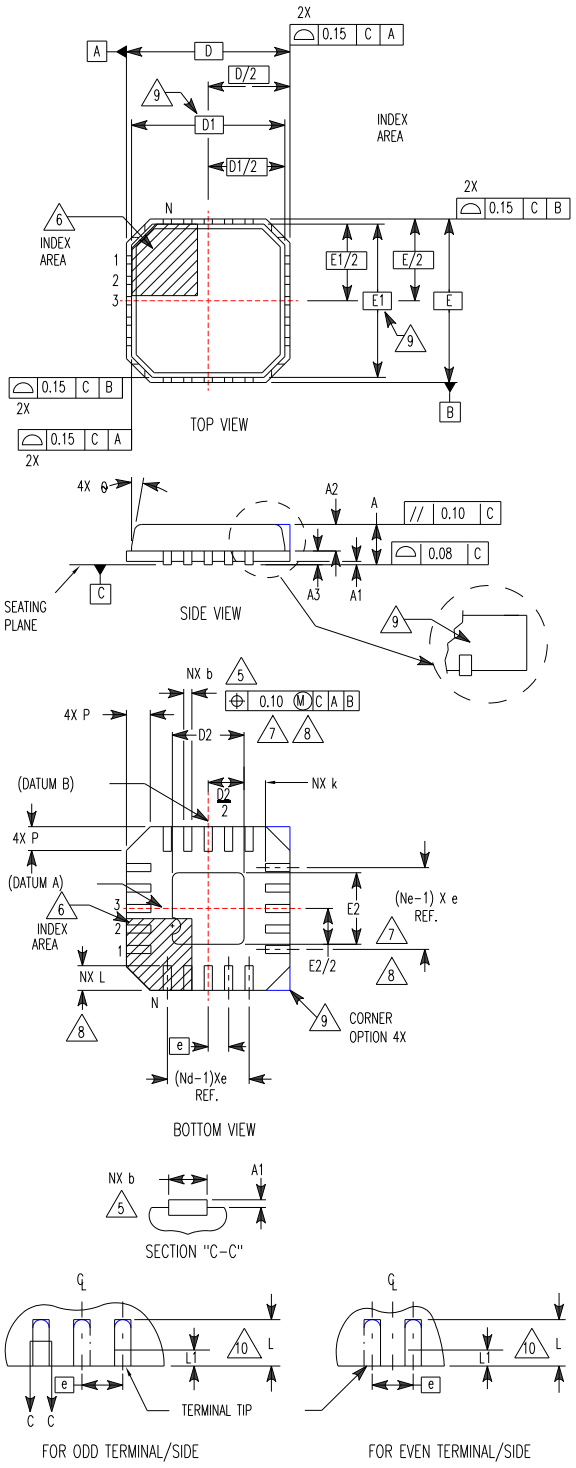
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Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

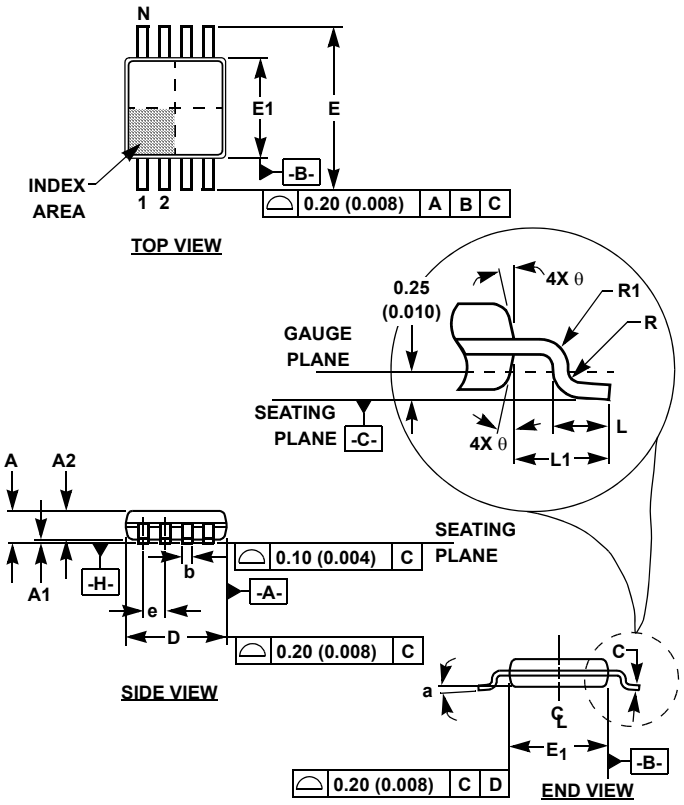
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

ISL6410, ISL6410A

Single Synchronous Buck Regulators with Integrated FET

FN9149
Rev 3.00
September 17, 2004

The ISL6410, ISL6410A are synchronous current-mode PWM regulators designed to provide a total DC-DC solution for microcontrollers, microprocessors, CPLDs, FPGAs, core processors/BBP/MAC, and ASICs. The ISL6410 should be selected for applications using 3.3V ±10% as an input voltage and the ISL6410A in applications requiring 5.0V ±10%.

These synchronous current mode PWM regulators have integrated N- and P-Channel power MOSFETs and provide pre-set pin programmable outputs. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and a reduced external component count. The operating frequency of 750kHz typical allows the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. A power good signal “PG” is generated when the output voltage falls outside the regulation limits. Other features include overcurrent protection and thermal overload shutdown. The ISL6410, ISL6410A are available in an MSOP 10 lead package.

Ordering Information

PART NUMBER*	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6410IR	-40 to 85	16 Ld 4x4 QFN	L16.4x4
ISL6410IRZ (Note)	-40 to 85	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6410IU	-40 to 85	10 Ld MSOP	M10.118
ISL6410IUZ (Note)	-40 to 85	10 Ld MSOP (Pb-free)	M10.118
ISL6410AIR	-40 to 85	16 Ld 4x4 QFN	L16.4x4
ISL6410AIRZ (Note)	-40 to 85	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6410AIU	-40 to 85	10 Ld MSOP	M10.118
ISL6410AIUZ (Note)	-40 to 85	10 Ld MSOP (Pb-free)	M10.118

*For tape and reel, add “-T”, “-TK” or “-T5K” suffix.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

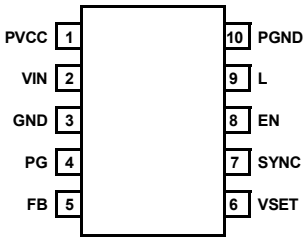
- Fully Integrated Synchronous Buck Regulator
- PWM Fixed Output Voltage Options
  - 1.8V, 1.5V or 1.2V with ISL6410 (VIN = 3.3V)
  - 3.3V, 1.8V or 1.2V with ISL6410A (VIN = 5.0V)
- Continuous Output Current 600mA
- Ultra-Compact DC-DC Converter Design
- Stable with Small Ceramic Output Capacitors
- High Conversion Efficiency
- Extensive Circuit Protection and Monitoring features
  - Overvoltage, UVLO
  - Overcurrent
  - Thermal Shutdown
- Available in MSOP and QFN packages
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Packaging Available

Applications

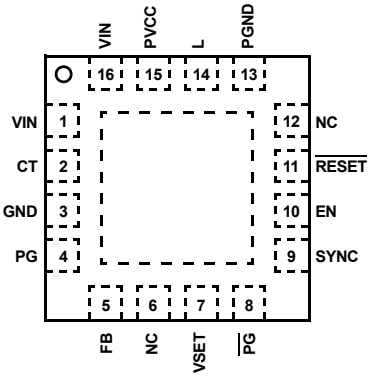
- CPUs, DSP, CPLDs, FPGAs
- ASICs
- DVD and DSL applications
- WLAN Cards
- Generic 5V to 3.3V Conversion

Pinouts

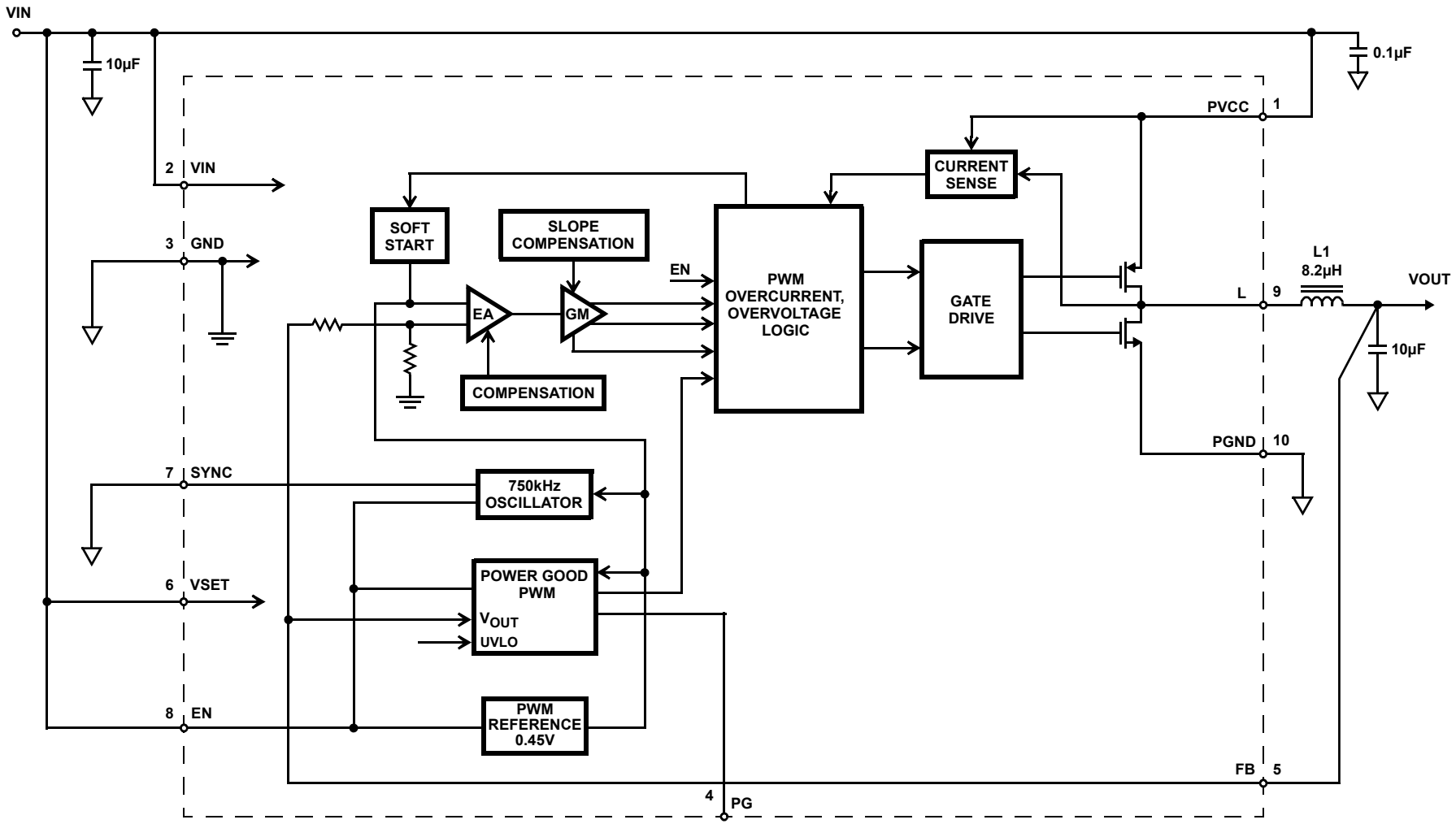
ISL6410 (MSOP)
TOP VIEW



ISL6410 (QFN)
TOP VIEW



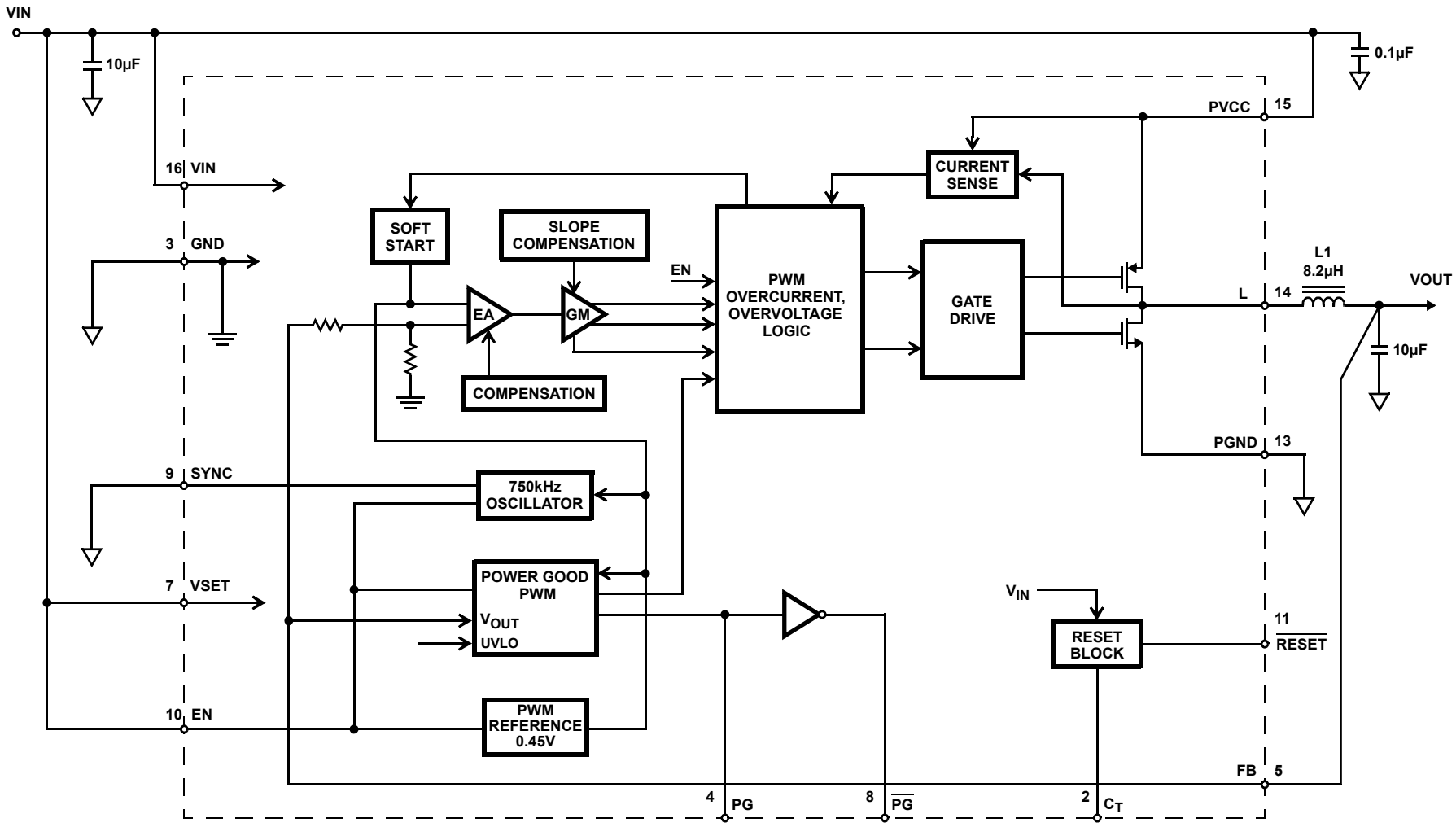
Functional Block Diagram for MSOP Version



NOTES:

1. VIN is 3.3V for ISL6410 and 5.0V for ISL6410A.
2. VSET in the above schematic is connected to VIN, so the VOUT is 1.8V for ISL6410 and 3.3V for ISL6410A.

Functional Block Diagram for QFN Version



NOTES:

1. VIN is 3.3V for ISL6410 and 5.0V for ISL6410A.
2. VSET in the above schematic is connected to VIN, so the VOUT is 1.8V for ISL6410 and 3.3V for ISL6410A.

Typical Application Schematics

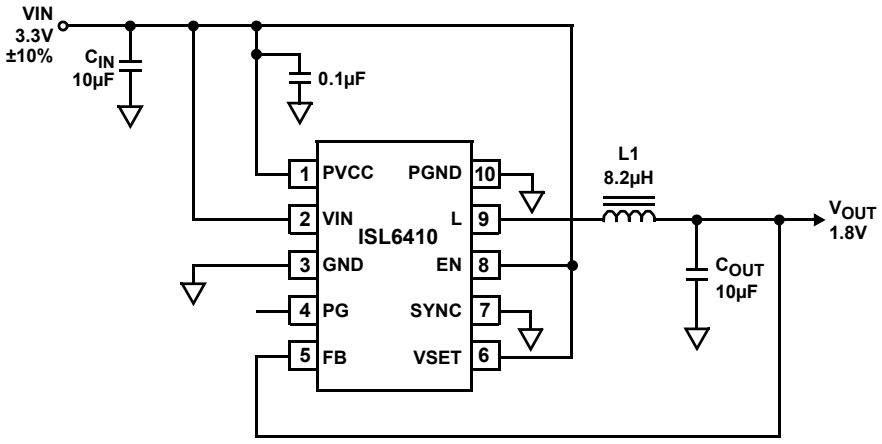


FIGURE 1. SCHEMATIC USING THE ISL6410 MSOP

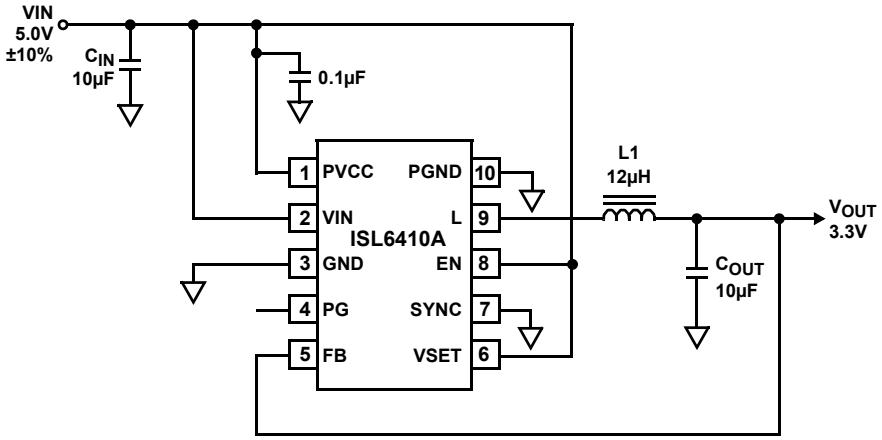


FIGURE 2. SCHEMATIC USING THE ISL6410A MSOP

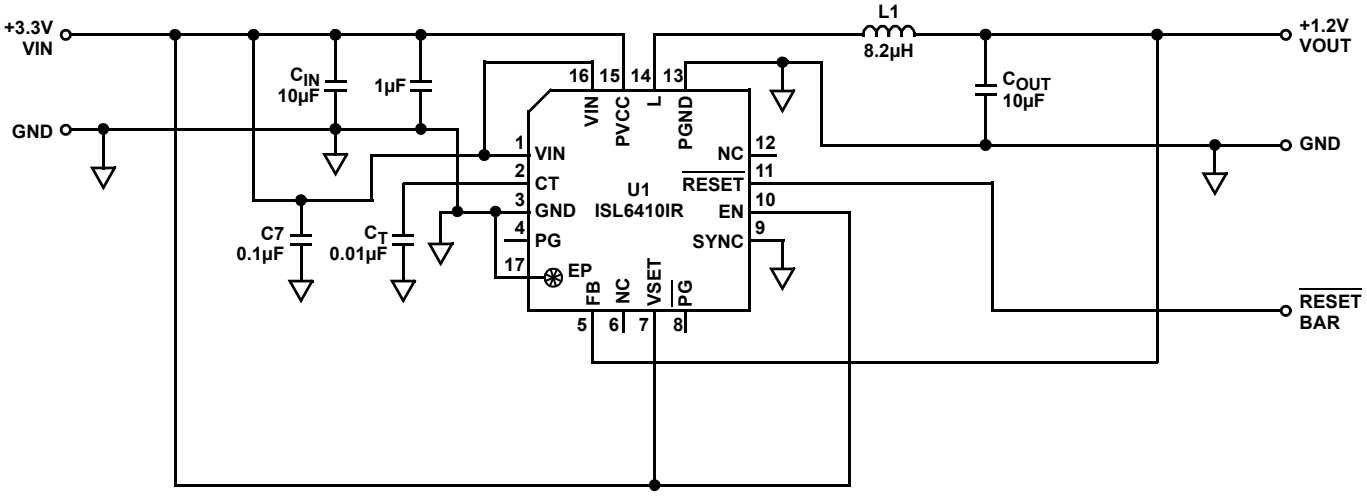


FIGURE 3. SCHEMATIC USING THE ISL6410 QFN

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . -0.3V to +6.0V
SYNC, FB, VSET & Enable Input (Note 3) . . . . -0.3V to VCC+0.3V
ESD Classification (Human Body Model) . . . . . Class 2

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
MSOP Package (Note 4)	128	NA
QFN Package (Notes 4, 5).	45	7.5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (10s, soldering . . . . . 260°C
Ambient Temperature Range. . . . . -40°C to 85°C
Junction Temperature Range. . . . . -40°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. All voltages are with respect to GND.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{IN} = 3.3V ±10% (ISL6410) or 5V ±10% (ISL6410A), T_A = 25°C (Note 6).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY					
Supply Voltage Range	VIN (ISL6410)	3.0	3.3	3.6	V
	VIN (ISL6410A)	4.5	5.0	5.5	V
Input UVLO Threshold	V_{TR} (ISL6410) Rising	2.62	2.68	2.73	V
	V_{TF} (ISL6410) Falling	2.53	2.59	2.64	V
	V_{TR} (ISL6410A) Rising	4.27	4.37	4.45	V
	V_{TF} (ISL6410A) Falling	4.1	4.22	4.32	V
Quiescent Supply Current	I_{OUT} = 0mA	-	2.3	-	mA
Shutdown Supply Current	EN = GND, T_A = 25°C	-	5	10	µA
	EN = GND, T_A = 85°C	-	10	15	µA
Thermal Shutdown Temperature (Note 7)	Rising Threshold	-	150	-	°C
Thermal Shutdown Hysteresis (Note 7)		-	20	25	°C
SYNCHRONOUS BUCK PWM REGULATOR					
Output Voltage	ISL6410, VSET = L	-	1.2	-	V
	ISL6410, VSET = H	-	1.8	-	V
	ISL6410, VSET = OPEN	-	1.5	-	V
	ISL6410A, VSET = L	-	1.2	-	V
	ISL6410A, VSET = H	-	3.3	-	V
	ISL6410A, VSET = OPEN	-	1.8	-	V
Output Voltage Accuracy	I_{OUT} = 3mA, T_A = -40°C to 85°C	-1.5	-	+1.5	%
Line Regulation	I_{OUT} = 3mA	-0.5	-	+0.5	%
Load Regulation	I_{OUT} = 3mA to 600mA	-1.5	-	+1.5	%
Maximum Output Current		-	-	600	mA
Peak Output Current Limit		700	-	1300	mA
PMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	230	-	mΩ
NMOS $r_{DS(ON)}$	I_{OUT} = 200mA	-	230	-	mΩ
Efficiency	I_{OUT} = 200mA, V_{IN} = 3.3V, V_O = 1.8V (ISL6410)	-	92	-	%

Electrical Specifications Recommended operating conditions unless otherwise noted. V_{IN} = 3.3V ±10% (ISL6410) or 5V ±10% (ISL6410A), T_A = 25°C (Note 6). **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Efficiency	I_{OUT} = 200mA, V_{IN} = 5.0V, V_O = 3.3V (ISL6410A)	-	93	-	%
Efficiency	I_{OUT} = 600mA, V_{IN} = 5.0V, V_O = 3.3V (ISL6410A)	-	91	-	%
Soft-Start Time	4096 Clock Cycles @ 750kHz	-	5.5	-	ms
OSCILLATOR					
Oscillator Frequency		620	750	860	kHz
Frequency Synchronization Range (f_{SYNC})	Clock signal on SYNC pin	500	-	1000	kHz
SYNC High Level Input Voltage	As % of VIN	70	-	-	%
SYNC Low Level Input Voltage	As % of VIN	-	-	30	%
Sync Input Leakage Current	SYNC = GND or V_{IN}	-1	-	1	µA
Duty Cycle of External Clock Signal (Note 7)		20	-	60	%
PGOOD (ISL6410 interfaces to 3.3V Logic, ISL6410A interfaces to 5.0V Logic)					
Rising Threshold	1mA minimum source/sink	+5.0	8.0	+10.5	%
Falling Threshold		-10.5	-8.0	-5.0	%
Rising/Falling Hysteresis		-	1	-	%
ENABLE					
EN High Level Input Voltage	As % of VIN	70	-	-	%
EN Low Level Input Voltage	As % of VIN	-	-	30	%
EN Input Leakage Current	EN = GND or V_{IN}	-1		1	µA
OVERVOLTAGE					
Overvoltage Threshold		27	30	33	%
RESET BLOCK SPECIFICATIONS					
RESET (reset released)	ISL6410, ISOURCE = 500µA, VIN = 2.90V	$0.8V_{IN}$	-	-	V
RESET (reset asserted)	ISL6410, ISINK = 1.2mA, VIN = 2.50V	-	-	0.3	V
RESET Rising Threshold	ISL6410	2.74	2.78	2.81	V
RESET Falling Threshold	ISL6410	2.72	2.77	2.79	V
RESET (reset released)	ISL6410A, ISOURCE = 800µA, VIN = 4.70V	$0.8V_{IN}$	-	-	V
RESET (reset asserted)	ISL6410A, ISINK = 3.2mA, VIN = 4.10V	-	-	0.4	V
RESET Rising Threshold	ISL6410A	4.5	4.58	4.64	V
RESET Falling Threshold	ISL6410A	4.47	4.55	4.61	V
RESET Threshold Hysteresis	ISL6410	-	20	-	mV
RESET Threshold Hysteresis	ISL6410A	-	30	-	mV
RESET Active Timeout Period (Note 8)	CT = 0.01mF	-	25	-	ms
V_{SET}					
V_{SET} High Level Input		V_{IN}-0.4V	-	-	V
V_{SET} Low Level Input		-	-	0.4	V
V_{SET} Open Level Input		-	$V_{IN}/2$	-	V

NOTES:

6. Specifications at -40°C and +85°C are guaranteed by design, not production tested.
7. Guaranteed by design, not production tested.
8. The RESET Timeout period is linear with C_T at a slope of 2.5ms/nF, thus a 10nF capacitor provides for 25ms.

Pin Description

VIN - Supply voltage for the IC. It is recommended to place a 1µF decoupling capacitor as close as possible to the IC.

GND - Small signal ground for the PWM controller stage. All internal control circuits are referenced to this pin.

PG - The Power good is an open-drain output. A pull-up resistor should be connected between PG and VIN. It is asserted active high when the output voltage reaches 94.5% of the nominal value.

FB - The Feedback pin is used to sense the output voltage, and should be connected to VOUT for normal operation.

VSET - This pin is used to program the output voltages. Refer to Table 1 below for details.

TABLE 1.

VSET	ISL6410 Vo	ISL6410A Vo
High	1.8V	3.3V
Open (NC)	1.5V	1.8V
Low	1.2V	1.2V

SYNC - This pin is used for synchronization. The converter switching frequency can be synchronized to an external CMOS clock signal in the range of (500kHz to 1MHz).

EN - A logic high enables the converter, logic low forces the device into shutdown mode reducing the supply current to less than 10µA at 25°C. This pin should be pulled up to VCC via a 10K resistor.

L - This pin is the drain junction of the internal power MOSFETs and is to be connected to the external inductor.

PGND - Power ground. Connect all power grounds to this pin.

PVCC - This pin provides the Input supply for the internal MOSFETs. It is recommended to place a 1µF decoupling capacitor as close as possible to the IC.

CT - Timing capacitor connection to set the 25ms minimum pulse width for the $\overline{\text{RESET}}$ signal.

$\overline{\text{RESET}}$ - The outputs of the reset supervisory circuit, which monitors VIN. The IC asserts these $\overline{\text{RESET}}$ signals whenever the supply voltage drops below a preset threshold and keeps it asserted for at least 25ms after VCC (VIN) has risen above the reset threshold. These outputs are push-pull. $\overline{\text{RESET}}$ is LOW when re-setting the microprocessor. The PWM will continue to operate until VIN drops below the UVLO threshold.

Functional Description

The ISL6410, ISL6410A is a synchronous buck regulator with integrated N- and P-channel power MOSFET and provides pre-set pin programmable outputs. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency of 750kHz typical allows the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG output indicates loss of regulation on PWM output.

The PWM is based on the peak current mode control topology with internal slope compensation. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. On exceeding a preset limit the high side switch is turned off causing the PWM comparator to trip. This occurs whenever the output voltage is in regulation or when the inductor current reaches the current limit. After a minimum dead time to prevent shoot through current, the low side N-channel MOSFET turns on and the current ramps down. As the clock cycle is completed, the low side switch turns off and the next clock cycle is initiated.

The control loop is internally compensated thus reducing the amount of external components.

The switch current is internally sensed and the maximum current limit is 1300mA peak.

Synchronization

The typical operating frequency for the converter is 750kHz. It is possible to synchronize the converter to an external clock frequency in the range of 500kHz to 1000kHz when an external signal is applied to SYNC pin. The device will automatically detect and synchronize to the rising edge of the first clock pulse. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues its operation without interruption. The switch over will be initiated if no rising edge triggers are present on the SYNC pin for a duration of four clock cycles.

Soft-Start

As the EN (Enable) pin goes high, the soft-start function will generate an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typically 5.5ms with 750kHz switching frequency. When the soft-start is completed, the error amplifier will be connected directly to the internal voltage reference.

Enable

Logic low on EN pin forces the PWM section into shutdown. In the shutdown mode all the major blocks of the PWM including power switches, drivers, voltage reference, and oscillator are turned off.

Undervoltage Lockout

An undervoltage lockout circuit prevents the converter from turning on when the voltage on VIN is less than the values specified in the Input UVLO Threshold section of the electrical specification.

Power Good

This output is asserted high when the PWM is enabled, and Vout is within 8.0% typical of its final value, and is active low outside this range. When disabled, the output turns active low. It is recommended to leave the PG pin unconnected when not used.

PWM Overvoltage and Overcurrent Protection

The PWM output current is sampled at the end of each PWM cycle, exceeding the overcurrent limit, causes a 4 bit up/down counter to increment by one LSB. A normal current state causes the counter to decrement by one LSB (the counter will not however “rollover” or count below 0000). When the PWM goes into overcurrent, the counter rapidly reaches count 1111 and the PWM output is shut down and the soft-start counter is reset. After 16 clocks the PWM output is enabled and the soft-start cycle is started.

If Vout exceeds the overvoltage limit for 32 consecutive clock cycles the PWM output is shut off and the soft-start cycle is initiated.

No Load Operation

If there is no load connected to the output, the converter will regulate the output voltage by allowing the inductor current to reverse for a short period of time.

Output Capacitor Selection

For best performance, a low ESR output capacitor is needed. Output voltages below 1.8V require a larger output capacitor and ESR value to improve the performance and stability of the converter. For 1.8V output applications, a ceramic capacitor of 10µF or higher value with ESR ≤50mΩ is recommended.

The RMS ripple current is calculated as:

$$I_{RMS(Co)} = Vo \times \frac{1 - \frac{Vo}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

L = the inductor value

f = the switching frequency

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR and the voltage ripple caused by charge and discharge of the output capacitor:

$$\Delta Vo = Vo \times \frac{1 - \frac{Vo}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Co \times f} + ESR \right)$$

Where the highest output voltage ripple occurs at the highest input voltage VIN.

TABLE 2. RECOMMENDED OUTPUT CAPACITORS

CAPACITOR VALUE	ESR (mΩ)	COMPONENT SUPPLIER	COMMENTS
10µF	<50	AVX 08056D106KAT2A	Ceramic

Input Capacitor Selection

The input current to the buck converter is pulsed, and therefore a low ESR input capacitor is required. This results in good input voltage filtering and minimizes the interference it causes to other circuits. The input capacitor should have a minimum value of 10µF and a higher value can be selected for improving input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = Io(max) \times \sqrt{\frac{Vo}{Vin} \times \left(1 - \frac{Vo}{Vin}\right)}$$

The worst case RMS ripple current occurs at D = 0.5 and is calculated as: Irms = Io/2.

D = Duty Cycle

Ceramic capacitors are preferred because of their low ESR value. They are also less sensitive to voltage transients when compared to tantalum capacitors. It is good practice to place the input capacitor as close as possible to the input pin of the IC for optimum performance.

Inductor Selection

The ISL6410 is an internally compensated device and hence a minimum of 8.2µH must be used for the ISL6410 and a minimum of 12µH for the ISL6410A. The selected inductor must have a low DC resistance and a saturation current greater than the maximum inductor current value can be calculated from the equations below

$$dIL = Vo \times \frac{1 - \frac{Vo}{Vin}}{L \times f}$$

$$IL\ max = Io\ max + \frac{dIL}{2}$$

where

dIL = the peak to peak inductor current
L = the inductor value
f = the switching frequency

ILmax = the max inductor current

TABLE 3. RECOMMENDED INDUCTORS

INDUCTOR VALUE	DCR (mΩ)	COMPONENT SUPPLIER
8.2µH	75	Coilcraft MSS6122-822MX
12µH	100	Coilcraft MSS6122-123MX

Layout Considerations

As in all switching power supplies, the layout is an important step in the design process, more so at high peak currents and switching frequencies. Improper layout practice will give rise to Stability and EMI issues. It is recommended that wide and short traces are used for the main current paths. The input capacitor should be placed as close as possible to the IC pins. This applies to the output inductor and capacitor as well. The analog ground, GND, and the power ground, PGND, need to be separated. Use a common ground node to minimize the effects of ground noise.

Performance Curves and Waveforms

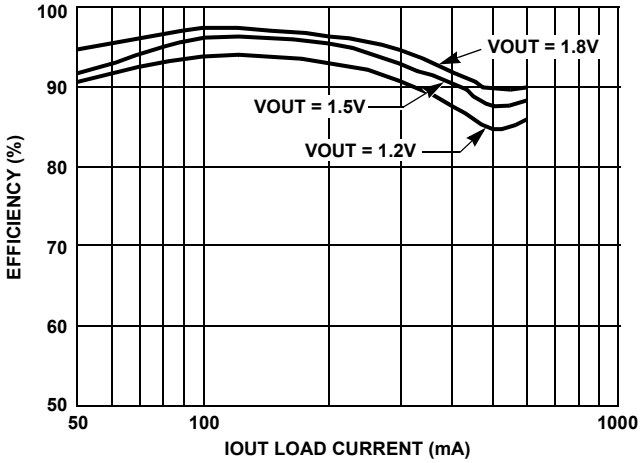


FIGURE 4. ISL6410 EFFICIENCY vs LOAD CURRENT

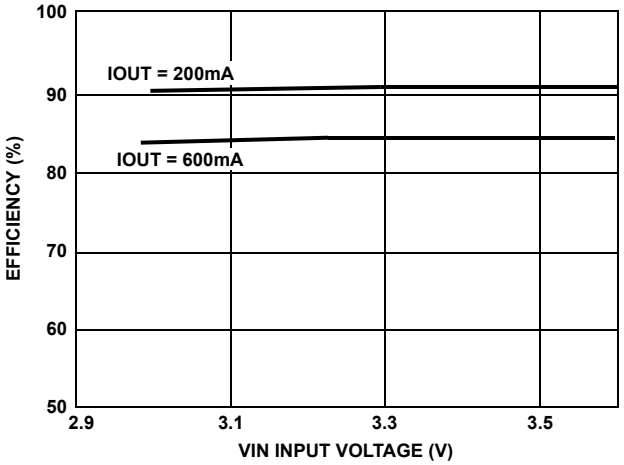


FIGURE 5. ISL6410 VIN vs EFFICIENCY

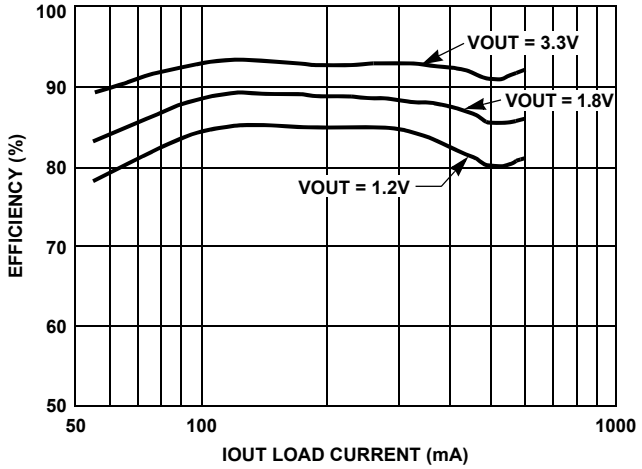


FIGURE 6. ISL6410A EFFICIENCY vs LOAD CURRENT

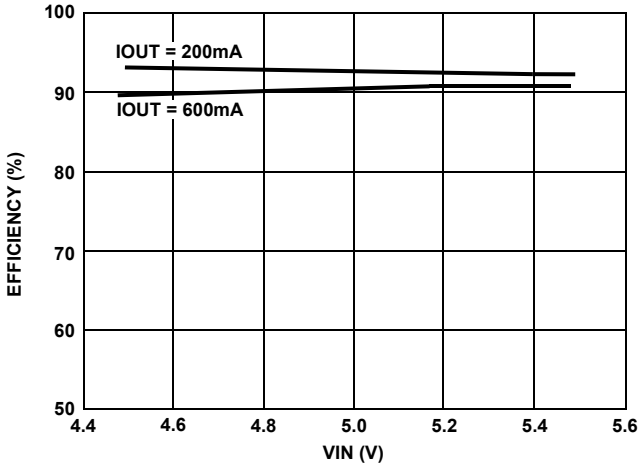


FIGURE 7. ISL6410A EFFICIENCY vs VIN

Performance Curves and Waveforms (Continued)

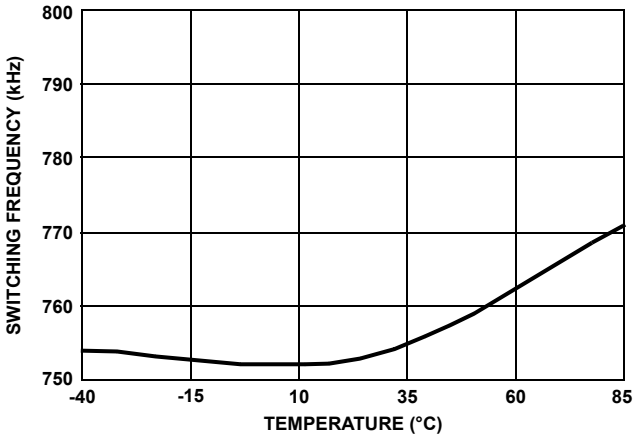


FIGURE 8. ISL6410 OSCILLATOR FREQUENCY vs TEMPERATURE

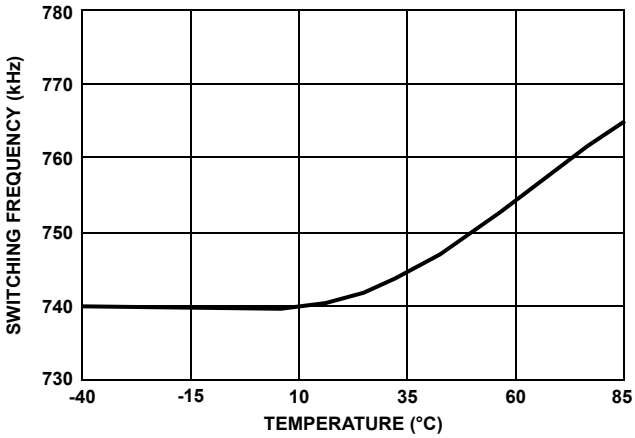


FIGURE 9. ISL6410A OSCILLATOR FREQUENCY vs TEMPERATURE

CH1 = Top, CH2 = Middle, CH4 = Bottom, where applicable

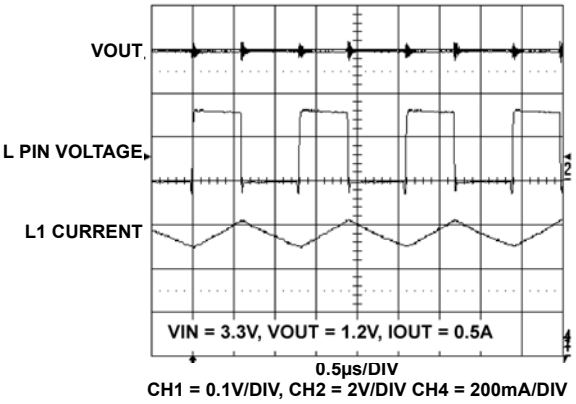


FIGURE 10. SWITCHING WAVEFORM FOR ISL6410

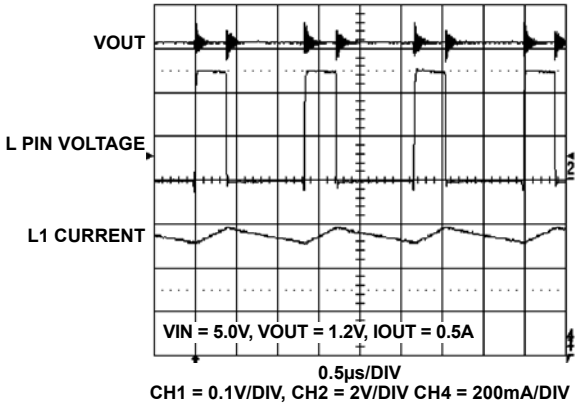


FIGURE 11. SWITCHING WAVEFORM FOR ISL6410A

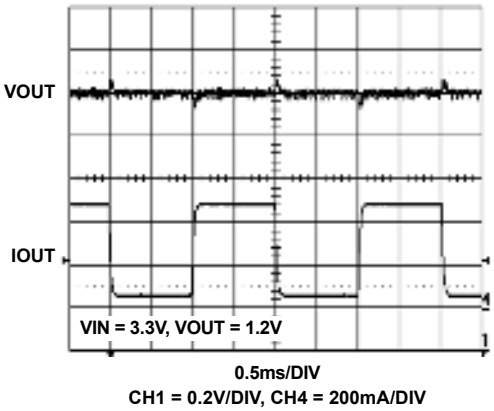


FIGURE 12. TRANSIENT LOAD WAVEFORM FOR ISL6410

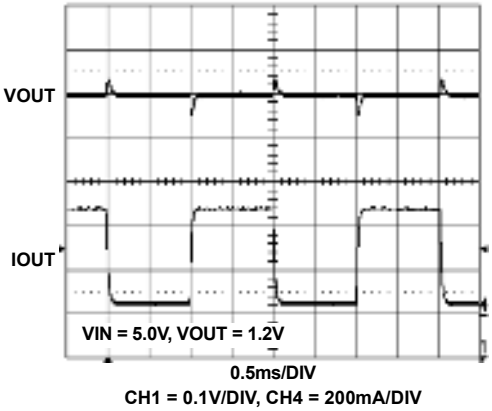


FIGURE 13. TRANSIENT LOAD WAVEFORM FOR ISL6410A

Performance Curves and Waveforms (Continued)

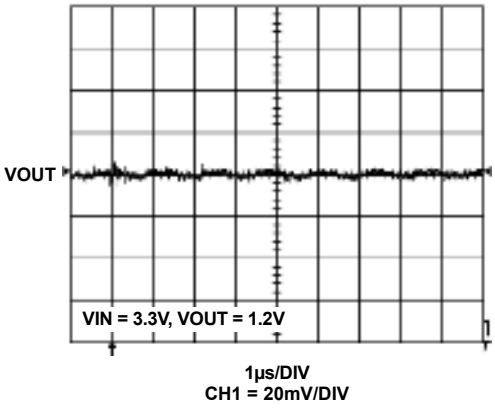


FIGURE 14. RIPPLE WAVEFORM FOR ISL6410

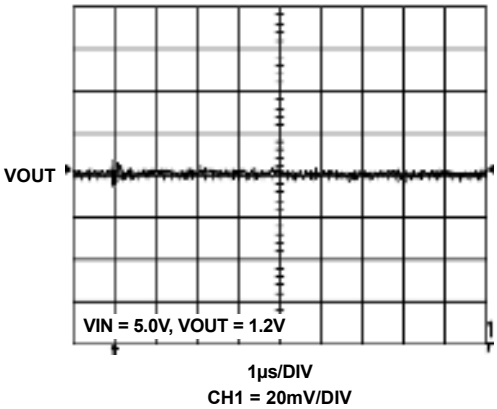


FIGURE 15. RIPPLE WAVEFORM FOR ISL6410A

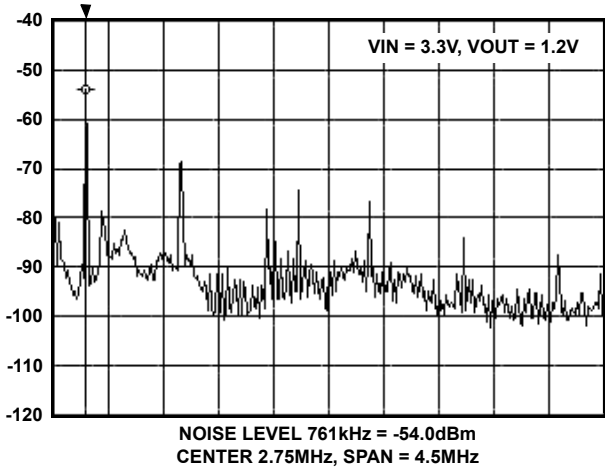


FIGURE 16. SWITCHING HARMONICS AND NOISE FOR ISL6410

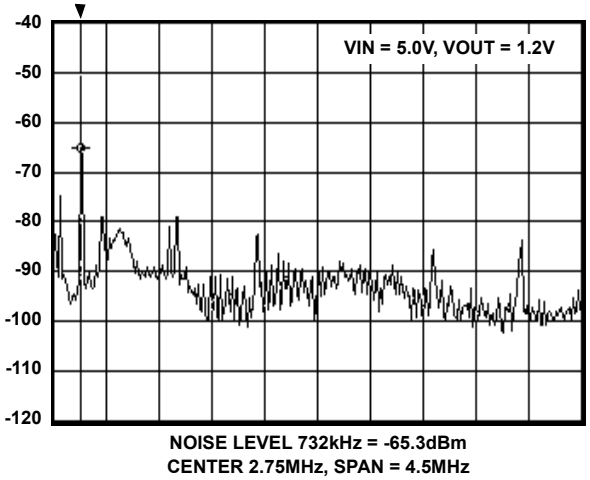


FIGURE 17. SWITCHING HARMONICS AND NOISE FOR ISL6410A

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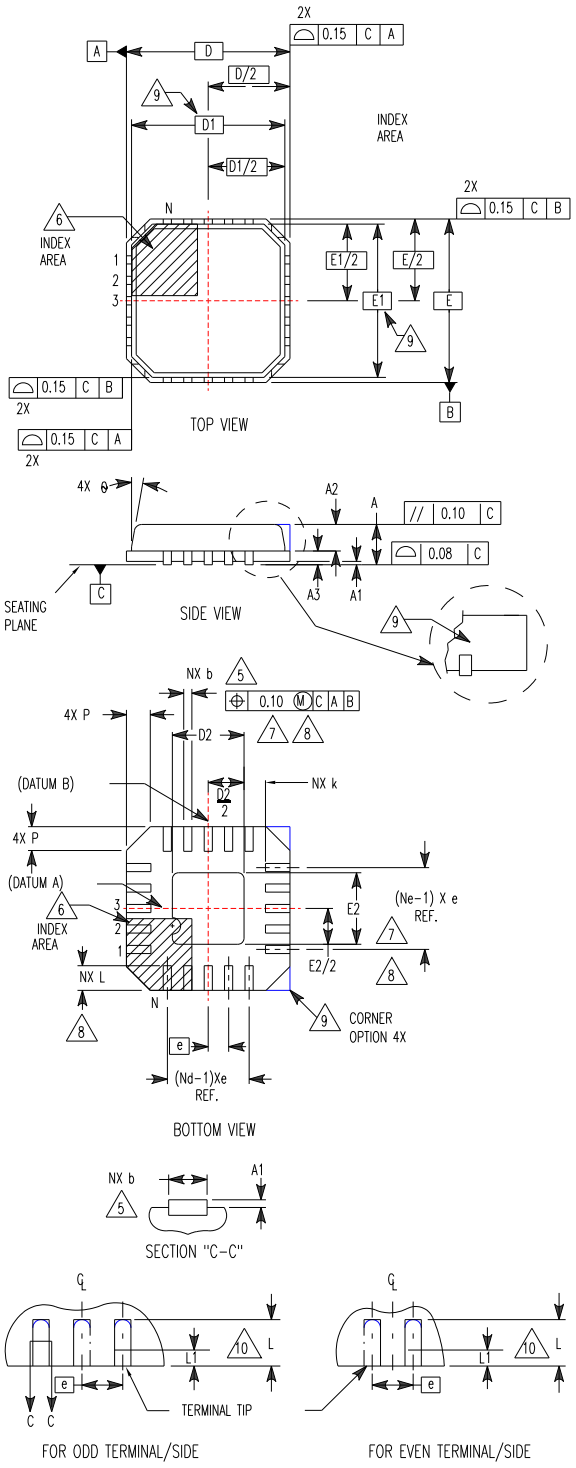
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Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

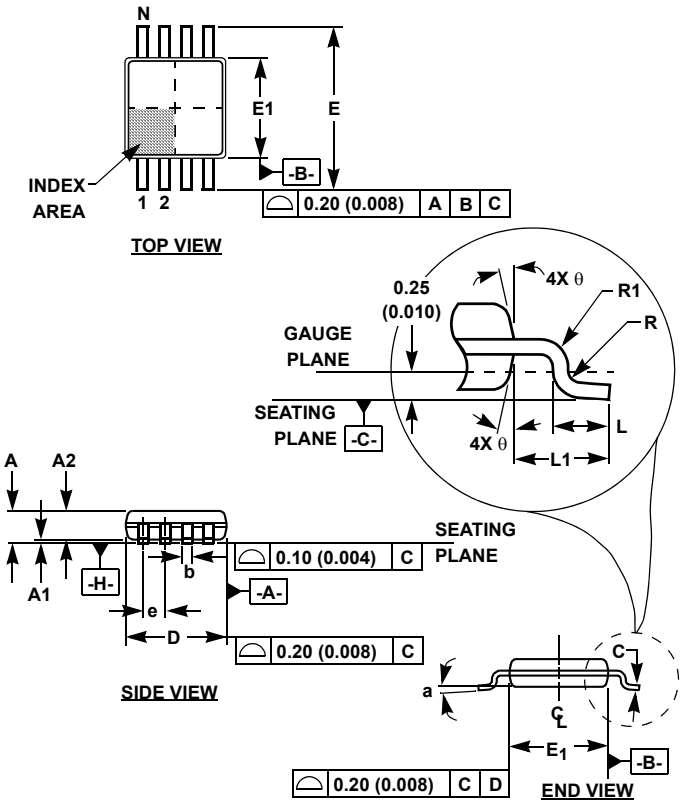
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only