DATASHEET

ISL12027, ISL12027A

Real Time Clock/Calendar with EEPROM

FN8232
Rev 9.00
September 23, 2015

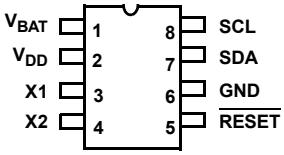
The ISL12027 device is a low power real time clock with timing and crystal compensation, clock/calender, power-fail indicator, two periodic or polled alarms, intelligent battery backup switching, CPU Supervisor and integrated 512x8-bit EEPROM, in 16 Byte per page format.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

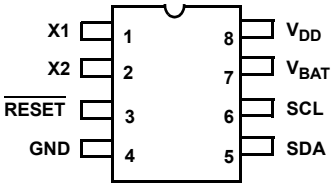
The ISL12027 and ISL12027A Power Control Settings are different. The ISL12027 uses the Legacy Mode Setting, and the ISL12027A uses the Standard Mode Setting. Applications that have $V_{BAT} > V_{DD}$ will require only the ISL12027A. Please refer to“Power Control Operation” on page 15 for more details. Also, please refer to “I²C Communications During Battery Backup and LVR Operation” on page 24 for important details.

Pinouts

ISL12027, ISL12027A
(8 LD TSSOP)
TOP VIEW



ISL12027, ISL12027A
(8 LD SOIC)
TOP VIEW



Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes and Seconds
  - Day of the Week, Day, Month and Year
- Two Non-Volatile Alarms
  - Settable on the Second, Minute, Hour, Day of the Week, Day, or Month
  - Repeat Mode (Periodic Interrupts)
- Automatic Backup to Battery or SuperCap
- On-Chip Oscillator Compensation
  - Internal Feedback Resistor and Compensation Capacitors
  - 64 Position Digitally Controlled Trim Capacitor
  - 6 Digital Frequency Adjustment Settings to ±30ppm
- 512x8-Bits of EEPROM
  - 16-Byte Page Write Mode (32 total pages)
  - 8 Modes of BlockLock™ Protection
  - Single Byte Write Capability
- High Reliability
  - Data Retention: 50 years
  - Endurance: >2,000,000 Cycles Per Byte
- I²C-bus™ Interface
  - 400kHz Data Transfer Rate
- 800nA Battery Supply Current
- Package Options
  - 8 Ld SOIC and 8 Ld TSSOP Packages
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- POS Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

Pin Descriptions

PIN NUMBER		SYMBOL	BRIEF DESCRIPTION
SOIC	TSSOP		
1	3	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source.
2	4	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
3	5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$. This is a reset signal output. This signal notifies a host processor that the “watchdog” time period has expired or that the voltage has dropped below a fixed V_{TRIP} threshold. It is an open drain active LOW output. Recommended value for the pull-up resistor is 5kΩ. If unused, connect to ground.
4	6	GND	Ground.
5	7	SDA	Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR’ed with other open drain or open collector outputs.
6	8	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated).
7	1	V_{BAT}	This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event that the V_{DD} supply fails. This pin should be tied to ground if not used.
8	2	V_{DD}	Power Supply.

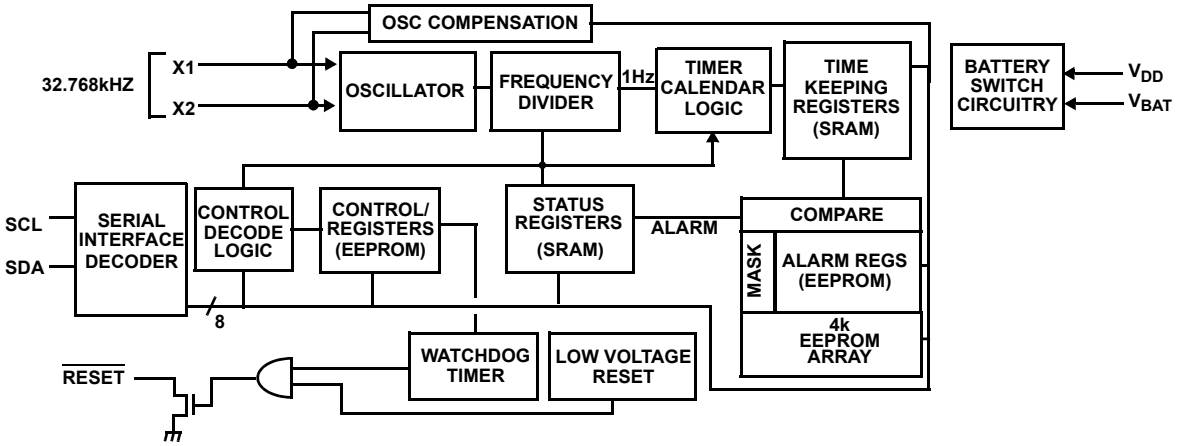
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{BAT} TRIP POINT (V)	BSW BIT DEFAULT SETTING	$V_{\overline{\text{RESET}}}$ VOLTAGE (V)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL12027IB27Z	12027 IB27Z	$V_{DD} < V_{BAT}$	BSW = 1	2.63	-40 to +85	8 Ld SOIC	M8.15
ISL12027IB27AZ	12027 IB27AZ	$V_{DD} < V_{BAT}$	BSW = 1	2.92	-40 to +85	8 Ld SOIC	M8.15
ISL12027IB30AZ	12027 IB30AZ	$V_{DD} < V_{BAT}$	BSW = 1	3.09	-40 to +85	8 Ld SOIC	M8.15
ISL12027IBZ	12027 IBZ	$V_{DD} < V_{BAT}$	BSW = 1	4.38	-40 to +85	8 Ld SOIC	M8.15
ISL12027IBAZ	12027 IBAZ	$V_{DD} < V_{BAT}$	BSW = 1	4.64	-40 to +85	8 Ld SOIC	M8.15
ISL12027IV27Z	2027 I27Z	$V_{DD} < V_{BAT}$	BSW = 1	2.63	-40 to +85	8 Ld TSSOP	M8.173
ISL12027IV27AZ	2027 27AZ	$V_{DD} < V_{BAT}$	BSW = 1	2.92	-40 to +85	8 Ld TSSOP	M8.173
ISL12027IV30AZ	2027 30AZ	$V_{DD} < V_{BAT}$	BSW = 1	3.09	-40 to +85	8 Ld TSSOP	M8.173
ISL12027IVZ **(No longer available or supported)**	2027 IVZ	$V_{DD} < V_{BAT}$	BSW = 1	4.38	-40 to +85	8 Ld TSSOP	M8.173
ISL12027IVAZ **(No longer available or supported)**	2027 IVAZ	$V_{DD} < V_{BAT}$	BSW = 1	4.64	-40 to +85	8 Ld TSSOP	M8.173
ISL12027AIB27Z **(No longer available or supported)**	12027A IB27Z	$V_{DD} < V_{BAT}$	BSW = 0	2.63	-40 to +85	8 Ld SOIC	M8.15
ISL12027AIV27Z **(No longer available or supported)**	2027A I27Z	$V_{DD} < V_{BAT}$	BSW =0	2.63	-40 to +85	8 Ld TSSOP	M8.173

NOTES:

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL12027, ISL12027A. For more information on MSL please see techbrief TB363.

Block Diagram



Absolute Maximum Ratings

Voltage on V_{DD}, V_{BAT}, SCL, SDA, and $\overline{RESET}$ pins (respect to ground) . . . . . -0.3V to 6.0V
Voltage on X1 and X2 pins (respect to ground) . . . . . -0.3V to 2.5V
Latchup (Note 4) . . . . . Class II, Level B @ +85°C
ESD Rating
Human Body Model . . . . . ±2kV
Machine Model 175V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 5, 6)	115	50
8 Ld TSSOP Package (Notes 5, 6) . . .	140	40

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: Using a max positive pulse of 8.35V on all pins except X1 and X2, Using a max positive pulse of 2.75V on X1 and X2, and using a max negative pulse of -1V for all pins.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the “case temp” location is taken at the package top center.

DC Electrical Specifications

Unless otherwise noted, V_{DD} = +2.7V to +5.5V, T_A = -40°C to +85°C, Typical values are at T_A = +25°C and V_{DD} = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT	NOTES
V_{DD}	Main Power Supply		**2.7**		**5.5**	V	
V_{BAT}	Backup Power Supply		**1.8**		**5.5**	V	

Electrical Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT	NOTES
I_{DD1}	Supply Current with I^2C Active	V_{DD} = 2.7V			**500**	µA	7, 8, 9
		V_{DD} = 5.5V			**800**	µA	
I_{DD2}	Supply Current for Non-Volatile Programming	V_{DD} = 2.7V			**2.5**	mA	7, 8, 9
		V_{DD} = 5.5V			**3.5**	mA	
I_{DD3}	Supply Current for Main Timekeeping (Low Power Mode)	$V_{DD} = V_{SDA} = V_{SCL}$ = 2.7V			**10**	µA	9
		$V_{DD} = V_{SDA} = V_{SCL}$ = 5.5V			**20**	µA	
I_{BAT}	Battery Supply Current	V_{BAT} = 1.8V, $V_{DD} = V_{SDA} = V_{SCL} = V_{\overline{RESET}}$ = 0V		800	**1000**	nA	7, 10, 11
		V_{BAT} = 3.0V, $V_{DD} = V_{SDA} = V_{SCL} = V_{\overline{RESET}}$ = 0V		850	**1200**	nA	
I_{BATLKG}	Battery Input Leakage	V_{DD} = 5.5V, V_{BAT} = 1.8V	**-100**		**100**	nA	
V_{TRIP}	V_{BAT} Mode Threshold		**1.8**	2.2	**2.6**	V	11
$V_{TRIPHYS}$	V_{TRIP} Hysteresis			30		mV	11, 14
V_{BATHYS}	V_{BAT} Hysteresis			50		mV	11, 14
$V_{DD\ SR-}$	V_{DD} Negative Slew rate				**10**	V/ms	12
$\overline{RESET}$ OUTPUT							
V_{OL}	Output Low Voltage	V_{DD} = 5.5V, I_{OL} = 3mA			**0.4**	V	
		V_{DD} = 2.7V, I_{OL} = 1mA			**0.4**	V	
I_{LO}	Output Leakage Current	V_{DD} = 5.5V, V_{OUT} = 5.5V		100	**400**	nA	

Watchdog Timer/Low Voltage Reset Parameters

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 16)	TYP (Note 5)	MA (Note 16)	UNITS	NOTES
t_{RPD}	V_{DD} Detect to RESET LOW			500		ns	13
t_{PURST}	Power-up Reset Time-Out Delay		**100**	250	**400**	ms	
V_{RVALID}	Minimum V_{DD} for Valid RESET Output		**1.0**			V	
$V_{\overline{RESET}}$	ISL12027-4.5A Reset Voltage Level		**4.59**	4.64	**4.69**	V	
	ISL12027 Reset Voltage Level		**4.33**	4.38	**4.43**	V	
	ISL12027-3 Reset Voltage Level		**3.04**	3.09	**3.14**	V	
	ISL12027-2.7A Reset Voltage Level		**2.87**	2.92	**2.97**	V	
	ISL12027-2.7 Reset Voltage Level		**2.58**	2.63	**2.68**	V	
t_{WDO}	Watchdog Timer Period	32.768kHz crystal between X1 and X2	**1.70**	1.75	**1.801**	s	
			725	750	**775**	ms	
			225	250	**275**	ms	
t_{RST}	Watchdog Timer Reset Time-Out Delay	32.768kHz crystal between X1 and X2	**225**	250	**275**	ms	
t_{RSP}	I^2C Interface Minimum Restart Time		**1.2**			µs	
EEPROM SPECIFICATIONS							
	EEPROM Endurance		>2,000,000			Cycles	
	EEPROM Retention	Temperature ≤ +75°C	50			Years	

Serial Interface (I^2C) Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{IL}	SDA, and SCL Input Buffer LOW Voltage	SBIB = 1 (Under V_{DD} mode)	-0.3		$0.3xV_{DD}$	V	
V_{IH}	SDA, and SCL Input Buffer HIGH Voltage	SBIB = 1 (Under V_{DD} mode)	$0.7xV_{DD}$		V_{DD} + 0.3	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis	SBIB = 1 (Under V_{DD} mode)	$0.05xV_{DD}$			V	
V_{OL}	SDA Output Buffer LOW Voltage	I_{OL} = 4mA	0		0.4	V	
I_{LI}	Input Leakage Current on SCL	V_{IN} = 5.5V		0.1	10	µA	
I_{LO}	I/O Leakage Current on SDA	V_{IN} = 5.5V		0.1	10	µA	
TIMING CHARACTERISTICS							
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			900	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	600			ns	

Serial Interface (I^2C) Specifications (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	600			ns	
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 70% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	0			ns	
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20 + 0.1xCb		250	ns	
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20 + 0.1xCb		250	ns	
Cpin	SDA, and SCL Pin Capacitance				10	pF	
t_{WC}	Non-Volatile Write Cycle Time			12	20	ms	14
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20 + 0.1xCb		250	ns	15
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20 + 0.1xCb		250	ns	15
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	15
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ	15

NOTES:

7. $\overline{RESET}$ Inactive (no reset).
8. $V_{IL} = V_{DD}$ x 0.1, $V_{IH} = V_{DD}$ x 0.9, f_{SCL} = 400kHz.
9. $V_{\overline{RESET}}$ = 2.63V (V_{DD} must be greater than $V_{\overline{RESET}}$), V_{BAT} = 0V.
10. Bit BSW = 0 (Standard Mode), ATR = 00h, V_{BAT} ≥1.8V.
11. Specified at +25°C.
12. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
13. Parameter is not 100% tested.
14. t_{WC} is the minimum cycle time to be allowed for any non-volatile Write by the user, it is the time from valid STOP condition at the end of Write sequence of a serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
15. These are I^2C specific parameters and are not directly tested, however they are used during device testing to validate device specification.
16. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Timing Diagrams

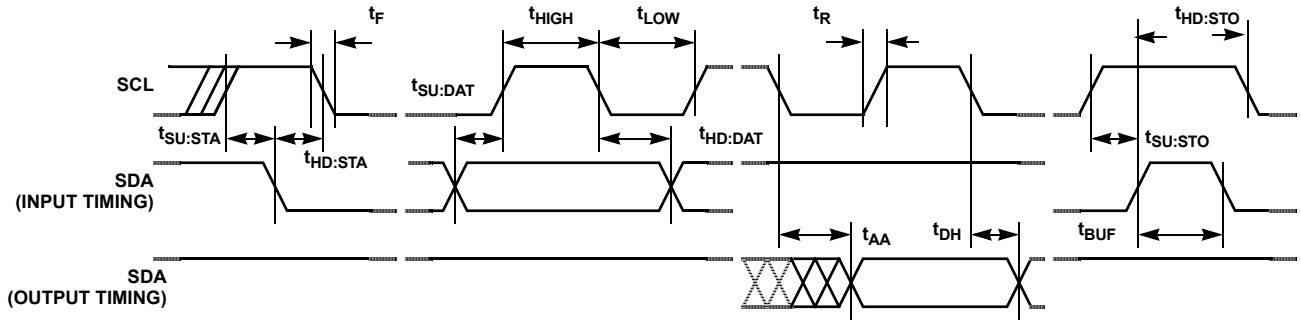


FIGURE 1. BUS TIMING

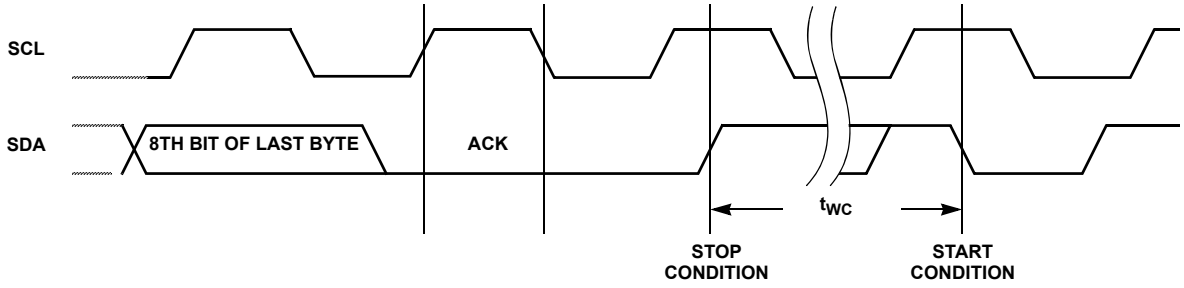
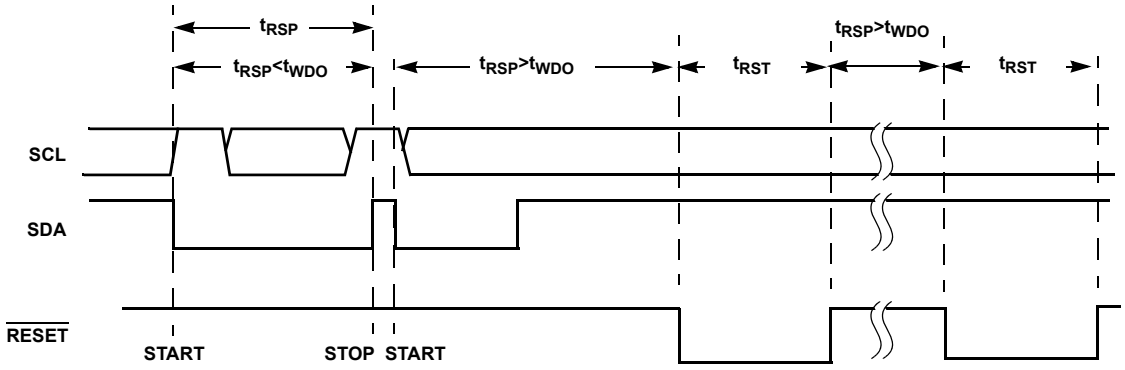


FIGURE 2. WRITE CYCLE TIMING



Note: All inputs are ignored during the active reset period (t_{RST}).

FIGURE 3. WATCHDOG TIMING

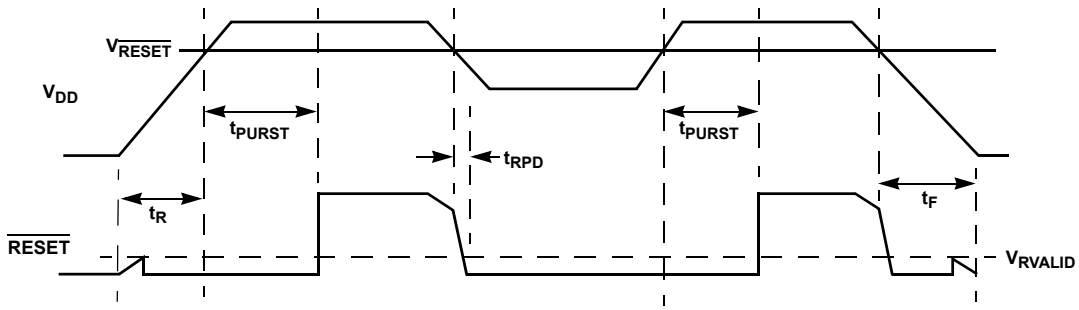


FIGURE 4. RESET TIMING

Typical Performance Curves Temperature is +25°C unless otherwise specified.

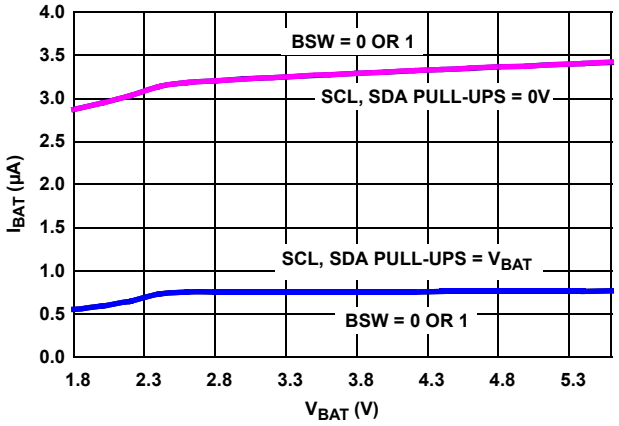


FIGURE 5. I_{BAT} vs V_{BAT}, SBIB = 0

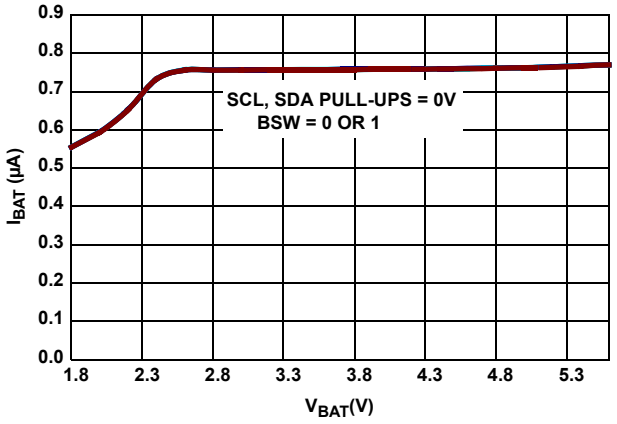


FIGURE 6. I_{BAT} vs V_{BAT}, SBIB = 1

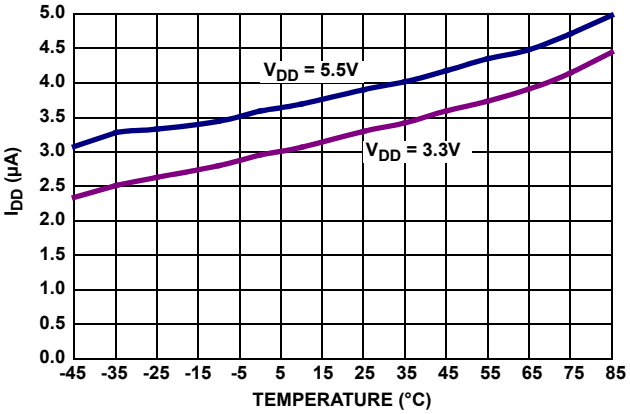


FIGURE 7. I_{DD3} vs TEMPERATURE

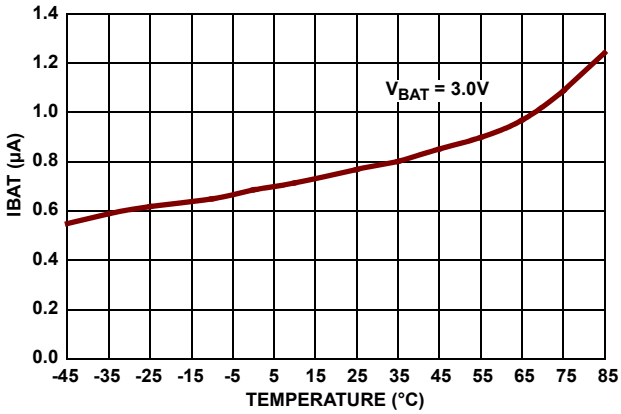


FIGURE 8. I_{BAT} vs TEMPERATURE

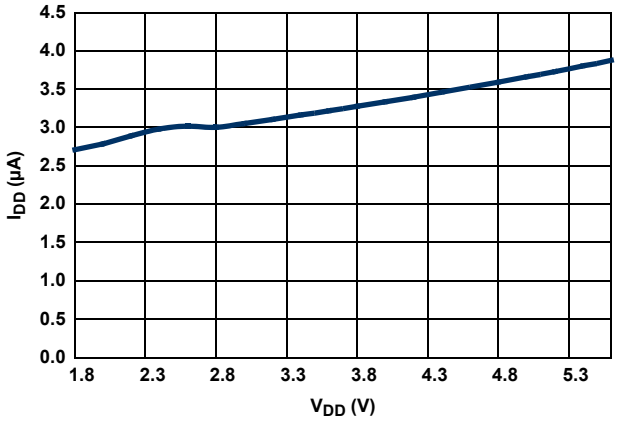


FIGURE 9. I_{DD3} vs V_{DD}

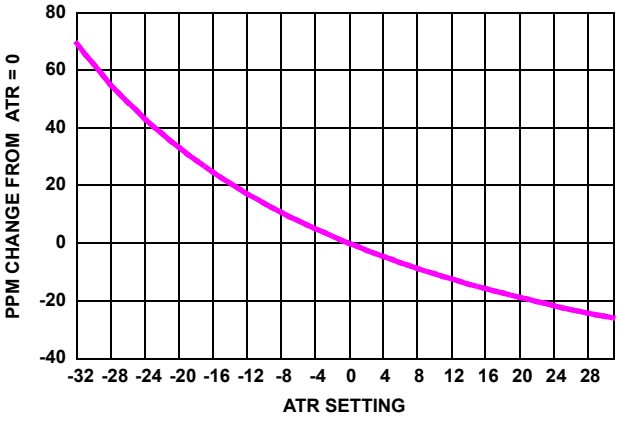


FIGURE 10. ΔF_{OUT} vs ATR SETTING

Description

The ISL12027 device is a Real Time Clock with clock/calendar, two polled alarms with integrated 512x8 EEPROM configured in 16 Byte per page format, oscillator compensation, CPU Supervisor (Power on Reset, Low Voltage Sensing and Watchdog Timer) and battery backup switch.

The oscillator uses an external, low-cost 32.768kHz crystal. All compensation and trim components are integrated on the chip. This eliminates several external discrete components and a trim capacitor, saving board area and component cost.

The Real-Time Clock keeps track of time with separate registers for Hours, Minutes and Seconds. The Calendar has separate registers for Date, Month, Year and Day-of-week. The calendar is correct through 2099, with automatic leap year correction.

The Dual Alarms can be set to any Clock/Calendar value for a match. For instance, every minute, every Tuesday, or 5:23 AM on March 21. The alarms can be polled in the Status Register. There is a repeat mode for the alarms allowing a periodic interrupt.

The ISL12027 device integrates CPU Supervisory functions (POR, WDT) and Battery Switch. There is Power-On-Reset ($\overline{\text{RESET}}$) output with 250ms delay from power on. It will also assert $\overline{\text{RESET}}$ when V_{DD} goes below the specified threshold. The V_{trip} threshold is selectable via VTS2/VTS1/VTS0 registers to five (5) preselected levels. There is Watchdog Timer (WDT) with 3 selectable time-out periods (0.25s, 0.75s and 1.75s) and disabled setting. The Watchdog Timer activates the $\overline{\text{RESET}}$ pin when it expires.

The device offers a backup power input pin. This V_{BAT} pin allows the device to be backed up by battery or SuperCap. The entire ISL12027 device is fully operational from 2.7V to 5.5V and the clock/calendar portion of the ISL12027 device remains fully operational down to 1.8V (Standby Mode).

The ISL12027 device provides 4k bits of EEPROM with 8 modes of BlockLock™ control. The BlockLock™ allows a safe, secure memory for critical user and configuration data, while allowing a large user storage area.

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device. The input buffer on this pin is always active (not gated). The pull-up resistor on this pin must use the same voltage source as V_{DD}.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. The input buffer is always active (not gated).

This open drain output requires the use of a pull-up resistor. The pull-up resistor on this pin must use the same voltage source as V_{DD}. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speed.

V_{BAT}

This input provides a backup supply voltage to the device. V_{BAT} supplies power to the device in the event the V_{DD} supply fails. This pin can be connected to a battery, a SuperCap or tied to ground if not used.

Note that the device is not guaranteed to operate with V_{BAT} < 1.8V. If the battery voltage is expected to drop lower than this minimum, correct operation of the device, (especially after a V_{DD} power-down cycle) is not guaranteed.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ signal output can be used to notify a host processor that the Watchdog timer has expired or the V_{DD} voltage supply has dipped below the $V_{\overline{\text{RESET}}}$ threshold. It is an open drain, active LOW output. Recommended value for the pull-up resistor is 5kΩ. If unused it can be tied to ground.

In battery mode, the Watchdog timer function is disabled. The $\overline{\text{RESET}}$ signal output is asserted LOW when the VDD voltage supply has dipped below the $V_{\overline{\text{RESET}}}$ threshold but the $\overline{\text{RESET}}$ signal output will not return HIGH until the device is back to V_{DD} mode (out of Battery Backup mode) even if the V_{DD} voltage is above $V_{\overline{\text{RESET}}}$ threshold.

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL12027 to supply a timebase for the real time clock. Internal compensation circuitry provides high accuracy over the operating temperature range from -40°C to +85°C. This oscillator compensation network can be used to calibrate the crystal timing accuracy over temperature either during manufacturing or with an external temperature sensor and microcontroller for active compensation. X2 is intended to drive a crystal only, and should not drive any external circuit (Figure 11).

NO EXTERNAL COMPENSATION RESISTORS OR CAPACITORS ARE NEEDED OR ARE RECOMMENDED TO BE CONNECTED TO THE X1 AND X2 PINS.

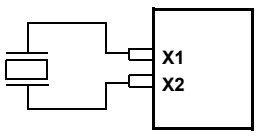


FIGURE 11. RECOMMENDED CRYSTAL CONNECTION

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of the second, minute, hour, day, date, month and year. The RTC has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12027 powers up after the loss of both V_{DD} and V_{BAT}, the clock will not operate until at least one byte is written to the clock register.

Reading the Real Time Clock

The RTC is read by initiating a Read command and specifying the address corresponding to the register of the Real Time Clock. The RTC Registers can then be read in a Sequential Read Mode. Since the clock runs continuously and read takes a finite amount of time, there is a possibility that the clock could change during the course of a read operation. In this device, the time is latched by the read command (falling edge of the clock on the ACK bit prior to RTC data output) into a separate latch to avoid time changes during the read operation. The clock continues to run. Alarms occurring during a read are unaffected by the read operation.

Writing to the Real Time Clock

The time and date may be set by writing to the RTC registers. RTC Register should be written ONLY with Page Write. To avoid changing the current time by an uncompleted write operation, write to the all 8 bytes in one write operation. When writing the RTC registers, the new time value is loaded into a separate buffer at the falling edge of the clock during the Acknowledge. This new RTC value is loaded into the RTC Register by a stop bit at the end of a valid write sequence. An invalid write operation aborts the time update procedure and the contents of the buffer are discarded. After a valid write operation, the RTC will reflect the newly loaded data beginning with the next “one second” clock cycle after the stop bit is written. The RTC continues to update the time while an RTC register write is in progress and the RTC continues to run during any non-volatile write sequences.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the accuracy of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal’s nominal frequency. For example, a >20ppm frequency deviation translates into an accuracy of >1 minute per month. These parameters are available from the crystal manufacturer. Intersil’s RTC family provides on-chip crystal compensation networks to adjust load-capacitance to tune oscillator frequency from -34ppm to +80ppm when using a 12.5pF load crystal. For more detailed information see “Application Section” on page 22.

Clock/Control Registers (CCR)

The Control/Clock Registers are located in an area separate from the EEPROM array and are only accessible following a slave byte of “1101111x” and reads or writes to addresses [0000h:003Fh]. The clock/control memory map has memory addresses from 0000h to 003Fh. The defined addresses are described in Table 2. Writing to and reading from the undefined addresses are not recommended.

CCR Access

The contents of the CCR can be modified by performing a byte or a page write operation directly to any address in the CCR. Prior to writing to the CCR (except the status register), however, the WEL and RWEL bits must be set using a three step process (see “Writing to the Clock/Control Registers” on page 14).

The CCR is divided into 5 sections. These are:

1. Alarm 0 (8 bytes; non-volatile)
2. Alarm 1 (8 bytes; non-volatile)
3. Control (5 bytes; non-volatile)
4. Real Time Clock (8 bytes; volatile)
5. Status (1 byte; volatile)

Each register is read and written through buffers. The non-volatile portion (or the counter portion of the RTC) is updated only if RWEL is set and only after a valid write operation and stop bit. A sequential read or page write operation provides access to the contents of only one section of the CCR per operation. Access to another section requires a new operation. A read or write can begin at any address in the CCR.

It is not necessary to set the RWEL bit prior to writing the status register. Section 5 (status register) supports a single byte read or write only. Continued reads or writes from this section terminates the operation.

The state of the CCR can be read by performing a random read at any address in the CCR at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. The read instruction latches all Clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read of the CCR will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read of the CCR, the address remains at the previous address +1 so the user can execute a current address read of the CCR and continue reading the next Register.

Real Time Clock Registers (Volatile)

SC, MN, HR, DT, MO, YR: Clock/Calendar Registers

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 00 to 59, HR (Hour) is 1 to 12 with an AM or PM indicator (H21 bit) or 0

to 23 (with MIL = 1), DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99.

DW: Day of the Week Register

This register provides a Day of the Week status and uses three bits DY2 to DY0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as ‘0’.

Y2K: Year 2000 Register

Can have value 19 or 20. As of the date of the introduction of this device, there would be no real use for the value 19 in a true real time clock, however.

24 Hour Time

If the MIL bit of the HR register is 1, the RTC uses a 24-hour format. If the MIL bit is 0, the RTC uses a 12-hour format and H21 bit functions as an AM/PM indicator with a ‘1’, representing PM. The clock defaults to standard time with H21 = 0.

Leap Years

Leap years add the day February 29 and are defined as those years that are divisible by 4.

Status Register (SR) (Volatile)

The Status Register is located in the CCR memory map at address 003Fh. This is a volatile register only and is used to control the WEL and RWEL write enable latches, read power status and two alarm bits. This register is separate from both the array and the Clock/Control Registers (CCR).

TABLE 1. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
003Fh	BAT	AL1	AL0	OSCF	0	RWEL	WEL	RTCF
Default	0	0	0	0	0	0	0	1

BAT: Battery Supply

This bit set to “1” indicates that the device is operating from V_{BAT}, not V_{DD}. It is a read-only bit and is set/reset by hardware (ISL12027 internally). Once the device begins operating from V_{DD}, the device sets this bit to “0”.

AL1, AL0: Alarm Bits

These bits announce if either alarm 0 or alarm 1 match the real time clock. If there is a match, the respective bit is set to ‘1’. The falling edge of the last data bit in a SR Read operation resets the flags. Note: Only the AL bits that are set when an SR read starts will be reset. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

OSCF: Oscillator Fail Indicator

This bit is set to “1” if the oscillator is not operating, or is operating but has clock jitter which does not affect the accuracy of RTC counting. The bit is set to “0” if the oscillator is functioning and does not have clock jitter. This bit is read only, and is set/reset by hardware.

RWEL: Register Write Enable Latch

This bit is a volatile latch that powers up in the LOW (disabled) state. The RWEL bit must be set to “1” prior to any writes to the Clock/Control Registers. Writes to RWEL bit do not cause a non-volatile write cycle, so the device is ready for the next operation immediately after the stop condition. A write to the CCR requires both the RWEL and WEL bits to be set in a specific sequence.

WEL: Write Enable Latch

The WEL bit controls the access to the CCR during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to the CCR address will be ignored, although acknowledgment is still issued. The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the Status Register. Once set, WEL remains set until either reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the Status Register) or until the part powers up again. Writes to WEL bit do not cause a non-volatile write cycle, so the device is ready for the next operation immediately after the stop condition.

RTCF: Real Time Clock Fail Bit

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12027 internally) when the device powers up after having lost all power to the device (both V_{DD} and V_{BAT} go to 0V). The bit is set regardless of whether V_{DD} or V_{BAT} is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. On power up after a total power failure, all registers are set to their default states and the clock will not increment until at least one byte is written to the clock register. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

Unused Bits:

Bit 3 in the SR is not used, but must be zero. The Data Byte output during a SR read will contain a zero in this bit location.

TABLE 2. CLOCK/CONTROL MEMORY MAP

ADDR.	TYPE	REG NAME	BIT 7	6	5	4	3	2	1	0	RANGE	ISL12027 DEFAULT	ISL12027A DEFAULT
003F	Status	SR	BAT	AL1	AL0	OSCF	0	RWEL	WEL	RTCF		01h	01h
0037	RTC (SRAM)	Y2K	0	0	Y2K21	Y2K20	Y2K13	0	0	Y2K10	19/20	20h	20h
0036		DW	0	0	0	0	0	DY2	DY1	DY0	0-6	00h	00h
0035		YR	Y23	Y22	Y21	Y20	Y13	Y12	Y11	Y10	0-99	00h	00h
0034		MO	0	0	0	G20	G13	G12	G11	G10	1-12	00h	00h
0033		DT	0	0	D21	D20	D13	D12	D11	D10	1-31	01h	01h
0032		HR	MIL	0	H21	H20	H13	H12	H11	H10	0-23	00h	00h
0031		MN	0	M22	M21	M20	M13	M12	M11	M10	0-59	00h	00h
0030		SC	0	S22	S21	S20	S13	S12	S11	S10	0-59	00h	00h
0014	Control (EEPROM)	PWR	SBIB	BSW	0	0	0	VTS2	VTS1	VTS0		**4Xh**	**0Xh**
0013		DTR	0	0	0	0	0	DTR2	DTR1	DTR0		00h	00h
0012		ATR	0	0	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0		00h	00h
0011		INT	IM	AL1E	AL0E	0	0	0	0	0		00h	00h
0010		BL	BP2	BP1	BP0	WD1	WD0	0	0	0		18h	18h
000F	Alarm1 (EEPROM)	Y2K1	0	0	A1Y2K21	A1Y2K20	A1Y2K13	0	0	A1Y2K10	19/20	20h	20h
000E		DWA1	EDW1	0	0	0	0	DY2	DY1	DY0	0-6	00h	00h
000D		YRA1	Unused - Default = RTC Year value (No EEPROM) - Future expansion										
000C		MOA1	EMO1	0	0	A1G20	A1G13	A1G12	A1G11	A1G10	1-12	00h	00h
000B		DTA1	EDT1	0	A1D21	A1D20	A1D13	A1D12	A1D11	A1D10	1-31	00h	00h
000A		HRA1	EHR1	0	A1H21	A1H20	A1H13	A1H12	A1H11	A1H10	0-23	00h	00h
0009		MNA1	EMN1	A1M22	A1M21	A1M20	A1M13	A1M12	A1M11	A1M10	0-59	00h	00h
0008		SCA1	ESC1	A1S22	A1S21	A1S20	A1S13	A1S12	A1S11	A1S10	0-59	00h	00h
0007	Alarm0 (EEPROM)	Y2K0	0	0	A0Y2K21	A0Y2K20	A0Y2K13	0	0	A0Y2K10	19/20	20h	20h
0006		DWA0	EDW0	0	0	0	0	DY2	DY1	DY0	0-6	00h	00h
0005		YRA0	Unused - Default = RTC Year value (No EEPROM) - Future expansion										
0004		MOA0	EMO0	0	0	A0G20	A0G13	A0G12	A0G11	A0G10	1-12	00h	00h
0003		DTA0	EDT0	0	A0D21	A0D20	A0D13	A0D12	A0D11	A0D10	1-31	00h	00h
0002		HRA0	EHR0	0	A0H21	A0H20	A0H13	A0H12	A0H11	A0H10	0-23	00h	00h
0001		MNA0	EMN0	A0M22	A0M21	A0M20	A0M13	A0M12	A0M11	A0M10	0-59	00h	00h
0000		SCA0	ESC0	A0S22	A0S21	A0S20	A0S13	A0S12	A0S11	A0S10	0-59	00h	00h

NOTE: (Shaded cells indicate that NO other value is to be written to that bit. X indicates the bits are set according to the product variation, see device “Ordering Information” on page 2).

Alarm Registers (Non-Volatile)

Alarm0 and Alarm1

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match. See “Device Operation” on page 14 and “Application Section” on page 22 for more information.

Control Registers (Non-Volatile)

The Control Bits and Registers described in the following section are non-volatile.

BL Register

BP2, BP1, BP0 - Block Protect Bits

The Block Protect Bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of eight segments of the array. The partitions are described in Table 3.

TABLE 3.

BP2	BP1	BP0	PROTECTED ADDRESSES ISL12027	ARRAY LOCK
0	0	0	None (Default)	None
0	0	1	180_h – $1FF_h$	Upper 1/4
0	1	0	100_h – $1FF_h$	Upper 1/2
0	1	1	000_h – $1FF_h$	Full Array
1	0	0	000_h – $03F_h$	First 4 Pages
1	0	1	000_h – $07F_h$	First 8 Pages
1	1	0	000_h – $0FF_h$	First 16 Pages
1	1	1	000_h – $1FF_h$	Full Array

Oscillator Compensation Registers

There are two trimming options.

- ATR. Analog Trimming Register
- DTR. Digital Trimming Register

These registers are non-volatile. The combination of analog and digital trimming can give up to -64 to +110ppm of total adjustment.

ATR Register - ATR5, ATR4, ATR3, ATR2, ATR1, ATR0: Analog Trimming Register

Six analog trimming bits, ATR0 to ATR5, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. For example, using a Citizen CFS-206 crystal with different ATR bit combinations provides an estimated ppm adjustment range from -34ppm to +80ppm to the nominal frequency compensation.

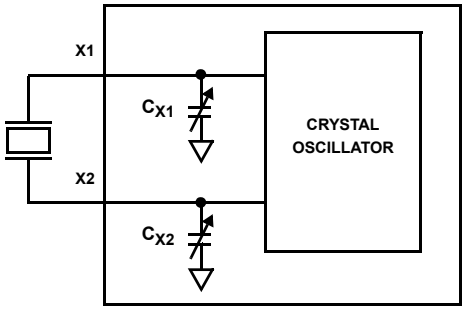


FIGURE 12. DIAGRAM OF ATR

The effective on-chip series load capacitance, C_{LOAD}, ranges from 4.5pF to 20.25pF with a mid-scale value of 12.5pF (default). C_{LOAD} is changed via two digitally controlled capacitors, C_{X1} and C_{X2}, connected from the X1 and X2 pins to ground (see Figure 12). The value of C_{X1} and C_{X2} is given Equation 1:

$$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)\text{pF} \quad \text{(EQ. 1)}$$

The effective series load capacitance is the combination of C_{X1} and C_{X2}:

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)} \quad \text{(EQ. 2)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right)\text{pF}$$

For example, C_{LOAD}(ATR = 00000) = 12.5pF, C_{LOAD}(ATR = 100000) = 4.5pF, and C_{LOAD}(ATR = 011111) = 20.25pF. The entire range for the series combination of load capacitance goes from 4.5pF to 20.25pF in 0.25pF steps. Note that these are typical values.

DTR Register - DTR2, DTR1, DTR0: Digital Trimming Register

The digital trimming Bits DTR2, DTR1 and DTR0 adjust the number of counts per second and average the ppm error to achieve better accuracy.

DTR2 is a sign bit. DTR2 = 0 means frequency compensation is >0. DTR2 = 1 means frequency compensation is <0.

DTR1 and DTR0 are scale bits. DTR1 gives 10ppm adjustment and DTR0 gives 20ppm adjustment.

A range from -30ppm to +30ppm can be represented by using the three DTR bits.

TABLE 4. DIGITAL TRIMMING REGISTERS

DTR REGISTER			ESTIMATED FREQUENCY PPM
DTR2	DTR1	DTR0	
0	0	0	0
0	1	0	+10
0	0	1	+20
0	1	1	+30
1	0	0	0
1	1	0	-10
1	0	1	-20
1	1	1	-30

PWR Register: SBIB, BSW, VTS2, VTS1, VTS0

SBIB: Serial Bus Interface (Enable)

The serial bus can be disabled in battery backup mode by setting this bit to “1”. This will minimize power drain on the battery. The Serial Interface can be enabled in battery backup mode by setting this bit to “0” (default is “0”). See “Power Control Operation” on page 15 and “RESET” on page 9.

BSW: Power Control Bit

The Power Control bit, BSW, determines the conditions for switching between V_{DD} and Backup Battery. There are two options:

Option 1. Standard: Set “BSW = 0” (default for ISL12027A)

Option 2. Legacy /Default Mode: Set “BSW = 1” (default for ISL12027)

See “Power Control Operation” on page 15 for more details. Also see “I^2C Communications During Battery Backup and LVR Operation” on page 24 for important details.

VTS2, VTS1, VTS0: $V_{\overline{RESET}}$ Select Bits

The ISL12027 is shipped with a default V_{DD} threshold ($V_{\overline{RESET}}$) per the “Ordering Information” table on page 2. This register is a non-volatile with no protection, therefore any writes to this location can change the default value from that marked on the package. If not changed with a non-volatile write, this value will not change over normal operating and storage conditions. However, ISL12027 has four (4) additional selectable levels to fit the customers application. Levels are: 4.64V (default), 4.38V, 3.09V, 2.92V and 2.63V. The $V_{\overline{RESET}}$ selection is via 3 bits (VTS2, VTS1 and VTS0). See Table 5.

Care should be taken when changing the $V_{\overline{RESET}}$ select bits. If the $V_{\overline{RESET}}$ voltage selected is higher than V_{DD}, then the device will go into RESET and unless V_{DD} is increased, the device will no longer be able to communicate using the I^2C bus.

TABLE 5.

VTS2	VTS1	VTS0	$V_{\overline{RESET}}$
0	0	0	4.64V
0	0	1	4.38V
0	1	0	3.09V
0	1	1	2.92V
1	0	0	2.63V

In battery mode, the $\overline{RESET}$ signal output is asserted LOW when the VDD voltage supply has dipped below the $V_{\overline{RESET}}$ threshold, but the $\overline{RESET}$ signal output will not return HIGH until the device is back to V_{DD} mode even the V_{DD} voltage is above $V_{\overline{RESET}}$ threshold.

Device Operation

Writing to the Clock/Control Registers

Changing any of the bits of the clock/control registers requires the following steps:

1. Write a 02h to the Status Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a start and ended with a stop).
2. Write a 06h to the Status Register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation proceeded by a start and ended with a stop).

Write all 8 bytes to the RTC registers, or one byte to the SR, or one to five bytes to the control registers. This sequence starts with a start bit, requires a slave byte of “11011110” and an address within the CCR and is terminated by a stop bit. A write to the EEPROM registers in the CCR will initiate a non-volatile write cycle and will take up to 20ms to complete. A write to the RTC registers (SRAM) will require much shorter cycle time (t = t_{BUF}). Writes to undefined areas have no effect. The RWEL bit is reset by the completion of a write to the CCR, so the sequence must be repeated to again initiate another change to the CCR contents. If the sequence is not completed for any reason (by sending an incorrect number of bits or sending a start instead of a stop, for example) the RWEL bit is not reset and the device remains in an active mode. Writing all zeros to the status register resets both the WEL and RWEL bits. A read operation occurring between any of the previous operations will not interrupt the register write operation.

Alarm Operation

Since the alarm works as a comparison between the alarm registers and the RTC registers, it is ideal for notifying a host processor of a particular time event and trigger some action as a result. The host can be notified by polling the Status Register (SR) Alarm bits. These two volatile bits (AL1 for Alarm 1 and AL0 for Alarm 0), indicate if an alarm has happened. The AL1 and AL0 bits in the status register are reset by the falling edge of the eighth clock of status register read.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

1. **Single Event Mode** is enabled by setting the AL0E or AL1E bit to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the AL0 or AL1 bit is set to “1”. Once the AL0 or AL1 bit is read, this will automatically reset it. Both Alarm registers can be set at the same time to trigger alarms. Polling the SR will reveal which alarm has been set.
2. **Interrupt Mode** (or “Pulsed Interrupt Mode” or PIM) is enabled by setting the AL0E or AL1E bit to “1” the IM bit to “1”, and disabling the frequency output. If both AL0E and AL1E bits are set to 1, then only the AL0E PIM alarm will function (AL0E overrides AL1E). This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading. Interrupt Mode CANNOT be used for general periodic alarms, however, since a specific time period cannot be programmed for interrupt, only matches to a specific time of day. The interrupt mode is only stopped by disabling the IM bit or the Alarm Enable bits.

Writing to the Alarm Registers

The Alarm Registers are non-volatile but require special attention to insure a proper non-volatile write takes place. Specifically, byte writes to individual registers are good for all but registers 0006h and 0000Eh, which are the DWA0 and DWA1 registers, respectively. Those registers will require a special page write for non-volatile storage. The recommended page write sequences are as follows:

1. **16-byte page writes:** The best way to write or update the Alarm Registers is to perform a 16-byte write beginning at address 0001h (MNA0) and wrapping around and ending at address 0000h (SCA0). This will insure that non-volatile storage takes place. This means that the code must be designed so that the Alarm0 data is written starting with Minutes register, and then all the Alarm1 data, with the last byte being the Alarm0 Seconds (the page ends at the Alarm1 Y2k register and then wraps around to address 0000h).

   Alternatively, the 16-byte page write could start with address 0009h, wrap around and finish with address 0008h. Note that any page write ending at address 0007h or 000Fh (the highest byte in each Alarm) will not trigger a non-volatile write, so wrapping around or overlapping to the following Alarm's Seconds register is advised.

2. **Other non-volatile writes:** It is possible to do writes of less than an entire page, but the final byte must always be addresses 0000h through 0004h or 0008h though 000Ch to trigger a non-volatile write. Writing to those blocks of 5 bytes sequentially, or individually, will trigger a non-volatile write. If the DWA0 or DWA1 registers need to be set, then enough bytes will need to be written to overlap with the other Alarm register and trigger the non-volatile write. For Example, if the DWA0 register is being set, then the code can start with a multiple byte write beginning at address 0006h, and then write 3 bytes ending with the SCA1 register as follows:

   Addr Name
   0006h DWA0
   0007h Y2K0
   0008h SCA1

If the Alarm1 is used, SCA1 would need to have the correct data written.

Power Control Operation

The power control circuit accepts a V_{DD} and a V_{BAT} input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power an Intersil RTC device for up to 10 years. Another option is to use a SuperCap for applications where V_{DD} is interrupted for up to a month. See “Application Section” on page 22 for more information.

There are two options for setting the change-over conditions from V_{DD} to Battery backup mode. The BSW bit in the PWR register controls this operation.

Option 1 - Standard Mode: Set “BSW = 0” (default for ISL12027A)

Option 2 - Legacy/Default Mode: Set “BSW = 1” (default for ISL12027)

TABLE 6. V_{BAT} TRIP POINT WITH DIFFERENT BSW SETTING

BSW BIT	V_{BAT} TRIP POINT (V)	POWER CONTROL SETTING
0	2.2	Standard Mode (ISL12027A)
1	0	Legacy Mode (ISL12027)

Note that applications that have $V_{BAT} > V_{DD}$ will require theISL12027A (standard mode) for proper start-up. The I^2C bus may or may not be operational during battery backup; that function is controlled by the SBIB bit. That operation is covered after the power control section.

OPTION 1 - STANDARD POWER CONTROL MODE (ISL12027A)

In the Standard mode, the supply will switch over to the battery when V_{DD} drops below V_{TRIP} or V_{BAT}, whichever is lower. In this mode, accidental operation from the battery is prevented since the battery backup input will only be used when the V_{DD} supply is shut off.

To select Option 1, BSW bit in the Power Register must be set to “BSW = 0”. A description of power switchover follows.

Standard Mode Power Switchover

- Normal Operating Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, both of the following conditions must be met:

- Condition 1:
  $V_{DD} < V_{BAT} - V_{BATHYS}$
  where $V_{BATHYS} \approx 50mV$
- Condition 2:
  $V_{DD} < V_{TRIP}$
  where $V_{TRIP} \approx 2.2V$
- Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The ISL12027 device will switch from the V_{BAT} to V_{DD} mode when one of the following conditions occurs:

- Condition 1:
  $V_{DD} > V_{BAT} + V_{BATHYS}$
  where $V_{BATHYS} \approx 50mV$
- Condition 2**:**
  $V_{DD} > V_{TRIP} + V_{TRIPHYS}$
  where $V_{TRIPHYS} \approx 30mV$

There are two discrete situations that are possible when using Standard Mode: $V_{BAT} < V_{TRIP}$ and $V_{BAT} > V_{TRIP}$. These two power control situations are illustrated in Figures 13 and 14.

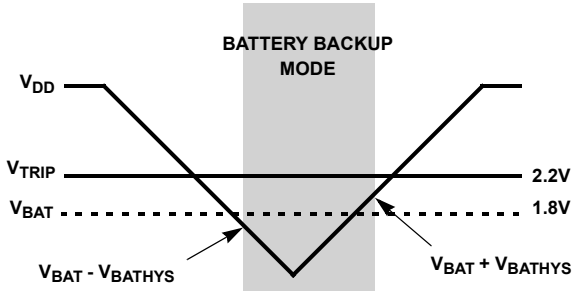


FIGURE 13. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$

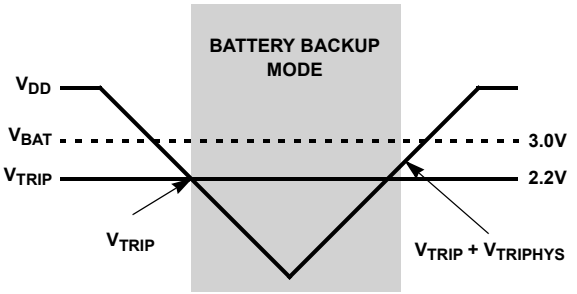


FIGURE 14. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$

OPTION 2 -LEGACY POWER CONTROL MODE (ISL12027 DEFAULT)

The Legacy Mode follows conditions set in X1226 products. In this mode, switching from V_{DD} to V_{BAT} is simply done by comparing the voltages and the device operates from whichever is the higher voltage. Care should be taken when changing from Normal to Legacy Mode. If the V_{BAT} voltage is higher than V_{DD}, then the device will enter battery back up and unless the battery is disconnected or the voltage decreases, the device will no longer operate from V_{DD}. If that is the situation on initial power-up, then I^2C communication may not be possible. For these applications, the ISL12027A should be used.

To select the Option 2, BSW bit in the Power Register must be set to “BSW = 1”.

- Normal Mode (V_{DD}) to Battery Backup Mode (V_{BAT})

To transition from the V_{DD} to V_{BAT} mode, the following conditions must be met:

$V_{DD} < V_{BAT} - V_{BATHYS}$

- Battery Backup Mode (V_{BAT}) to Normal Mode (V_{DD})

The device will switch from the V_{BAT} to V_{DD} mode when the following condition occurs:

$V_{DD} > V_{BAT} + V_{BATHYS}$

The Legacy Mode power control conditions are illustrated in Figure 15.

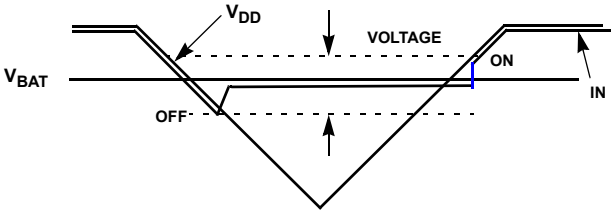


FIGURE 15. BATTERY SWITCHOVER IN LEGACY MODE

Power On Reset

Application of power to the ISL12027 activates a Power On Reset Circuit that pulls the $\overline{RESET}$ pin active. This signal provides several benefits.

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.
- It prevents communication to the EEPROM, greatly reducing the likelihood of data corruption on power-up.

When V_{DD} exceeds the device $V_{\overline{RESET}}$ threshold value for typically 250ms the circuit releases $\overline{RESET}$, allowing the system to begin operation. Recommended slew rate is between 0.2V/ms and 50V/ms.

NOTE: If the V_{BAT} voltage drops below the data sheet minimum of 1.8V and the V_{DD} power cycles to 0V then back to V_{DD} voltage, then the $\overline{RESET}$ output may stay low and the I^2C communications will not operate. The V_{BAT} and V_{DD} power will need to be cycled to 0V together to allow normal operation again.

Watchdog Timer Operation

The Watchdog timer timeout period is selectable. By writing a value to WD1 and WD0, the Watchdog timer can be set to 3 different time out periods or off. When the Watchdog timer is set to off, the watchdog circuit is configured for low power operation (see Table 7).

TABLE 7.

WD1	WD0	DURATION
1	1	disabled
1	0	250ms
0	1	750ms
0	0	1.75s

Watchdog Timer Restart

The Watchdog Timer is started by a falling edge of SDA when the SCL line is high (START condition). The start signal restarts the watchdog timer counter, resetting the period of the counter back to the maximum. If another START fails to be detected prior to the Watchdog timer expiration, then the $\overline{RESET}$ pin becomes active for one reset time out period. In the event that the start signal occurs during a reset time out period, the start will have no effect. When using a single START to refresh Watchdog timer, a STOP condition should be followed to reset the device back to stand-by mode.(see Figure 3).

In battery mode, the Watchdog timer function is disabled.

Low Voltage Reset (LVR) Operation

When a power failure occurs, a voltage comparator compares the level of the V_{DD} line versus a preset threshold voltage ($V_{\overline{RESET}}$), then generates a $\overline{RESET}$ pulse if it is below $V_{\overline{RESET}}$. The reset pulse will timeout 250ms after the V_{DD} line rises above $V_{\overline{RESET}}$. If the V_{DD} remains below $V_{\overline{RESET}}$, then the $\overline{RESET}$ output will remain asserted low. Power-up and power-down waveforms are shown in Figure 4. The LVR circuit is to be designed so the $\overline{RESET}$ signal is valid down to V_{DD} = 1.0V.

When the LVR signal is active, unless the part has been switched into the battery mode, the completion of an in-progress non-volatile write cycle is unaffected, allowing a non-volatile write to continue as long as possible (down to the Reset Valid Voltage). The LVR signal, when active, will terminate any in-progress communications to the device and prevents new commands from disrupting any current write operations. See “I²C Communications During Battery Backup and LVR Operation” on page 24.

In battery mode, the $\overline{RESET}$ signal output is asserted LOW when the VDD voltage supply has dipped below the $V_{\overline{RESET}}$ threshold. The $\overline{RESET}$ signal output will not return HIGH until the device is back to VDD mode even if the VDD voltage is above $V_{\overline{RESET}}$ threshold.

Serial Communication

Interface Conventions

The device supports the I²C Protocol.

Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. (see Figure 16).

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. (see Figure 17).

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. (see Figure 17).

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting 8-bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the 8-bits of data. Refer to Figure 18.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent 8-bit word. The device will not acknowledge if the slave address byte is incorrect.

In the read mode, the device will transmit 8-bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

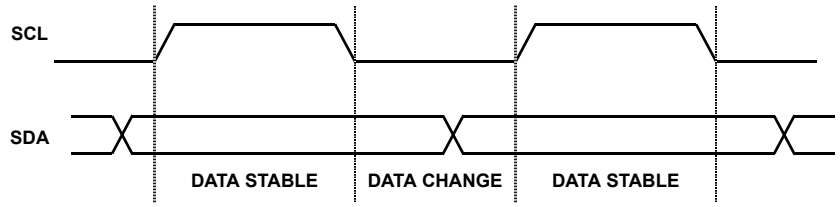


FIGURE 16. VALID DATA CHANGES ON THE SDA BUS

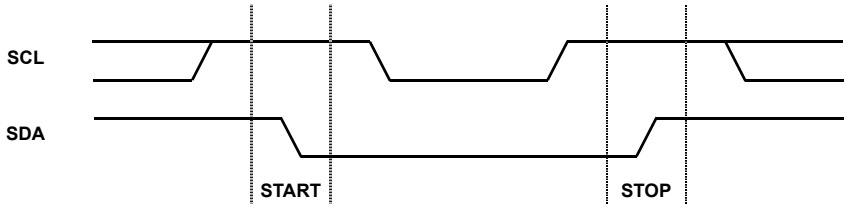


FIGURE 17. VALID START AND STOP CONDITIONS

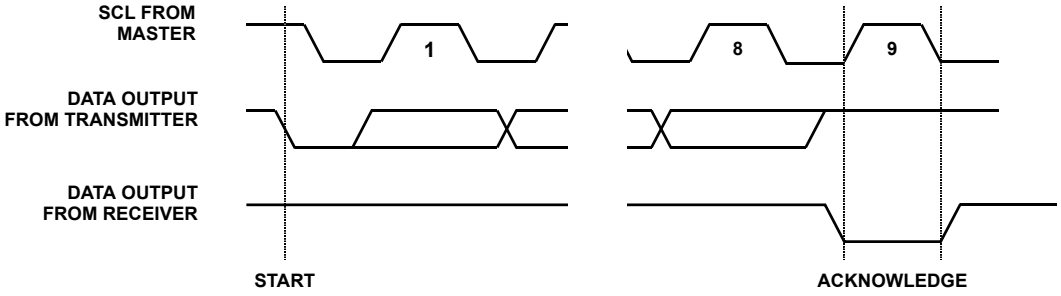


FIGURE 18. ACKNOWLEDGE RESPONSE FROM RECEIVER

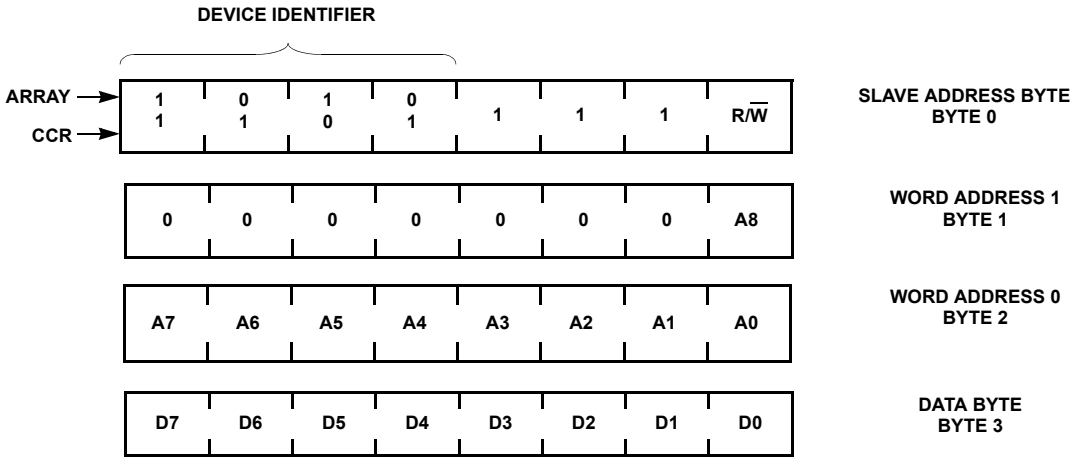


FIGURE 19. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES (64 BYTE PAGES)

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The first 4 bits of the Slave Address Byte specify access to either the EEPROM array or to the CCR. Slave bits ‘1010’ access the EEPROM array. Slave bits ‘1101’ access the CCR.

When shipped from the factory, EEPROM array is UNDEFINED, and should be programmed by the customer to a known state.

Bit 3 through Bit 1 of the slave byte specify the device select bits. These are set to ‘111’.

The last bit of the Slave Address Byte defines the operation to be performed. When this R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 19.

After loading the entire Slave Address Byte from the SDA bus, the ISL12027 compares the device identifier and device select bits with ‘1010111’ or ‘1101111’. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a 2 byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up the internal address counter is set to address 0h, so a current address read of the EEPROM array starts at address 0. When required, as part of a random read, the master must supply the 2 Word Address Bytes as shown in Figure 19.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. That is if the random read is from the array the slave byte must be 1010111x in both instances. Similarly, for a random read of the Clock/Control Registers, the slave byte must be 1101111x in both places.

Write Operations

Byte Write

For a write operation, the device requires the Slave Address Byte and the Word Address Bytes. This gives the master access to any one of the words in the array or CCR. (Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceding operations to enable the write operation. See “Writing to the Clock/Control Registers”). Upon receipt of each address byte, the ISL12027 responds with an acknowledge. After receiving both address bytes the ISL12027 awaits the 8-bits of data. After receiving the 8-data bits, the ISL12027 again responds with an acknowledge. The master then terminates the transfer by generating a stop condition. The ISL12027 then begins an internal write cycle of the data to the non-volatile memory. During the internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance (see Figure 20).

A write to a protected block of memory is ignored, but will still receive an acknowledge. At the end of the write command, the ISL12027 will not initiate an internal write cycle, and will continue to ACK commands.

Byte writes to all of the non-volatile registers are allowed, except the DWAn registers which require multiple byte writes or page writes to trigger non-volatile writes. See “Device Operation” on page 14 for more information.

Page Write

The ISL12027 has a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 15 more bytes to the memory array and up to 7 more bytes to the clock/control registers. The RTC registers require a page write (8 bytes), individual register writes are not allowed. (Note: Prior to writing to the CCR, the master must write a 02h, then 06h to the status register in two preceding operations to enable the write operation. See “Writing to the Clock/Control Registers” on page 14”)

After the receipt of each byte, the ISL12027 responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the page, it “rolls over” and goes back to the first address on the same page. This means that the master can write 16 bytes to a memory array page or 8 bytes to a CCR section starting at any location on that page. For example, if the master begins writing at location 10 of the memory and loads 15 bytes, then the first 6 bytes are written to addresses 10 through 15, and the last 6 bytes are written to columns 0 through 5. Afterwards, the address counter would point to location 6 on the page that was just written. If the master supplies more than the maximum bytes in a page, then the previously loaded data is over-written by the new data, one byte at a time. Refer to Figure 21.The master terminates the Data Byte loading by issuing a stop condition, which causes the ISL12027 to begin the non-volatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 22 for the address, acknowledge and data transfer sequence.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it’s associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the ISL12027 resets itself without performing the write. The contents of the array are not affected.

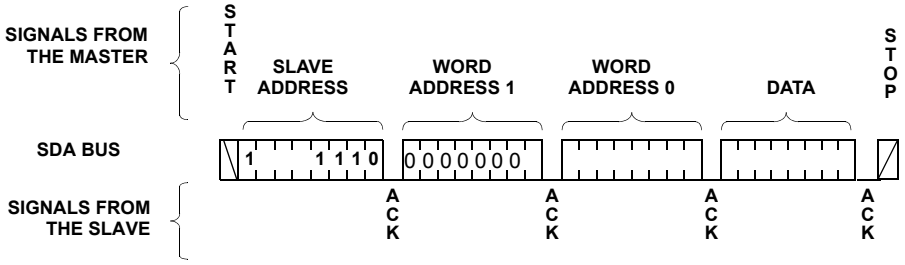


FIGURE 20. BYTE WRITE SEQUENCE

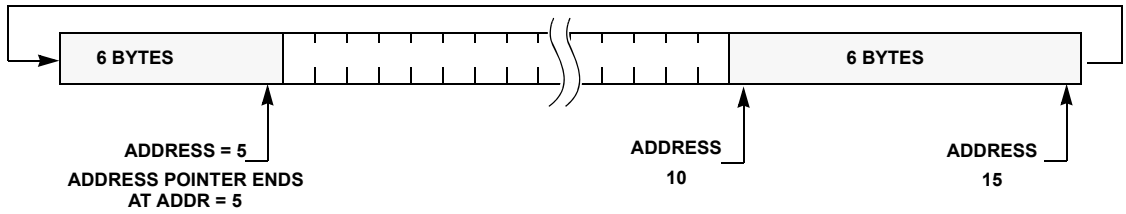


FIGURE 21. WRITING *12* BYTES TO A *16*-BYTE MEMORY PAGE STARTING AT ADDRESS *10*

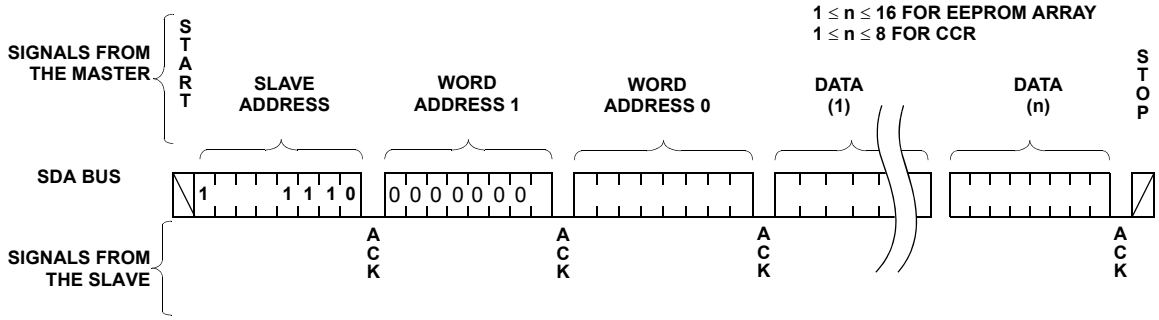


FIGURE 22. PAGE WRITE SEQUENCE

Acknowledge Polling

Disabling of the inputs during non-volatile write cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the ISL12027 initiates the internal non-volatile write cycle. Acknowledge polling can begin immediately. To do this, the master issues a start condition followed by the Memory Array Slave Address Byte for a write or read operation (AEh or AFh). If the ISL12027 is still busy with the non-volatile write cycle, then no ACK will be returned. When the ISL12027 has completed the write operation, an ACK is returned and the host can proceed with the read or write operation. Refer to the flow chart in Figure 24. Note: Do not use the CCR Slave byte (DEh or DFh) for Acknowledge Polling.

Read Operations

There are three basic read operations: Current Address Read, Random Read and Sequential Read.

Current Address Read

Internally the ISL12027 contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n + 1. On power-up, the 16 bit address is initialized to 0h. In this way, a current address read immediately after the power on reset can download the entire contents of memory starting at the first location. Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the ISL12027 issues an acknowledge, then transmits 8 data bits. The master terminates the read operation by not responding with an acknowledge during the ninth clock and issuing a stop condition. Refer to Figure 23 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

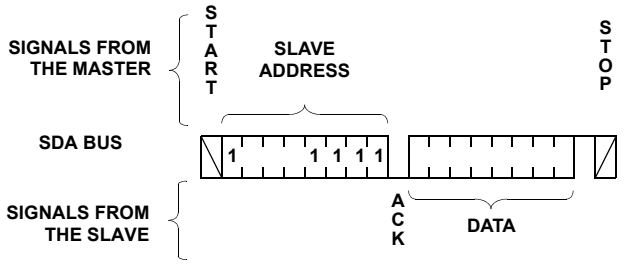


FIGURE 23. CURRENT ADDRESS READ SEQUENCE

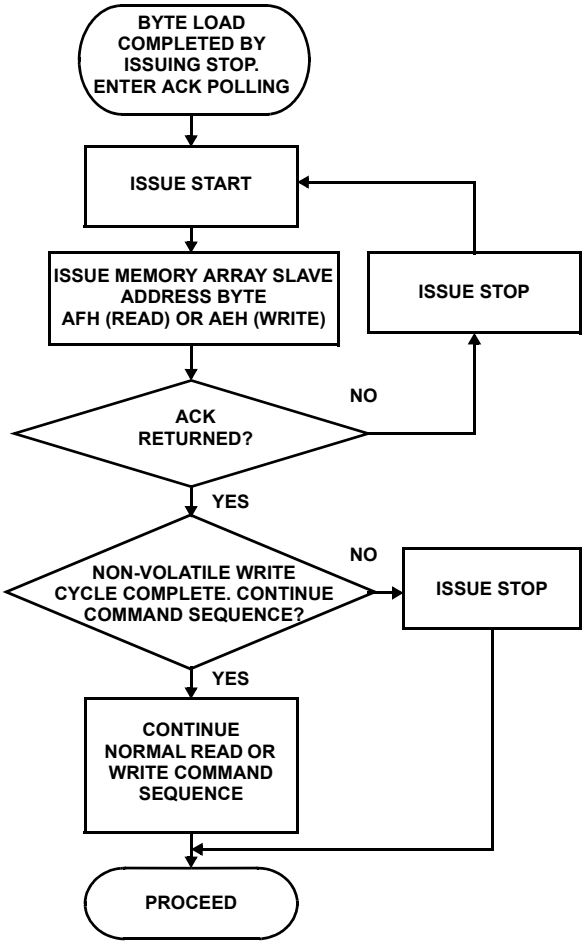


FIGURE 24. ACKNOWLEDGE POLLING SEQUENCE

Random Read

Random read operations allow the master to access any location in the ISL12027. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to zero, the master must first perform a “dummy” write operation.

The master issues the start condition and the slave address byte, receives an acknowledge, then issues the word address bytes. After acknowledging receipt of each word address byte, the master immediately issues another start condition and the slave address byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the 8 bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 25 for the address, acknowledge, and data transfer sequence.

In a similar operation called “Set Current Address,” the device sets the address if a stop is issued instead of the second start shown in Figure 25. The ISL12027 then goes into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first data byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to the start of the address space and the ISL12027 continues to output data for each acknowledge received. Refer to Figure 26 for the acknowledge and data transfer sequence.

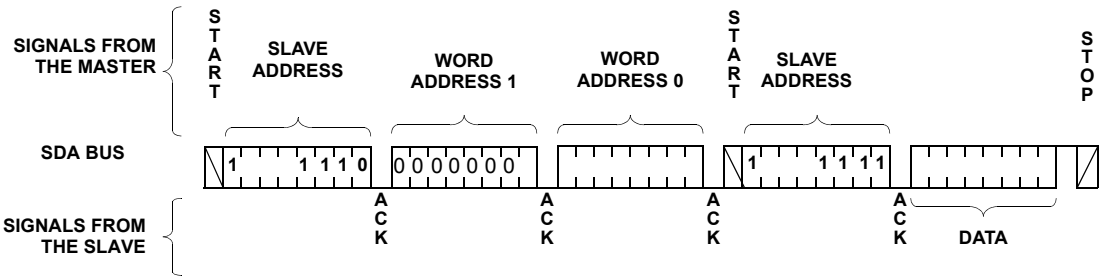


FIGURE 25. RANDOM ADDRESS READ SEQUENCE

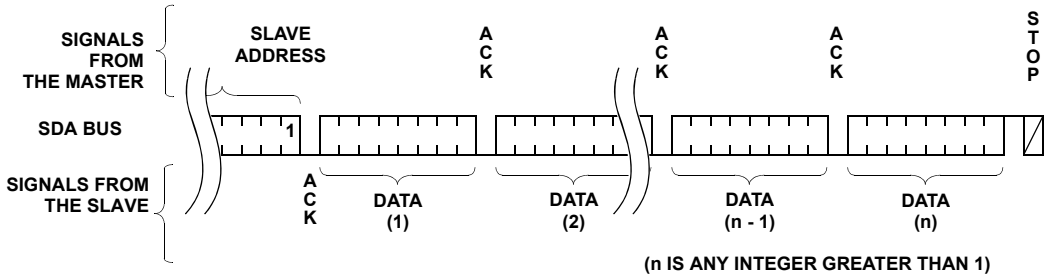


FIGURE 26. SEQUENTIAL READ SEQUENCE

Application Section

Crystal Oscillator and Temperature Compensation

Intersil has now integrated the oscillator compensation circuity on-chip, to eliminate the need for external components and adjust for crystal drift over-temperature and enable very high accuracy time keeping (<5ppm drift).

The Intersil RTC family uses an oscillator circuit with on-chip crystal compensation network, including adjustable load-capacitance. The only external component required is the crystal. The compensation network is optimized for operation with certain crystal parameters which are common in many of the surface mount or tuning-fork crystals available today. Table 8 summarizes these parameters.

Table 9 contains some crystal manufacturers and part numbers that meet the requirements for the Intersil RTC products.

The turnover temperature in Table 8 describes the temperature where the apex of the of the drift vs temperature curve occurs. This curve is parabolic with the drift increasing as $(T - T0)^2$. For an Epson MC-405 device, for example, the turnover temperature is typically +25°C, and a peak drift of >110ppm occurs at the temperature extremes of -40°C and +85°C. It is possible to address this variable drift by adjusting the load capacitance of the crystal, which will result in predictable change to the crystal frequency. The Intersil RTC family allows this adjustment over temperature since the devices include on-chip load capacitor trimming. This control is handled by the Analog Trimming Register, or ATR, which has 6-bits of control. The load capacitance range covered by the ATR circuit is approximately 3.25pF to 18.75pF, in 0.25pF increments. Note that actual capacitance would also include about 2pF of package related capacitance. In-circuit tests with commercially available crystals demonstrate that this range of capacitance allows frequency control from +116ppm to -37ppm, using a 12.5pF load crystal.

In addition to the analog compensation afforded by the adjustable load capacitance, a digital compensation feature is available for the Intersil RTC family. There are 3-bits known as the Digital Trimming Register or DTR, and they operate by adding or skipping pulses in the clock signal. The range provided is ±30ppm in increments of 10ppm. The default setting is 0ppm. The DTR control can be used for coarse adjustments of frequency drift over-temperature or for crystal initial accuracy correction.

A final application for the ATR control is in-circuit calibration for high accuracy applications, along with a temperature sensor chip. Once the RTC circuit is powered up with battery backup, and frequency drift is measured. The ATR control is then adjusted to a setting, which minimizes drift. Once adjusted at a particular temperature, it is possible to adjust at other discrete temperatures for minimal overall drift, and store the resulting settings in the EEPROM. Extremely low overall temperature drift is possible with this method. The Intersil evaluation board contains the circuitry necessary to implement this control.

Layout Considerations

The crystal input at X1 has a very high impedance and will pick up high frequency signals from other circuits on the board. Since the X2 pin is tied to the other side of the crystal, it is also a sensitive node. These signals can couple into the oscillator circuit and

produce double clocking or mis-clocking, seriously affecting the accuracy of the RTC. Care needs to be taken in layout of the RTC circuit to avoid noise pickup. Figure 27 shows a suggested layout for the ISL12027 or ISL12026 devices.

The X1 and X2 connections to the crystal are to be kept as short as possible. A thick ground trace around the crystal is advised to minimize noise intrusion, but ground near the X1 and X2 pins should be avoided as it will add to the load capacitance at those pins. Keep in mind these guidelines for other PCB layers in the vicinity of the RTC device. A small decoupling capacitor at the V_{DD} pin of the chip is mandatory, with a solid connection to ground (see Figure 27).

TABLE 8. CRYSTAL PARAMETERS REQUIRED FOR INTERSIL RTC'S

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Frequency		32.768		kHz	
Frequency Tolerance			±100	ppm	Down to 20ppm if desired
Turnover Temperature	20	25	30	°C	Typically the value used for most crystals
Operating Temperature Range	-40		85	°C	
Parallel Load Capacitance		12.5		pF	
Equivalent Series Resistance			50	kΩ	For best oscillator performance

TABLE 9. CRYSTAL MANUFACTURERS

MANUFACTURER	PART NUMBER	TEMP RANGE (°C)	+25°C FREQUENCY TOLERANCE (ppm)
Citizen	CM201, CM202, CM200S	-40 to +85	±20
Epson	MC-405, MC-406	-40 to +85	±20
Raltron	RSM-200S-A or B	-40 to +85	±20
SaRonix	32S12A or B	-40 to +85	±20
Ecliptek	ECPSM29T-32.768K	-10 to +60	±20
ECS	ECX-306/ECX-306I	-10 to +60	±20
Fox	FSM-327	-40 to +85	±20

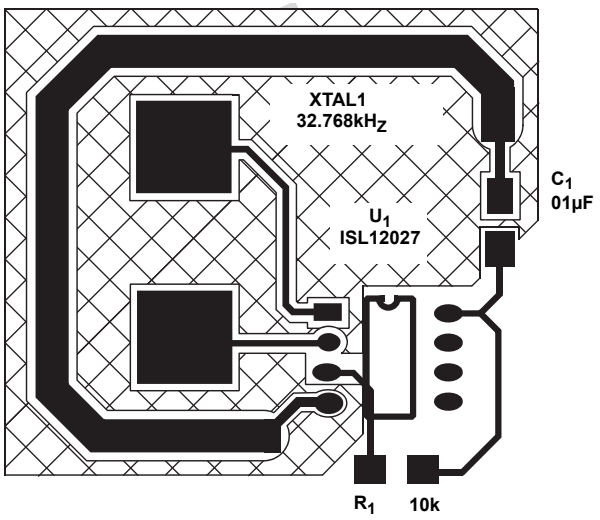


FIGURE 27. SUGGESTED LAYOUT FOR INTERSIL RTC IN SO-8

Oscillator Measurements

When a proper crystal is selected and the layout guidelines above are observed, the oscillator should start up in most circuits in less than one second. Some circuits may take slightly longer, but start-up should definitely occur in less than 5s. When testing RTC circuits, the most common impulse is to apply a scope probe to the circuit at the X2 pin (oscillator output) and observe the waveform. DO NOT DO THIS! Although in some cases you may see a usable waveform, due to the parasitics (usually 10pF to ground) applied with the scope probe, there will be no useful information in that waveform other than the fact that the circuit is oscillating. The X2 output is sensitive to capacitive impedance so the voltage levels and the frequency will be affected by the parasitic elements in the scope probe. Applying a scope probe can possibly cause a faulty oscillator to start-up, hiding other issues (although in the Intersil RTC's, the internal circuitry assures startup when using the proper crystal and layout).

The best way to analyze the RTC circuit is to power it up and read the real time clock as time advances. Alternatively the frequency can be checked by setting an alarm for each minute. Using the pulse interrupt mode setting, the once-per-minute interrupt functions as an indication of proper oscillation.

Backup Battery Operation

Many types of batteries can be used with the Intersil RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power a Intersil RTC device for up to 10 years. Another option is to use a supercapacitor for applications where V_{DD} may disappear intermittently for short periods of time. Depending on the value of supercapacitor used, backup time can last from a few days to two weeks (with

>1F). A simple silicon or Schottky barrier diode can be used in series with V_{DD} to charge the supercapacitor, which is connected to the V_{BAT} pin. Try to use Schottky diodes with very low leakages, <1µA desirable. Do not use the diode to charge a battery (especially lithium batteries!).

Note that whether a battery or supercap is used, if the V_{BAT} voltage drops below the data sheet minimum of 1.8V and the V_{DD} power cycles to 0V then back to V_{DD} voltage, then the $\overline{RESET}$ output may stay low and the I^2C communications will not operate. The V_{BAT} and V_{DD} power will need to be cycled to 0V together to allow normal operation again.

There are two possible modes for battery backup operation, Standard and Legacy mode. In Standard mode, there are no operational concerns when switching over to battery backup since all other devices functions are disabled. Battery drain is minimal in Standard mode, and return to Normal V_{DD} powered operations predictable. In Legacy modes the V_{BAT} pin can power the chip if the voltage is above V_{DD} and V_{TRIP}. This makes it possible to generate alarms and communicate with the device under battery backup, but the supply current drain is much higher than the Standard mode and backup time is reduced. During initial power-up, the default mode is the Legacy mode.

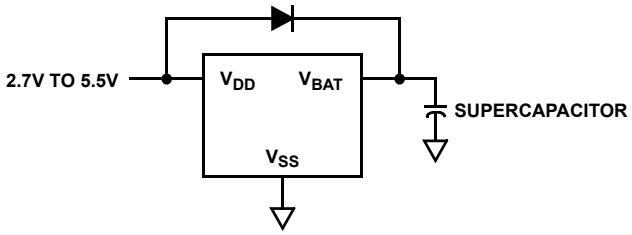


FIGURE 28. SUPERCAPACITOR CHARGING CIRCUIT

I^2C Communications During Battery Backup and LVR Operation

Operation in Battery Backup mode and LVR is affected by the BSW and SBIB bits as described earlier. These bits allow flexible operation of the serial bus and EEPROM in battery backup mode, but certain operational details need to be clear before utilizing the different modes. The most significant detail is that once V_{DD} goes below V_{RESET}, then I^2C communications cease regardless of whether the device is programmed for I^2C operation in battery backup mode.

Table 10 describes 4 different modes possible with using the BSW and SBIB bits, and how they are affect LVR and battery backup operation.

- **Mode A** - In this mode, selection bits indicate a low V_{DD} switchover combined with I^2C operation in battery backup mode. In actuality the V_{DD} will go below $V_{\overline{RESET}}$ before switching to battery backup, which will disable I^2C ANYTIME the device goes into battery backup mode. Regardless of the battery voltage, the I^2C will work down to the $V_{\overline{RESET}}$ voltage (see Figure 29).
- **Mode B** - In this mode, the selection bits indicate switchover to battery backup at $V_{DD}<V_{BAT}$, and I^2C communications in battery backup. In order to communicate in battery backup mode, the $V_{\overline{RESET}}$ voltage must be less than the V_{BAT} voltage AND V_{DD} must be greater than $V_{\overline{RESET}}$. Also, pull-ups on the I^2C bus pins must go to V_{BAT} to communicate. This mode is the same as the normal operating mode of the X1228 device.
- **Mode C** - In this mode, the selection bits indicate a low V_{DD} switchover combined with no communications in battery backup. Operation is actually identical to Mode A with I^2C communications down to $V_{DD} = V_{\overline{RESET}}$, then no communications (see Figure 28).
- **Mode D** - In this mode, the selection bits indicate switchover to battery backup at $V_{DD} < V_{BAT}$, and no I^2C communications in battery backup. This mode is unique in that there is I^2C communication as long as V_{DD} is higher than V_{RESET} or V_{BAT}, whichever is greater. This mode is the safest for guaranteeing I^2C communications only when there is a Valid V_{DD} (see Figure 29).

TABLE 10. I^2C, LV RESET, AND BATTERY BACKUP OPERATION SUMMARY (Shaded Row is same as X12028 operation)

MODE	SBIB BIT	BSW BIT	V_{BAT} SWITCHOVER VOLTAGE	I^2C ACTIVE IN BATTERY BACKUP?	EE PROM WRITE/ READ IN BATTERY BACKUP?	FREQ/IRQ ACTIVE?	NOTES
A	0	0	Standard Mode, V_{TRIP} = 2.2V typ Default for ISL12027A	NO	NO	N/A	Operation of I^2C bus down to $V_{DD} = V_{\overline{RESET}}$, then below that no communications. Battery switchover at V_{TRIP}.
B (X12028 mode)	0	1	Legacy Mode, $V_{DD} < V_{BAT}$ Default for ISL12027	YES, only if $V_{BAT} > V_{\overline{RESET}}$	YES	Yes	Operation of I^2C bus into battery backup mode, but only for $V_{BAT} > V_{DD} > V_{\overline{RESET}}$. Bus must have pull-ups to V_{BAT}. No non-volatile writes with $V_{BAT} > V_{DD}$
C	1	0	Standard Mode, V_{TRIP} = 2.2V typ	NO	NO	YES	Operation of I^2C bus down to $V_{DD} = V_{\overline{RESET}}$, then below that no communications. Battery switchover at V_{TRIP}.
D	1	1	Legacy Mode, $V_{DD} < V_{BAT}$	NO	NO	YES	Operation of I^2C busdown to $V_{\overline{RESET}}$ or V_{BAT}, whichever is higher.

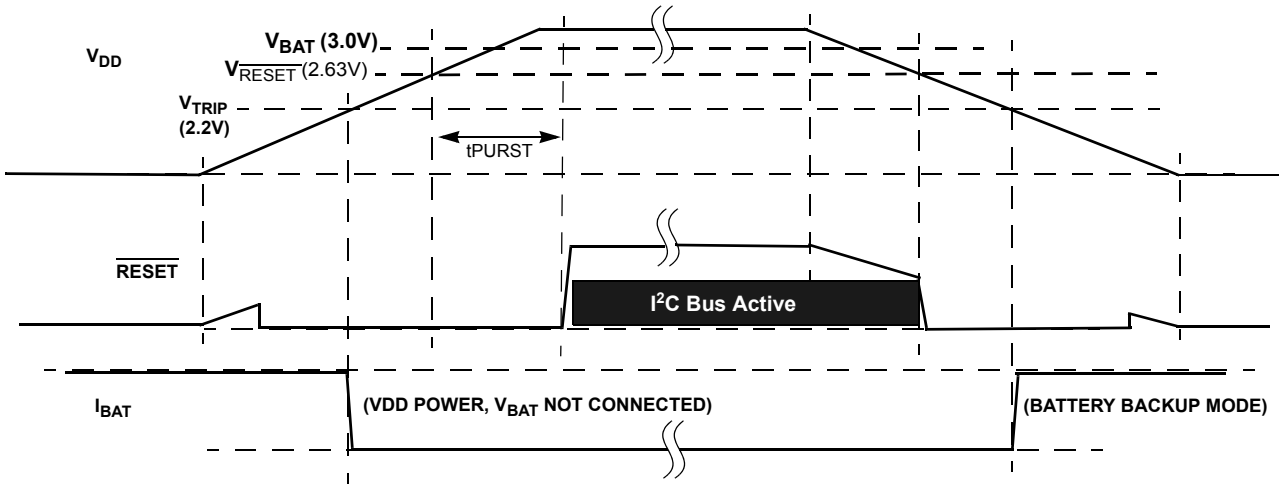


FIGURE 29. EXAMPLE RESET OPERATION IN MODE A OR C

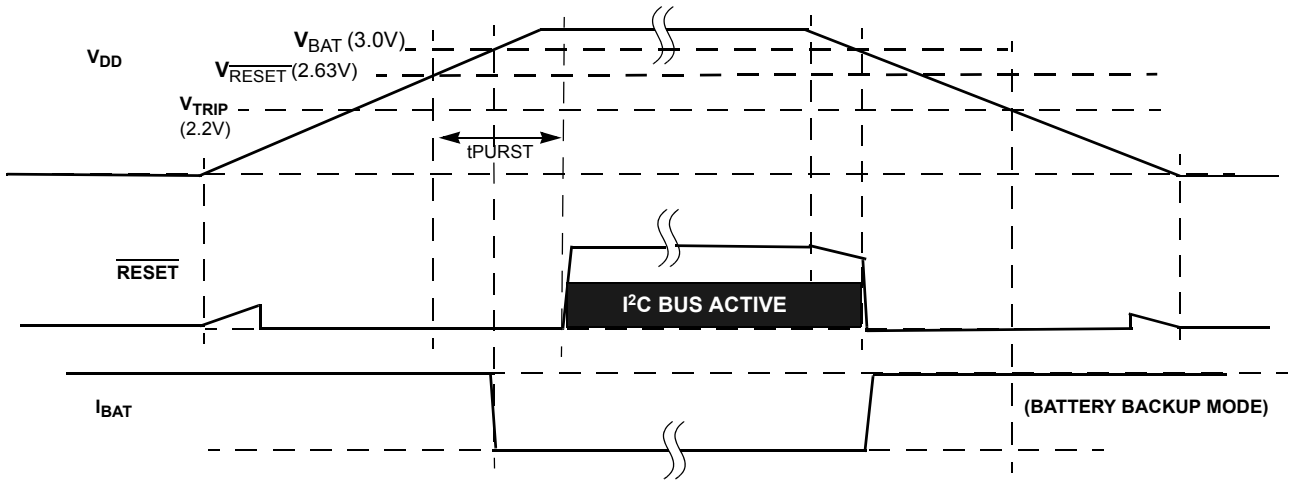


FIGURE 30. RESET OPERATION IN MODE D

Alarm Operation Examples

Following are examples of both Single Event and periodic Interrupt Mode alarms.

EXAMPLE 1

Alarm 0 set with single interrupt (IM=”0”)

A single alarm will occur on January 1 at 11:30am.

A. Set Alarm 0 registers as follows:

ALARM0 REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA0	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA0	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA0	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA0	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Also the AL0E bit must be set as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	0	0	1	0	0	0	0	0	x0h	Enable Alarm

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the AL0 bit in the status register to “1”.

EXAMPLE 2

Pulsed interrupt once per minute (IM = ”1”)

Interrupts at one minute intervals when the seconds register is at 30s.

A. Set Alarm 0 registers as follows:

ALARM0 REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA0	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA0	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA0	0	0	0	0	0	0	0	0	00h	Date disabled
MOA0	0	0	0	0	0	0	0	0	00h	Month disabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Set the Interrupt register as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	1	0	1	0	0	0	0	0	x0h	Enable Alarm and Int Mode

Note that the status register AL0 bit will be set each time the alarm is triggered, but does not need to be read or cleared.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 23, 2015	FN8232.9	- Updated Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M8.15 to latest revision changes are as follows: -Revision 1 to Revision 2 Changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Revision 2 to Revision 3 Changes: Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 Changes: Changed Note 1 "1982" to "1994"

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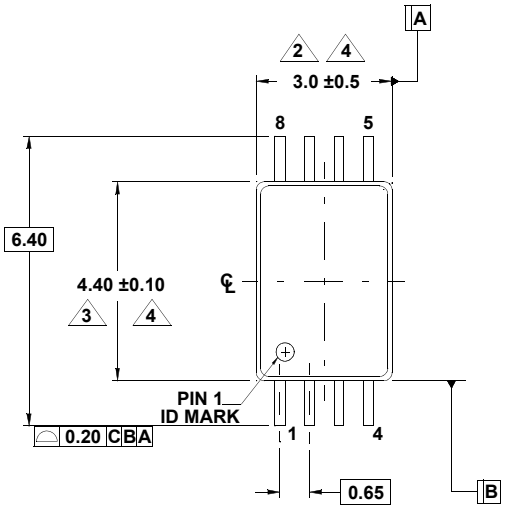
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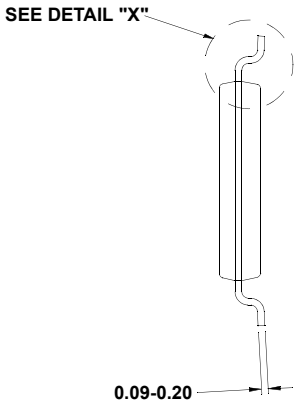
Package Outline Drawing

M8.173

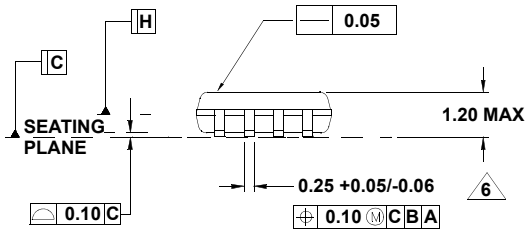
8 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 01/10



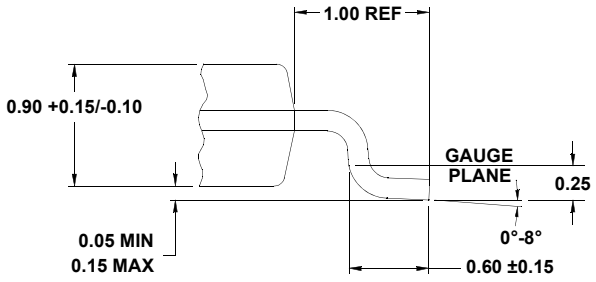
TOP VIEW



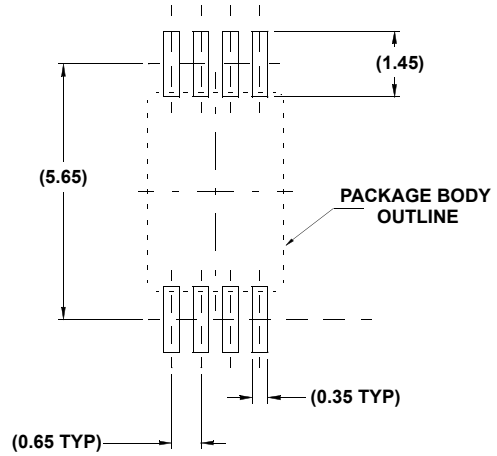
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

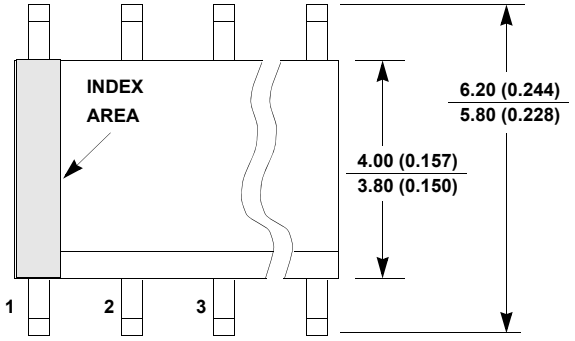
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 per side.
4. Dimensions are measured at datum plane H.
5. Dimensioning and tolerancing per ASME Y14.5M-1994.
6. Dimension on lead width does not include dambar protrusion. Allowable protrusion shall be 0.08 mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
7. Conforms to JEDEC MO-153, variation AC. Issue E

Package Outline Drawing

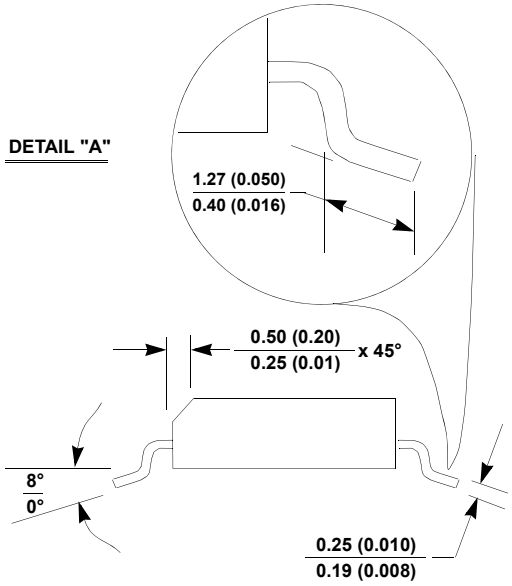
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

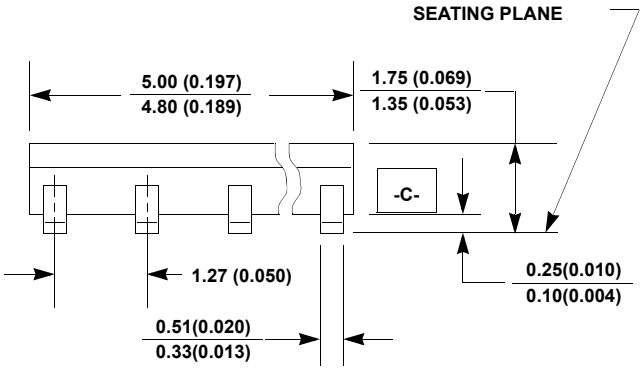
Rev 4, 1/12



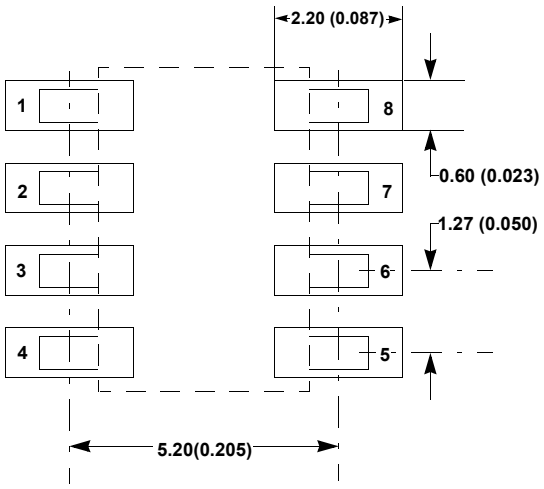
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.