HIN202E, HIN206E, HIN207E, HIN208E, HIN211E, HIN213E, HIN232E

±15kV, ESD-Protected, +5V Powered, RS-232 Transmitters/Receivers

FN4315
Rev 17.00
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The HIN202E, HIN206E, HIN207E, HIN208E, HIN211E, HIN213E, HIN232E family of RS-232 transmitters/receivers interface circuits meet all EIA high-speed RS-232E and V.28 specifications, and are particularly suited for those applications where ±12V is not available. A redesigned transmitter circuit improves data rate and slew rate, which makes this suitable for ISDN and high speed modems. The transmitter outputs and receiver inputs are protected to ±15kV ESD (Electrostatic Discharge). They require a single +5V power supply and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offers a wide variety of high-speed RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN206E, HIN211E and HIN213E feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213E provides two active receivers in shutdown mode allowing for easy “wakeup” capability.

The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V input, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Features

- Pb-Free Plus Anneal Available (RoHS Compliant)
- High Speed ISDN Compatible 230kbits/s
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Meets All RS-232E and V.28 Specifications
- Requires Only 0.1µF or Greater External Capacitors
- Two Receivers Active in Shutdown Mode (HIN213E)
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (Typ) 5mA
- Low Power Shutdown Function (Typ) 1µA
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - ±10V Output Swing for +5V Input
  - 300Ω Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
- Multiple Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

Applications

- Any System Requiring High-Speed RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptop
  - Peripheral - Printers and Terminals
  - Instrumentation, UPS
  - Modems, ISDN Terminal Adaptors

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	NUMBER OF 0.1µF EXTERNAL CAPACITORS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN202E	+5V	2	2	4 Capacitors	No/No	0
HIN206E	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207E	+5V	5	3	4 Capacitors	No/No	0
HIN208E	+5V	4	4	4 Capacitors	No/No	0
HIN211E	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213E	+5V	4	5	4 Capacitors	Yes/Yes	2
HIN232E	+5V	2	2	4 Capacitors	No/No	0

Ordering Information

PART NO. (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
HIN202ECBZ	202ECBZ	0 to 70	16 Ld SOIC (W)	M16.3
HIN202ECBZ-T (Note 2)	202ECBZ		16 Ld SOIC (W) Tape and Reel	M16.3
HIN202ECBNZ	202ECBNZ		16 Ld SOIC (N)	M16.15
HIN202ECBNZ-T (Note 2)	202ECBNZ		16 Ld SOIC (N) Tape and Reel	M16.15
HIN202ECPZ	202ECPZ		16 Ld PDIP*	E16.3
HIN202EIBZ	202EIBZ	-40 to 85	16 Ld SOIC (W)	M16.3
HIN202EIBZ-T (Note 2)	202EIBZ		16 Ld SOIC (W) Tape and Reel	M16.3
HIN202EIBNZ	202EIBNZ		16 Ld SOIC (N)	M16.15
HIN202EIBNZ-T (Note 2)	202EIBNZ		16 Ld SOIC (N) Tape and Reel	M16.15
HIN206ECBZ	HIN206ECBZ	0 to 70	24 Ld SOIC	M24.3
HIN206ECBZ-T (Note 2)	HIN206ECBZ		24 Ld SOIC Tape and Reel	M24.3
HIN206EIAZ	HIN206EIAZ	-40 to 85	24 Ld SSOP	M24.209
HIN206EIAZ-T (Note 2)	HIN206EIAZ		24 Ld SSOP Tape and Reel	M24.209
HIN207ECAZ	HIN207ECAZ	0 to 70	24 Ld SSOP	M24.209
HIN207ECAZ-T (Note 2)	HIN207ECAZ		24 Ld SSOP Tape and Reel	M24.209
HIN207ECBZ	HIN207ECBZ		24 Ld SOIC	M24.3
HIN207ECBZ-T (Note 2)	HIN207ECBZ		24 Ld SOIC Tape and Reel	M24.3
HIN207EIAZ	HIN207EIAZ	-40 to 85	24 Ld SSOP	M24.209
HIN207EIAZ-T (Note 2)	HIN207EIAZ		24 Ld SSOP Tape and Reel	M24.209
HIN207EIBZ	HIN207EIBZ		24 Ld SOIC	M24.3
HIN207EIBZ-T (Note 2)	HIN207EIBZ		24 Ld SOIC Tape and Reel	M24.3
HIN208ECAZ	HIN208ECAZ	0 to 70	24 Ld SSOP	M24.209
HIN208ECAZ-T (Note 2)	HIN208ECAZ		24 Ld SSOP Tape and Reel	M24.209
HIN208ECBZ	HIN208ECBZ		24 Ld SOIC	M24.3
HIN208ECBZ-T (Note 2)	HIN208ECBZ		24 Ld SOIC Tape and Reel	M24.3
HIN208EIAZ	HIN208EIAZ	-40 to 85	24 Ld SSOP	M24.209
HIN208EIAZ-T (Note 2)	HIN208EIAZ		24 Ld SSOP Tape and Reel	M24.209
HIN208EIBZ	HIN208EIBZ		24 Ld SOIC	M24.3
HIN211ECAZ	HIN211ECAZ	0 to 70	28 Ld SSOP	M28.209
HIN211ECAZ-T (Note 2)	HIN211ECAZ		28 Ld SSOP Tape and Reel	M28.209
HIN211ECBZ	HIN211ECBZ		28 Ld SOIC	M28.3
HIN211ECBZ-T (Note 2)	HIN211ECBZ		28 Ld SOIC Tape and Reel	M28.3
HIN211EIAZ	HIN211EIAZ	-40 to 85	28 Ld SSOP	M28.209
HIN211EIAZ-T (Note 2)	HIN211EIAZ		28 Ld SSOP Tape and Reel	M28.209
HIN211EIBZ	HIN211EIBZ		28 Ld SOIC	M28.3
HIN213ECAZ	HIN213ECAZ	0 to 70	28 Ld SSOP	M28.209
HIN213ECAZ-T (Note 2)	HIN213ECAZ		28 Ld SSOP Tape and Reel	M28.209
HIN213EIAZ	HIN213EIAZ	-40 to 85	28 Ld SSOP	M28.209
HIN213EIAZ-T (Note 2)	HIN213EIAZ		28 Ld SSOP Tape and Reel	M28.209
HIN213EIBZ	HIN213EIBZ		28 Ld SOIC	M28.3

Ordering Information (Continued)

PART NO. (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
HIN232ECAZ	HIN232ECAZ	0 to 70	16 Ld SSOP	M16.209
HIN232ECAZ-T (Note 2)	HIN232ECAZ		16 Ld SSOP Tape and Reel	M16.209
HIN232ECBNZ	232ECBNZ		16 Ld SOIC (N)	M16.15
HIN232ECBNZ-T (Note 2)	232ECBNZ		16 Ld SOIC (N) Tape and Reel	M16.15
HIN232ECBZ	232ECBZ		16 Ld SOIC (W)	M16.3
HIN232ECBZ-T (Note 2)	232ECBZ		16 Ld SOIC (W) Tape and Reel	M16.3
HIN232ECPZ	HIN232ECPZ		16 Ld PDIP*	E16.3
HIN232EIBNZ	232EIBNZ	-40 to 85	16 Ld SOIC (N)	M16.15
HIN232EIBNZ-T (Note 2)	232EIBNZ		16 Ld SOIC (N) Tape and Reel	M16.15
HIN232EIVZ **(No longer available, recommended replacement: HIN232ECAZ)**	232EIVZ		16 Ld TSSOP	M16.173
HIN232EIVZ-T (Note 2) **(No longer available, recommended replacement: HIN232ECAZ-T)**	232EIVZ		16 Ld TSSOP Tape and Reel	M16.173

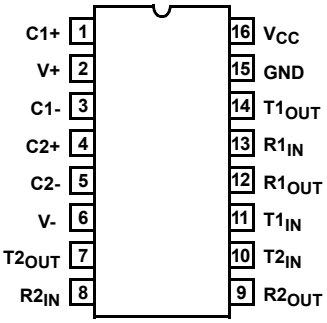
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTES:

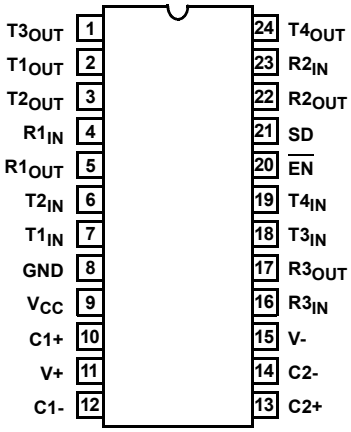
1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Please refer to TB347 for details on reel specifications.

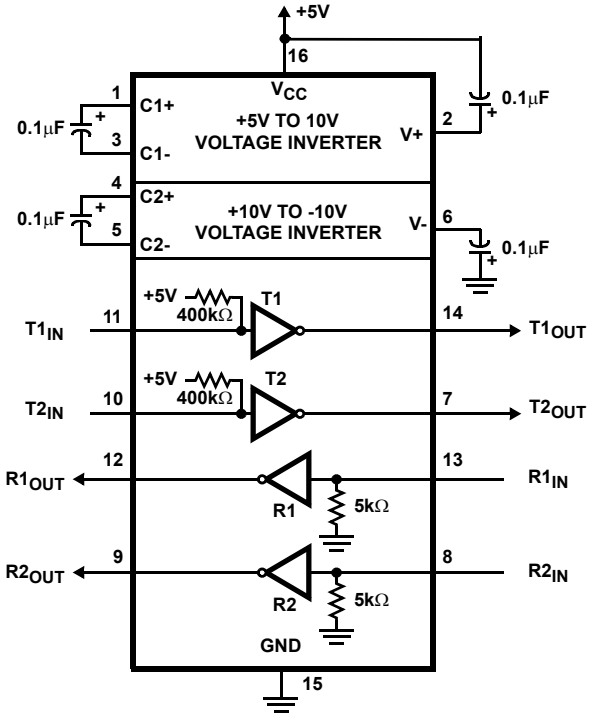
Pinouts

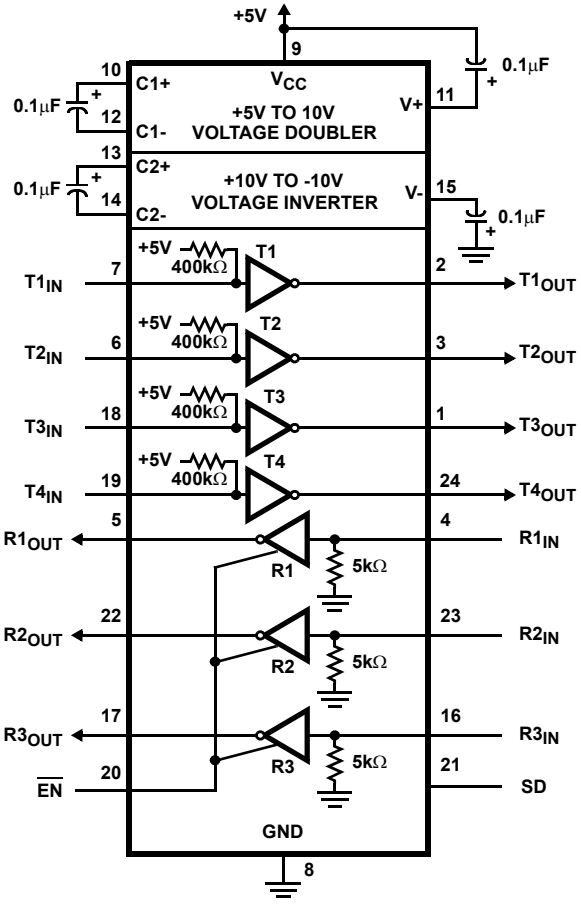
HIN202E (PDIP, SOIC)
TOP VIEW



HIN206E (SOIC, SSOP)
TOP VIEW

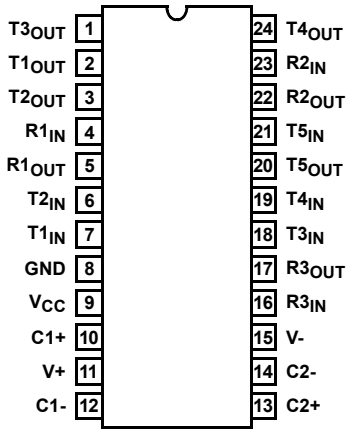




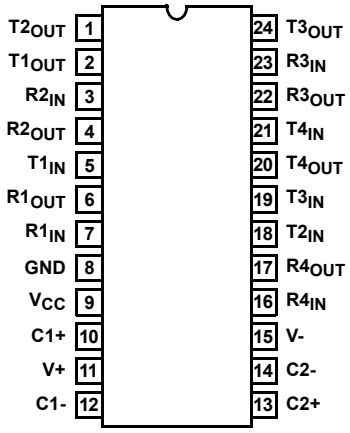


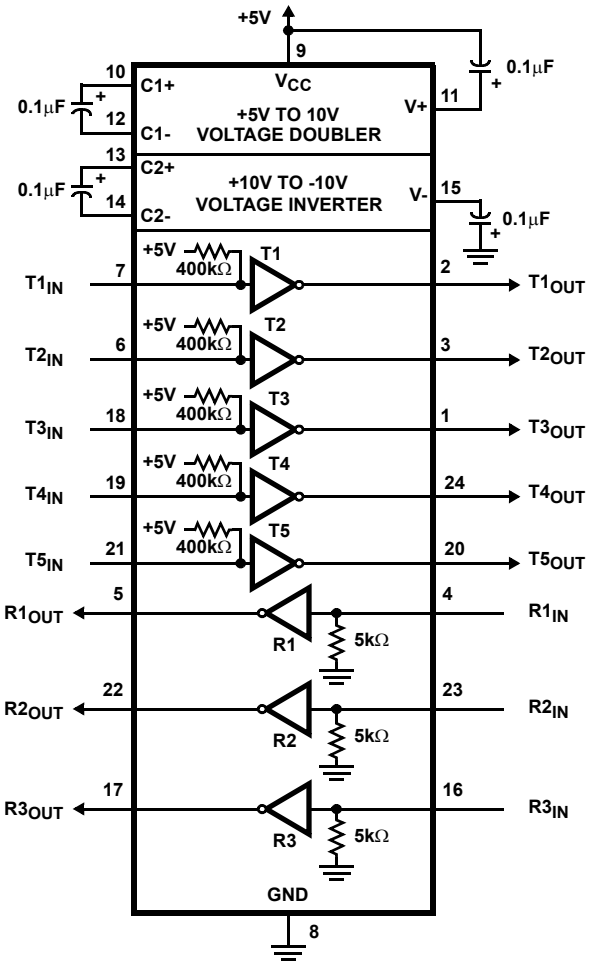
Pinouts (Continued)

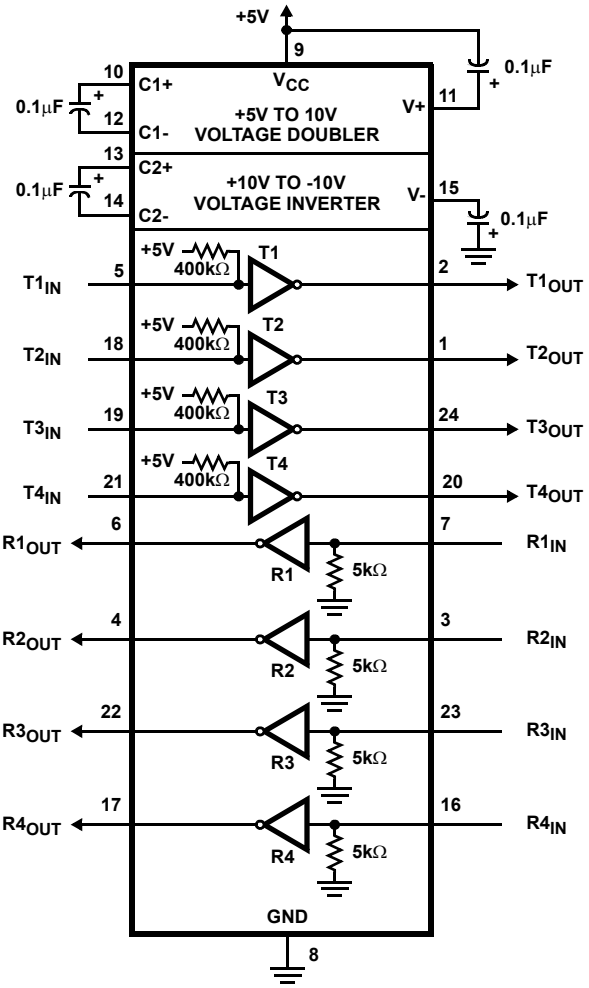
HIN207E (SOIC, SSOP)
TOP VIEW



HIN208E (SOIC, SSOP)
TOP VIEW

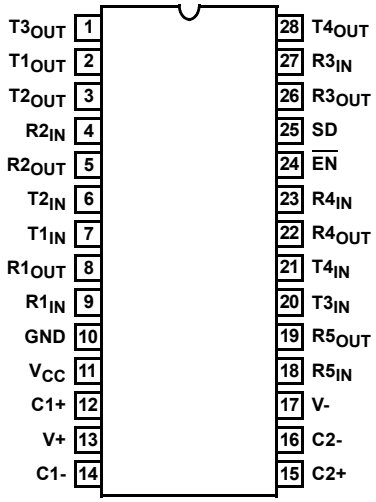




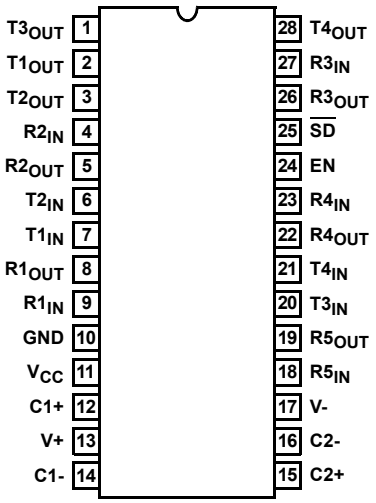


Pinouts (Continued)

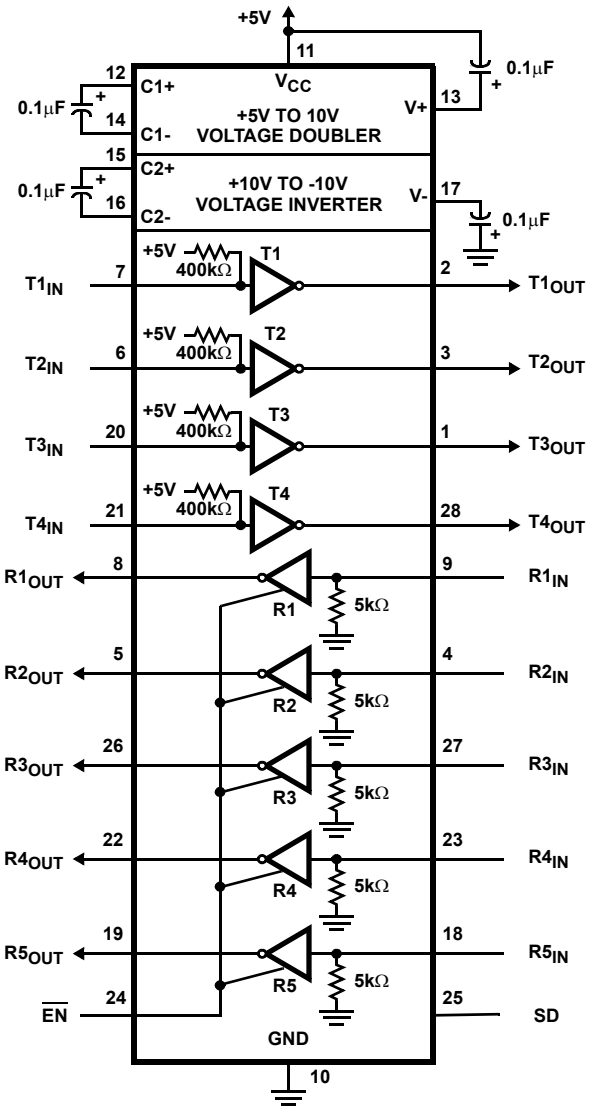
HIN211E (SOIC, SSOP)
TOP VIEW

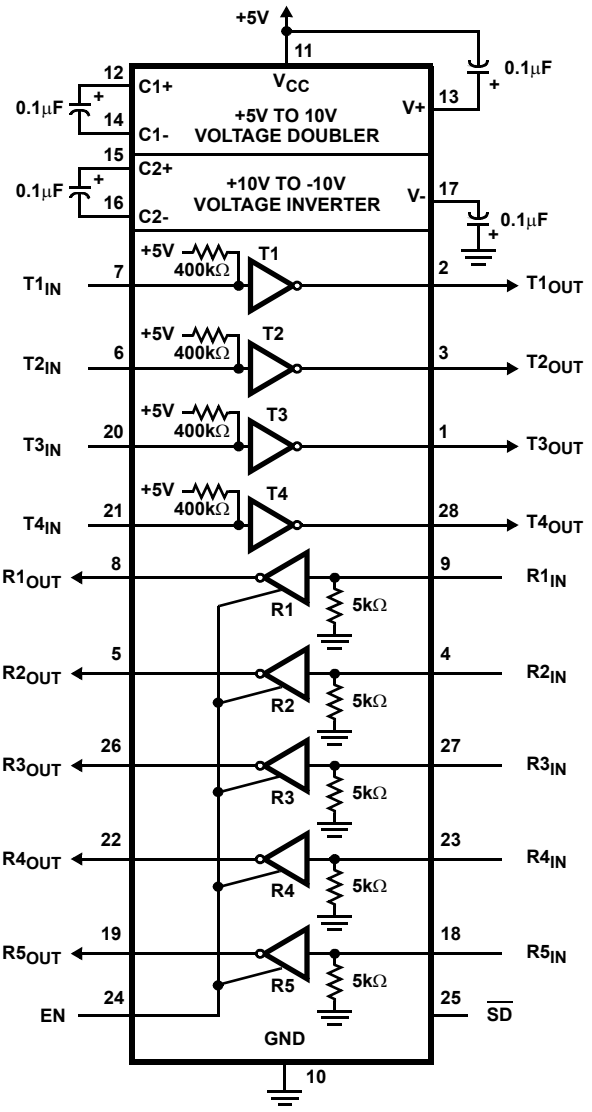


HIN213E (SOIC, SSOP)
TOP VIEW



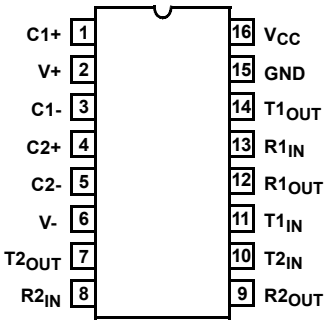
NOTE: R4 and R5 active in shutdown.

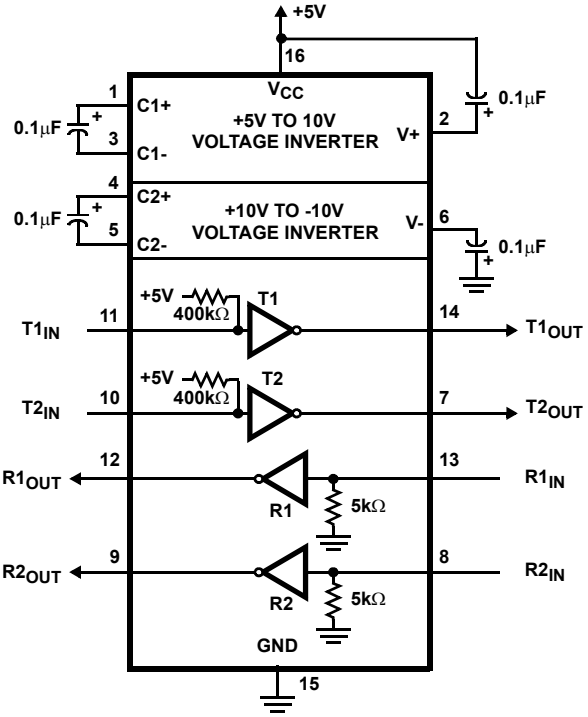




Pinouts (Continued)

HIN232E (PDIP, SOIC, SSOP)
(TSSOP - NO LONGER AVAILABLE OR SUPPORTED)
TOP VIEW





Pin Descriptions

PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%, (5V ±5% HIN207E).
V+	Internally generated positive supply (+10V nominal).
V-	Internally generated negative supply (-10V nominal).
GND	Ground Lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$, EN	Receiver Enable Input. With $\overline{EN}$ = 5V (HIN213E EN=0V), the receiver outputs are placed in a high impedance state.
SD, $\overline{SD}$	Shutdown Input. With SD = 5V (HIN213E $\overline{SD}$ = 0V), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN213E) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) < V_{CC} < 6V
V+ to Ground . . . . . (V_{CC} -0.3V) < V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
T_{IN} . . . . . -0.3V < V_{IN} < (V+ +0.3V)
R_{IN} . . . . . ±30V
Output Voltages
T_{OUT} . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
R_{OUT} . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
T_{OUT} . . . . . Continuous
R_{OUT} . . . . . Continuous
ESD Classification . . . . . See Specification Table

Operating Conditions

Temperature Range
HIN2XXECX . . . . . 0°C to 70°C
HIN2XXEIX . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld SOIC (N) Package	110
16 Ld SOIC (W) Package	100
16 Ld SSOP Package	155
16 Ld TSSOP Package	145
16 Ld PDIP Package*	90
24 Ld SOIC Package	75
24 Ld SSOP Package	135
28 Ld SOIC Package	70
28 Ld SSOP Package	100

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN207E); C1-C4 = 0.1µF; T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY CURRENTS						
Power Supply Current, I_{CC}	No Load, T_A = 25°C	HIN202E	-	8	15	mA
		HIN206E - HIN208E, HIN211E, HIN213E	-	11	20	mA
		HIN232E	-	5	10	mA
Shutdown Supply Current, I_{CC}(SD)	T_A = 25°C	HIN206E, HIN211E	-	1	10	µA
		HIN213E	-	15	50	µA
LOGIC AND TRANSMITTER INPUTS, RECEIVER OUTPUTS						
Input Logic Low, V_{IL}	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$		-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}		2.0	-	-	V
	$\overline{EN}$, SD, EN, $\overline{SD}$		2.4	-	-	V
Transmitter Input Pullup Current, I_P	T_{IN} = 0V		-	15	200	µA
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (HIN202E, HIN232E, I_{OUT} = 3.2mA)		-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1mA		3.5	4.6	-	V
TTL/CMOS Receiver Output Leakage	$\overline{EN}$ = V_{CC}, EN = 0, 0V < R_{OUT} < V_{CC}		-	0.5	±10	µA
RECEIVER INPUTS						
RS-232 Input Voltage Range, V_{IN}			-30	-	+30	V
Receiver Input Impedance, R_{IN}	T_A = 25°C, V_{IN} = ±3V		3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5V, T_A = 25°C	Active Mode	-	1.2	-	V
		Shutdown Mode HIN213E R4 and R5	-	1.5	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5V, T_A = 25°C	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213E R4 and R5	-	1.5	2.4	V
Receiver Input Hysteresis, V_{HYST}	V_{CC} = 5V, No Hysteresis in Shutdown Mode		0.2	0.5	1.0	V

Electrical Specifications Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN207E); C1-C4 = 0.1µF; T_A = Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS					
Output Enable Time, t_{EN}	HIN206E, HIN211E, HIN213E	-	600	-	ns
Output Disable Time, t_{DIS}	HIN206E, HIN211E, HIN213E	-	200	-	ns
Transmitter, Receiver Propagation Delay, t_{PD}	HIN213E $\overline{SD}$ = 0V, R4, R5	-	4.0	40	µs
	HIN213E $\overline{SD}$ = V_{CC}, R1 - R5	-	0.5	10	µs
	All except HIN213E	-	0.5	10	µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 1000pF Measured from +3V to -3V or -3V to +3V, 1 Transmitter Switching (Note 2)	3	20	45	V/µs
TRANSMITTER OUTPUTS					
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground	±5	±9	±10	V
Output Resistance, T_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} Shorted to GND	-	±10	-	mA
ESD PERFORMANCE					
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model	-	±15	-	kV
	IEC61000-4-2 Contact Discharge	-	±8	-	kV
	IEC61000-4-2 Air Gap (Note 3)	-	±15	-	kV
All Other Pins	Human Body Model	-	±2	-	kV

NOTES:

4. Guaranteed by design.
5. Meets Level 4.

Test Circuits (HIN232E)

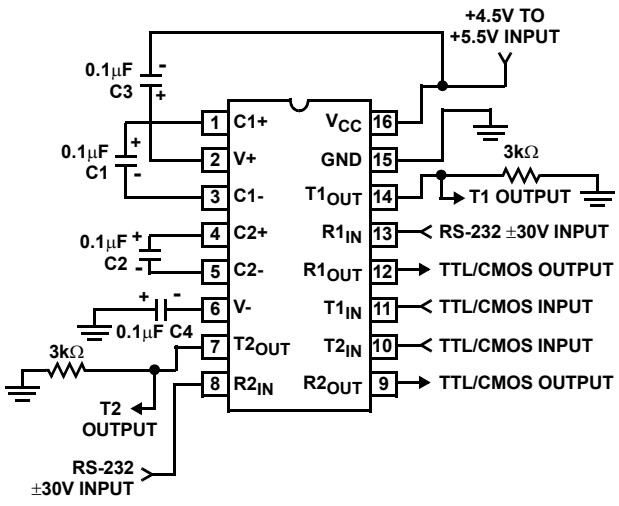


FIGURE 1. GENERAL TEST CIRCUIT

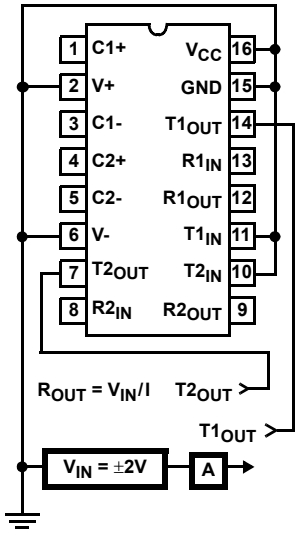


FIGURE 2. POWER-OFF SOURCE RESISTANCE CONFIGURATION

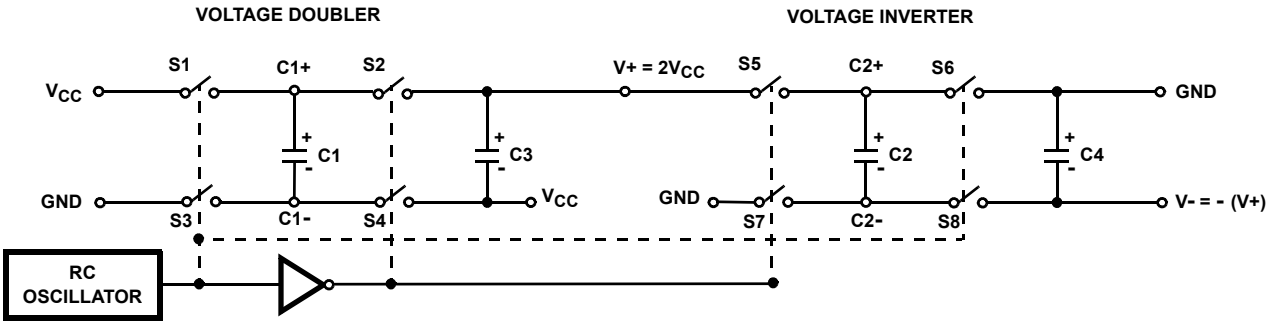


FIGURE 3. CHARGE PUMP

Detailed Description

The HIN2XXE family of high-speed RS-232 transmitters/receivers are powered by a single +5V power supply, feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 3. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 0.1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN206E, HIN211E and HIN213E) the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10µA. The transmitter outputs are disabled and the receiver outputs (except for HIN213E, R4 and R5) are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line $\overline{EN}$, (EN on HIN213E) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213E R4 and R5).

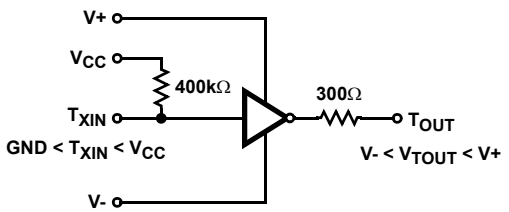


FIGURE 4. TRANSMITTER

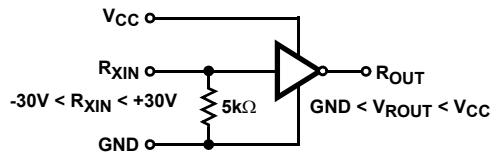
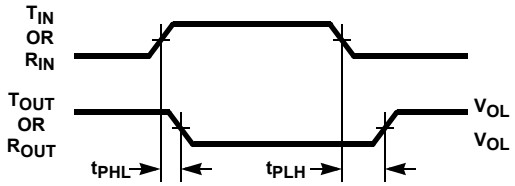


FIGURE 5. RECEIVER



$$\text{AVERAGE PROPAGATION DELAY} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 6. PROPAGATION DELAY DEFINITION

HIN213E Operation in Shutdown

The HIN213E features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5µs. This propagation delay may increase slightly during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80µs after $\overline{SD} = V_{IL}$. When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1µF capacitors.

Application Information

The HIN2XXE may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 7. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 8), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

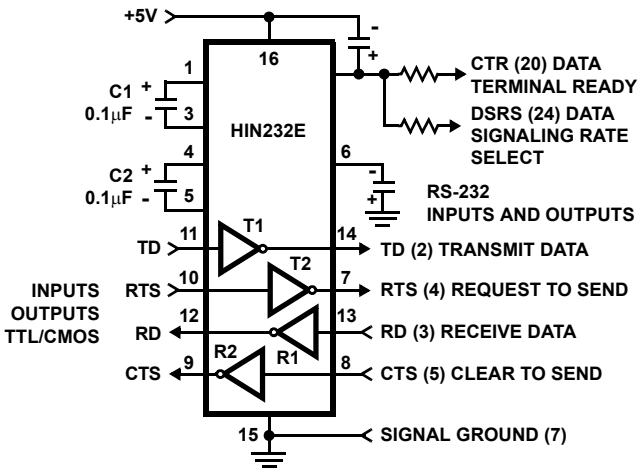


FIGURE 7. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

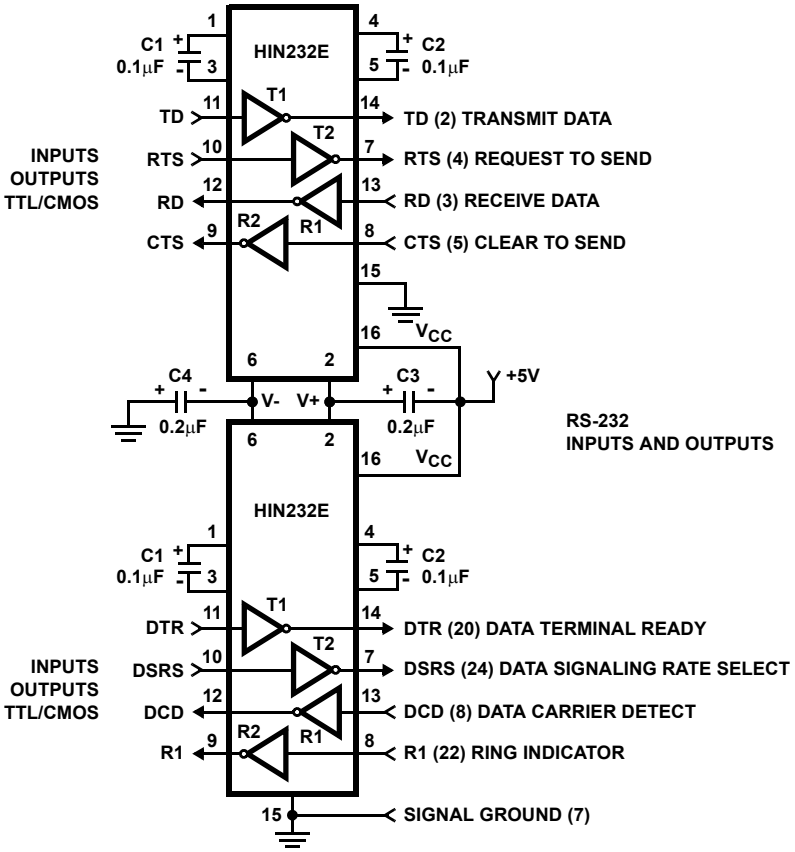


FIGURE 8. COMBINING TWO HIN232Es FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Typical Performance Curves

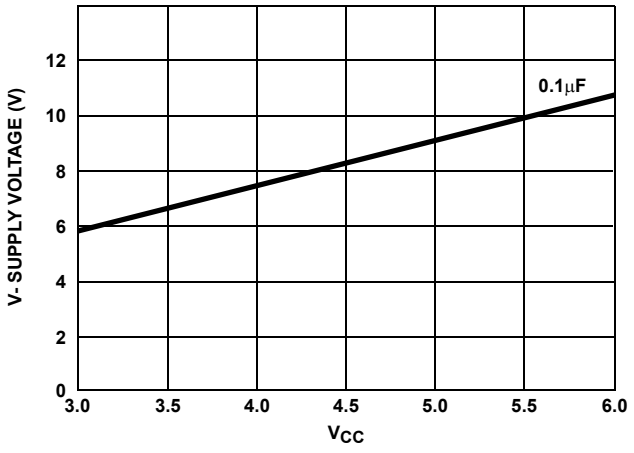


FIGURE 9. V- SUPPLY VOLTAGE vs V_{CC}

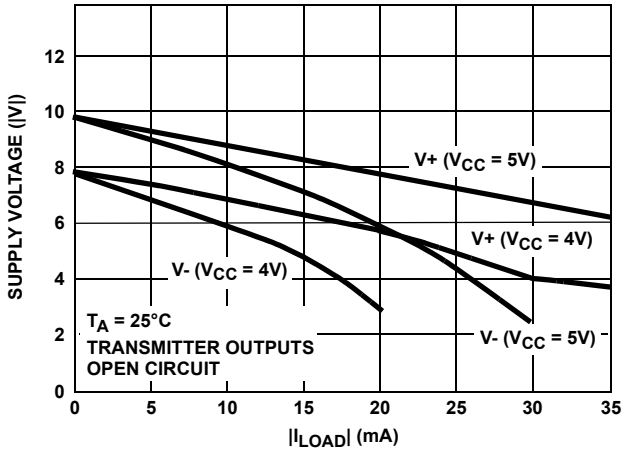


FIGURE 10. V+, V- OUTPUT VOLTAGE vs LOAD

Die Characteristics

METALLIZATION:

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

GND

PASSIVATION:

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

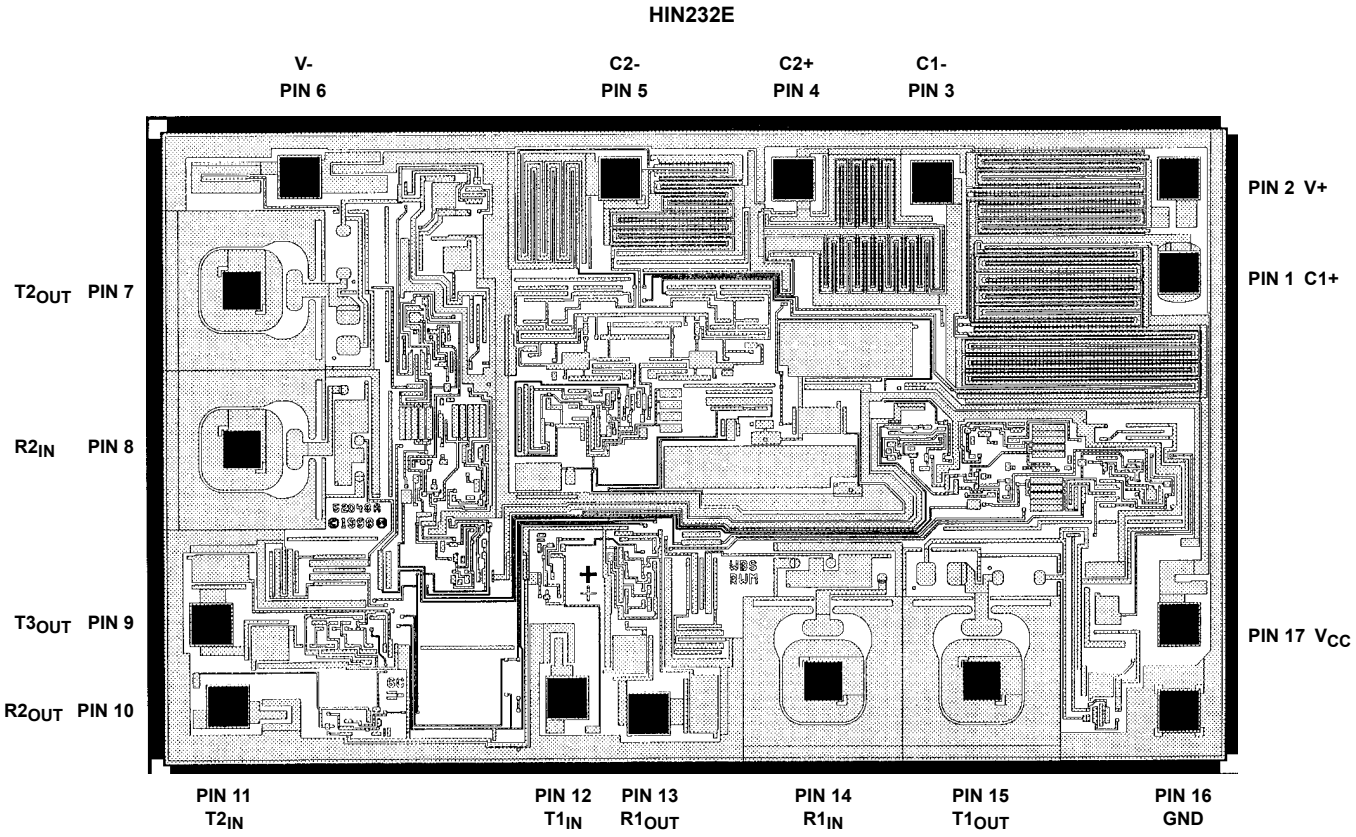
TRANSISTOR COUNT:

185

PROCESS:

CMOS Metal Gate

Metallization Mask Layout



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 14, 2015	FN4315.17	Updated the Ordering Information table starting on page 2. Added Revision History and About Intersil sections. Updated Package Outline drawing M24.3 to the latest revision. -Revision 0 to Revision 1 changes - Remove µ symbol which is overlapping the alpha symbol in the diagram. -Revision 1 to Revision 2 changes - Updated to new POD standard by removing table listing dimensions and putting dimensions on drawing. Added Land Pattern. Updated Package Outline drawing M28.3 to the latest revision. -Revision 0 to Revision 1 changes - Added land pattern.

About Intersil

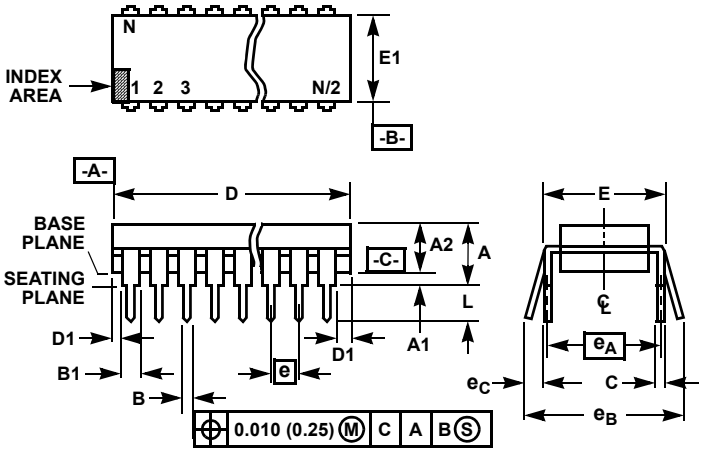
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

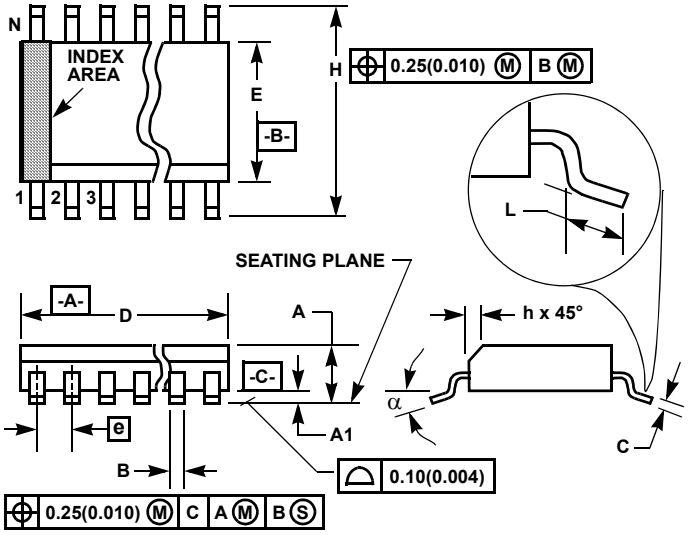
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

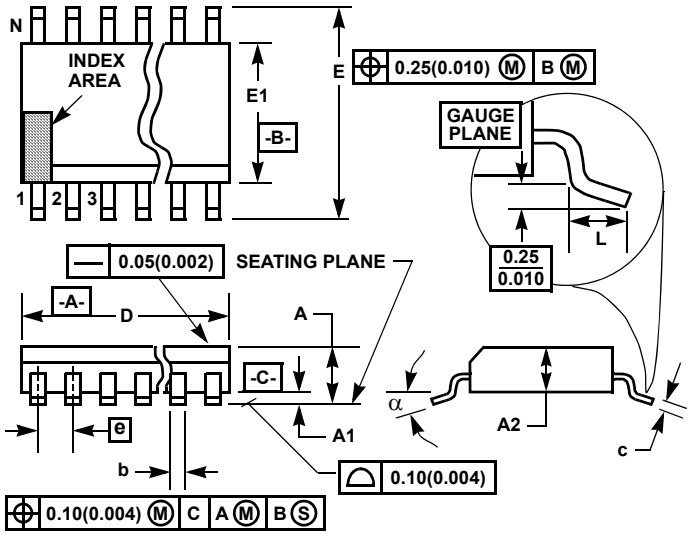
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

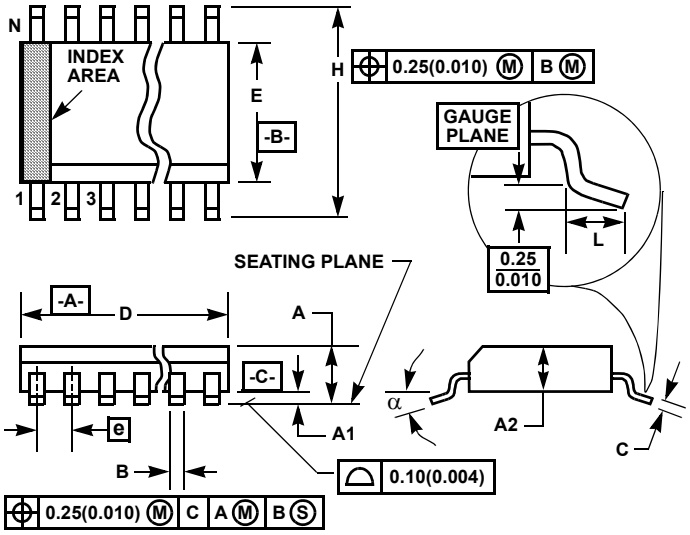
M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 2/02

Small Outline Plastic Packages (SSOP)



M16.209 **(JEDEC MO-150-AC ISSUE B)**

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

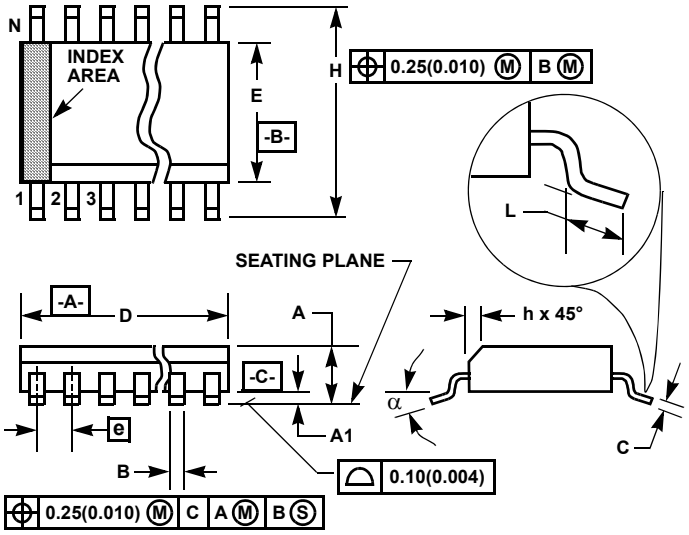
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 3 6/05

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



NOTES:

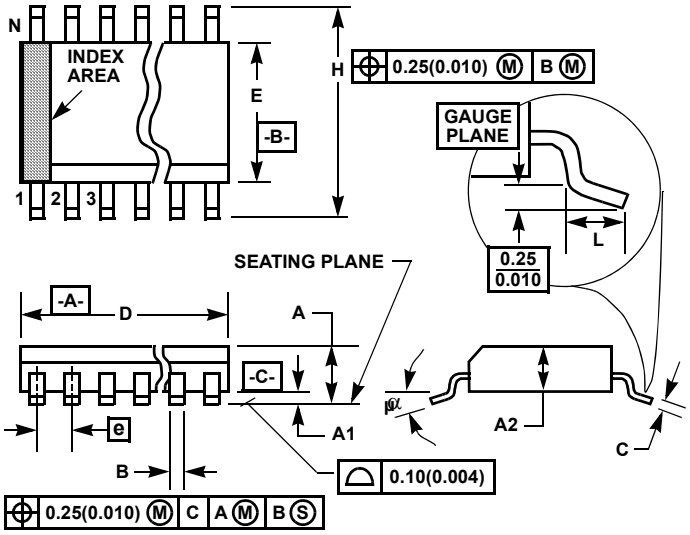
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.209 **(JEDEC MO-150-AG ISSUE B)**
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

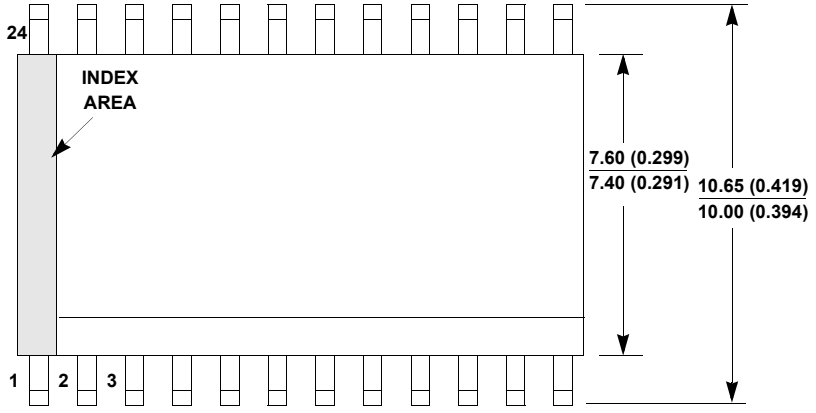
Rev. 1 3/95

Package Outline Drawing

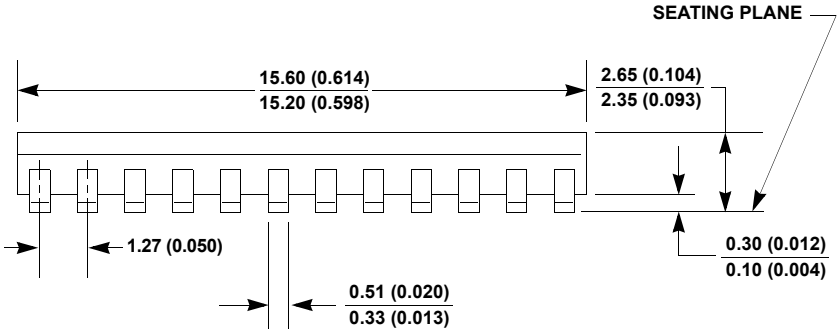
M24.3

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

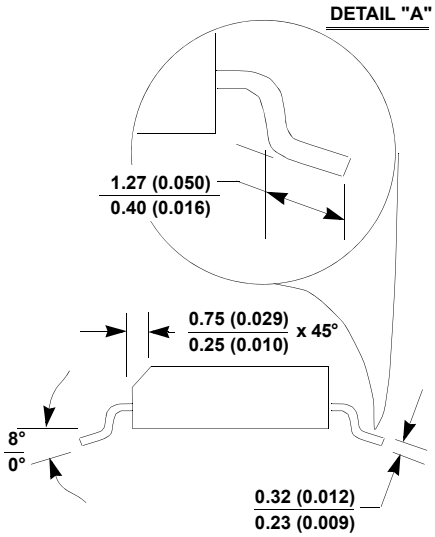
Rev 2, 3/11



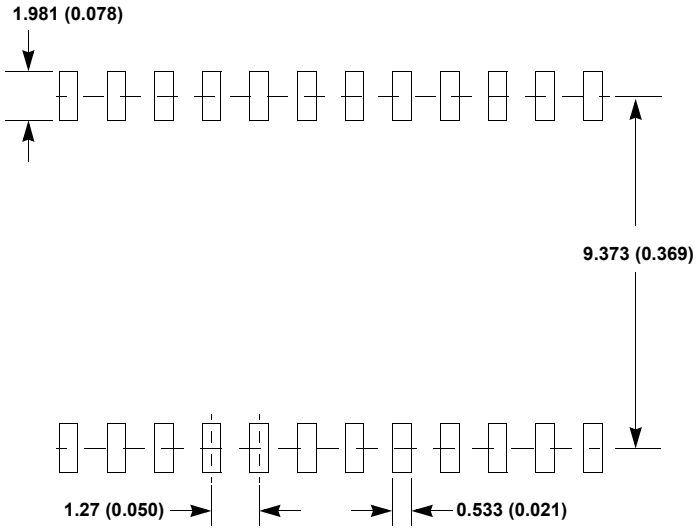
TOP VIEW



SIDE VIEW "A"



SIDE VIEW "B"

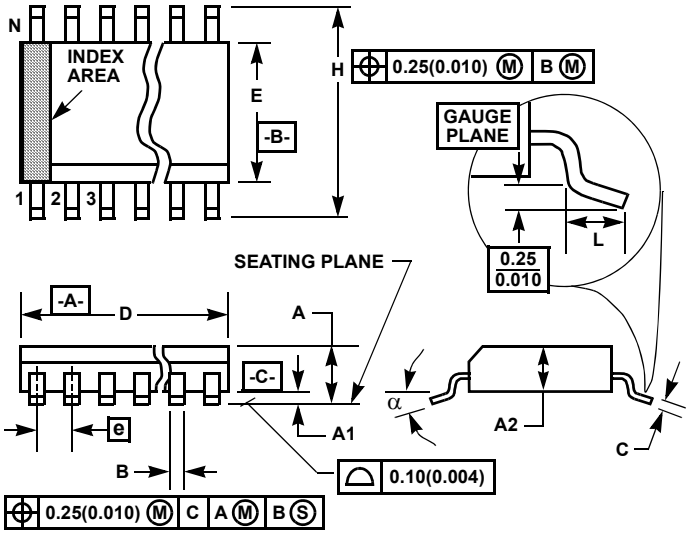


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions in ( ) are not necessarily exact.
8. This outline conforms to JEDEC publication MS-013-AD ISSUE C.

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

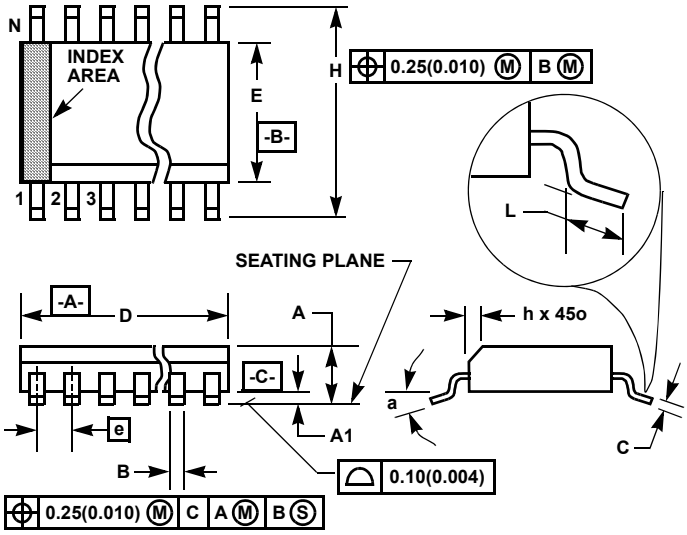
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.209 **(JEDEC MO-150-AH ISSUE B)**
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

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Small Outline Plastic Packages (SOIC)

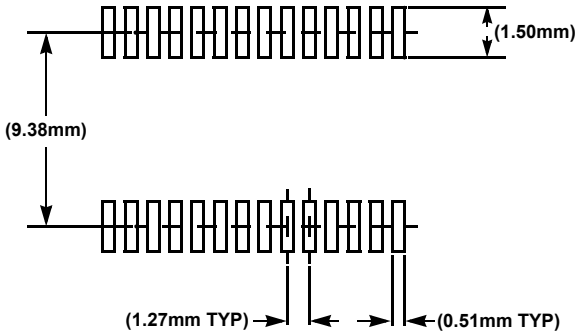


M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 1, 1/13

TYPICAL RECOMMENDED LAND PATTERN



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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