PRODUCT PREVIEW

# SMART 5 BOOT BLOCK FLASH MEMORY FAMILY 2, 4, 8 MBIT

*28F200B5, 28F400B5, 28F800B5*

- **SmartVoltage Technology**
  - **Smart 5 Flash: 5V Reads, 5V or 12V Writes**
  - **Increased Programming Throughput at 12V $V_{PP}$**
- **Very High-Performance Read**
  - **2-, 4-Mbit: 60 ns Access Time**
  - **8-Mbit: 70 ns Access Time**
- **x8/x16-Configurable Input/Output Bus**
- **Low Power Consumption**
  - **Max 60 mA Read Current at 5V**
  - **Auto Power Savings: <1 mA Typical Standby Current**
- **Optimized Array Blocking Architecture**
  - **16-KB Protected Boot Block**
  - **Two 8-KB Parameter Blocks**
  - **96-KB and 128-KB Main Blocks**
  - **Top or Bottom Boot Locations**
- **Extended Temperature Operation**
  - **–40°C to +85°C**
- **Industry-Standard Packaging**
  - **44-Lead PSOP, 48-Lead TSOP**
- **Extended Block Erase Cycling**
  - **100,000 Cycles at Commercial Temp**
  - **10,000 Cycles at Extended Temp**
- **Hardware Data Protection Feature**
  - **Absolute Hardware-Protection for Boot Block**
  - **Write Lockout during Power Transitions**
- **Automated Word/Byte Program and Block Erase**
  - **Command User Interface**
  - **Status Registers**
  - **Erase Suspend Capability**
- **SRAM-Compatible Write Interface**
- **Reset/Deep Power-Down Input**
  - **Provides Low-Power Mode and Reset for Boot Operations**
- **Pinout Compatible 2, 4, and 8 Mbit**
- **ETOX™ Flash Technology**
  - **0.6 µ ETOX IV Initial Production**
  - **0.4 µ ETOX V Later Production**

Intel's word-wide Smart 5 boot block flash memory family provides 2-, 4-, and 8-Mbit memories featuring high-density, low-cost, nonvolatile, read/write storage solutions for a wide range of applications. Their asymmetrically-blocked architecture, flexible voltage, and extended cycling provide highly flexible components suitable for embedded code execution applications, such as networking infrastructure and office automation.

Based on Intel's boot block architecture, the word-wide Smart 5 boot block memory family enables quick and easy upgrades for designs that demand state-of-the-art technology. This family of products comes in industry-standard packages: the 48-lead TSOP, ideal for board-constrained applications, and the rugged, easy to handle 44-lead PSOP.

December 1996

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## REVISION HISTORY

| Number | Description |
|---|---|
| -001 | Original Version |
| -002 | Minor changes throughout document.<br>Section 3.1.5 and Figure 13 redone to clarify program/erase operation abort.<br>Information added to Table 2, Figure 1, and Section 3.3 to clarify WP# on 8-Mbit, 44-PSOP.<br>Read and Write Waveforms changed to numbered format.<br>Typical numbers removed from DC Characteristics and Erase/Program Timings. |
| -003 | Minor text changes throughout document.<br>Figure 1, 44-PSOP pinout: mistake on pin 3 on 2-Mbit pinout corrected from $A_{17}$ to NC.<br>Specs $t_{EHQZ}$ and $t_{GHQZ}$ improved.<br>Explanations of program/erase abort commands reworked in Table 6, Command Codes. |



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## 1.0 INTRODUCTION

This datasheet contains specifications for 2-, 4-, and 8-Mbit Smart 5 boot block flash memories. Section 1 provides a feature overview. Sections 2, 3, and 4 describe the product and functionality. Section 5 details the electrical and timing specifications for both commercial and extended temperature operation.

### 1.1 New Features in the Smart 5 Memory Products

The Smart 5 boot block flash memory family offers identical features with the BV/CV/BE/CE SmartVoltage products, except the Smart 5 boot block -B5 parts only support 5V $V_{CC}$ read voltage.

The following differences distinguish the Smart 5 boot block products from their predecessors:

- A delay is required if the part is reset during an in-progress program or erase operation.
- On the fly word-byte mode switching is no longer supported. Word-byte mode must be configured at power-up and remain stable during operation.
- Write operations are no longer specified as WE#- or CE#-controlled in favor of a simpler "unified" write method, which is compatible with either of the old methods.

### 1.2 Product Overview

The word-wide Smart 5 boot block memory family provides pinout-compatible flash memories at the 2-, 4- and 8-Mbit densities. The 28F200B5, 28F400B5, and 28F800B5 can be configured to operate either in 16-bit or 8-bit bus mode, with the data divided into individually erasable blocks.

**Table 1. Smart 5 Boot Block Family: Feature Summary**

| Feature | | 28F200B5 | 28F400B5 | 28F800B5 | Reference |
|---|---|---|---|---|---|
| $V_{CC}$ Read Voltage | | 5V ± 5%, 5V ± 10% | | | Table 10 |
| $V_{PP}$ Prog/Erase Voltage | | 5V ± 10% or 12V ± 5%, auto-detected | | | Table 10 |
| Bus-width | | 8- or 16-bit configurable | | | Table 2 |
| Speed (ns) | Commercial | 60, 80 | 60, 80 | 70, 90 | Table 14 |
| | Extended | 80 | 80 | 90 | Table 14 |
| Memory Arrangement | | x8: 256K x 8<br>x16: 128K x 16 | x8: 512K x 8<br>x16: 256K x 16 | x8: 1M x 8<br>x16: 512K x 16 | |
| Blocking<br>(Top or Bottom boot locations available) | | 1 x 16k Boot Block<br>2 x 8k Parameter<br>1 x 96k Main Block<br>1 x 128k Main Block | 1 x 16k Boot Block<br>2 x 8k Parameter<br>1 x 96k Main Block<br>3 x 128k Main Block | 1 x 16k Boot Block<br>2 x 8k Parameter<br>1 x 96k Main Block<br>7 x 128k Main Block | Sect. 2.3,<br>Fig. 3-6 |
| Locking | | Boot Block lockable using WP# and/or RP#<br>All others protectable using $V_{PP}$ switch | | | Sect. 3.3 |
| Operating Temperature | | Commercial: 0°C – +70 °C<br>Extended: -40°C – +85 °C | | | Table 10 |
| Erase Cycling | | 100,000 cycles at Commercial Temperature<br>10,000 cycles at Extended Temperature | | | |
| Packages | | 44-PSOP, 48-TSOP | | | Figs. 1-2 |

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SmartVoltage technology enables fast factory programming and low-power designs. Specifically designed for 5V systems, Smart 5 components support read operations at 5V $V_{CC}$ and internally configure to program/erase at 5V or 12V. The 12V $V_{PP}$ option renders the fastest program and erase performance which will increase your factory throughput. With the 5V $V_{PP}$ option, $V_{CC}$ and $V_{PP}$ can be tied together for a simple 5V design. In addition, the dedicated $V_{PP}$ pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

The memory array is asymmetrically divided into blocks in an asymmetrical architecture to accommodate microprocessors that boot from the top (denoted by **-T** suffix) or the bottom (**-B** suffix) of the memory map. The blocks include a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and main blocks (one block of 98,304 bytes and additional block(s) of 131,072 bytes). See Figures 3–6 for memory maps. Each block can be independently erased and programmed 100,000 times at commercial temperature or 10,000 times at extended temperature. Unlike erase operations, which erase all locations within a block simultaneously, each byte or word in the flash memory can be programmed independently of other memory locations.

The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by WP# and/or RP# (see Section 3.3 for details).

The system processor interfaces to the flash device through a Command User Interface (CUI), using valid command sequences to initiate device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations. The Status Register (SR) indicates the status of the WSM and whether it successfully completed the desired program or erase operation.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical $I_{CCR}$ current is 1 mA.

When CE# and RP# pins are at $V_{CC}$, the component enters a CMOS standby mode. Driving RP# to GND enables a deep power-down mode which significantly reduces power consumption, provides write protection, resets the device, and clears the status register. A reset time ($t_{PHQV}$) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time ($t_{PHEL}$) from RP#-high until writes to the CUI are recognized. See Section 4.2.

The deep power-down mode can also be used as a device reset, allowing the flash to be reset along with the rest of the system. For example, when the flash memory powers-up, it automatically defaults to the read array mode, but during a warm system reset, where power continues uninterrupted to the system components, the flash memory could remain in a non-read mode, such as erase. Consequently, the system Reset signal should be tied to RP# to reset the memory to normal read mode upon activation of the Reset signal. This also provides protection against unwanted command writes due to invalid system bus conditions during system reset or power-up/down sequences.

These devices are configurable at power-up for either byte-wide or word-wide input/output using the BYTE# pin. Please see Table 2 for a detailed description of BYTE# operations, especially the usage of the $DQ_{15}/A_{-1}$ pin.

These Smart 5 memory products are available in the 44-lead PSOP (Plastic Small Outline Package), which is ROM/EPROM-compatible, and the 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick) as shown in Figure 1, and 2, respectively.

## 2.0 PRODUCT DESCRIPTION

This section describes the pinout and block architecture of the device family.

### 2.1 Pin Descriptions

The pin descriptions table details the usage of each of the device pins.



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**Table 2. Pin Descriptions**

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0$–$A_{18}$ | INPUT | **ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. **28F200: A[0-16], 28F400: A[0-17], 28F800: A[0-18]** |
| $A_9$ | INPUT | **ADDRESS INPUT:** When $A_9$ is at $V_{HH}$ the signature mode is accessed. During this mode, $A_0$ decodes between the manufacturer and device IDs. When BYTE# is at a logic low, only the lower byte of the signatures are read. $DQ_{15}/A_{-1}$ is a don't care in the signature mode when BYTE# is low. |
| $DQ_0$–$DQ_7$ | INPUT/ OUTPUT | **DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched during the write cycle. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled. |
| $DQ_8$–$DQ_{15}$ | INPUT/ OUTPUT | **DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched during the write cycle. Outputs array data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled as in the byte-wide mode (BYTE# = "0"). In the byte-wide mode $DQ_{15}/A_{-1}$ becomes the lowest order address for data output on $DQ_0$–$DQ_7$. |
| CE# | INPUT | **CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# input stages. |
| OE# | INPUT | **OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read cycle. OE# is active low. |
| WE# | INPUT | **WRITE ENABLE:** Controls writes to the Command Register and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse. |
| RP# | INPUT | **RESET/DEEP POWER-DOWN:** Uses three voltage levels ($V_{IL}$, $V_{IH}$, and $V_{HH}$) to control two different functions: reset/deep power-down mode and boot block unlocking. It is backwards-compatible with the BX/BL/BV products.<br>**When RP# is at logic low, the device is in reset/deep power-down mode**, which puts the outputs at High-Z, resets the Write State Machine, and draws minimum current.<br>**When RP# is at logic high, the device is in standard operation**. When RP# transitions from logic-low to logic-high, the device defaults to the read array mode.<br>**When RP# is at $V_{HH}$, the boot block is unlocked** and can be programmed or erased. This overrides any control from the WP# input. |



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**Table 2. Pin Descriptions** (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| WP# | INPUT | **WRITE PROTECT:** Provides a method for unlocking the boot block with a logic level signal in a system without a 12V supply.<br><br>**When WP# is at logic low, the boot block is locked**, preventing program and erase operations to the boot block. If a program or erase operation is attempted on the boot block when WP# is low, the corresponding status bit (bit 4 for program, bit 5 for erase) will be set in the Status Register to indicate the operation failed.<br><br>**When WP# is at logic high, the boot block is unlocked** and can be programmed or erased.<br><br>**NOTE:** This feature is overridden and the boot block unlocked when RP# is at $V_{HH}$. This pin can not be left floating. Because the 8-Mbit 44-PSOP package does not have enough pins, it does not include this pin and thus 12V on RP# is required to unlock the boot block. See Section 3.3 for details on write protection. |
| BYTE# | INPUT | **BYTE# ENABLE:** Configures whether the device operates in byte-wide mode (x8) or word-wide mode (x16). This pin must be set at power-up or return from deep power-down and not changed during device operation. BYTE# pin must be controlled at CMOS levels to meet the CMOS current specification in standby mode.<br><br>**When BYTE# is at logic low, the byte-wide mode is enabled**, where data is read and programmed on $DQ_0$–$DQ_7$ and $DQ_{15}/A_{-1}$ becomes the lowest order address that decodes between the upper and lower byte. $DQ_8$–$DQ_{14}$ are tri-stated during the byte-wide mode.<br><br>**When BYTE# is at logic high, the word-wide mode is enabled**, where data is read and programmed on $DQ_0$–$DQ_{15}$. |
| $V_{CC}$ | | **DEVICE POWER SUPPLY:** 5.0V ± 10% |
| $V_{PP}$ | | **PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block, a voltage either of 5V ± 10% or 12V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands. |
| GND | | **GROUND:** For all internal circuitry. |
| NC | | **NO CONNECT:** Pin may be driven or left floating. |

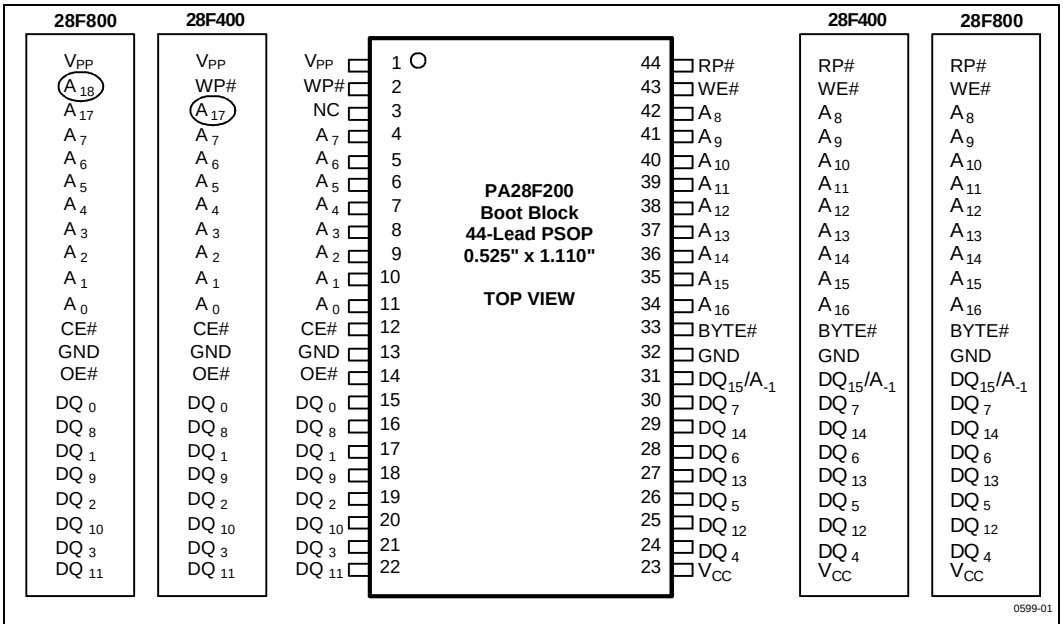
## 2.2 Pinouts

Intel's Smart 5 boot block architecture provides upgrade paths in each package pinout up to the 8-Mbit density. The 44-lead PSOP pinout follows the industry-standard ROM/EPROM pinout, as shown in Figure 1. Designs with space concerns should consider the 48-lead pinout shown in Figure 2.

Pinouts for the corresponding 2-, 4- and 8-Mbit components are provided on the same diagram for convenient reference. 2-Mbit pinouts are given on the chip illustration in the center, with 4-Mbit and 8-Mbit pinouts going outward from the center.



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**NOTE:** Pin 2 is WP# on 2- and 4-Mbit devices but $A_{18}$ on the 8-Mbit because no other pins were available for the high order address. Thus, the 8-Mbit in 44-PSOP cannot unlock the boot block without RP# = $V_{HH}$. See Section 3.3 for details. To allow upgrades to 8-Mbit from 2/4-Mbit in this package design pin 2 to control WP# at the 2/4-Mbit level and $A_{18}$ at the 8-Mbit density.

**Figure 1. 44-Lead PSOP Pinout Diagram**

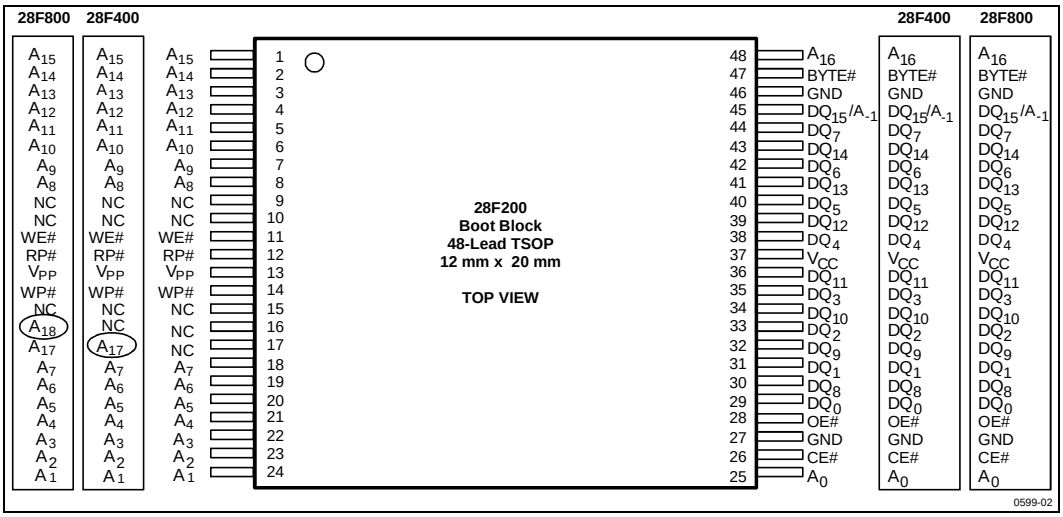



**Figure 2. 48-Lead TSOP Pinout Diagram**

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## 2.3 Memory Blocking Organization

The boot block product family features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times for commercial temperature or up to 10,000 times for extended temperature. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. The combination of block sizes in the boot block architecture allow the integration of several memories into a single chip. For the address locations of the blocks, see the memory maps in Figures 3, 4, 5 and 6.

### 2.3.1 ONE 16-KB BOOT BLOCK

The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. The 16-Kbyte (16,384 bytes) boot block is located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map to accommodate different microprocessor protocols for boot code location. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the $V_{PP}$, RP#, and WP# pins, as is detailed in Section 3.3.

### 2.3.2 TWO 8-KB PARAMETER BLOCKS

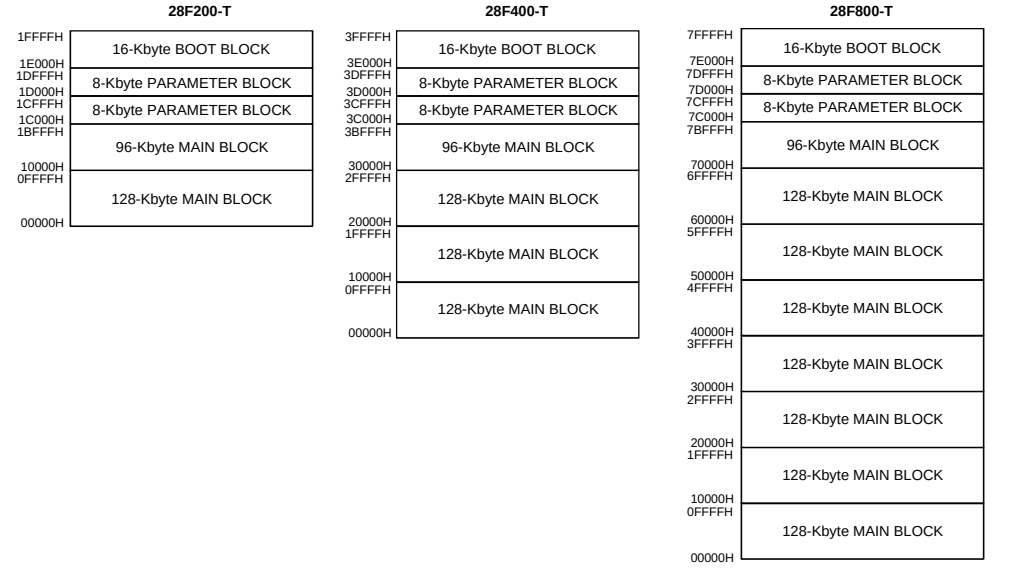
Each boot block component contains two parameter blocks of 8 Kbytes (8,192 bytes) each to facilitate storage of frequently updated small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. These techniques are detailed in Intel's application note, *AP-604 Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM.* The parameter blocks are not write-protectable.

### 2.3.3 MAIN BLOCKS - ONE 96-KB + ADDITIONAL 128-KB BLOCKS

After the allocation of address space to the boot and parameter blocks, the remainder is divided into main blocks for data or code storage. Each device contains one 96-Kbyte (98,304 byte) block and additional 128-Kbyte (131,072 byte) blocks. The 2-Mbit has one 128-KB block; the 4-Mbit, three; and the 8-Mbit, seven.

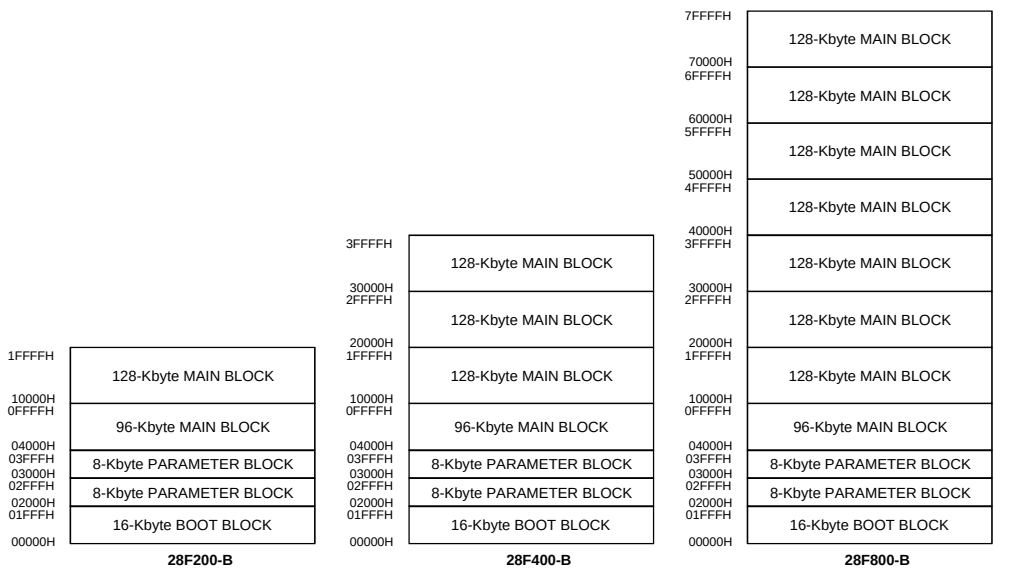


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**NOTE:** Word addresses shown.

**Figure 3. Word-Wide x16-Mode Memory Maps (Top Boot)**

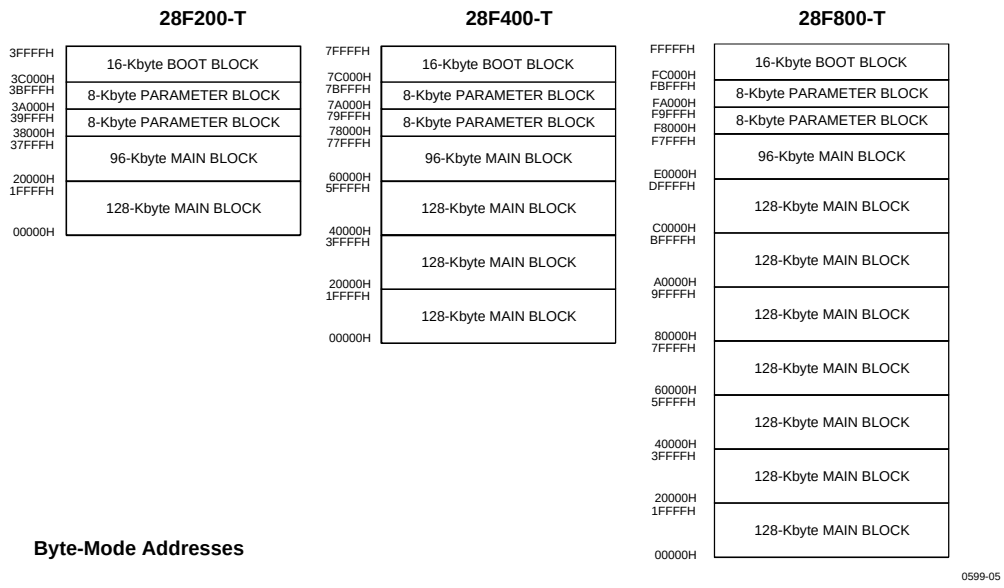



**NOTE:** Word addresses shown.

**Figure 4. Word-Wide x16-Mode Memory Maps (Bottom Boot)**

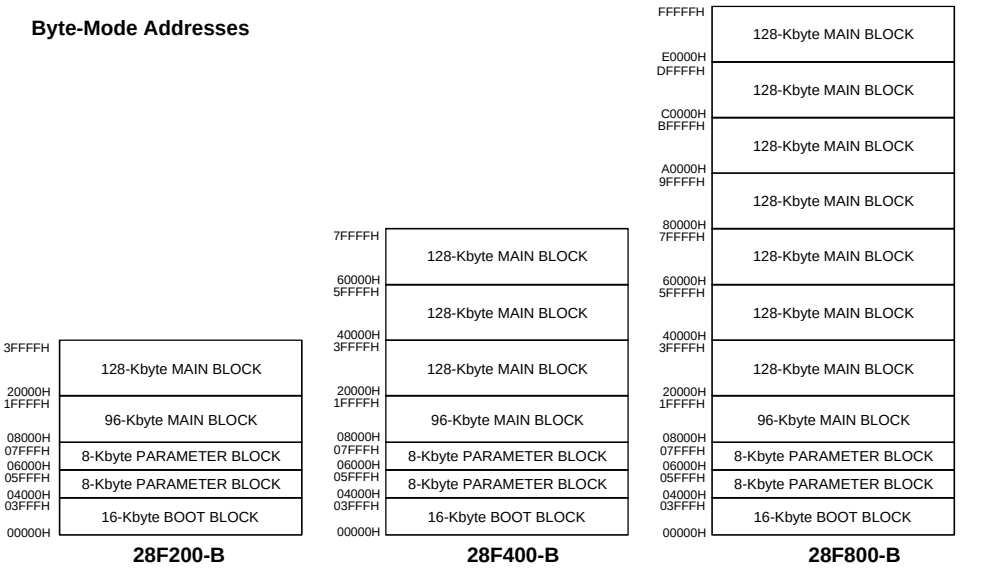


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**NOTE:** In x8 operation, the least significant system address should be connected to $A_1$.

**Figure 5. Byte-Wide x8-Mode Memory Maps (Top Boot)**




**NOTE:** In x8 operation, the least significant system address should be connected to $A_1$.

**Figure 6. Byte-Wide x8-Mode Memory Maps (Bottom Boot)**



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## 3.0 PRINCIPLES OF OPERATION

The system processor accesses the Smart 5 boot block memories through the Command User Interface (CUI), which accepts commands written with standard microprocessor write timings and TTL-level control inputs. The flash can be switched into each of its read and write modes through commands issued to the CUI.

The flash memory has three read modes and two write modes. The read modes are read array, read identifier, and read status. The write modes are program and block erase. An additional mode, erase suspend to read, is available only during suspended block erasures. A comprehensive chart showing the state transitions is in Appendix B.

After initial device power-up or return from deep power-down mode, the device defaults to read array mode. In this mode, manipulation of the memory control pins allows array read, standby, and output disable operations. The other read modes, read identifier and read status register, can be reached by issuing the appropriate command to the CUI. Array data, Identifier codes and status register results can be accessed using these commands independently from the $V_{PP}$ voltage. Read identifier mode can also be accessed by PROM programming equipment by raising $A_9$ to high voltage ($V_{ID}$).

CUI commands sequences also control the write functions of the flash memory, Program and Erase. Issuing program or erase command sequences internally latches addresses and data and initiates Write State Machine (WSM) operations to execute the requested write function. The WSM internally regulates the program and erase algorithms, including pulse repetition, internal verification, and margining of data, freeing the host processor from these tasks and allowing precise control for high reliability. To execute Program or Erase commands, $V_{PP}$ must be at valid write voltage (5V or 12V).

While the WSM is executing a program operation, the device defaults to the read status register mode and all commands are ignored. Thus during the programming process, only status register data can be accessed from the device. While the WSM is executing a erase operation, the device also defaults to the read status register mode but one additional command is available, erase suspend to read, which will suspend the erase operation and allow reading of array data. The suspended erase operation can be completed by issuing the Erase Resume command. After the program or erase operation has completed, the device remains in read status register mode. From this mode any of the other read or write modes can be reached with the appropriate command. For example, to read data, issue the Read Array command. Additional Program or Erase commands can also be issued from this state.

During program or erase operations, the array data is not available for reading or code execution, except during an erase suspend. Consequently, the software that initiates and polls progress of program and erase operations must be copied to and executed from system RAM during flash memory update. After successful completion, reads are again possible via the Read Array command.

Each of the device modes will be discussed in detail in the following sections.

### 3.1 Bus Operations

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. Four control pins dictate the data flow in and out of the component: CE#, OE#, WE#, and RP#. These bus operations are summarized in Table 3 and 4.

#### 3.1.1 READ

The flash memory has three read modes available, read array, read identifier, and read status. These read modes are accessible independent of the $V_{PP}$ voltage. RP# can be at either $V_{IH}$ or $V_{HH}$. The appropriate read-mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from deep power-down mode, the device automatically defaults to read array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and, when active, enables the selected memory device. OE# is the data output ($DQ_0$–$DQ_{15}$) control and when active drives the selected memory data onto the I/O bus. In read modes, WE# must be at $V_{IH}$ and RP# must be at $V_{IH}$ or $V_{HH}$. Figure 14 illustrates a read cycle.



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### 3.1.2 OUTPUT DISABLE

With OE# at a logic-high level ($V_{IH}$), the device outputs are disabled. Output pins $DQ_0$–$DQ_{15}$ are placed in a high-impedance state.

### 3.1.3 STANDBY

Deselecting the device by bringing CE# to a logic-high level ($V_{IH}$) places the device in standby mode which substantially reduces device power consumption. In standby, outputs $DQ_0$–$DQ_{15}$ are placed in a high-impedance state independent of OE#. If deselected during program or erase operation, the device continues functioning and consuming active power until the operation completes.

### 3.1.4 WORD/BYTE CONFIGURATION

The device can be configured for either an 8-bit or 16-bit bus width by setting the BYTE# pin before power-up.

When BYTE# is set to logic low, the byte-wide mode is enabled, where data is read and programmed on $DQ_0$–$DQ_7$ and $DQ_{15}/A_{-1}$ becomes the lowest order address that decodes between the upper and lower byte. $DQ_8$–$DQ_{14}$ are tri-stated during the byte-wide mode.

When BYTE# is at logic high, the word-wide mode is enabled, and data is read and programmed on $DQ_0$–$DQ_{15}$.

### 3.1.5 DEEP POWER-DOWN/RESET

RP# at $V_{IL}$ initiates the deep power-down mode, also referred to as Reset mode.

From read mode, RP# going low for time $t_{PLPH}$ deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from power-down, a time $t_{PHQV}$ is required until the initial memory access outputs are valid. A delay ($t_{PHWL}$ or $t_{PHEL}$) is required after return from power-down before a write can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H. This case is shown in Figure 13A.

If RP# is taken low for time $t_{PLPH}$ during a program or erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence: When RP# goes low, the device shuts down the operation in progress, a process which takes time $t_{PLRH}$ to complete. After this time $t_{PLRH}$, the part will either reset to read array mode (if RP# has gone high during $t_{PLRH}$, Figure 13B) or enter deep power-down mode (if RP# is still logic low after $t_{PLRH}$, Figure 13C). In both cases, after returning from an aborted operation, the relevant time $t_{PHQV}$ or $t_{PHWL}/t_{PHEL}$ must be waited before a read or write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of $t_{PLRH}$ rather than when RP# goes high.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, processor expects to read from the flash memory. Automated flash memories provide status information when read during program or block erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel's Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

### 3.1.6 WRITE

The CUI does not occupy an addressable memory location. Instead, commands are written into the CUI using standard microprocessor write timings when WE# and CE# are low, OE# = $V_{IH}$, and the proper address and data (command) are presented. The address and data for a command are latched on the rising edge of WE# or CE#, whichever goes high first. Figure 15 illustrates a write operation.



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**Table 3. Bus Operations for Word-Wide Mode (BYTE# = $V_{IH}$)**

| Mode | Notes | RP# | CE# | OE# | WE# | $A_9$ | $A_0$ | $V_{PP}$ | $DQ_{0–15}$ |
|---|---|---|---|---|---|---|---|---|---|
| Read | 1,2,3 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | X | $D_{OUT}$ |
| Output Disable | | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | X | High Z |
| Standby | | $V_{IH}$ | $V_{IH}$ | X | X | X | X | X | High Z |
| Deep Power-Down | 9 | $V_{IL}$ | X | X | X | X | X | X | High Z |
| Intelligent Identifier (Mfr.) | 4 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{IL}$ | X | 0089 H |
| Intelligent Identifier (Device) | 4,5 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{IH}$ | X | See Table 5 |
| Write | 6,7,8 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | X | $D_{IN}$ |

**Table 4. Bus Operations for Byte-Wide Mode (BYTE# = $V_{IL}$)**

| Mode | Notes | RP# | CE# | OE# | WE# | $A_9$ | $A_0$ | $A_{–1}$ | $V_{PP}$ | $DQ_{0–7}$ | $DQ_{8–14}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 1,2,3 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | X | X | $D_{OUT}$ | High Z |
| Output Disable | | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | X | X | High Z | High Z |
| Standby | | $V_{IH}$ | $V_{IH}$ | X | X | X | X | X | X | High Z | High Z |
| Deep Power-Down | 9 | $V_{IL}$ | X | X | X | X | X | X | X | High Z | High Z |
| Intelligent Identifier (Mfr.) | 4 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{IL}$ | X | X | 89H | High Z |
| Intelligent Identifier (Device) | 4,5 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{IH}$ | X | X | See Table 5 | High Z |
| Write | 6,7,8 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | X | X | $D_{IN}$ | High Z |

**NOTES:**

1. Refer to DC Characteristics.
2. X can be $V_{IL}$, $V_{IH}$ for control pins and addresses, $V_{PPLK}$ or $V_{PPH}$ for $V_{PP}$.
3. See DC Characteristics for $V_{PPLK}$, $V_{PPH1}$, $V_{PPH2}$, $V_{HH}$, $V_{ID}$ voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, $A_0$ selects, all other addresses = X.
5. See Table 5 for device IDs.
6. Refer to Table 7 for valid $D_{IN}$ during a write operation.
7. Command writes for block erase or program are only executed when $V_{PP}$ = $V_{PPH1}$ or $V_{PPH2}$.
8. To program or erase the boot block, hold RP# at $V_{HH}$ or WP# at $V_{IH}$. See Section 3.3.
9. RP# must be at GND ± 0.2V to meet the maximum deep power-down current specified.



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## 3.2 Modes of Operation

The flash memory has three read modes and two write modes. The read modes are read array, read identifier, and read status. The write modes are program and block erase. An additional mode, erase suspend to read, is available only during suspended block erasures. These modes are reached using the commands summarized in Table 6. A comprehensive chart showing the state transitions is in Appendix B.

### 3.2.1 READ ARRAY

After initial device power-up or return from deep power-down mode, the device defaults to read array mode. This mode can also be entered by writing the Read Array command (FFH). The device remains in this mode until another command is written.

Data is read by presenting the address of the read location in conjunction with a read bus operation.

Once the WSM has started a program or block erase operation, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend command. The Read Array command functions independently of the $V_{PP}$ voltage and RP# can be $V_{IH}$ or $V_{HH}$.

During system design, consideration should be taken to ensure address and control inputs meet required input slew rates of <10 ns as defined in Figures 10 and 11.

### 3.2.2 READ IDENTIFIER

To read the manufacturer and device codes, the device must be in intelligent identifier read mode, which can be reached using two methods: by writing the intelligent identifier command (90H) or by taking the $A_9$ pin to $V_{ID}$. Once in intelligent identifier read mode, $A_0$ = 0 outputs the manufacturer's identification code and $A_0$ = 1 outputs the device code. In byte-wide mode, only the lower byte of the above signatures is read ($DQ_{15}/A_{-1}$ is a "don't care" in this mode). See Table 5 for product signatures. To return to read array mode, write a Read Array command (FFH).

**Table 5. Word-Mode Intelligent Identifier Codes**

| Product | Mfr. ID | Device ID | |
|---|---|---|---|
| | | -T Top Boot | -B Bottom Boot |
| 28F200 | 0089 H | 2274 H | 2275 H |
| 28F400 | 0089 H | 4470 H | 4471 H |
| 28F800 | 0089 H | 889C H | 889D H |

**NOTE:** In byte-mode, the upper byte will be tri-stated.

### 3.2.3 READ STATUS REGISTER

The device Status Register indicates when a program or erase operation is complete, and the success or failure of that operation. The status register is output when the device is read in read status register mode, which can be entered by issuing the Read Status (70H) command to the CUI. This mode is automatically entered when a program or erase operation is initiated, and the device remains in this mode after the operation has completed. The status register bit codes are defined in Table 8

The Status Register bits are output on $DQ_0$–$DQ_7$, in both byte-wide (x8) or word-wide (x16) mode. In the word-wide mode, the upper byte, $DQ_8$–$DQ_{15}$, outputs 00H during a Read Status command. In the byte-wide mode, $DQ_8$–$DQ_{14}$ are tri-stated and $DQ_{15}/A_{-1}$ retains the low order address function.

Note that the contents of the Status Register are latched on the falling edge of OE# or CE#, whichever occurs last in the read cycle. This prevents possible bus errors which might occur if Status Register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the Status Register will not indicate completion of a program or erase operation.

To return to reading from the array, issue a Read Array (FFH) command.

#### 3.2.3.1 Clearing the Status Register

Status register bits SR.5, SR.4, and SR.3 are set to "1"s when appropriate by the WSM but can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 8). By requiring system software to reset these bits, several operations (such as cumulatively





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erasing multiple blocks or programming several bytes in sequence) may be performed before polling the Status Register to determine if an error occurred during the series.

Issue the Clear Status Register command (50H) to clear the status register. It functions independently of the applied $V_{PP}$ voltage and RP# can be $V_{IH}$ or $V_{HH}$. This command is not functional during block erase suspend modes. Resetting the part with RP# also clears the Status Register.

### 3.2.4 WORD/BYTE PROGRAM

Word or byte program operations are executed by a two-cycle command sequence. Program Setup (40H) is issued, followed by a second write that specifies the address and data (latched on the rising edge of WE# or CE#, whichever comes first). The WSM then takes over, controlling the program and program verify algorithms internally. While the WSM is working, the device automatically enters read status register mode and remains there after the word/byte program is complete. (see Figure 7). The completion of the program event is indicated on status register bit SR.7.

When a word/byte program is complete, check status register bit SR.4 for an error flag (“1”). The cause of a failure may be found on SR.3, which indicates “1” if $V_{PP}$ was out of program/erase voltage range ($V_{PPH1}$ or $V_{PPH2}$). The Status Register should be cleared before the next operation. The internal WSM verify only detects errors for “1”s that do not successfully write to “0”s.

Since the device remains in Status Register Read mode after programming is completed, a command must be issued to switch to another mode before beginning a different operation.

### 3.2.5 BLOCK ERASE

A block erase changes all block data to 1’s (FFFFH) and is initiated by a two-cycle command. An Erase Setup command (20H) is issued first, followed by an Erase Confirm command (D0H) along with an address within the target block. The address will be latched at the rising edge of WE# or CE#, whichever comes first.

Internally, the WSM will program all bits in the block to “0,” verify all bits are adequately programmed to “0,” erase all bits to “1,” and verify that all bits in the block are sufficiently erased. After block erase command sequence is issued, the device automatically enters read status register mode and outputs status register data when read (see Figure 8). The completion of the erase event is indicated on status register bit SR.7.

When an erase is complete, check status register bit SR.5 for an error flag (“1”). The cause of a failure may be found on SR.3, which indicates “1” if $V_{PP}$ was out of program/erase voltage range ($V_{PPH1}$ or $V_{PPH2}$). If an Erase Setup (20H) command is issued but not followed by an Erase Confirm (D0H) command, then both the Program Status (SR.4) and the Erase Status (SR.5) will be set to “1.”

The Status Register should be cleared before the next operation. Since the device remains in Status Register Read mode after erasing is completed, a command must be issued to switch to another mode before beginning a different operation.

#### 3.2.5.1 Erase Suspend/Resume

The Erase Suspend command (B0H) interrupts an erase operation in order to read data in another block of memory. While the erase is in progress, issuing the Erase Suspend command requests that the WSM suspend the erase algorithm after a certain latency period. The device outputs Status Register data when read after the Erase Suspend command is issued. Status Register bits SR.7 and SR.6 indicate when the block erase operation has been suspended (both will be set to “1”).

At this point, a Read Array command (FFH) can be written to read from blocks other than that which is suspended. The only other valid commands at this time are Erase Resume (D0H) or Read Status Register.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking CE# to $V_{IH}$, which reduces active current draw. $V_{PP}$ must remain at $V_{PPH1}$ or $V_{PPH2}$ (the same $V_{PP}$ level used for block erase) while erase is suspended. RP# must also remain at $V_{IH}$ or $V_{HH}$ (the same RP# level used for block erase).

To resume the erase operation, enable the chip by taking CE# to $V_{IL}$, then issue the Erase Resume command, which continues the erase sequence to completion. As with the end of a standard erase operation, the status register must be read, cleared, and the next instruction issued in order to continue.



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**Table 6. Command Codes and Descriptions**

| Code | Device Mode | Description |
|---|---|---|
| 00 | Invalid/ Reserved | Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions. |
| FF | Read Array | Places the device in read array mode, so that array data will be output on the data pins. |
| 40 | Program Set-Up | Sets the CUI into a state such that the next write will load the Address and Data registers. The next write after the Program Set-Up command will latch addresses and data on the rising edge and begin the program algorithm. The device then defaults to the read status mode, where the device outputs Status Register data when OE# is enabled. To read the array, issue a Read Array command.<br><br>To cancel a program operation after issuing a Program Set-Up command, write all 1's (FFH for x8, FFFFH for x16) to the CUI. This will return to read status register mode after a standard program time without modifying array contents. If a program operation has already been initiated to the WSM this command can not cancel that operation in progress. |
| 10 | Alternate Prog Set-Up | (See 40H/Program Set-Up) |
| 20 | Erase Set-Up | Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status (SR.4) and Erase Status (SR.5) bits of the Status Register to a "1," place the device into the read Status Register state, and wait for another command without modifying array contents. This can be used to cancel an erase operation after the Erase Setup command has been issued. If an operation has already been initiated to the WSM this can not cancel that operation in progress. |
| D0 | Erase Resume/ Erase Confirm | If the previous command was an Erase Set-Up command, then the CUI will latch address and data, and begin erasing the block indicated on the address pins. During erase, the device will respond only to the Read Status Register and Erase Suspend commands and will output Status Register data when OE# is toggled low. Status Register data is updated by toggling either OE# or CE# low. |
| B0 | Erase Suspend | Valid only while an erase operation is in progress and will be ignored in any other circumstance. Issuing this command will begin to suspend erase operation. The Status Register will indicate when the device reaches erase suspend mode. In this mode, the CUI will respond only to the Read Array, Read Status Register, and Erase Resume commands and the WSM will also set the WSM Status bit to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is made active. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path. See Section 3.2.5.1. |
| 70 | Read Status Register | Puts the device into the read status register mode, so that reading the device outputs status register data, regardless of the address presented to the device. The device automatically enters this mode after program or erase has completed. This is one of the two commands that is executable while the WSM is operating. See Section 3.2.3. |



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**Table 6. Command Codes and Descriptions** (Continued)

| Code | Device Mode | Description |
|---|---|---|
| 50 | Clear Status Register | The WSM can only set the Program Status and Erase Status bits in the status register to "1"; it cannot clear them to "0."<br><br>The status register operates in this fashion for two reasons. The first is to give the host CPU the flexibility to read the status bits at any time. Second, when programming a string of bytes, a single status register query after programming the string may be more efficient, since it will return the accumulated error status of the entire string. See Section 3.2.3.1. |
| 90 | Intelligent Identifier | Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes. ($A_0$ = 0 for manufacturer, $A_0$ = 1 for device, all other address inputs are ignored). See Section 3.2.2. |

**Table 7. Command Bus Definitions**

| Command | Note | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|
| | | Oper | Addr | Data | Oper | Addr | Data |
| Read Array | | Write | X | FFH | | | |
| Intelligent Identifier | 2,4 | Write | X | 90H | Read | IA | IID |
| Read Status Register | 3 | Write | X | 70H | Read | X | SRD |
| Clear Status Register | 3 | Write | X | 50H | | | |
| Word/Byte Program | 6,7 | Write | PA | 40H/10H | Write | PA | PD |
| Block Erase/Confirm | 5 | Write | BA | 20H | Write | BA | D0H |
| Erase Suspend | | Write | X | B0H | | | |
| Erase Resume | | Write | X | D0H | | | |

**ADDRESS**
BA = Block Address
IA = Identifier Address
PA = Program Address
X = Don't Care

**DATA**
SRD = Status Register Data
IID = Identifier Data
PD = Program Data

**NOTES:**
1. Bus operations are defined in Tables 3 and 4.
2. IA = Identifier Address: $A_0$ = 0 for manufacturer code, $A_0$ = 1 for device code.
3. SRD - Data read from Status Register.
4. IID = Intelligent Identifier Data. Following the Intelligent Identifier command, two read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. PA = Address to be programmed. PD = Data to be programmed at location PA.
7. Either 40H or 10H commands is valid.
8. When writing commands to the device, the upper data bus [$DQ_8$–$DQ_{15}$] = X which is either $V_{IL}$ or $V_{IH}$, to minimize current draw.



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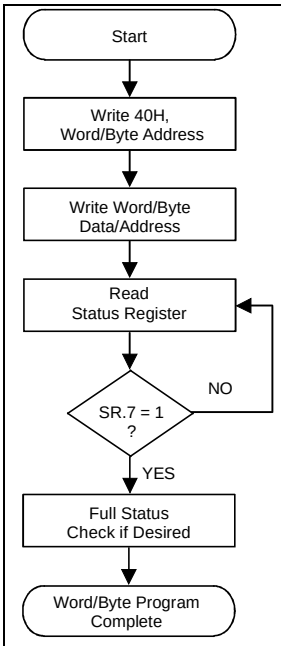
**Table 8. Status Register Bit Definition**

| WSMS | ESS | ES | DWS | VPPS | R | R | R |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | NOTES: |
|---|---|
| SR.7 WRITE STATE MACHINE STATUS<br>1 = Ready (WSMS)<br>0 = Busy | Check WSM bit first to determine word/byte program or block erase completion, before checking Program or Erase Status bits. |
| SR.6 = ERASE-SUSPEND STATUS (ESS)<br>1 = Erase Suspended<br>0 = Erase In Progress/Completed | When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued. |
| SR.5 = ERASE STATUS (ES)<br>1 = Error In Block Erasure<br>0 = Successful Block Erase | When this bit is set to "1," one of the following has occurred:<br>1. $V_{PP}$ out of range.<br>2. WSM has applied the max number of erase pulses to the block and is still unable to verify successful block erasure.<br>3. Erase Setup command was followed by a command other than Erase Confirm. |
| SR.4 = PROGRAM STATUS (DWS)<br>1 = Error in Byte/Word Program<br>0 = Successful Byte/Word Program | When this bit is set to "1," one of the following has occurred:<br>1. $V_{PP}$ out of range.<br>2. WSM has applied the max number of program pulses and is still unable to verify a successful program.<br>3. Erase Setup command was followed by a command other than Erase Confirm. |
| SR.3 = $V_{PP}$ STATUS (VPPS)<br>1 = $V_{PP}$ Low Detect, Operation Abort<br>0 = $V_{PP}$ OK | The $V_{PP}$ Status bit does not provide continuous indication of $V_{PP}$ level. The WSM interrogates $V_{PP}$ level only after the Program or Erase command sequences have been entered, and informs the system if $V_{PP}$ is out of range. The $V_{PP}$ Status bit is not guaranteed to report accurate feedback between $V_{PPLK}$ and $V_{PPH}$. |
| SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | These bits are reserved for future use and should be masked out when polling the Status Register. |



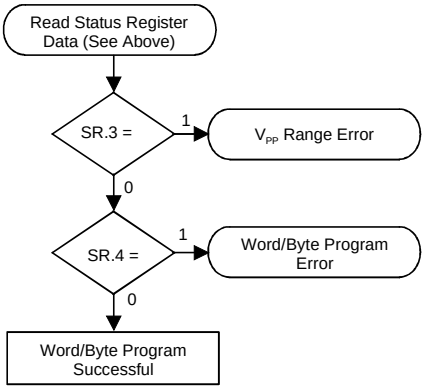
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| Bus Operation | Command | Comments |
|---|---|---|
| Write | Setup Program | Data = 40H<br>Addr = Word/Byte to Program |
| Write | Program | Data = Data to Program<br>Addr = Location to Program |
| Read | | Status Register Data<br>Toggle CE# or OE#<br>to Update SRD. |
| Standby | | Check SR.7<br>1 = WSM Ready<br>0 = WSM Busy |

Repeat for subsequent word/byte program operations.
SR Full Status Check can be done after each word/byte program operation, or after a sequence of word/byte programs.
Write FFH after the last program operation to reset device to read array mode.

**FULL STATUS CHECK PROCEDURE**




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1 = $V_{PP}$ Low Detect |
| Standby | | Check SR.4<br>1 = Word Byte Program Error |

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked.

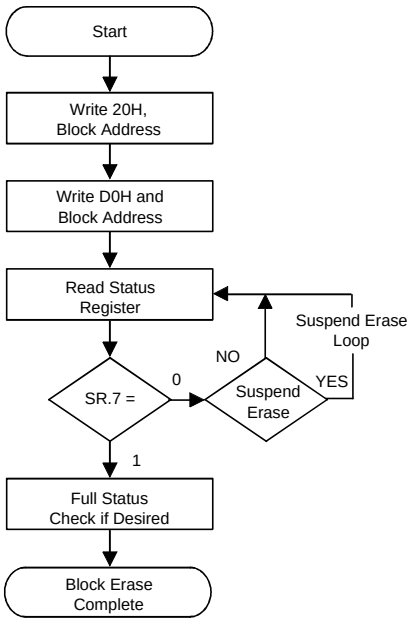
If error is detected, clear the Status Register before attempting retry or other error recovery.

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**Figure 7. Automated Word/Byte Program Flowchart**



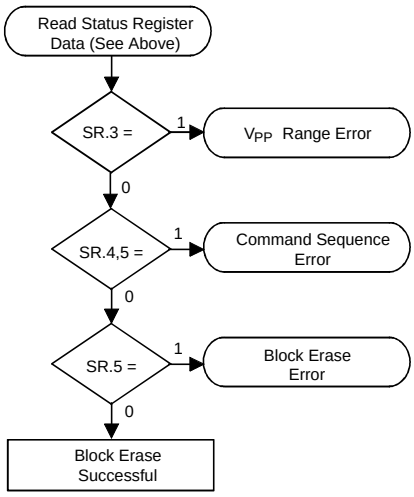
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| Bus Operation | Command | Comments |
|---|---|---|
| Write | Erase Setup | Data = 20H<br>Addr = Within Block to be Erased |
| Write | Erase Confirm | Data = D0H<br>Addr = Within Block to be Erased |
| Read | | Status Register Data<br>Toggle CE# or OE#<br>to Update Status Register |
| Standby | | Check SR.7<br>1 = WSM Ready<br>0 = WSM Busy |

Repeat for subsequent block erasures.
Full Status Check can be done after each block erase, or after a sequence of block erasures.
Write FFH after the last operation to reset device to read array mode.

**FULL STATUS CHECK PROCEDURE**




| Bus Operation | Command | Comments |
|---|---|---|
| Standby | | Check SR.3<br>1 = $V_{PP}$ Low Detect |
| Standby | | Check SR.4,5<br>Both 1 = Command Sequence Error |
| Standby | | Check SR.5<br>1 = Block Erase Error |

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erase before full status is checked.

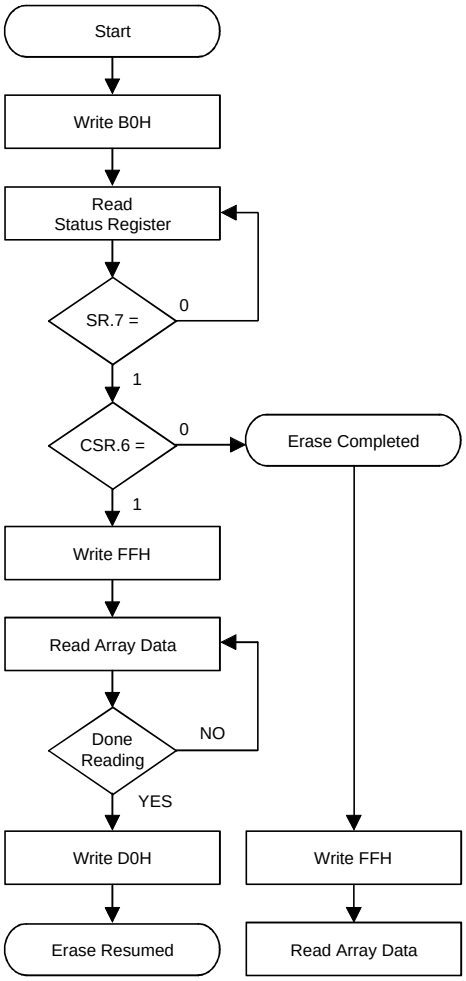
If error is detected, clear the Status Register before attempting retry or other error recovery.

0599-08

**Figure 8. Automated Block Erase Flowchart**



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| Bus Operation | Command | Comments |
|---|---|---|
| Write | Erase Suspend | Data = B0H<br>Addr = X |
| Read | | Status Register Data<br>Toggle CE# or OE#<br>to update SRD.<br>Addr = X |
| Standby | | Check SR.7<br>1 = WSM Ready<br>0 = WSM Busy |
| Standby | | Check SR.6<br>1 = Erase Suspended<br>0 = Erase Completed |
| Write | Read Array | Data = FFH<br>Addr = X |
| Read | | Read array data from block other than the one being erased. |
| Write | Erase Resume | Data = D0H<br>Addr = X |

**Figure 9. Erase Suspend/Resume Flowchart**



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## 3.3 Boot Block Locking

The boot block family architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

### 3.3.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the device, the $V_{PP}$ voltage can be held low. When $V_{PP}$ is below $V_{PPLK}$, any program or erase operation will result in a error in the Status Register.

### 3.3.2 WP# = $V_{IL}$ FOR BOOT BLOCK LOCKING

When WP# = $V_{IL}$, the boot block is locked and any program or erase operation to the boot block will result in an error in the Status Register. All other blocks remain unlocked in this condition and can be programmed or erased normally. Note that this feature is overridden and the boot block unlocked when RP# = $V_{HH}$.

### 3.3.3 RP# = $V_{HH}$ OR WP# = $V_{IH}$ FOR BOOT BLOCK UNLOCKING

Two methods can be used to unlock the boot block:

1. WP# = $V_{IH}$
2. RP# = $V_{HH}$

If both or either of these two conditions are met, the boot block will be unlocked and can be programmed or erased.

The truth table, Table 9, clearly defines the write protection methods.

### 3.3.4 NOTE FOR 8-MBIT 44-PSOP PACKAGE

The 8-Mbit in the 44-PSOP package does not have a WP# because no other pins were available for the 8-Mbit upgrade address. Thus, in this density-package combination only, $V_{HH}$ (12V) on RP# is required to unlock the boot block and unlocking with a logic-level signal is not possible. If this unlocking functionality is required, and 12V is not available in-system, please consider using the 48-TSOP package, which has a WP# pin and can be unlocked with a logic-level signal. All other density-package combinations have WP# pins.

**Table 9. Write Protection Truth Table**

| $V_{PP}$ | RP# | WP# | Write Protection Provided |
|---|---|---|---|
| $V_{IL}$ | X | X | All Blocks Locked |
| ≥ $V_{PPLK}$ | $V_{IL}$ | X | All Blocks Locked (Reset) |
| ≥ $V_{PPLK}$ | $V_{HH}$ | X | All Blocks Unlocked |
| ≥ $V_{PPLK}$ | $V_{IH}$ | $V_{IL}$ | Boot Block Locked |
| ≥ $V_{PPLK}$ | $V_{IH}$ | $V_{IH}$ | All Blocks Unlocked |

## 4.0 DESIGN CONSIDERATIONS

The following section discusses recommended design considerations which can improve the robustness of system designs using flash memory.

## 4.1 Power Consumption

Intel flash components contain features designed to reduce power requirements. The following sections will detail how to take advantage of these features.

### 4.1.1 ACTIVE POWER

Asserting CE# to a logic-low level and RP# to a logic-high level places the device in the active mode. Refer to the DC Characteristics table for $I_{CCR}$ current values.

### 4.1.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings (APS) provides low-power operation in active mode. Power Reduction Control (PRC) circuitry allows the device to put itself into a low current state when not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical $I_{CC}$ current is less than 1 mA. The device stays in this static state with outputs valid until a new location is read.





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#### 4.1.3 STANDBY POWER

When CE# is at a logic-high level ($V_{IH}$), and the device is not programming or erasing, the memory enters in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs ($DQ_0$–$DQ_{15}$ or $DQ_0$–$DQ_7$) are placed in a high-impedance state independent of the status of the OE# signal. When CE# is at logic-high level during program or erase operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

#### 4.1.4 DEEP POWER-DOWN MODE

The Smart 5 boot block family supports a low typical $I_{CCD}$ in deep power-down mode, which turns off all circuits to save power. This mode is activated by the RP# pin when it is at a logic-low (GND ± 0.2V). Note: BYTE# pin must be at CMOS levels to meet the $I_{CCD}$ specification.

During read modes, the RP# pin going low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum access time of $t_{PHQV}$. RP# transitions to $V_{IL}$, or turning power off to the device will clear the Status Register.

During an program or erase operation, RP# going low for time $t_{PLPH}$ will abort the operation, but the location's memory contents will no longer valid and additional timing must be met. See Section 3.1.5 and 6.1 for additional information.

### 4.2 Power-Up/Down Operation

The device protects against accidental block erasure or programming during power transitions. Power supply sequencing is not required, so either $V_{PP}$ or $V_{CC}$ can power-up first. The CUI defaults to the read mode after power-up, but the system must drop CE# low or present an address to receive valid data at the outputs.

A system designer must guard against spurious writes when $V_{CC}$ voltages are above $V_{LKO}$ and $V_{PP}$ is active. Since both WE# and CE# must be low for a command write, driving either signal to $V_{IH}$ will inhibit writes to the device. Additionally, alteration of memory can only occur after successful completion of a two-step command sequences. The device is also disabled until RP# is brought to $V_{IH}$, regardless of the state of its control inputs. By holding the device in reset (RP# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

#### 4.2.1 RP# CONNECTED TO SYSTEM RESET

Using RP# properly during system reset is important with automated program/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may in a mode other than Read Array. Intel's Flash memories allow proper CPU initialization following a system reset by connecting the RP# pin to the same RESET# signal that resets the system CPU.

### 4.3 Board Design

#### 4.3.1 POWER SUPPLY DECOUPLING

Flash memory's switching characteristics require careful decoupling methods. System designers should consider three supply current issues: standby current levels ($I_{CCS}$), active current levels ($I_{CCR}$), and transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between $V_{CC}$ and GND, and between $V_{PP}$ and GND. These high- frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

#### 4.3.2 $V_{PP}$ TRACE ON PRINTED CIRCUIT BOARDS

In-system updates to the flash memory requires special consideration of the $V_{PP}$ power supply trace by the printed circuit board designer. Since the $V_{PP}$ pin supplies the current for programming and erasing, it should have similar trace widths and layout considerations as given to the $V_{CC}$ power supply trace. Adequate $V_{PP}$ supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.



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# 5.0 SPECIFICATIONS

## 5.1 Absolute Maximum Ratings*

Commercial Operating Temperature

During Read/Erase/Program .....0°C to +70°C

Temperature Under Bias .....–10°C to +80°C

Extended Operating Temperature

During Read/Erase/Program ....–40°C to +85°C

Temperature Under Bias .....–40°C to +85°C

Storage Temperature.....–65°C to +125°C

Voltage on Any Pin

(except $V_{CC}$, $V_{PP}$, $A_9$ and RP#)
with Respect to GND.....–2.0V to +7.0V(2)

Voltage on Pin RP# or Pin $A_9$
with Respect to GND..... –2.0V to +13.5V(2,3)

$V_{PP}$ Program Voltage with Respect to GND during Block Erase

and Word/Byte Program.... –2.0V to +14.0V(2,3)

$V_{CC}$ Supply Voltage
with Respect to GND.....–2.0V to +7.0V(2)

Output Short Circuit Current .....100 mA (4)

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output pins is $V_{CC}$ + 0.5V which, during transitions, may overshoot to $V_{CC}$ + 2.0V for periods <20 ns.
3. Maximum DC voltage on $V_{PP}$ may overshoot to +14.0V for periods <20 ns. Maximum DC voltage on RP# or $A_9$ may overshoot to 13.5V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

## 5.2 Test Conditions

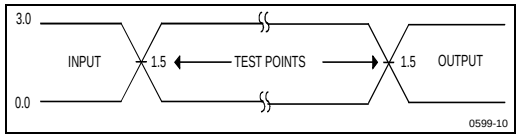



**Figure 10. High Speed Test Waveform**

NOTE: AC test inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

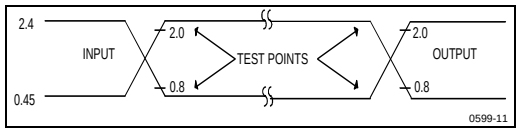
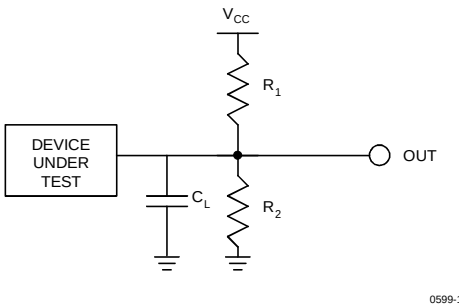



**Figure 11. Standard Test Waveform**

**NOTE:** AC test inputs driven at $V_{OH}$ (2.4 $V_{TTL}$) for logic "1" and $V_{OL}$ (0.45 $V_{TTL}$) for logic "0." Input timing begins at $V_{IH}$ (2.0 $V_{TTL}$) and $V_{IL}$ (0.8 $V_{TTL}$) . Output timing ends at $V_{IH}$ and $V_{IL}$. Input rise and fall times (10% to 90%) <10 ns.




**NOTE:**
$C_L$ includes jig capacitance.

**Figure 12. Test Configuration**

**Test Configuration Component Values**

| Test Configuration | $C_L$ (pF) | $R_1$ (Ω) | $R_2$ (Ω) |
|---|---|---|---|
| 5V Standard Test | 100 | 580 | 390 |
| 5V High-Speed Test | 30 | 580 | 390 |





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## 5.3 Operating Conditions

**Table 10. Temperature and $V_{CC}$ Operating Conditions**

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_A$ | Commercial Operating Temperature | | 0 | +70 | °C |
| | Extended Operating Temperature | | -40 | +85 | °C |
| $V_{CC}$ | 5V $V_{CC}$ Supply Voltage (10%) | 1 | 4.50 | 5.50 | Volts |
| | 5V $V_{CC}$ Supply Voltage (5%) | 2 | 4.75 | 5.25 | Volts |
| $V_{PP}$ | 5V $V_{PP}$ Supply Voltage (10%) | 1 | 4.50 | 5.50 | Volts |
| | 12V $V_{CC}$ Supply Voltage (5%) | 1 | 11.4 | 12.6 | Volts |

**NOTES:**
1. 10% $V_{CC}$ specifications apply to the standard test configuration (Figures 11 and 12).
2. 5% $V_{CC}$ specifications apply to the high-speed test configuration (Figures 10 and 12).

## 5.4 Reset Operations

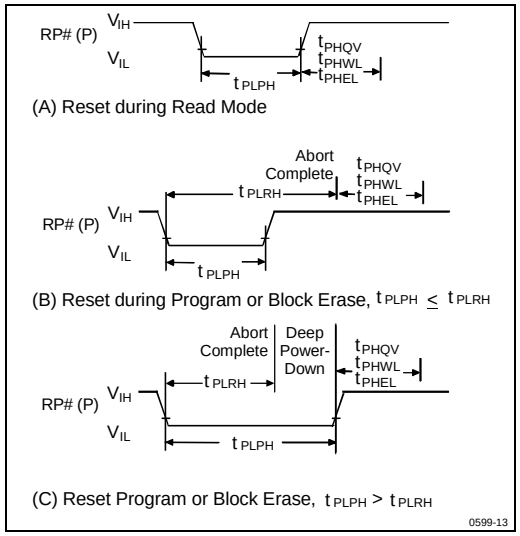



**Figure 13. AC Waveform for Reset Operation**

**Table 11. Reset Specifications(1)**

| Sym | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PLPH}$ | RP# Pulse Low Time | 60 | | ns |
| $t_{PLRH}$ | RP# Low to Reset during Prog/Erase | | 12 | µs |

1. If RP# is tied to $V_{CC}$, these specs are not applicable.
2. These specifications are valid for all product versions (packages and speeds).
3. If RP# is asserted while a program or block erase, is not executing, the reset will complete within $t_{PLPH}$.
4. A reset time, $t_{PHQV}$, is required after $t_{PLRH}$ until outputs are valid. See Section 3.1.5 for detailed information.



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## 5.6 Electrical Specifications

**Table 12. DC Characteristics (Commercial and Extended Temperature)**

| Sym | Parameter | Temp Note | Comm Typ | Comm Max | Extended Typ | Extended Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Load Current | 1 | | ±1.0 | | ±1.0 | µA | $V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND |
| $I_{LO}$ | Output Leakage Current | 1 | | ± 10 | | ± 10 | µA | $V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND |
| $I_{CCS}$ | $V_{CC}$ Standby Current | 1,3 | | 2.0 | | 2.5 | mA | $V_{CC} = V_{CC}$ Max, CE# = RP# = BYTE# = WP# = $V_{IH}$ |
| | | | | 130 | | 150 | µA | $V_{CC} = V_{CC}$ Max<br>CE# = RP# = $V_{CC}$ ± 0.2V |
| $I_{CCD}$ | $V_{CC}$ Deep Power-Down Current | 1 | | 8 | | 8 | µA | $V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND<br>RP# = GND ± 0.2V |
| $I_{CCR}$ | $V_{CC}$ Read Current (Word or Byte Mode) | 1,5, 6 | | 60 | | 65 | mA | **CMOS INPUTS**<br>$V_{CC} = V_{CC}$ Max, CE# = GND, OE# = $V_{CC}$, f = 10 MHz (5V), $I_{OUT}$ = 0 mA, Inputs=GND or $V_{CC}$ |
| | | | | 65 | | 70 | mA | **TTL INPUTS**<br>$V_{CC} = V_{CC}$ Max, CE# = $V_{IL}$, OE# = $V_{IH}$ , f = 10 MHz (5V), $I_{OUT}$ = 0 mA, Inputs = $V_{IL}$ or $V_{IH}$ |
| $I_{CCW}$ | $V_{CC}$ Program Current | 1,4 | | 50 | | 50 | mA | $V_{PP} = V_{PPH}1$ (at 5V) |
| | (Word or Byte Mode) | | | 45 | | 45 | mA | $V_{PP} = V_{PPH}2$ (at 12V) |
| $I_{CCE}$ | $V_{CC}$ Erase Current | 1,4 | | 35 | | 45 | mA | $V_{PP} = V_{PPH}1$ (at 5V) |
| | | | | 30 | | 40 | mA | $V_{PP} = V_{PPH}2$ (at 12V) |
| $I_{CCES}$ | $V_{CC}$ Erase Susp Current | 1,2 | | 10 | | 12.0 | mA | CE# = $V_{IH}$ , Block Erase Suspend |
| $I_{PPS}$ | $V_{PP}$ Standby Current | 1 | | ± 10 | | ± 15 | µA | $V_{PP} < V_{PPH}2$ |
| $I_{PPD}$ | $V_{PP}$ Deep Power-Down Current | 1 | | 5.0 | | 10 | µA | RP# = GND ± 0.2V |
| $I_{PPR}$ | $V_{PP}$ Read Current | 1 | | 200 | | 200 | µA | $V_{PP} \geq V_{PPH}2$ |
| $I_{PPW}$ | $V_{PP}$ Program Current | 1,4 | | 25 | | 30 | mA | $V_{PP} = V_{PPH}1$ (at 5V) |
| | (Word or Byte Mode) | | | 20 | | 25 | | $V_{PP} = V_{PPH}2$ (at 12V) |
| $I_{PPE}$ | $V_{PP}$ Erase Current | 1,4 | | 20 | | 25 | mA | $V_{PP} = V_{PPH}1$ (at 5V) |
| | | | | 15 | | 20 | | $V_{PP} = V_{PPH}2$ (at 12V) |
| $I_{PPES}$ | $V_{PP}$ Erase Susp Current | 1 | | 200 | | 200 | µA | $V_{PP} = V_{PPH}$ , Block Erase Suspend |
| $I_{RP\#}$ | RP# Unlock Current | 1,4 | | 500 | | 500 | µA | RP# = $V_{HH}$ (to unlock Boot Block) |
| $I_{ID}$ | $A_9$ Identifier Current | 1,4 | | 500 | | 500 | µA | $A_9 = V_{ID}$ |





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**Table 12. DC Characteristics (Commercial and Extended Temperature)** (Continued)

| Sym | Parameter | Temp Note | Comm/Ext Min | Comm/Ext Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{ID}$ | $A_9$ Intelligent Identifier Voltage | | 11.4 | 12.6 | V | |
| $V_{IL}$ | Input Low Voltage | | –0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$ + 0.5V | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.45 | V | $V_{CC} = V_{CC}$ Min, $I_{OL}$ = 5.8 mA |
| $V_{OH}1$ | Output High Voltage (TTL) | | 2.4 | | V | $V_{CC} = V_{CC}$ Min, $I_{OH}$ = –2.5 mA |
| $V_{OH}2$ | Output High Voltage (CMOS) | | 0.85 x $V_{CC}$ | | V | $V_{CC} = V_{CC}$ Min, $I_{OH}$ = –2.5 mA |
| | | | $V_{CC}$ – 0.4V | | V | $V_{CC} = V_{CC}$ Min, $I_{OH}$ = –100 µA |
| $V_{PPLK}$ | $V_{PP}$ Lock-Out Voltage | 3 | 0.0 | 1.5 | V | Complete Data Protection |
| $V_{PPH}1$ | $V_{PP}$ (Prog/Erase Operations) | | 4.5 | 5.5 | V | $V_{PP}$ at 5V |
| $V_{PPH}2$ | $V_{PP}$ (Prog/Erase Operations) | | 11.4 | 12.6 | V | $V_{PP}$ at 12V |
| $V_{LKO}$ | $V_{CC}$ Erase/Prog Lock Voltage | | 2.0 | | V | |
| $V_{HH}$ | RP# Unlock Voltage | | 11.4 | 12.6 | V | Boot Block Program/Erase |

**NOTES:**

1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC}$ = 5.0V, T = +25°C. These currents are valid for all product versions (packages and speeds).
2. $I_{CCES}$ is specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of $I_{CCES}$ and $I_{CCR}$.
3. Block erases and word/byte program operations are inhibited when $V_{PP} = V_{PPLK}$, and not guaranteed in the range between $V_{PPH}1$ and $V_{PPLK}$.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces $I_{CCR}$ to less than 1 mA typical, in static operation.
6. CMOS Inputs are either $V_{CC}$ ± 0.2V or GND ± 0.2V. TTL Inputs are either $V_{IL}$ or $V_{IH}$.

**Table 13. Capacitance ($T_A$ = 25 °C, f = 1 MHz)**

| Symbol | Parameter | Note | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4 | 6 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | Output Capacitance | 4, 7 | 10 | 12 | pF | $V_{OUT}$ = 0V |

1. Sampled, not 100% tested.

## PRODUCT PREVIEW



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**Table 14. AC Characteristics: Read Operations (Commercial and Extended Temperature)**

| # | Sym | Parameter | | Temp | Commercial | | | | | | Extended | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Speed | -60/-70 | | | | -80/-90 | | -80/-90 | | |
| | | | | $V_{CC}$ | 5V ± 5% (4) | | 5V±10% (5) | | 5V± 10%(5) | | 5V± 10%(5) | | |
| | | | | Load | 30 pF | | 100 pF | | 100 pF | | 100 pF | | |
| | | | | Notes | Min | Max | Min | Max | Min | Max | Min | Max | |
| R1 | $t_{AVAV}$ | Read Cycle | 2-, 4-Mbit | | 60 | | 70 | | 80 | | 80 | | ns |
| | | Time | 8-Mbit | | 70 | | 80 | | 90 | | 90 | | ns |
| R2 | $t_{AVQV}$ | Address to | 2-, 4-Mbit | | | 60 | | 70 | | 80 | | 80 | ns |
| | | Output Delay | 8-Mbit | | | 70 | | 80 | | 90 | | 90 | ns |
| R3 | $t_{ELQV}$ | CE# to | 2-, 4-Mbit | 2 | | 60 | | 70 | | 80 | | 80 | ns |
| | | Output Delay | 8-Mbit | | | 70 | | 80 | | 90 | | 90 | ns |
| R4 | $t_{GLQV}$ | OE# to Output Delay | | 2 | | 30 | | 35 | | 40 | | 40 | ns |
| R5 | $t_{PHQV}$ | RP# to Output Delay | | | | 450 | | 450 | | 450 | | 450 | ns |
| R6 | $t_{ELQX}$ | CE# to Output in Low Z | | 3 | 0 | | 0 | | 0 | | 0 | | ns |
| R7 | $t_{GLQX}$ | OE# to Output in Low Z | | 3 | 0 | | 0 | | 0 | | 0 | | ns |
| R8 | $t_{EHQZ}$ | CE# to Output in High Z | | 3 | | 20 | | 20 | | 20 | | 25 | ns |
| R9 | $t_{GHQZ}$ | OE# to Output in High Z | | 3 | | 20 | | 20 | | 20 | | 25 | ns |
| R10 | $t_{OH}$ | Output Hold from Address, CE#, or OE# Change, Whichever Occurs First | | 3 | 0 | | 0 | | 0 | | 0 | | ns |

**NOTES:**

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to $t_{CE}$–$t_{OE}$ after the falling edge of CE# without impact on $t_{CE}$.
3. Sampled, but not 100% tested.
4. See Test Configurations (Figure 12), 5V High-Speed Test component values.
5. See Test Configurations (Figure 12), 5V Standard Test component values.
6. Dynamic BYTE# switching between word and byte modes is not supported. Mode changes must be made when the device is in deep power-down or powered down.



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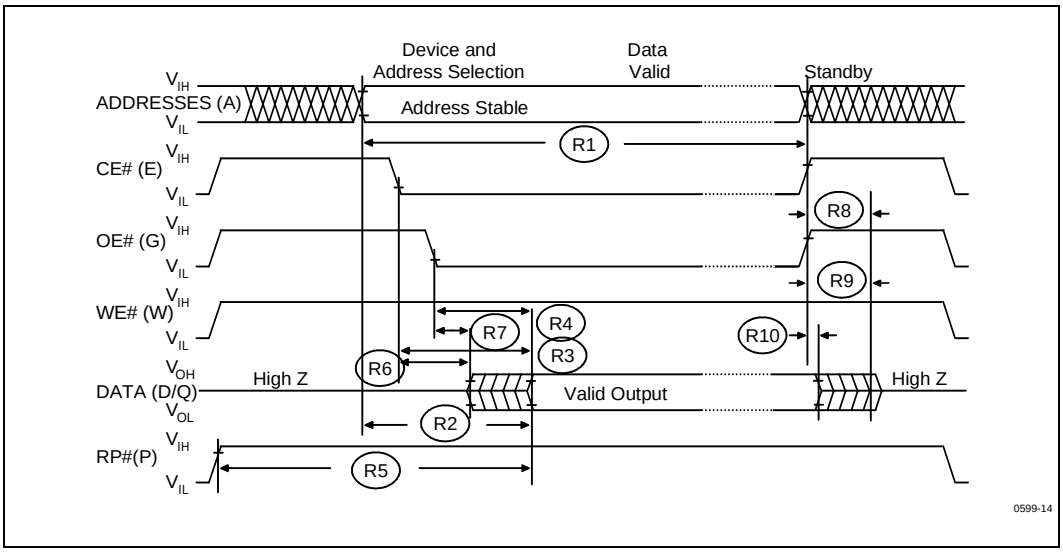



**Figure 14. AC Waveforms for Read Operations**



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**Table 15. AC Characteristics: Write Operations (Commercial and Extended Temperature)**

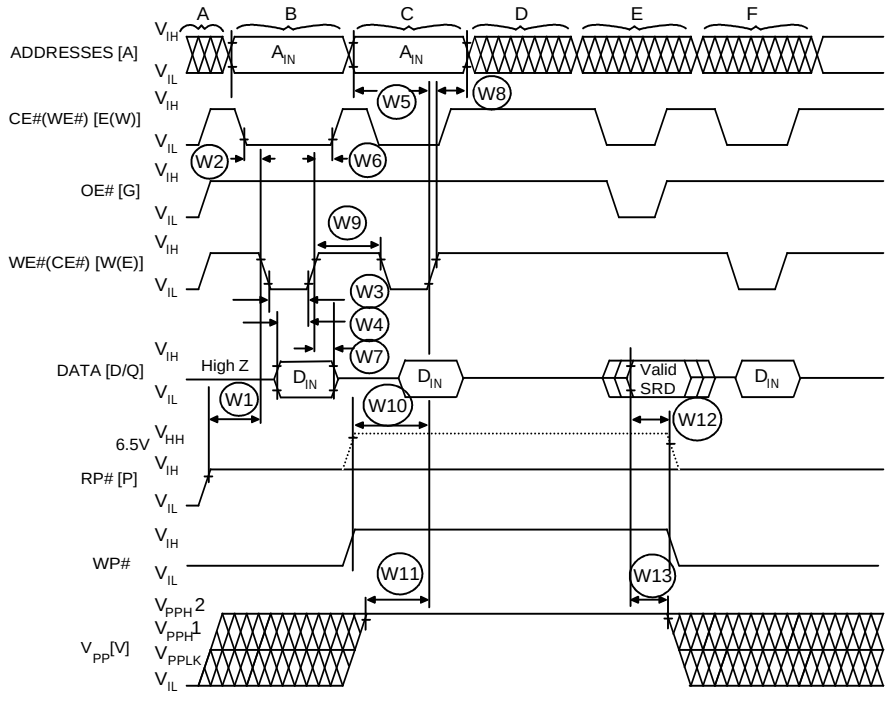
| # | Sym | Parameter | | Note | Comm | | Extended | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | Min | Max | |
| W1 | $t_{PHWL}$ ($t_{PHEL}$) | RP# High Recovery to WE# (CE#) Going Low | | | 450 | | 450 | | ns |
| W2 | $t_{ELWL}$ ($t_{WLEL}$) | CE# (WE#) Setup to WE# (CE#) Going Low | | | 0 | | 0 | | ns |
| W3 | $t_{WP}$ | Write Pulse Width | | 9 | 50 | | 60 | | ns |
| W4 | $t_{DVWH}$ ($t_{DVEH}$) | Data Setup to WE# (CE#) Going High | | 4 | 50 | | 60 | | ns |
| W5 | $t_{AVWH}$ ($t_{AVEH}$) | Address Setup to WE# (CE#) Going High | | 3 | 50 | | 60 | | ns |
| W6 | $t_{WHEH}$ ($t_{EHWH}$) | CE# (WE#) Hold from WE# (CE#) High | | | 0 | | 0 | | ns |
| W7 | $t_{WHDX}$ ($t_{EHDX}$) | Data Hold from WE# (CE#) High | | 4 | 0 | | 0 | | ns |
| W8 | $t_{WHAX}$ ($t_{EHAX}$) | Address Hold from WE# (CE#) High | | 3 | 0 | | 0 | | ns |
| W9 | $t_{WPH}$ | Write Pulse Width High | $V_{CC}$ = 5V ± 5% | | 10 | | 10 | | ns |
| | | | $V_{CC}$ = 5V ± 10% | | 20 | | 20 | | ns |
| W10 | $t_{PHHWH}$ ($t_{PHHEH}$) | RP# $V_{HH}$ Setup to WE# (CE#) Going High | | 6,8 | 100 | | 100 | | ns |
| W11 | $t_{VPWH}$ ($t_{VPEH}$) | $V_{PP}$ Setup to WE# (CE#) Going High | | 5,8 | 100 | | 100 | | ns |
| W12 | $t_{QVPH}$ | RP# $V_{HH}$ Hold from Valid SRD | | 6,8 | 0 | | 0 | | ns |
| W13 | $t_{QVVL}$ | $V_{PP}$ Hold from Valid SRD | | 5,8 | 0 | | 0 | | ns |
| W14 | $t_{PHBR}$ | Boot Block Lock Delay | | 7,8 | | 100 | | 100 | ns |

**NOTES:**

1. Read timing characteristics during program and erase operations are the same as during read-only operations. Refer to AC characteristics for read operations.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled internally which includes verify operations.
3. Refer to command definition table for valid $A_{IN}$. (Table 7)
4. Refer to command definition table for valid $D_{IN}$. (Table 7)
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, RP# should be held at $V_{HH}$ or WP# should be held at $V_{IH}$ until operation completes successfully.
7. Time $t_{PHBR}$ is required for successful locking of the boot block.
8. Sampled, but not 100% tested.
9. Write pulse width ($t_{WP}$) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
10. Write pulse width high ($t_{WPH}$) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.



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**NOTE:**

A. $V_{CC}$ Power-up and standby.
B. Write Program Setup or Erase Setup Command.
C. Write valid address & data (if program operation) or Erase Confirm (if erase operation) command.
D. Automated program or erase delay.
E. Read Status Register Data.
F. Write Read Array command if write operations are completed.

**Figure 15. AC Waveforms for Write Operations**



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**Table 16. Erase and Program Timings, $V_{CC}$ = 5V ± 10% (Commercial and Extended Temperature)**

| | Temp | Commercial | | | | Extended | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{PP}$ | 5V ± 10% | | 12V ± 5% | | 5V ± 10% | | 12V ± 5% | | |
| Parameter | | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Units |
| Boot/Parameter Block Erase Time | | | 7 | | 7 | | 7 | | 7 | s |
| Main Block Erase Time | | | 14 | | 14 | | 14 | | 14 | s |
| Main Block Write Time (Byte Mode) | | | | | | | | | | s |
| Main Block Write Time (Word Mode) | | | | | | | | | | s |
| Byte Program Time | | | 100 | | 100 | | 100 | | 100 | µs |
| Word Program Time | | | 100 | | 100 | | 100 | | 100 | µs |

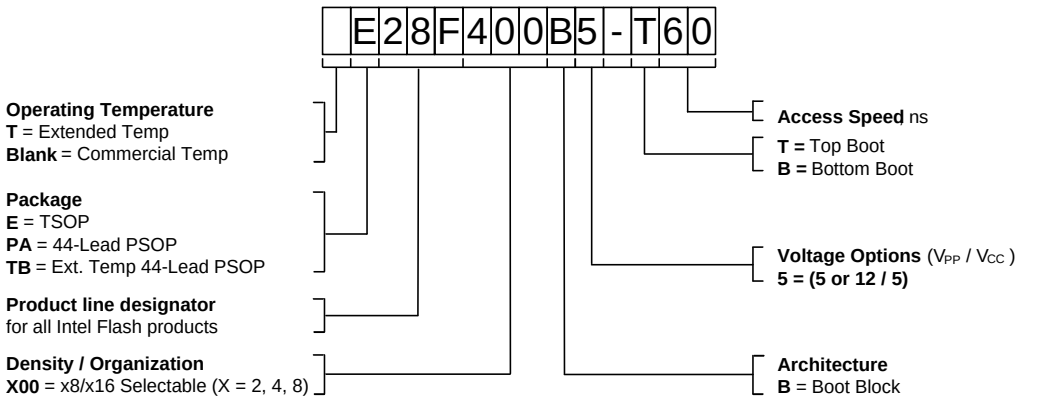
NOTES:

1. All numbers are sampled, not 100% tested.
2. Max erase times are specified under worst case conditions. The max erase times are tested at the same value independent of $V_{CC}$ and $V_{PP}$. See Note 3 for typical conditions.
3. Typical conditions are 25°C with $V_{CC}$ and $V_{PP}$ at the center of the specified voltage range. Production programming using $V_{CC}$ = 5.0V, $V_{PP}$ = 12.0V typically results in a 60% reduction in programming time.
4. Contact your Intel representative for information regarding maximum byte/word write specifications.
5. Max program times are guaranteed for the two parameter blocks and 96-KB main block only.



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# APPENDIX A
# ORDERING INFORMATION




**VALID COMBINATIONS**

| | | 44-Lead PSOP | 48-Lead TSOP |
|---|---|---|---|
| **Commercial** | **2M** | PA28F200B5T60 | E28F200B5T60 |
| | | PA28F200B5B60 | E28F200B5B60 |
| | | PA28F200B5T80 | E28F200B5T80 |
| | | PA28F200B5B80 | E28F200B5B80 |
| | **4M** | PA28F400B5T60 | E28F400B5T60 |
| | | PA28F400B5B60 | E28F400B5B60 |
| | | PA28F400B5T80 | E28F400B5T80 |
| | | PA28F400B5B80 | E28F400B5B80 |
| | **8M** | PA28F800B5T70 | E28F800B5T70 |
| | | PA28F800B5B70 | E28F800B5B70 |
| | | PA28F800B5T90 | E28F800B5T90 |
| | | PA28F800B5B90 | E28F800B5B90 |
| **Extended** | **2M** | TB28F200B5T80 | TE28F200B5T80 |
| | | TB28F200B5B80 | TE28F200B5B80 |
| | **4M** | TB28F400B5T80 | TE28F400B5T80 |
| | | TB28F400B5B80 | TE28F400B5B80 |
| | **8M** | TB28F800B5T90 | TE28F800B5T90 |
| | | TB28F800B5B90 | TE28F800B5B90 |

**PRODUCT PREVIEW**



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# APPENDIX B
# WRITE STATE MACHINE: CURRENT-NEXT STATE CHART

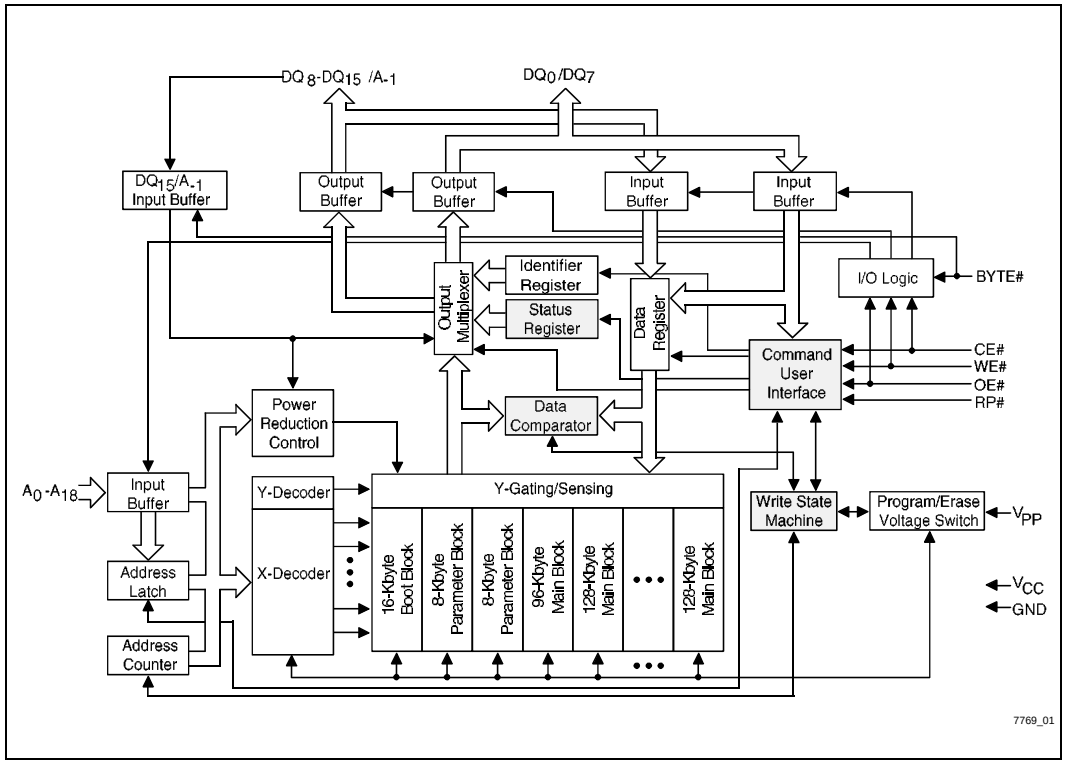
**Write State Machine Current/Next States**

| Current State | SR.7 | Data When Read | Command Input (and Next State) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Read Array (FFH) | Program Setup (10/40H) | Erase Setup (20H) | Erase Confirm (D0H) | Erase Susp. (B0H) | Erase Resume (D0H) | Read Status (70H) | Clear Status (50H) | Read ID (90H) |
| Read Array | "1" | Array | Read Array | Program Setup | Erase Setup | Read Array | | | Read Status | Read Array | Read ID |
| Program Setup | "1" | Status | Program (Command Input = Data to be programmed) | | | | | | | | |
| Program: Not Complete | "0" | Status | Program | | | | | | | | |
| Program: Complete | "1" | Status | Read Array | Program Setup | Erase Setup | Read Array | | | Read Status | Read Array | Read ID |
| Erase Setup | "1" | Status | Erase Command Error | | | Erase | Erase Cmd. Error | Erase | Erase Command Error | | |
| Erase Cmd. Error | "1" | Status | Read Array | Program Setup | Erase Setup | Read Array | | | Read Status | Read Array | Read ID |
| Erase: Not Complete | "0" | Status | Erase | | | | Erase Susp. to Status | Erase | | | |
| Erase: Complete | "1" | Status | Read Array | Program Setup | Erase Setup | Read Array | | | Read Status | Read Array | Read ID |
| Erase Suspend to Status | "1" | Status | Erase Susp. to Array | Res'd. | Erase Susp. to Array | Erase | Erase Susp. to Array | Erase | Erase Susp. to Status | Erase Susp. to Array | Res'd. |
| Erase Suspend to Array | "1" | Array | Erase Susp. to Array | Res'd. | Erase Susp. to Array | Erase | Erase Susp. to Array | Erase | Erase Susp. to Status | Erase Susp. to Array | Res'd. |
| Read Status | "1" | Status | Read Array | Program Setup | Erase Setup | Read Array | | | Read Status | Read Array | Read ID |
| Read Identifier | "1" | ID | Read Array | Program Setup | Erase Setup | Read Array | | | Read Status | Read Array | Read ID |



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# APPENDIX C
# PRODUCT BLOCK DIAGRAM






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# APPENDIX D
# ADDITIONAL INFORMATION

| Order Number | Document |
|---|---|
| 292194 | *AB-65 Migrating SmartVoltage Boot Block Flash Designs to Smart 5 Flash* |
| 292154 | *AB-60 SmartVoltage Boot Block Flash Memory Family Overview* |
| 290531 | *2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet* |
| 290530 | *4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet* |
| 290539 | *8-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet* |
| 290448 | *28F002/200BX-T/B 2-Mbit Boot Block Flash Memory Datasheet* |
| 290449 | *28F002/200BL-T/B 2-Mbit Low Power Boot Block Flash Memory Datasheet* |
| 290450 | *28F002/400BL-T/B 4-Mbit Low Power Boot Block Flash Memory Datasheet* |
| 290451 | *28F002/400BX-T/B 4-Mbit Boot Block Flash Memory Datasheet* |



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