FEATURES

- Integrated 6.8V/0.8A Buck Regulator provides bias to Control and Driver IC(s)
- Adjustable switching frequency from 250 KHz up to 1.5MHz per phase based on the synchronization SCLK input
- Sink and source tracking capability
- Margining via SVID for both rails
- Pre-bias compatible
- Soft Stop capability
- 0.5% overall system set point accuracy
- Voltage Mode Modulation for excellent transient performance
- Single NTC thermistor for current reporting, OC Threshold, and Load Line thermal compensation
- Complete protection including over-current, over-voltage, over-temperature, open remote sense and open control loop
- Thermally enhanced 48L 7mm x 7mm MLPQ package
- RoHS compliant

DESCRIPTION

The IR3531 control IC provides all the necessary control, communication and protection to support compact dual output power solutions up to 210W. The IR3531 can be combined with either discrete IR3535 driver ICs and Direct Fets™ or our IR35XX family of footprint compatible and scalable PowIRstages™ which integrate the MOSFETs and driver into the same package.

The IR3531 provides overall system control and current sharing while the Driver IC or power stages senses per-phase current locally and communicates it to the Control IC. The IR3531 has tri-state PWM outputs to allow diode emulation during light load events.

The IR3531 provides a high performance transient solution through classic voltage mode control and our non-linear transient solutions, Turbo™ and Body Braking™. Turbo™ automatically turns on all phases to minimize load turn-on transients while Body Braking™ automatically turns off the low-side MOSFET to help dissipate stored inductor energy at load turn-off.

BASIC APPLICATION CIRCUIT

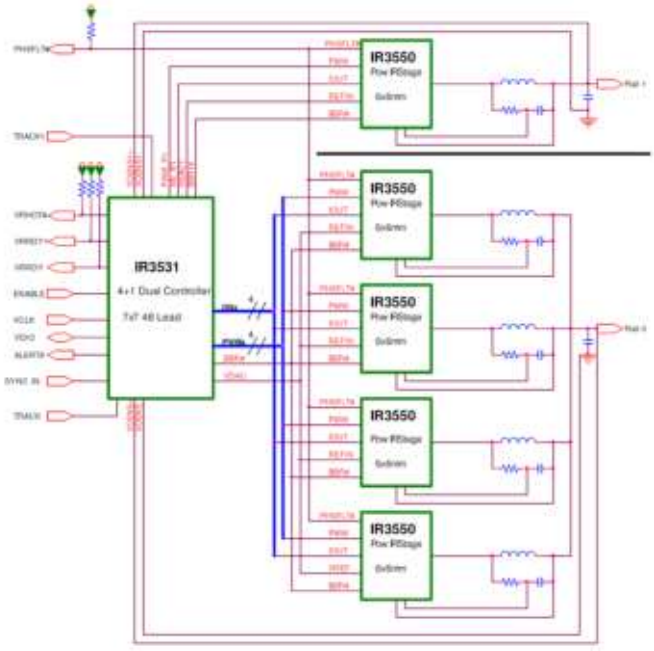

Figure 1: IR3531 Basic Application Circuit, showing a 4+1 Configuration

PIN DIAGRAM

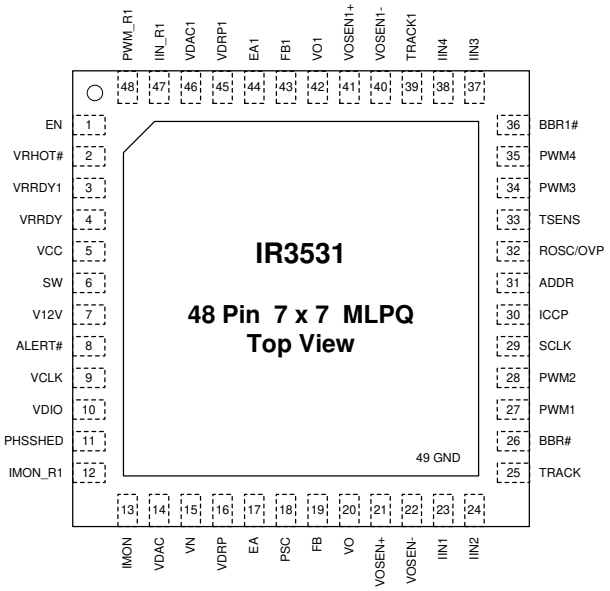

Figure 2: IR3531 Package Top View

ORDERING INFORMATION

IR3531 — M □□□□□

PBF – Lead Free

TR – Tape and Reel

Package	Tape & Reel Qty	Part Number
48 Lead MLPQ (7x7 mm body)	100	**IR3531-MPBF**
48 Lead MLPQ (7x7 mm body)	3000	**IR3531-MTRPBF**[1]

Note [1]**:** Samples only.

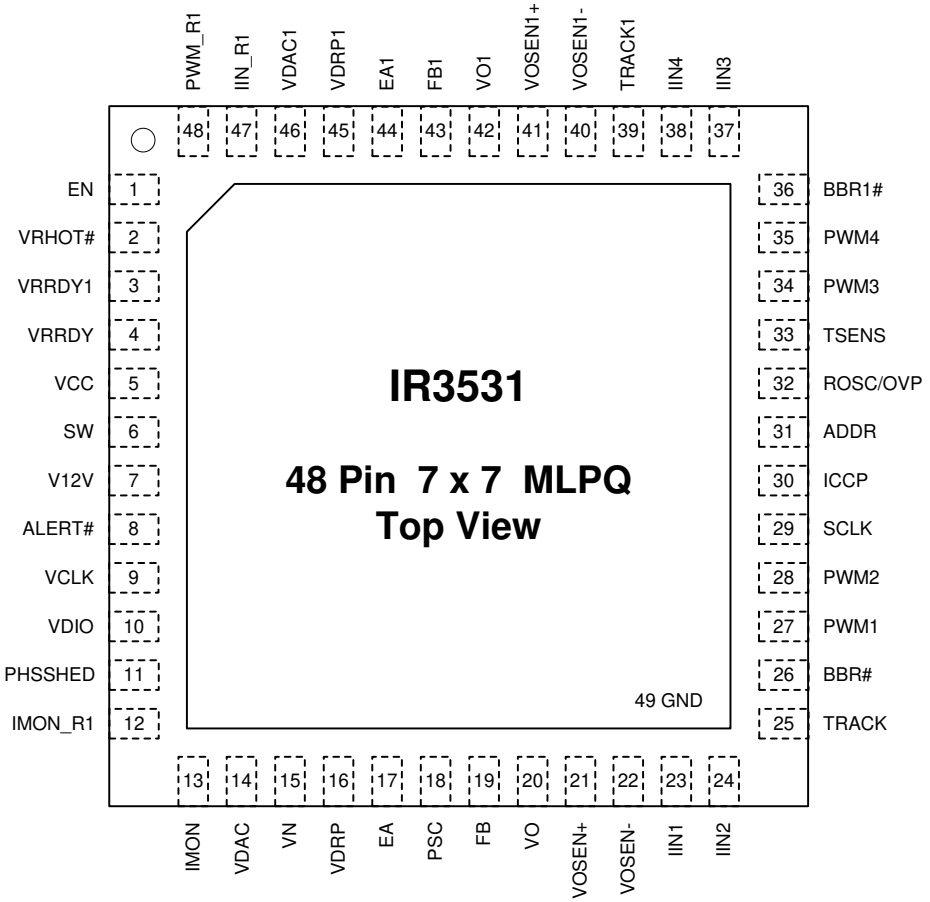

Figure 3: Package Top View, Enlarged

FUNCTIONAL BLOCK DIAGRAM

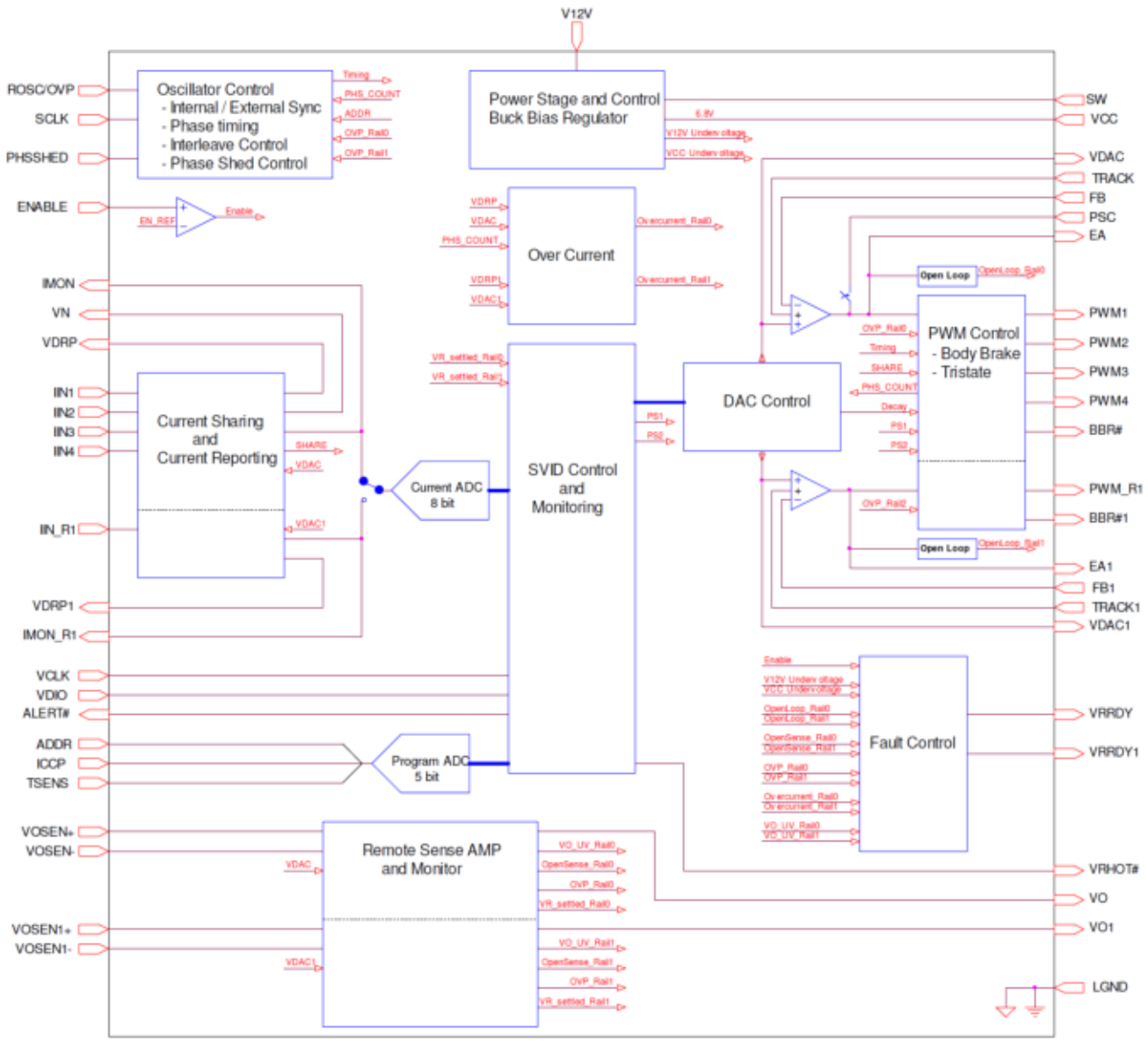

Figure 4: IR3531 Block Diagram

TYPICAL APPLICATION DIAGRAM

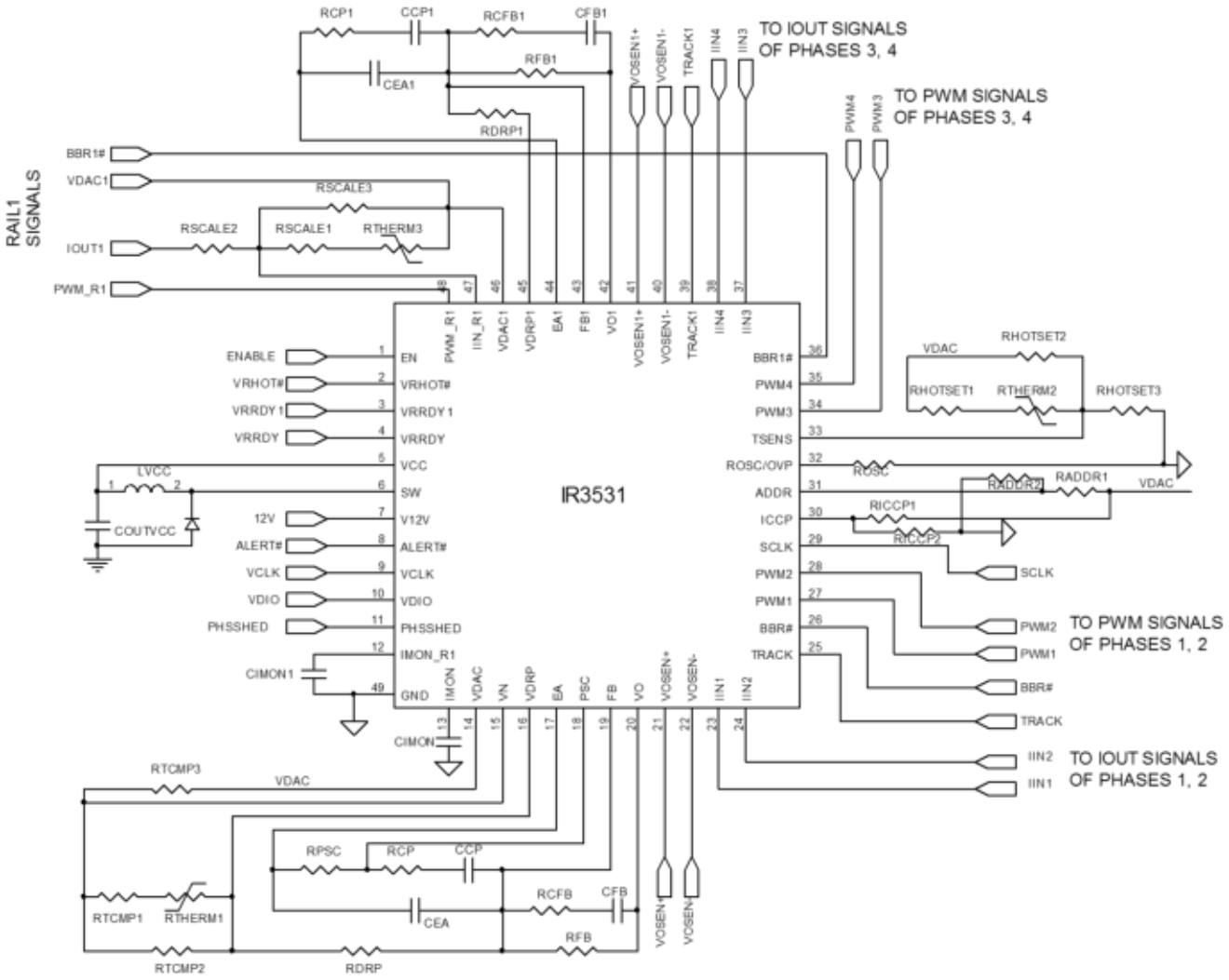

Figure 5: IR3531 Typical Application Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	EN	Enable input. Grounding this pin shuts down the voltage regulators. Do not float this pin as the logic state will be undefined.
2	VRHOT#	Open collector output of the VRHOT# comparator which drives low if Rail0 temperature exceeds the programmed threshold. Connect external pull-up to bias.
3	VDRRY1	Open collector output that drives low during startup and under any external fault condition for Rail1 regulator. Connect external pull-up to bias.
4	VDRRY	Open collector output that drives low during startup and under any external fault condition for Rail0 regulator. Connect external pull-up to bias.
5	VCC	Bias buck regulator output, feedback pin, and bias input for internal circuitry.
6	SW	Switching node for bias buck regulator.
7	V12V	Power Supply input supply rail.
8	ALERT#	Output pin for SVID Alert# interrupt. Open collector output that drives low to notify the master.
9	VCLK	SVID Clock Input. Clock is a high impedance input pin. It is driven by the open collector output of a microprocessor and requires a pull-up resistor.
10	VDIO	SVID Data Input/Output. High impedance input when address, command or data bits are shifted in, open drain output when acknowledging or sending data back to the microprocessor. Pin requires a pull up resistor.
11	PHSSHED	Analog signal that represents the number of phases to be disabled. 0% to 25% VCC, no phases disabled. 25% to 50% VCC, disable 1 phase. 50% to 75% VCC, disable 2 phases. 75% to 100% VCC, disable 3 phases (if available).
12	IMON_R1	Voltage at this pin is proportional to Rail1 load current. It is also the input to the ADC for output current register.
13	IMON	Voltage at this pin is proportional to Rail0 load current. It is also the input to the ADC for output current register.
14	VDAC	Voltage Regulator Rail 0 reference voltage programmed by SVID. VDAC is also used as the A/D reference during power up for pins ADDR/PSN, TSENS and ICCP.
15	VN	Node for DCR thermal compensation network.
16	VDRP	Buffered, scaled and thermally compensated current signal for Rail0. Connect an external resistor to FB to program converter output impedance.
17	EA	Output of the error amplifier for Rail0.
18	PSC	Node for Power Savings mode compensation input.
19	FB	Inverting input to the Error Amplifier for Rail0.
20	VO	Remote sense amplifier output for Rail0.
21	VOSEN+	Rail0 remote sense amplifier input. Connect to output at the load.
22	VOSEN-	Rail0 remote sense amplifier input. Connect to ground at the load.
23, 24, 37, 38	IIN1-4	Current signals from the driver IC-s of Rail0.
25	TRACK	External tracking reference for Rail0.
26	BBR#	Body-braking™ bus for Rail0 driver ICs to disable synchronous switches.
27, 28, 34, 35	PWM1-4	PWM outputs for Rail0. Each output is connected to the input of the driver IC. Connecting the PWMx output to LGND disables the phase, allowing the IR3531 to operate as a 1, 2, 3, or 4 phase controller.
29	SCLK	Synchronization clock input. Program ROSC using ROSC vs. Frequency to match the SCLK frequency.

PIN #	PIN NAME	PIN DESCRIPTION
30	ICCP	Program maximum load current for both Rail0 and Rail1.
31	ADDR	Programs SVID address for Rail0 and Rail1, discrete or coupled inductor operation for Rail0, enable/disable turbo function for Rail0.
32	ROSC/OVP	Connect a resistor to LGND to program oscillator frequency. Oscillator frequency equals switching frequency per phase. ROSC/OVP pin is pulled up to VCC when an over voltage event occurs.
33	TSENS	Pin for thermal network that senses the temperature of Rail0 and Rail1.
36	BBR1#	Body-braking™ bus for Rail1 driver ICs to disable synchronous switches.
39	TRACK1	External tracking reference for Rail1.
40	VOSEN1-	Rail1 remote sense amplifier input. Connect to ground at the load.
41	VOSEN1+	Rail1 remote sense amplifier input. Connect to output at the load.
42	VO1	Remote sense amplifier output for Rail1.
43	FB1	Inverting input to the Error Amplifier for Rail1.
44	EA1	Output of the error amplifier for Rail1.
45	VDRP1	Buffered, scaled and thermally compensated current signal for Rail1. Connect an external resistor to FB1 to program converter output impedance.
46	VDAC1	Buffered Rail1 reference voltage. Voltage can be margined via SVID.
47	IIN_R1	Current signal from Rail1 driver IC.
48	PWM_R1	PWM output for Rail1.
49	GND	Local Ground for internal circuitry and IC substrate connection.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	-65°C To 150°C
Operating Junction Temperature	0°C To 150°C
ESD Rating	HBM Class 1C JEDEC Standard
MSL Rating	2
Reflow Temperature	260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	EN	3.5V	-0.3V	25mA	1mA
2	VRHOT#	VCC	-0.3V	1mA	50mA
3	VDRRY1	VCC	-0.3V	1mA	20mA
4	VDRRY	VCC	-0.3V	1mA	20mA
5	VCC	8V	-0.3V	1mA	20mA
6	SW	16V	-1.0V	3A	1mA
7	V12V	16V	-0.5V	1mA	1.5A
8	ALERT#	3.5V	-0.3V	1mA	50mA
9	VCLK	3.5V	-0.3V	1mA	1mA
10	VDIO	3.5V	-0.3V	1mA	50mA
11	PHSSHED	VCC	-0.3V	1mA	1mA
12	IMON_R1	3.5V	-0.3V	25mA	1mA
13	IMON	3.5V	-0.3V	25mA	1mA
14	VDAC	3.5V	-0.3V	5mA	35mA
15	VN	VCC	-0.3V	1mA	1mA
16	VDRP	VCC	-0.3V	35mA	1mA
17	EA	VCC	-0.3V	35mA	5mA
18	PSC	VCC	-0.3V	1mA	1mA
19	FB	VCC	-0.3V	1mA	1mA
20	VO	VCC	-0.3V	35mA	5mA
21	VOSEN+	VCC	-0.5V	5mA	1mA
22	VOSEN-	1.0V	-0.5V	5mA	1mA
23	IIN1	VCC	-0.3V	1mA	1mA
24	IIN2	VCC	-0.3V	1mA	1mA
25	TRACK	VCC	-0.3V	1mA	1mA
26	BBR#	VCC	-0.3V	1mA	5mA
27	PWM1	VCC	-0.3V	1mA	5mA

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
28	PWM2	VCC	-0.3V	1mA	5mA
29	SCLK	3.5V	-0.3V	1mA	5mA
30	ICCP	3.5V	-0.3V	1mA	1mA
31	ADDR	3.5V	-0.3V	1mA	1mA
32	ROSC	VCC	-0.3V	1mA	1mA
33	TSEN	3.5V	-0.3V	1mA	1mA
34	PWM3	VCC	-0.3V	1mA	5mA
35	PWM4	VCC	-0.3V	1mA	5mA
36	BBR1#	VCC	-0.3V	1mA	5mA
37	IIN3	VCC	-0.3V	1mA	1mA
38	IIN4	VCC	-0.3V	1mA	1mA
39	TRACK1	VCC	-0.3V	1mA	1mA
40	VOSEN1-	1.0V	-0.5V	5mA	1mA
41	VOSEN1+	VCC	-0.5V	5mA	1mA
42	VO1	VCC	-0.5V	35mA	5mA
43	FB1	VCC	-0.3V	1mA	1mA
44	EA1	VCC	-0.3V	35mA	5mA
45	VDRP1	VCC	-0.3V	35mA	1mA
46	VDAC1	3.5V	-0.3V	1mA	35mA
47	IIN_R1	VCC	-0.3V	1mA	1mA
48	PWM_R1	VCC	-0.3V	1mA	1mA
49	GND	N/A	N/A	20mA	1mA

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

The electrical characteristics table lists the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C. Unless otherwise specified, these specifications apply over: -0.3V ≤ VOSEN- ≤ 0.3V, 7.75KΩ ≤ ROSC ≤ 50.0 KΩ

Recommended V12V Range	10.8V	12	13.2V	V
Recommended VCC Range	6.6	6.8	7.0	V
VOSEN- and VOSEN1- to LGND offset	-0.3	0	0.3	V
ROSC Resistor Programming Range	7.75		50	KΩ
Recommended Operating Junction Temperature	0	T_J	100	ºC

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VDAC Reference						
System Set-Point Accuracy	SETACC	VID ≥ 1V	-0.5	-	0.5	%
		0.8 ≤ VID < 1V	-5	-	+5	mV
		0.25V ≤ VID < 0.8V	-8	-	+8	mV
Slew Rate – Fast Mode	VIDFAST		15	20	25	mV/µs
Slew Rate – Slow Mode	VIDSLOW		3.75	5	6.25	mV/µs
Default VBOOT Rail 0	VBOOT0	Note 3	-	1.5	-	V
Default VBOOT Rail 1	VBOOT1	Note 3	-	1.5	-	V
Oscillator (Note 4)						
ROSC Voltage	VROSC	ROSC = 24.5 KΩ	0.570	0.595	0.620	V
VDAC Buffer Amplifier						
Input Outset Voltage	DACOFF	V(VDAC, VDAC1) — VID code + VID offset, 0.25V ≤ V(VDAC, VDAC1) ≤ 1.52V, < 1mA load	-15	0	15	mV
Source Current	DACSRC	0.25V ≤ V(VDAC1) ≤ 1.52V	0.3	0.44	0.6	mA
		0.25V ≤ V(VDAC) ≤ 1.52V	0.9	1.65	2.4	
Sink Current	DACSNK	0.5V ≤ V(VDAC1) ≤ 1.52V	2	13	20	mA
		V(VDAC1) = 0.25V	0.5	1.5	2	
		0.5V ≤ V(VDAC) ≤ 1.52V	3	15	30	
		V(VDAC) = 0.25V	0.5	1.5	3	
Unity Gain Bandwidth			-	3.5	-	MHz
Slew Rate			-	1.5	-	V/µs
Thermal Compensation Amplifier (VDRP)						
Output Offset Voltage	VDRPOUTOFF	0V ≤ V(IIN) – V(VDAC) ≤ 1.52V, 0.25V ≤ V(VDAC) ≤ 1.52V,	-14	0	14	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		Req/R2 = 2				
Source Current	VDRPSRC	0.25V ≤ V(VDAC) ≤ 1.52V	3	8	15	mA
Sink Current	VDRPSNK	0.5V ≤ V(VDRP) ≤ 1.52V	0.2	0.4	0.7	mA
		V(VDRP) = 0.25V	0.175	0.25	0.4	
Unity Gain Bandwidth		Req/R2 = 2, Note 1	2	4.5	7	MHz
Slew Rate			-	5.5	-	V/µs
VN Bias Current		V(VN) = 2 V	-2	0	2	µA
Power Savings Mode Operation						
PS2/PS3 Turn-on Threshold	PS2THRSH	VID = 250 mV	250	350	385	mV
		VID = 1.52 V	2	2.15	2.26	V
PS2/PS3 Pulse Width Rail0	PS2COT0	VID = 250 mV, SF = 500 kHz	60	151	200	ns
		VID = 1.52 V, SF = 500 kHz	220	409	480	
PS2/PS3 Pulse Width Rail1	PS2COTMIN1	VID = 250 mV, SF = 500 kHz	50	100	200	ns
	PS2COTMAX1	VID = 1.52 V, SF = 500 kHz	220	358	480	
PS Mode Enter Delay	PS1DELAY	PS0 to PS1 only	-	8	-	PWM Cycle
Enable Input						
Rising Threshold	ENRISE		625	650	675	mV
Falling Threshold	ENFALL		575	600	625	mV
Hysteresis	ENHYST		25	50	75	mV
Bias Current	ENBIAS	0V ≤ V(ENABLE) ≤ 3.3V	-5	0	5	µA
Blanking Time		Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
IMONx Current Report Amplifier						
Output Offset Voltage	IMONOFF	VDRP–VDAC = 0, 225, 450, 900mV	15	50	90	mV
Unity Gain Bandwidth		Note 1	-	1	-	MHz
Input Filter Time Constant			-	1	-	**µs**
Max Output Voltage	IMONMAX		1.00	1.09	1.145	V
Current Report A/D Accuracy	IMONACC	VDRP–VDAC = 900mV	-2	0	2	%
Rail1 VDRP Amplifier						
Output Outset Voltage	VDRP1OFF	0V≤ V(IIN_R1) - V(VDAC1) ≤ 0.2V 0.25V ≤ V(IIN_R1) - V(VDAC1) ≤ 1.52V	-75	0	75	mV
Source Current	VDRP1SRC	0.25V ≤ V(VDAC1) ≤ 1.52V	3	8	15	mA
Sink Current	VDRP1SNK	0.5V≤ V(VDRP1) ≤ 1.52V	0.2	0.4	0.6	mA
		V(VDRP1) = 0.25V	0.175	0.25	0.375	
Closed Loop Gain		Note 1	-	9	-	V/V
Unity Gain Bandwidth		Note 1	0.8	1.5	3	MHz
Slew Rate		Note 1	-	5.5	-	V/µs
Error Amplifier						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage		Note 2 (test mode only)	-	0	-	mV
FB Bias Current			-1	0	1	µA
DC Gain		Note 1	100	110	120	dB
Unity Gain Bandwidth		Note 1	20	30	40	MHz
Slew Rate		Note 1	7	12	20	V/µs
Sink Current	EASRC		0.40	0.85	1.35	mA
Source Current	EASNK		5	8	12	mA
Maximum Voltage	EAMAX	Measure V(VCC) – V(EA), V(EA1)	500	925	1100	mV
Minimum Voltage	EAMIN		-	120	250	mV
Open Voltage Loop Detection Threshold	EAOPENTHR	Measure V(VCCx) - V(EA), V(EA1), Relative to Error Amplifier maximum voltage	100	300	1100	mV
Open Loop Detection Delay	EAOPENDEL	V(EA), V(EA1) = V(VCC) to VRRDY = low	-	8	-	PWM
PS2 Clamp Voltage	EAPS2CLMP	With respect to VDAC	-240	-70	-10	mV
Phase Firing Comparators						
Input Offset	KEEPOFF		-30	0	30	mV
Propagation Delay	KEEPDEL		-	-	320	ns
Phase Shedding Comparators						
Bias Current	PHSDBIAS		-2	0	2	µA
Threshold	PHSDTHRS	Comparator 1	1.3	1.7	2.0	V
		Comparator 2	3.0	3.4	3.85	
		Comparator 3	4.8	5.1	5.55	
PWM Comparator						
PWM Ramp Slope	PWMSLP	V12V= 12V	42	52.5	57	mV/ %DC
Minimum Pulse Width	PWMMIN	Note 1		55	70	ns
Input Offset Voltage	PWMOFF	Note 1	-5	0	5	mV
Share Adjust Amplifier						
Input Offset Voltage	SAAOFF	Note 1	-3	0	3	mV
Gain	SAAGAIN	CSIN+ = CSIN- = DACIN, Note 1	4	5.0	6	V/V
Unity Gain Bandwidth		Note 1	4	8.5	17	kHz
Maximum PWM Ramp Floor Voltage	MINFLOOR	IOUT = DACIN – 200mV Measure relative to floor voltage	100	180	22 0	mV
Minimum PWM Ramp Floor Voltage	MAXFLOOR	IOUT = DACIN + 200mV Measure relative to floor voltage	-220	-160	-100	mV
Over Voltage Protection (OVP) Comparators						
Threshold at Power-up	OVPPUP		1.615	1.65	1.67	V
Threshold during Normal Operation	OVPTHR	Compare to VID Voltage + VID offset	100	130	150	mV
Propagation Delay to OVP	OVPPROP	Measure time from V(FB), V(FB1) > VID voltage + VID offset (250mV overdrive) to V(PWM) transition to > 0.5 * V(VCC)	-	90	180	ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Turbo Circuit						
Activation Threshold Voltage	TURBACT Note 1	Compare to EA, Note 1	-	390	-	mV
Turbo Comparator Hysteresis	TURBHYST Note 1	Note 1	-	90	-	mV
Filter Time Constant	TURBTIME Note 1	Note 1	-	8	-	µs
Turbo Pulse Width	TURBPW	500kHz 600mV Peak sine wave on EAIN, measure GATEH pulse width	115	230	280	ns
Peak Detect Reset Time Constant	TURBRESET		-	400	-	ns
Over-Current Comparator						
Input Filter Time Constant			-	2	-	µs
Over-Current Threshold	OCTHRSH	VDRP-VDAC, VDRP1-VDAC1	0.94	1.08	1.18	V
OC Threshold PSI Reduction Factor	OCPSI	PSI mode, 4ph to 2ph, 2ph to 1ph	450	540	610	mV
		PSI mode, 3ph to 1ph	310	360	410	
		3ph to 2ph	640	720	800	
		PSI mode, 4ph to 1ph	220	270	310	
		4ph to 3ph	690	800	900	
OC Delay Time	OCDELAY	Delay to OC shutdown	225	256	285	µs
OC Hiccup Time		Relaxation Delay	-	4096	-	µs
VCC Undervoltage						
VCC UVL Start	VCCSTART		5.5	5.85	6.4	V
VCC UVL Stop	VCCSTOP		4.85	5.2	5.65	V
VCC UVL Hysteresis	VCCHYST		515	650	830	mV
VRRDY Output						
Output Voltage	VRRDYLO	I(VRRDY, VDRRY1) = 4mA	-	150	300	mV
Leakage Current	VRRDYLEAK	V(VRRDY, VDRRY1) = 5.5V	-	0	10	µA
VCC Activation Voltage	VRRDYVCC	I(VDRRY, VDRRY1) = 4mA, <300mV	1	2	3.6	V
VO-VDAC Undervoltage Threshold	VOUVRISE	Reference to VDAC	-340	-290	-230	mV
Open Sense Line Detection						
Sense Line Detection Active Comparator Threshold Voltage	OPENACT		100	150	200	mV
Sense Line Detection Active Comparator Offset Voltage	OPENOFF	V(VO) < [V(VOSEN+) – V(LGND)] / 2	25	60	80	mV
VOSEN+ Open Sense Line Comparator Threshold	OPENCOMP+	Compare to V(VCC)	82	90	92	%
VOSEN- Open Sense Line Comparator Threshold	OPENCOMP-		0.36	0.40	0.44	V
Sense Line Detection Source Currents	OPENSRC	V(VO) = 100mV	200	500	700	µA
VCC Buck Regulator						
VCC Output Voltage	VCC100	100–400 mA load current	6.5	6.8	7.1	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Switch Node Rise Time	SWRISE	Note 1	-	5	-	ns
Switch Node Fall Time	SWFALL	Note 1	-	15	-	ns
A/D Program Inputs						
ADDR Pin Bias Current	ADDRBIAS		-2	0	2	µA
ICCP Pin Bias Current	ICCPBIAS		-2	0	2	µA
TSENS Pin Bias Current	TSENBIAS		-2	0	2	µA
A/D Comparator Offset	ADOFFSET		-5	0	5	mV
V12V Undervoltage						
VCC V12V Start	VCCSTART		8.8	9.6	10.2	V
VCC V12V Stop	VCCSTOP		7.8	8.6	9.2	V
VCC V12V Hysteresis	VCCHYST		0.8	1	1.3	V
SerialVID						
ALERT#, VDIO Buffer On Resistance	ALERTRES		-	-	14.3	Ω
ALERT#, VDIO Leakage Current	ALERTLEAK		-10	0	10	µA
VCLK Bias Current	VCLKBIAS		-1	0	1	µA
VDIO Bias Current	VDIOBIAS		-1	0	1	µA
Transmit Data Prop Delay	XMITDELAY	VCLK rising to VDIO change	4	6	12	ns
Comparator Threshold	SVIDTHRSH	VCLK, VDIO rising	500	590	650	mV
		VCLK, VDIO falling	450	515	650	
Comparator Hysteresis	SVIDHYST		50	75	-	mV
Link States Reset Timer	SVIDTIME		200	-	600	ns
PWMx Outputs						
Source Resistance	PWMSRCR		50	144	500	Ω
Sink Resistance	PWMSNKR		75	117	290	Ω
Tri-state Source Impedance	PWMTRIZ		2.0	5.4	7.5	KΩ
Tri-state Bias Current	PWMTRIBIAS	V(PWMx) = 1.65V	-5	0	5	µA
Tri-state Active Pull-up	PWMTRIPUP	V(PWMx) while sourcing 100 µA to GND	0.5	1	1.2	V
Disable Comparator Threshold	PWMDISTHR		0.4	0.6	0.9	V
PWM High Voltage	PWMHIGH	I(PWM) = -1mA, measure VCC-PWM	-	-	1	V
PWM Low Voltage	PWMLOW	I(PWM) = -1mA	-	-	1	V
Body Braking Comparator						
Threshold Voltage with EAIN Decreasing	BBRTHRFALL	Measure relative to floor voltage	-300	-200	-110	mV
Threshold Voltage with EAIN Increasing	BBRTHRRISE	Measure relative to floor voltage	-200	-100	-10	mV
Hysteresis	BBRTHRHYS		70	105	130	mV
Propagation Delay	BBRDELAY	VCC = 5V Measure time from EAIN < V(DACIN) (200mV overdrive) to GATEL transition to < 4V.	30	65	90	ns
BBR1# Source Resistance	BBRSRCRES		20	40	75	Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
BBR1# Sink Resistance	BBRSNKRES		10	35	60	Ω
BBR1# High Voltage	BBRHIGH	I(BBR1#) = -1mA, measure V(VCC) – V(BBR1#)	0	0.4	0.8	V
BBR1# Low Voltage	BBRLOW	I(BBR1#) = 1mA	0	0.35	0.8	V
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	RSABW	Note 1	1.5	3.2	4.5	mV
Input Outset Voltage	RSAOFF	0.25V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.52V, 0.25V≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.52V	-5	0	5	mV
Sink Current	RSASINK	0.5V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.52V, 0.5V≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.52V	0.4	1	2	mA
		V(VOSEN+) - V(VOSEN-) = 0.25V, V(VOSEN1+) - V(VOSEN1-) = 0.25V	0.225	0.5	0.8	
Source Current	RSASRC	0.25V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.52V, 0.25V≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.52V	3	9	20	mA
Slew Rate	RSASLEW	0.25V≤ V(VOSEN+) - V(VOSEN-) ≤ 1.52V, 0.25V≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.52V	2	4	8	V/µs
VOSEN+ Bias Current	VOSNS-BIAS	0.25 V < V(VOSEN+) < 1.52V, 0.25 V < V(VOSEN1+) < 1.52V	-	27	50	µA
VOSEN- Bias Current	VOSNS+BIAS	-0.3V ≤ VOSEN- ≤ 0.3V, All VID Codes, -0.3V ≤ VOSEN1- ≤ 0.3V, All VID Codes	-	27	70	µA
High Voltage	VOHIGH	V(VCC) – V(VO), V(VCC) – V(VO1)	1.5	2	2.5	V
Low Voltage	VOLOW	V(VCC) = 7V	-	60	100	mV
VRHOT# Comparator						
Output Voltage	VRHTOUT	I(VRHOT#) = 30mA	-	150	400	mV
VRHOT# Leakage Current	VRHTLEAK	V(VRHOT#) = 5.5V	-	0	10	µA
Platform Test Mode						
Comparator Threshold	PTMTHR	Raise ADDR voltage after VIN power-up	2.2	2.6	3.1	V
Link States Reset Timer	PTMTIME		20	-	24	µs
VR Settled						
Comparator Offset	VRSTLOFF	Compare FB to VDAC reference	-	20	-	mV
Delay to ALERT#	VRSTLDELAY	Delay after DAC settled to within 2 VID steps of final value	-	5	-	µs
Current Inputs						
IINx to IINx Impedance	IINRES		-	3000	-	Ω
IINx to IINx Leakage Current	IINLEAK		-1	0	1	µA
TRACK Inputs						
Input Leakage			-1	0	1	µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
TRACK to FB Offset		Error amp in unity gain	15	36	65	mV
Release Error Voltage		TRACK = VDAC+100mV, VDAC-FB	-1	0	1	mV
VO Discharge Comparators						
Tri-state Enable Threshold		VO when PWM outputs enter tri-state	200	250	300	mV
SCLK Synchronization Input						
Rising Threshold			0.8	1.2	1.3	V
Falling Threshold		Note 1	0.625	0.85	1.025	V
Input Leakage			-5	0	5	µA
Propagation Delay Rising			-	-	60	ns
Input Capacitance		Note 1	-	-	10	pF
General						
VCC Supply Current	VCCBIAS		3	7	12	mA

Notes:

1. Guaranteed by design but not tested in production
2. Error Amplifier input offset is trimmed to within ±1% for optimal system set point accuracy.
3. Final test VBOOT options of 0, 0.9, 1.35 and 1.5V are feasible.
   Contact International Rectifier Enterprise Power Business Unit for details.
4. Use of internal oscillator is not recommended, use SCLK input to set PWM frequency.

THEORY OF OPERATION

SYSTEM DESCRIPTION

The IR3531 Multiphase Buck power system provides voltage regulation solutions for two individual supply outputs. The main output, Rail0, controls up to four phases and produce up to 200A when paired with appropriate power stages. The secondary output, Rail1, is a single phase output capable of up to 50A, again with appropriate power stage. The IR3531 control IC is specialized to allow external clock synchronization and tracking capability for each rail. Features include a serial control and telemetry bus that can control output voltage settings and slew rates while allowing monitoring of the system thermals and load currents. The IR3531 control IC contains all necessary housekeeping, protection and control functions and communicates a three-level PWM signal to each power stage.

FREQUENCY AND PHASE TIMING CONTROL

The IR3531 operates with external frequency synchronization which can be used to control input ripple from multiple paralleled power supply systems. Systems can be forced to operate out of phase thereby reducing instantaneous peak input currents and also controlling system noise signatures. The internal oscillator is used to calibrate the PWM ramp slopes and other functions at power up therefore it is desirable for the externally applied synchronization frequency to be very near the ROSC programmed internal frequency times the number of active phases. Calibration can take up to 1ms. This results in the PWM gain to be near the desired 50mV/% duty cycle. Furthermore, it is desired the SCLK input be stable prior to enabling the IR3531 voltage regulator.

The SCLK input frequency provided needs to equal the desired base switching frequency multiplied by the active number of phases. Phase shedding is available however SCLK needs to be adjusted accordingly to match the number of active phases.

Phase timing and interleave spacing is automatically optimized inside the controller and can accommodate changing phases on the fly (phase shedding). The PHSSHD pin can be used to dynamically drop from 1-3 phases while minimizing output voltage transients. Also, phases can be disabled by grounding the PWM outputs of the IR3531. Notice the driver ICs should be removed since a PWM low signal indicates a 0% duty cycle state which turns on the low-side MOSFETs and can potentially develop large negative inductor currents. The control IC detects which PWM pins are grounded during power up to determine the populated number of phases and automatically optimizes phase timing for minimal system ripple.

TRACK FUNCTIONALITY

Both Rail outputs of the IR3531 can be independently controlled through their respective TRACK inputs. TRACK pins override the internal VDAC reference inputs to the Error Amplifiers allowing users to control power up and power down VR output voltage characteristics. The IR3531 is fully soft-stop and pre-bias compatible. The control loop is full synchronous during soft stop events thereby preventing COUT capacitor discharge-induced inductive kicks. The control system allows non-synchronous buck operation once VO <=250mV — this allows outputs to return to their pre-biased operating points if available.

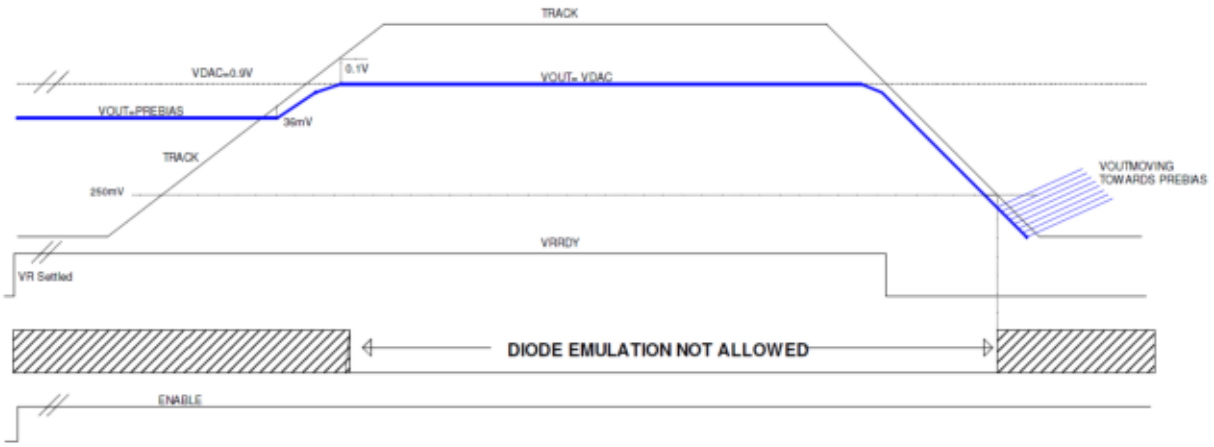

Figure 6: TRACK Operation with Pre-Bias

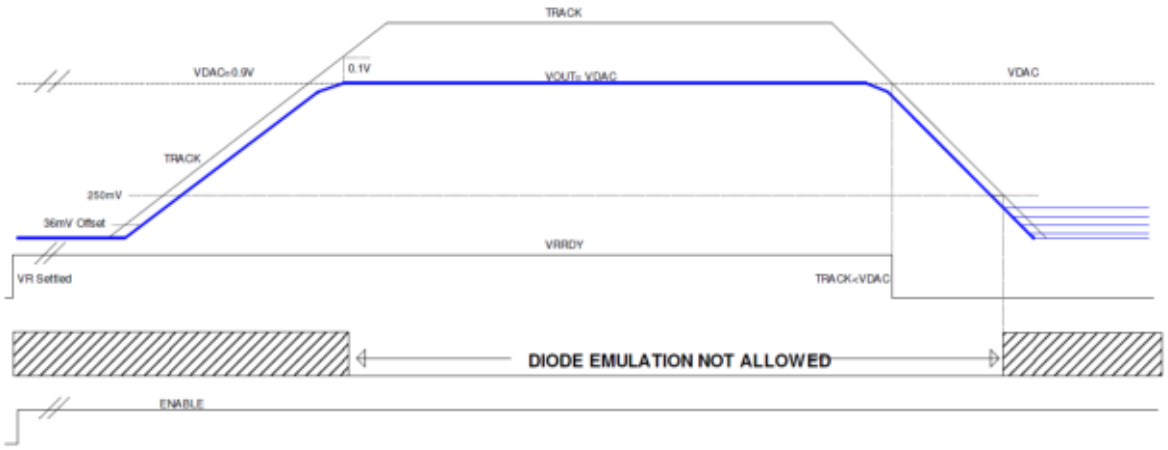

Figure 7: TRACK Operation without Pre-Bias

The TRACK inputs have a typical 36mV offset from the closed loop feedback operating point to ensure the error amplifier is in an off state when TRACK=0V. Furthermore, TRACK must exceed the respective VDAC by at least 100mV to ensure VDAC has complete control of the Error Amplifier as shown in Figures 6 and 7.

As a cautionary note the track input provides direct control of the output PWM duty cycle. The presence of excessive noise or glitches on TRACK when this input is active can cause sudden increases in the PWM duty cycle (up to 100%), potentially causing damage to the power converter.

PWM CONTROL METHOD

The steady state control architecture utilized in the IR3531 is feed-forward voltage mode control with trailing edge modulation. A high-gain wide-bandwidth voltage type error amplifier is used to achieve accurate voltage regulation and ultra-fast transient response. Feed-forward control is established by varying the PWM ramp slope proportionally to the input voltage resulting in the error amplifier operating point being independent of the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current. All PWM ramp slopes are calibrated at initial power-up. The PWM pulse is terminated once the PWM ramp exceeds the Error Amplifier output voltage.

Under dynamic load transitions, the IR3531 utilizes our patented Body Braking™ algorithm allows all low-side MOSFETs to be turned off during a load relaxation event allowing the MOSFET body diodes to conduct and dissipate some of the stored inductor energy and also speed up the inductor current slew rate by introducing a larger voltage across the inductor. Body Braking™ reduces the peak overshoot of the converter.

An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. The resulting PWM control loop is capable of transitioning from 0% duty cycle to 100% duty cycle with overlapping phases within a few tens of nanoseconds in response to a load step decrease. Figure 8 on the next page depicts PWM operating waveforms under various conditions.

BODY BRAKING™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load-step decrease is:

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load-step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now:

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented

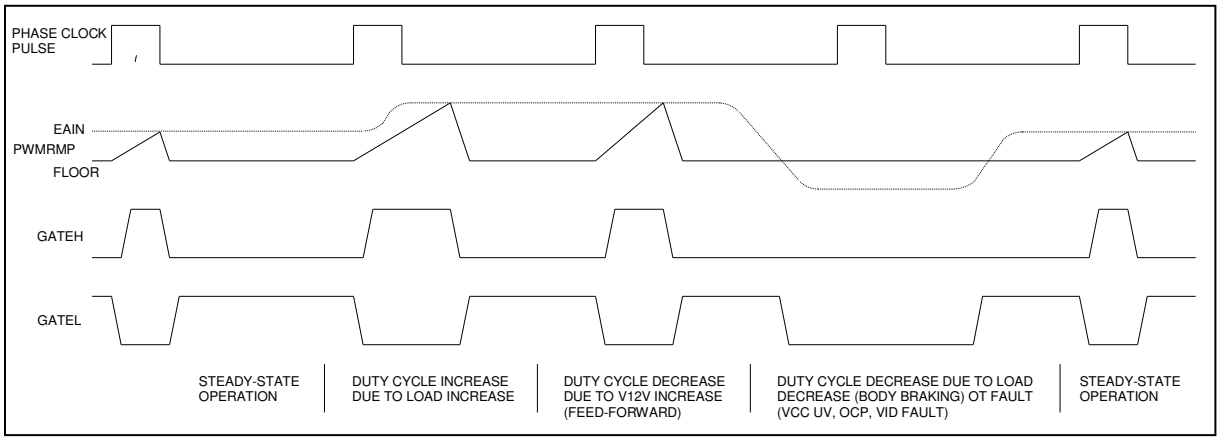

Figure 8: PWM Operating Waveforms

technique is referred to as "body braking" and is accomplished through the "body braking comparator." If the error amplifier's output voltage drops below VDAC, this comparator turns off the low-side gate driver, enabling the bottom FET body diode to take over. There is 100mV upslope and 200mV down slope hysteresis for the body braking comparator.

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Since the voltage drop in the body diode is often comparable to the output voltage, the inductor current slew rate can be increased significantly. This patented technique is referred to as "body braking" and is accomplished through the "body braking comparator." If the error amplifier's output voltage drops below VDAC, this comparator turns off the low-side gate driver, enabling the bottom FET body diode to take over. There is 100mV upslope and 200mV down slope hysteresis for the body braking comparator.

LOSSLESS AVERAGE INDUCTOR CURRENT SENSING

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 8. The equation of the sensing network is:

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen, such that, the time constant of Rcs and Ccs equals the time constant of the inductor, which is the inductance L over the inductor DCR R_L. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

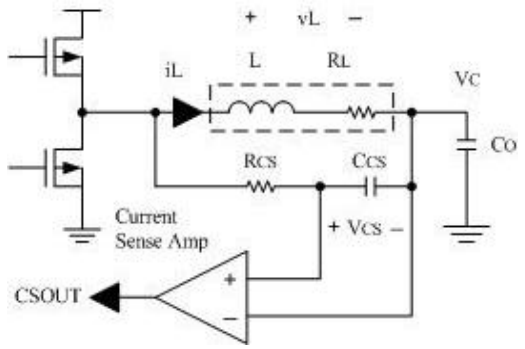

Figure 9: Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high-side or low-side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents.
The output voltage can be positioned to meet a load line based on real-time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response.
Other methods provide no information during either load increase (low-side sensing) or load decrease (high-side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will appear in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak-to-peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

CURRENT SENSE AMPLIFIER

A high speed differential current sense amplifier is located in our driver ICs, as shown in Figure 9. Its gain is nominally 32.5 over the entire temperature operating range therefore the 3850 ppm/ºC inductor DCR temperature coefficient should be compensated in the voltage loop feedback path. This can be accurately compensated by using a linearized Negative TC resistor network where the NTC can be located near the output inductors. The resulting temperature compensated current information is used by the control IC for voltage positioning and current reporting, and over current limit protection.

The input offset of this amplifier is calibrated to within +/- 450µV (6 sigma limits) with a 200uV typical LSB calibration bit. This calibration routine is continuous and occurs at every 56 PWM cycles.

The current sense amplifier can accept positive differential input up to 50mV and negative up to -10mV before clipping. The output of the current sense amplifier is summed with the VDAC voltage and is returned to the control IC through the IIN pin. The IIN pins in the control IC are internally tied together through 3 KOhm resistors to produce a voltage representative of the average phase inductor current.

AVERAGE CURRENT SHARE LOOP

A current sharing loop is also incorporated in the IR3531 to ensure balance between the multiphase buck power stages. Poor current sharing can hamper transient response and degrade overall system efficiency.
The current information of each phase is compared against the average phase current through a Share Adjust Amplifier which then manipulates the respective PWM ramp start voltage to add or subtract PWM output duty cycle. The current share amplifier is internally compensated such that the crossover frequency of the current share loop is much slower than that of the voltage loop and the two loops do not interact.

INSTANTANEOUS CURRENT BALANCE

A form of coarse current sharing is also incorporated into the IR3531 to protect against Synchronized High Load Repetition Rate transients which can saturate inductors and cause OVP conditions. The phase firing order of the multiphase system is continually being re-assessed and adjusted if required on a cycle-by-cycle basis to prevent instantaneous phase currents from deviating from each other. This also improves transient response by ensuring all phase currents track each other within a few switching cycles. Individual switch nodes will appear to be variable frequency however input and output ripple are unaffected by the varying phase firing order.

SVID CONTROL

The SVID bus allows the processor to communicate with the IR3531. The processor can program the voltage regulator output voltage and monitor telemetry data the IR3531 offers such as temperature and both rail currents. VCLK, VDIO and ALERT# communication lines are designed for external 50-75 ohm pull up resistors to 1.0-1.2V bias voltage and should not be floated. Note that ALERT# may assert twice for VID transitions of 2 VID steps or less. Addressing is programmed as a percentage of VDAC as shown by selecting the appropriate ADDR pin resistor divider combination and supports up to 14 addresses and 2 all call addresses (refer to Table 1). Table 2 provides a list of supported SVID commands. Table 3 provides a list of supported required SVID registers. The SVID communicates VID codes listed in Table 4a and 4b to program the VDAC set point.

The IR3531 can accept changes in the VID code and will vary the VDAC voltage accordingly. The slew rate of the voltage at the VDAC pin can be set by the appropriate command. The slew rate is internally programmed and no external pins or components are necessary. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents, false over current conditions and overshoot of the output voltage.

The VID data from the SVID bus is stored in registers and is sent to the Digital-to-Analog Converter (DAC), whose output is sent to the VDAC buffer amplifier. The output of the buffer amplifier is the VDAC pin. To achieve optimal system setpoint voltage accuracy, first all contributing offsets of the IR3531 are independently trimmed and lastly the internal VDAC reference is trimmed to take into account all sum of all the offset components. Note that the resulting final VDAC voltage will have a slightly wider tolerance as it is compensating for the sum of all other offset components. This results in an overall 0.5% system set-point accuracy for VID range between 1V to 1.52V.

TABLE 1: ADDR/PSN A/D VOLTAGE PROGRAMMING (AS % OF VDAC)

% of VDAC	Binary Code	Address Name	Sync	Turbo
1.5%	00000	A0/A1	Ext. Sync	Enable
4.7%	00001	A0/A1	Ext. Sync	Disable
7.8%	00010	A0/A1	Int. Clock	Enable
11%	00011	A0/A1	Int. Clock	Disable
14%	00100	A2/A3	Ext. Sync	Enable
17.2%	00101	A2/A3	Ext. Sync	Disable
20.3%	00110	A2/A3	Int. Clock	Enable
23.4%	00111	A2/A3	Int. Clock	Disable
26.5%	01000	A4/A5	Ext. Sync	Enable
29.7%	01001	A4/A5	Ext. Sync	Disable
32.8%	01010	A4/A5	Int. Clock	Enable
36%	01011	A4/A5	Int. Clock	Disable
39%	01100	A6/A7	Ext. Sync	Enable
42.2%	01101	A6/A7	Ext. Sync	Disable
45.3%	01110	A6/A7	Int. Clock	Enable
48.4%	01111	A6/A7	Int. Clock	Disable
51.5%	10000	A8/A9	Ext. Sync	Enable
54.7%	10001	A8/A9	Ext. Sync	Disable
57.8%	10010	A8/A9	Int. Clock	Enable
61%	10011	A8/A9	Int. Clock	Disable
64%	10100	A10/A11	Ext. Sync	Enable
67.2%	10101	A10/A11	Ext. Sync	Disable
70.3%	10110	A10/A11	Int. Clock	Enable
73.4%	10111	A10/A11	Int. Clock	Disable
76.6%	11000	A12/A13	Ext. Sync	Enable
79.7%	11001	A12/A13	Ext. Sync	Disable
82.8%	11010	A12/A13	Int. Clock	Enable
86%	11011	A12/A13	Int. Clock	Disable

Note: A14/A15 are reserved all-call address.

SVID COMMAND STRUCTURE

SVID protocol has two main command groups: the Get and Set commands. The Get commands retrieve data from the voltage regulator controller, while the Set commands make changes to voltage regulator operating points and power states.

When the processor (master) issues a Get command, it transmits the intended controller address and the address of the register it wants to read. The addressed controller acknowledges the command and returns the requested data. Similarly, when the processor issues a Set command, it transmits the intended controller address and the data it wants to insert. The only exception is the SetRegADR command which is used to declare the register address that SetRegDAT will alter. The controller acknowledges these commands. Parity checking is not enforced on SetRegADR/SetRegDAT.

Table 2: Supported Command

Command	Description
SetVIDfast	Slews VOUT to a new Programmed setpoint at 20mV/usec
SetVIDslow	Slews VOUT to a new Programmed setpoint at 5mV/usec
SetPS	Sets power state
SetRegADR	Declares the address of the register to be written to
SetRegDAT	Writes data to the SetRegADR declared register
GetReg	Read data of a specified register
TestMode	Test mode is used for final test trimming of the IR3531 and is not available to users.

Note: SetVID decay is not supported

Table 3: Supported Register

Register	Description
VendorID	Identifies the VR vendor
ProductID	Identifies the product model
ProductRev	Identifies the product revision
SVID Protocol ID	Identifies the version of SVID protocol
VR Capability	Communicates functions the IR3531 supports
Status1 Reg	Stores VR status data
Status2 Reg	Stores SVID bus errors
Temp Zone	Temperature zone from Rail0 sensor
Output Current	Stores output current for Rail0/Rail1
Status2_last_read	Stores previous data of status 2
ICC Max	Programs the maximum supported output current
Temp Max	Programs maximum operating temperature
SR-fast	Stores the fast slew rate value
SR-slow	Stores the slow slew rate value
Vboot	Overrides the default Vboot value
Vout Max	Programs the maximum supported operational Vout
VID Setting	Register contains the current VID setting
Power State	Register contains the current power state
VID Offset[1]	Allows margining around the VID setpoint
Multi VR Config	Configures other VR-s on the same SVID bus
SetRegADR	Scratch pad register for temporary storage of the SetRegADR pointer register

Note 1: VID Offset commands that attempt to push the VID above 1.52V or below 0V are not acknowledged.

TABLE 4: VID VALUES

VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage	VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage	VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage
00	00000000	0	**26**	00100110	0.435	**4C**	01001100	0.625
01	00000001	0.250	**27**	00100111	0.440	**4D**	01001101	0.630
02	00000010	0.255	**28**	00101000	0.445	**4E**	01001110	0.635
03	00000011	0.260	**29**	00101001	0.450	**4F**	01001111	0.640
04	00000100	0.265	**2A**	00101010	0.455	**50**	01010000	0.645
05	00000101	0.270	**2B**	00101011	0.460	**51**	01010001	0.650
06	00000110	0.275	**2C**	00101100	0.465	**52**	01010010	0.655
07	00000111	0.280	**2D**	00101101	0.470	**53**	01010011	0.660
08	00001000	0.285	**2E**	00101110	0.475	**54**	01010100	0.665
09	00001001	0.290	**2F**	00101111	0.480	**55**	01010101	0.670
0A	00001010	0.295	**30**	00110000	0.485	**56**	01010110	0.675
0B	00001011	0.300	**31**	00110001	0.490	**57**	01010111	0.680
0C	00001100	0.305	**32**	00110010	0.495	**58**	01011000	0.685
0D	00001101	0.310	**33**	00110011	0.500	**59**	01011001	0.690
0E	00001110	0.315	**34**	00110100	0.505	**5A**	01011010	0.695
0F	00001111	0.320	**35**	00110101	0.510	**5B**	01011011	0.700
10	00010000	0.325	**36**	00110110	0.515	**5C**	01011100	0.705
11	00010001	0.330	**37**	00110111	0.520	**5D**	01011101	0.710
12	00010010	0.335	**38**	00111000	0.525	**5E**	01011110	0.715
13	00010011	0.340	**39**	00111001	0.530	**5F**	01011111	0.720
14	00010100	0.345	**3A**	00111010	0.535	**60**	01100000	0.725
15	00010101	0.350	**3B**	00111011	0.540	**61**	01100001	0.730
16	00010110	0.355	**3C**	00111100	0.545	**62**	01100010	0.735
17	00010111	0.360	**3D**	00111101	0.550	**63**	01100011	0.740
18	00011000	0.365	**3E**	00111110	0.555	**64**	01100100	0.745
19	00011001	0.370	**3F**	00111111	0.560	**65**	01100101	0.750
1A	00011010	0.375	**40**	01000000	0.565	**66**	01100110	0.755
1B	00011011	0.380	**41**	01000001	0.570	**67**	01100111	0.760
1C	00011100	0.385	**42**	01000010	0.575	**68**	01101000	0.765
1D	00011101	0.390	**43**	01000011	0.580	**69**	01101001	0.770
1E	00011110	0.395	**44**	01000100	0.585	**6A**	01101010	0.775
1F	00011111	0.400	**45**	01000101	0.590	**6B**	01101011	0.780
20	00100000	0.405	**46**	01000110	0.595	**6C**	01101100	0.785

VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage	VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage	VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage
21	00100001	0.410	47	01000111	0.600	6D	01101101	0.790
22	00100010	0.415	48	01001000	0.605	6E	01101110	0.795
23	00100011	0.420	49	01001001	0.610	6F	01101111	0.800
24	00100100	0.425	4A	01001010	0.615	70	01110000	0.805
25	00100101	0.430	4B	01001011	0.620	71	01110001	0.810
72	01110010	0.815	99	10011001	1.010	C0	11000000	1.205
73	01110011	0.820	9A	10011010	1.015	C1	11000001	1.210
74	01110100	0.825	9B	10011011	1.020	C2	11000010	1.215
75	01110101	0.830	9C	10011100	1.025	C3	11000011	1.220
76	01110110	0.835	9D	10011101	1.030	C4	11000100	1.225
77	01110111	0.840	9E	10011110	1.035	C5	11000101	1.230
78	01111000	0.845	9F	10011111	1.040	C6	11000110	1.235
79	01111001	0.850	A0	10100000	1.045	C7	11000111	1.240
7A	01111010	0.855	A1	10100001	1.050	C8	11001000	1.245
7B	01111011	0.860	A2	10100010	1.055	C9	11001001	1.250
7C	01111100	0.865	A3	10100011	1.060	CA	11001010	1.255
7D	01111101	0.870	A4	10100100	1.065	CB	11001011	1.260
7E	01111110	0.875	A5	10100101	1.070	CC	11001100	1.265
7F	01111111	0.880	A6	10100110	1.075	CD	11001101	1.270
80	10000000	0.885	A7	10100111	1.080	CE	11001110	1.275
81	10000001	0.890	A8	10101000	1.085	CF	11001111	1.280
82	10000010	0.895	A9	10101001	1.090	D0	11010000	1.285
83	10000011	0.900	AA	10101010	1.095	D1	11010001	1.290
84	10000100	0.905	AB	10101011	1.100	D2	11010010	1.295
85	10000101	0.910	AC	10101100	1.105	D3	11010011	1.300
86	10000110	0.915	AD	10101101	1.110	D4	11010100	1.305
87	10000111	0.920	AE	10101110	1.115	D5	11010101	1.310
88	10001000	0.925	AF	10101111	1.120	D6	11010110	1.315
89	10001001	0.930	B0	10110000	1.125	D7	11010111	1.320
8A	10001010	0.935	B1	10110001	1.130	D8	11011000	1.325
8B	10001011	0.940	B2	10110010	1.135	D9	11011001	1.330
8C	10001100	0.945	B3	10110011	1.140	DA	11011010	1.335
8D	10001101	0.950	B4	10110100	1.145	DB	11011011	1.340
8E	10001110	0.955	B5	10110101	1.150	DC	11011100	1.345

VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage	VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage	VID7:VID0 (Hex)	VID7:VID0 (Bin)	Voltage
8F	10001111	0.960	**B6**	10110110	1.155	**DD**	11011101	1.350
90	10010000	0.965	**B7**	10110111	1.160	**DE**	11011110	1.355
91	10010001	0.970	**B8**	10111000	1.165	**DF**	11011111	1.360
92	10010010	0.975	**B9**	10111001	1.170	**E0**	11100000	1.365
93	10010011	0.980	**BA**	10111010	1.175	**E1**	11100001	1.370
94	10010100	0.985	**BB**	10111011	1.180	**E2**	11100010	1.375
95	10010101	0.990	**BC**	10111100	1.185	**E3**	11100011	1.380
96	10010110	0.995	**BD**	10111101	1.190	**E4**	11100100	1.385
97	10010111	1.000	**BE**	10111110	1.195	**E5**	11100101	1.390
98	10011000	1.005	**BF**	10111111	1.200	**E6**	11100110	1.395
E7	11100111	1.400	**F0**	11110000	1.445	**F9**	11111001	1.490
E8	11101000	1.405	**F1**	11110001	1.450	**FA**	11111010	1.495
E9	11101001	1.410	**F2**	11110010	1.455	**FB**	11111011	1.500
EA	11101010	1.415	**F3**	11110011	1.460	**FC**	11111100	1.505
EB	11101011	1.420	**F4**	11110100	1.465	**FD**	11111101	1.510
EC	11101100	1.425	**F5**	11110101	1.470	**FE**	11111110	1.515
ED	11101101	1.430	**F6**	11110110	1.475	**FF**	11111111	1.520
EE	11101110	1.435	**F7**	11110111	1.480			
EF	11101111	1.440	**F8**	11111000	1.485			

ADAPTIVE VOLTAGE POSITIONING

Adaptive Voltage Positioning (AVP) is a control algorithm where the output voltage is reduced as the load current increases. This may also be referred to as VR output impedance, Voltage Droop or Load Line. AVP is implemented to reduce the amount of bulk capacitance for a given load transient and regulation window and reduces power dissipation at heavy load. The IR3531 implementation of voltage positioning for Rail0 and Rail1 is shown in Figure 10. The output voltage is set by the VDAC or TRACK reference voltage at the positive input of the error amplifier.

INDUCTOR DCR TEMPERATURE COMPENSATION

The load current information for all the phases is fed back to the control IC through the Driver IC IOUT pins where this information is averaged and buffered to the Thermal Compensation Amplifier. The gain of the Thermal Compensation Amplifier is modified by temperature by introducing a negative temperature coefficient (NTC) thermistor (RTHERM1) and linearizing resistor network (RTCMP1 and 2) connected between the VN and VDRP pins. The thermistor should be placed close to the power stage to accurately sense the thermal performance of the inductor DCR.

The VDRP pin is connected to the FB pin through the resistor RDRP. As load current increases, the VDRP voltage increases proportionally. Since the error amplifier will force the loop to maintain FB to be equal to the VDAC reference voltage, the additional RDRP current has to flow through the RFB resistor which introduces an offset voltage that is proportional to the load current. The RFB current is equal to (VDRP-VDAC)/RDRP. The positioning voltage can be programmed by the resistors RDRP and RFB so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

CURRENT MONITOR (IMON)

The control IC generates a current monitor signal IMON using the VDRP voltage and the VDAC reference, also shown in Figure 10. The voltage at this pin reports the average load current information referenced to LGND. The slope of the IMON signal with respect to the load current can be adjusted with the resistors RTCMP2 and RTCMP3. The IMON signal is clamped at 1.09V in order to facilitate direct interfacing with the master.

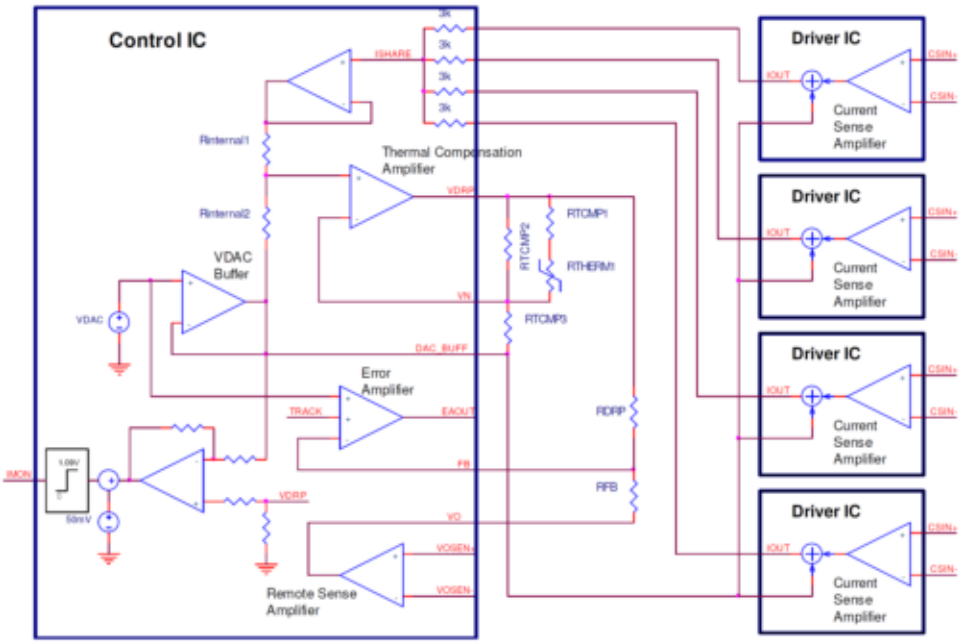

Figure 10: Adaptive voltage positioning with thermal compensation

REMOTE VOLTAGE SENSING

The remote sense differential amplifier in the IR3531 is a high speed, low input offset unity gain buffer that provides accurate voltage sensing and fast transient response. VOSEN+ and VOSEN- are the remote-sensing Kelvin connections that are tied directly to the load. Internal resistors to the differential amplifier produce VOSEN+ and VOSEN- bias currents of up to 50µA maximum and limits the size series resistors for acceptable regulation of the output voltage. Open sense lead detection is also included in this amplifier and is discussed further in the fault section.

PHASE SHEDDING

IR3531 allows phases to be disabled through the PHSSHED pin. Shedding can be performed either statically at power up or can be exercised dynamically during normal operation. One, two or three phases can be disabled to help enhance light load efficiency. The internal clock frequency is automatically adjusted to achieve graceful transition. Phase shedding is not recommended if an external synchronization clock is being applied.

TABLE 5: PHASE SHEDDING PROGRAMMING THRESHOLDS

Threshold	Action
PHSSHED < 0.25VCC	No Phases Shed
0.25VCC < PHSSHED < 0.5VCC	Shed 1 Phase
0.5VCC < PHSSHED < 0.75VCC	Shed 2 Phases
PHSSHED < 0.75VCC	Shed 3 Phases

POWER STATES AND HIGH EFFICIENCY MODE AT LOW LOADS

System processors can request the VR to enter higher efficiency Power Savings modes. The IR3531 enters single phase operation when a PS1 command is issued from the processor. This mode is intended for loads less than 20A. There is an 8 switching cycle delay before the VR transitions from PS0 to PS1. PS2 mode is not supported.

PLATFORM TEST MODE

Platform test mode allows users to test the VR solution when the default VBOOT voltage programmed on IR3531 is 0V and there is no communication capability to send commands. The address pin needs to be pulled up to 3.3V for IR3531 to go into platform test mode. IR3531 will boot to 1V in this mode.

PROTECTION

The Fault Table below describes the different faults that can occur and how the IR3531 reacts to protect the supply and the load from possible damage. The fault types that can occur are listed in row 1. Row 2 has the method that a fault is cleared. The first 3 faults are latched in the UV fault latch and the VCC power has to be recycled to clear. An over voltage fault can be cleared by recycling either VCC or the Enable signal. The rest of the faults (except for UVLO VOUT and SVID faults) are temporarily latched in the SS fault latch until the fault condition clears. Most faults disable the error amplifier (except for SVID and VOUT UVLO). Most faults (except SVID) flag VRRDY. VRRDY returns to active high when all faults are cleared. The delay row shows reaction time after detecting a fault condition. Delays are provided to minimize the possibility of nuisance faults. The table applies for both rails of the IC.

TABLE 6: FAULT OPERATION

	FAULT TYPE								
	Open Control Loop	**Open Sense Line**	**Over Voltage**	**SVID**	**Enable Low**	**V12V UVLO**	**VCC UVLO**	**Over Current**	**VO UVLO**
Fault Clearing Method	Recycle VCC		Recycle VCC or Enable	Resume Normal Operation when Condition Clears					
Error Amp Disabled	Yes			No	Yes				No
ROSC/OVP drives high until OV clears	No		Yes	No					
VRRDY Low?	Yes			No	Yes				
VDAC Response?	Transition to 250mV and holds until fault is cleared							Cycles from VBOOT to 250mV	No Change
If fault occurs on Rail0 will Rail1 continue to operate?	No	No	No	Yes	No	No	No	Hiccup	Yes
If fault occurs on Rail1 will Rail0 continue to operate?	No	No	No	Yes	No	No	No	Hiccup	Yes
Delay	8 PWM Cycles	No	No	4 SVID Clock Cycles to send NAK	250 ns Blank Time	No	No	256µs OC duration, 4ms off duration	No

ENABLE INPUT

The Enable pin has a 0.6V falling threshold that sets the Fault Latch, a 650mV rising threshold that clears the fault latch and has a 250ns filter to prevent chatter due to system noise.

OPEN VOLTAGE LOOP DETECTION

If for some reason the control loop fails during operation, the system protects itself by latching an open loop fault that requires VCC recycling to clear. Detection is performed by monitoring the output of the error amplifier. The fault is latched if EAOUT operates above VCC-1.08V for 8 switching cycles indicating the control loop is broken.

OPEN REMOTE SENSE LINE PROTECTION

The VOSEN+ and VOSEN- remote sense line impedances are checked prior to power up to verify they are connected to low impedances. If high impedance is detected, an Open Sense Line fault is latched and requires VCC to be recycled to clear. During normal operation, the remote sense amp operating environment is monitored to ensure the remote sense lines are connected. Again, if an abnormal mode is detected, the sense line impedances are again checked. If high impedance is detected, an Open Sense Line fault is latched and requires VCC to be recycled to clear.

V12V AND VCC UNDER VOLTAGE LOCKOUT (UVLO)

The IR3531 monitors the converter input voltage rails (V12V and VCC) and issues a UVLO fault if either voltage is below the desired operating range. The maximum power up clear thresholds are 10.2V for V12V and 6.2V for VCC.

START-UP AND SHUT-DOWN SEQUENCE

The IR3531 has a programmable, digitally controlled soft-start function to limit the surge current during the voltage regulator start-up. The default boot voltage for Rail0 rail is 0.9V, for Rail1 it is 1.5V. Figure 11 depicts an Enable gated power-up and V12V UVLO shutdown followed by a V12V UVLO gated power up and an Enable low shutdown.

The IR3531 requires less than 1ms to perform calibration routines once V12V (VIN) UVLO is cleared. Note VDAC is forced to 1.52V during calibration and A/D sampling and settles to 250mV once calibration is complete.

Figure 12 shows two different power-up responses where Enable going high is gating the first VDAC slew and the calibration routine is gating the second VDAC slew. The default slew rate is 5mV/µsec. The control loop ensures the regulator output voltage will track VDAC. The soft start sequence finishes when VOUT is settled to the VBOOT set point and VRRDY is asserted.

The IR3531 has soft stop capability which allows the voltage regulator to power down in a controlled fashion without producing negative undershoots resulting from fast discharge of output capacitance. Pre-biased outputs are also supported as shown in Figure 13.

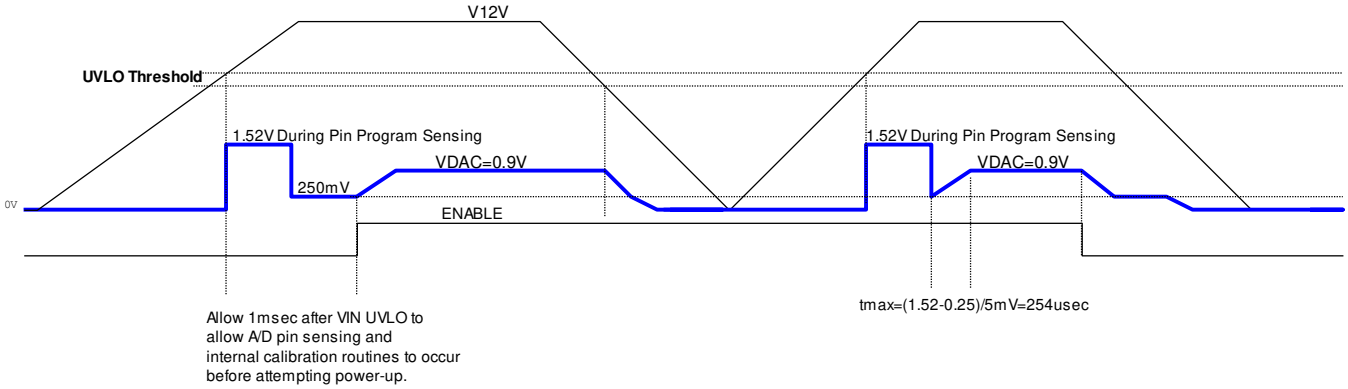

Figure 12: V12V Power and Enable Cycling

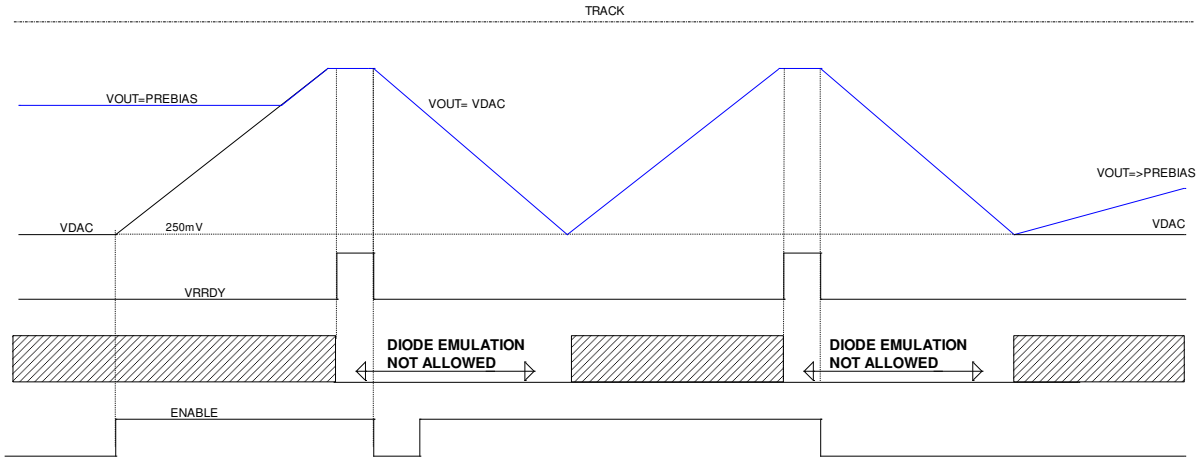

Figure 13: Enable Power Cycling Under Pre-bias

OVER-CURRENT CONTROL DURING SOFT-START

Over current protection is performed internally by comparing the VDRP pin voltage against an OC offset voltage that is added to the respective VDAC pin voltage. This OC offset voltage is adjusted to match the active number of phases since VDRP represents average per-phase current. This ensures that the current limit is correctly adjusted during phase shedding operation. The OC offset voltage is set as percentages of 1.025V above VDAC.

An over current condition is registered if the VDRP pin voltage, which is proportional to the average current plus VDAC voltage, exceeds the VDAC+ OC offset voltage.

Figure 14 shows the over-current control with delay during various soft start events. The delay time is fixed at 256µs. The delay is required since over-current conditions can occur as part of normal operation due to inrush current. If an over-current occurs during soft start (before VRRDY is asserted), the control IC will not react until the over current delay time has elapsed. If the over-current condition persists after delay time is reached, the fault latch will be set pulling the error amplifier's output low and inhibiting switching in the driver ICs. The VDAC voltage will slowly ramp down until it reaches 0.25V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle, the constant over-current control actions will repeat and the converter will be in hiccup mode.

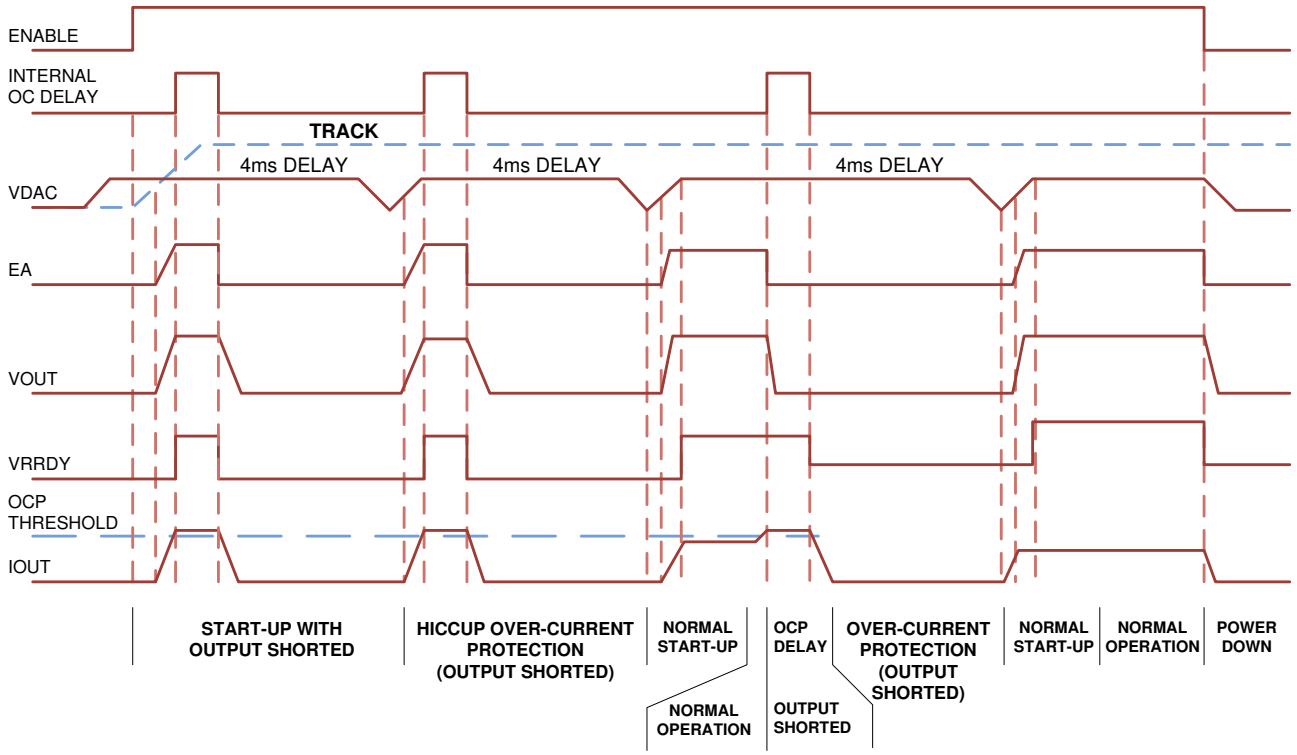

Figure 14: Over-Current Waveforms during and after start-up

ICCP (ICC MAX) PROGRAMMING

SVID register ICC MAX contains information on the maximum allowable current supported by the voltage regulator solution and can be equivalent to the CPU's ICC_MAX. The CPU reads this register for platform compatibility during boot and uses this data in conjunction with the IOUT register for performance management. This data is in an 8-bit binary formant equivalent to amps, i.e. 75A=4Bh.

The voltage is programmed by an external resistor divider string referenced to VDAC. Table 7 lists the available current thresholds

TABLE 7: ICCP (ICC MAX) A/D VOLTAGE PROGRAMMING (AS % OF VDAC)

%VDAC	Binary Code	Current Level
1.5	00000	60A/25A
4.7	00001	60A/35A
7.8	00010	70A/25A
11	00011	70A/35A
14	00100	80A/25A
17.2	00101	80A/35A
20.3	00110	90A/25A
23.4	00111	90A/35A
26.5	01000	100A/25A
29.7	01001	100A/35A
32.8	01010	110A/25A
36	01011	110A/35A
39	01100	120A/25A
42.2	01101	120A/35A
45.3	01110	130A/25A
48.4	01111	130A/35A
51.5	10000	140A/25A
54.7	10001	140A/35A
57.8	10010	150A/25A
61	10011	150A/35A
64	10100	160A/25A
67.2	10101	160A/35A
70.3	10110	170A/25A
73.4	10111	170A/35A
76.6	11000	180A/25A
79.7	11001	180A/35A
82.8	11010	190A/25A
86	11011	190A/35A
89	11100	200A/25A
92.2	11101	200A/35A
95.3	11110	225A/25A
98.4	11111	225A/35A

TEMPERATURE TELEMETRY

The maximum temperature TMAX (22h) value is factory programmed to 110C. This register contains the maximum temperature the VR supports prior to issuing a thermal alert or VR_Hot. The master reads this register and uses this data in conjunction with the Temperature Zones for performance management. Factory trim options are listed in Table 8.

TABLE 8: TEMP MAX (PROGRAMMED AT FINAL TEST)

Binary Code	Temperature	Binary Code	Temperature
0000	90 Deg C	1000	106 Deg C
0001	92 Deg C	1001	108 Deg C
0010	94 Deg C	**1010**	**110 Deg C**
0011	96 Deg C	1011	112 Deg C
0100	98 Deg C	1100	114 Deg C
0101	100 Deg C	1101	116 Deg C
0110	102 Deg C	1110	118 Deg C
0111	104 Deg C	1111	120 Deg C

THERMAL MONITORING (VRHOT#)

The IR3531 provides two methods of thermal monitoring: a VRHOT# pin which flags an over temperature event and temperature telemetry is available through the SVID bus and the Temperature Zone register.

A thermal sense network which includes an NTC thermistor provides board temperature information at TSENS pin as shown in Figure 15. The thermistor is usually placed in a temperature sensitive region of the converter and is linearized by a resistor network. VRHOT# will be active low once the voltage on TSENS crosses Zone 7, or 56.3% of VDAC. VRHOT# will de-assert once TSENS falls below Zone 5. The VRHOT# pin is an open-collector output and should be pulled up to a voltage source through a resistor.

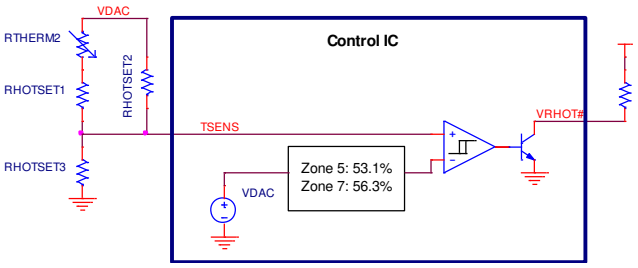

Figure 15: Over Temperature Detection Circuit

The IR3531 compares the TSENS pin voltage against fixed percentages of VDAC thresholds as indicated in Table 9. The user can program the external TSENS network to achieve a desired offset and slope to associate a zone (stored in register 12h) with a desired temperature. Zones correspond to the bit number of this 8-bit register, i.e. Zone 0=bit 0 and Zone 3=bit3 and therefore register 12h behaves like a thermometer. Notice that the zones 1 through 7 thresholds are equally spaced (~1.6% between thresholds) and the separation between Zone0 and Zone1 is approximately double. Since these zone thresholds are fixed and equally separated, the respective zone temperature values will also be equally separated for a TSENS voltage which has a linear slope vs. temperature.

The SVID status register bit#1 and the ALERT# serve as thermal warning flags when zones 5 and 6 are crossed as indicated in Table 9. These warning flags may be used by the system to reduce the load, increase airflow, and prevent the system from entering thermal shutdown. The VRHOT# pin is asserted as zones 6 and 7 are crossed and can be used as a thermal shutdown flag.

TMAX is merely a reference point to communicate with downstream system monitors what temperature a zone equates to. For example, the TMAX register is defaulted in the IR3531 as 110°C. The micro processor can perform a GetReg on TMAX and is now able to associate a Zone 4 declaration by the IR3531 to equate to 100.1°C

TABLE 9: TEMPERATURE ZONES

Temperature Zone	TSENS Threshold % VDAC	% of TMAX	Degrees C based on 110°C TMAX
Zone 0	43.8%	75%	82.5C
Zone 1	46.9%	82%	90.2
Zone 2	48.4%	85%	93.5
Zone 3	50%	88%	96.8
Zone 4	51.6%	91%	100.1 Falling, Status bit 1 de-asserted, ALERT#.
Zone 5	53.1%	94%	103.4 Falling, VRHOT# de-asserted
Zone 6	54.7%	97%	106.7 Rising, Status bit 1 asserted, ALERT#.
Zone 7	56.3%	100%	110 Rising, VRHOT# asserted

OVER VOLTAGE PROTECTION (OVP)

The IR3531 offers multilevel output over-voltage protection to ensure no conflicts occur during pre-biased conditioned power-up or no/light load soft stop. OVP is sensed through the FB which allows users to externally use FB resistor dividers if output voltages greater than 1.52V are desired. The OVP threshold is set to 1.65V during power up until VR Settled is reached, then the threshold is reduced to VDAC+130mV. This OVP threshold is maintained during normal operation and remains until VO, the output of the remote sense amplifier, reaches 250mV with respect to ground. This ensures OVP protection during soft stop events or down tracking events. The OVP threshold then returns to 1.65V on the FB pin to allow pre-bias startup.

IR3531 drives the ROSC/OVP pin above V(VCC)–1V to indicate an over voltage event has occurred. This ROSC/OVP flag can be used by the system designer to shut the input if desired.

The over voltage condition also sets the over voltage fault latch which ensures the voltage regulator is off. OVP overrides the normal PWM operation and will regulate the output voltage by modulating the low-side MOSFET within approximately 150ns to prevent the FB pin from exceeding the OVP threshold. The OVP fault condition can only be cleared by cycling VCC UVLO or ENABLE.

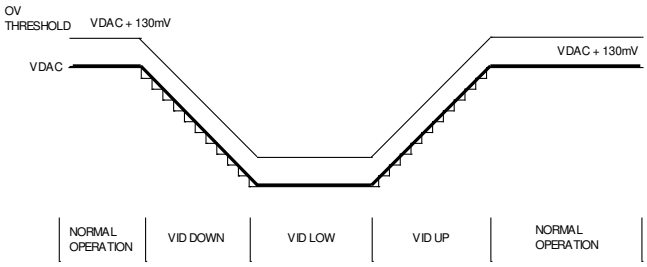

Figure 16: Over Voltage Protection during SETVID Fast/Slow

DESIGN PROCEDURES

IR3531 EXTERNAL COMPONENTS

Switching Frequency Setting

Use of internal oscillator mode is not recommended. Use the SCLK input to set PWM frequency. When SCLK is used, ROSC should be present, and selected for the per phase switching frequency in use. The chart below shows the relationship between the per-phase switching frequency and the ROSC value.

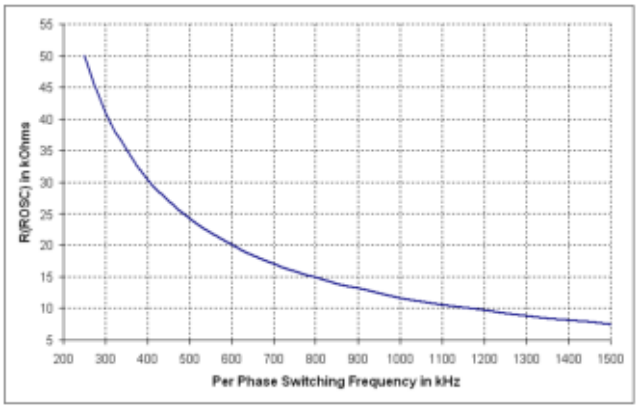

Figure 17: RROSC vs. Per-phase Switching Frequency

ADDRESS AND PHASE NUMBER PROGRAMMING RESISTORS RADDR1 AND RADDR2

The ADDR pin is multi-function: SVID addressing for Rail0 and Rail1, internal/external clock synchronization and Turbo enable/disable is selected through this pin. Choose RADDR2 and apply the following equation to determine RADDR1:

$$RADDR1 = \frac{1 - \frac{\%VDAC}{100}}{\%VDAC} * 100 * RADDR2$$

where, %VDAC is the desired percentage of VDAC found in Table 1.

ICCP PROGRAMMING RESISTORS RICCP1 AND RICCP2

The ICCP programming resistors are used to program the maximum currents Rail0 and Rail1 can support. Choose RICCP2 and follow the equation below to calculate RICCP1.

$$RICCP1 = \frac{1 - \frac{\%VDAC}{100}}{\%VDAC} * 100 * RICCP2$$

where, %VDAC is the desired percentage of VDAC found in Table 7.

PHASE SHEDDING IMPLEMENTATION CIRCUITS

The following is a proposed circuit to implement phase shedding. Two signals (S1 and S2) drive logic level MOSFETs to produce a four level PHSSHED signal. The operation is described in Table 6.

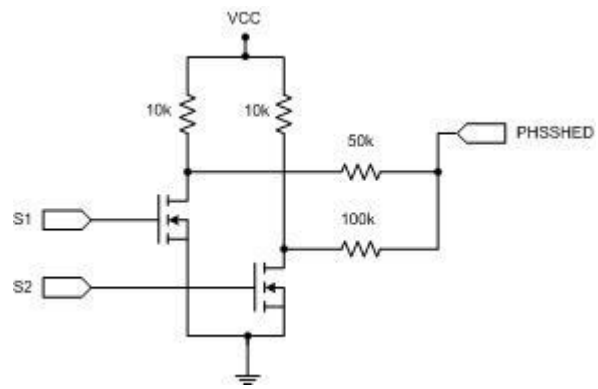

Figure 18: Phase Shedding Implementation

TABLE 10: PHASE SHEDDING CONTROL

S1	S2	V(PHSSHED)	Phases
0	0	VCC	Drop 3 Phases
0	1	0.625* VCC	Drop 2 Phases
1	0	0.31* VCC	Drop 1 Phases
1	1	0V	Drop 0 Phases

IMON AND IMON1 CAPACITORS

Use 100nF for CIMON and CIMON1 to provide an approximate 1ms filtered time constant for current reporting data.

VCC BIAS REGULATOR POWER STAGE COMPONENTS

Use a 10 µH inductor with a current rating no less than 2 A. Use a Schottky diode with operating current of 1 A or higher and capable of withstanding 2 A for short periods of time. A 10 µF capacitor ceramic capacitor rated for 16V is recommended for charge storage and filtering.

TEMPERATURE SENSING

The TSENS pin is used to provide temperature information of the voltage regulator by providing temperature zone information to the microprocessor through the SVID. This information is also used to flag VRHOT#. Temperature is sensed via a linearized NTC resistor network. Temperature sensing and temperature zones are represented as a percentage of the reference voltage VDAC as required by the processor specification. A properly designed network will get the TSENS voltage very close to the required target. 1% thermistors are highly recommended to achieve the specified accuracy. Thermistor Beta is the biggest factor in attaining accuracy. The target and TSENS voltages are calculated from the equations below. The analysis is done at VDAC of 1.5, because that is where the biggest error occurs.

$$V_{TARGET} = \frac{0.11*1.5}{T\max - T\min}*T + 0.453*1.5 - \frac{0.11*1.5}{T\max - T\min}*T\min$$

$$V_{TSENSE} = \frac{RHOTSET3}{RHOTSET3 + RTSeq}*1.5$$

$$RTSeq = \frac{(RHOTSET1 + RTHERM2)*RHOTSET2}{RHOTSET1 + RHOTSET2 + RTHERM2}$$

$$RTHERM2 = RTHERM2_{ROOM} * \exp(beta(\frac{1}{T} - \frac{1}{T_{ROOM}}))$$

where $RTHERM2_{ROOM}$ is the thermistor value at room temperature, beta is the thermistor coefficient, Tmax and Tmin are the temperatures of the highest and lowest temperature zone respectively. The temperature sensing components are chosen by finding an approximate solution that brings the target and TSENS as close to each other as possible. This can be done using an optimization routine of your choice such as the IR3531 excel design tool.

RAIL0 THERMAL COMPENSATION

Thermal compensation is required to counter the effect of the inductor DCR positive temperature coefficient. Failure to compensate results in large current reporting errors and poor load line regulation. Thermal compensation is done using a NTC thermistor and a linearizing resistor network. A properly design network is necessary to achieve the required accuracy targets. 1% thermistors are highly recommended to achieve the specified accuracy. Thermistor Beta is the biggest factor in attaining accuracy.

The goal is to keep VDRP-VDAC at 900 mV for all temperatures at the maximum current. Thus, the equation below has to be satisfied.

$$VDRP - VDAC = \frac{1}{3}*(\frac{DCR*Gcs}{n})*(1+\frac{RTCeq}{RTCMP3})*\mathrm{Im}ax = 900mV$$

$$RTCeq = \frac{RTCMP2*(RTCMP1 + RTHERM1)}{RTCMP1 + RTCMP2 + RTHERM1}$$

$$RTHERM1 = RTHERM1_{ROOM} * \exp(beta(\frac{1}{T} - \frac{1}{T_{ROOM}}))$$

$$DCR = DCR_{ROOM} * (1 + 3850e-6*(T - T_{ROOM}))$$

where $RTHERM1_{ROOM}$ is the thermistor value at room temperature, beta is the thermistor coefficient, Tmax and Tmin are the temperatures of the highest and lowest temperature zone respectively, Gcs is the typical current sense amplifier gain of 32.5, and DCR_{ROOM} is the inductor series resistance at room temperature. The temperature sensing components are chosen by finding an approximate solution that results in VDRP-VDAC=900mV over the entire temperature operating range. This can be done using an optimization routine of your choice such as the IR3531 excel design tool.

RAIL0 DROOP RESISTOR CALCULATION

RDRP in combination with the feedback resistor RFB sets the load line of Rail0. RFB is first chosen with a typical suggested value of 2kOhm. The following equation calculates RDRP.

$$RDRP = \frac{RFB*DCR_{ROOM}*Gcs}{3*Ro*n}*(1+\frac{RTCeq_{ROOM}}{RTCMP3})$$

where Ro is the load line, DCR_{ROOM} is the inductor series resistance at room temperature, Gcs is the typical current sense amplifier gain of 32.5, n is the number of phases and $RTCeq_{ROOM}$ is the same as RTCeq in section Rail0 Thermal Compensation with RTHERM1 value at room temperature.

RAIL1 THERMAL COMPENSATION

RSCALE1, RSCALE2, RSCALE3 and RTHERM3 are used to provide current reporting thermal compensation for Rail1. The purpose is to keep VDRP1-VDAC1 equal to 900mV for all temperatures at the maximum load current. This is expressed mathematically in the following equation.

$$VDRP1 - VDAC1 = 9 * DCR * Gcs * \mathrm{Im}ax * \left(\frac{\frac{(RSCALE1 + RTHERM3) * RSCALE2}{RSCALE1 + RTHERM3 + RSCALE3}}{RSCALE2 + \frac{(RSCALE1 + RTHERM3) * RSCALE3}{RSCALE1 + RTHERM3 + RSCALE3}} \right) = 900mV$$

where DCR and RTHERM3 are expressed in section Rail0 Thermal Compensation. Imax is the maximum current for Rail1 and Gcs is the typical current sense amplifier gain of 32.5. The temperature sensing components are chosen by finding an approximate solution that results in VDRP1-VDAC1=900mV over the entire temperature operating range. This can be done using an optimization routine of your choice such as the IR3531 excel design tool.

RAIL 1 DROOP RESISTOR CALCULATION

RDRP1 in combination with the feedback resistor RFB1 sets the load line of Rail1. RFB1 is first chosen with a typical suggested value of 2kOhm. The equation below calculates RDRP1.

$$RDRP1 = 9 * \frac{RFB1 * DCR_{ROOM} * Gcs}{Ro} * \left(\frac{\frac{(RSCALE1 + RTHERM3_{ROOM}) * RSCALE3}{RSCALE1 + RTHERM3_{ROOM} + RSCALE3}}{RSCALE2 + \frac{RSCALE1 + RTHERM3_{ROOM}) * RSCALE3}{RSCALE1 + RTHERM3_{ROOM} + RSCALE3}} \right)$$

where Ro is the load line, DCR_{ROOM} is the inductor series resistance at room temperature, Gcs is the typical current sense amplifier gain of 32.5, $RTHERM3_{ROOM}$ value at room temperature.

COMPENSATION NETWORKS

IR3531 utilizes voltage mode control for small signal loop regulation. The compensation scheme is a classic type 3 system consisting of components RFB(1), CFB(1), RCFB(1), CEA(1), CCP(1) and RCP(1).

The system dynamics can change significantly when transitioning from 4 phases to 1 phase. Loop 0 has an additional component, RPSC, that is inserted in the loop when in PS1 mode (single phase) to optimize phase margin. RPSC adds to RCP thereby reducing the system bandwidth if desired. To disable this feature, place RPSC as a zero ohm resistor. The IR3531 excel design tool can be used to calculate an initial starting point.

Note RDRP needs to be recalculated if RFB is changed.

LAYOUT GUIDELINES

- VCC bias inductor LVCC must be close to SW pin. VCC bias bulk cap COUTVCC must be located near LVCC and connections for COUTVCC must be as short as possible.
- For both rails, all components connected to EA, FB, VDRP, and VO pins must be located on the same layer as the IR3531 as close to these pins as possible.
- Insert 9 equally spaced connection vias to GND tab of IR3531.
- V12V decoupling cap must be near pin of IR3531 with GND connection as short as possible.
- ROSC must be located close to pin of IR3531.
- RTHERM1 and RTHERM3 must be located close to inductor of associated voltage regulator. Locate RTHERM2 to provide overall temperature reading of the power converter.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize prevent shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- A single 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.
- No PCB traces should routed nor Vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.

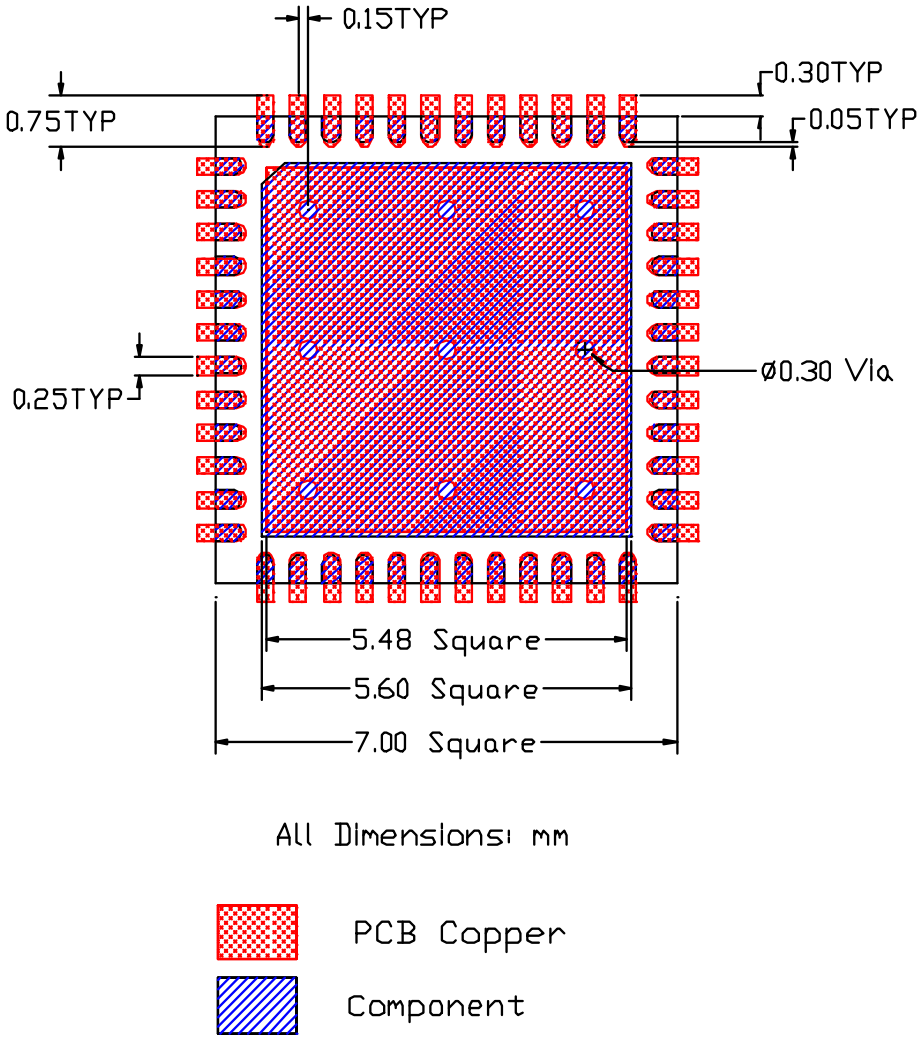

Figure 19: Metal and Component Placement

* Contact International Rectifier to receive an electronic PCB Library file in your preferred format.

SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist misalignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist miss-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The vias in the large center pad should be tented or plugged from bottom board side with solder resist.

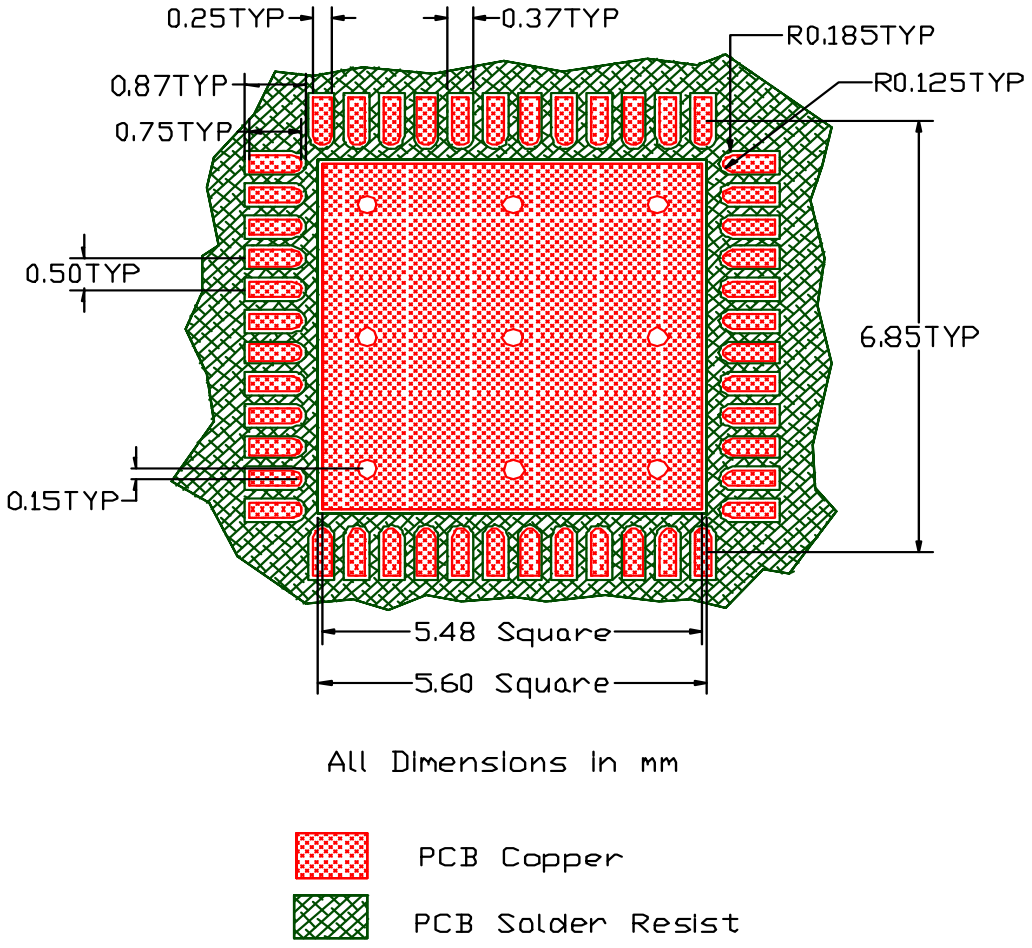

Figure 20: Solder Resist

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STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be approximately 70% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

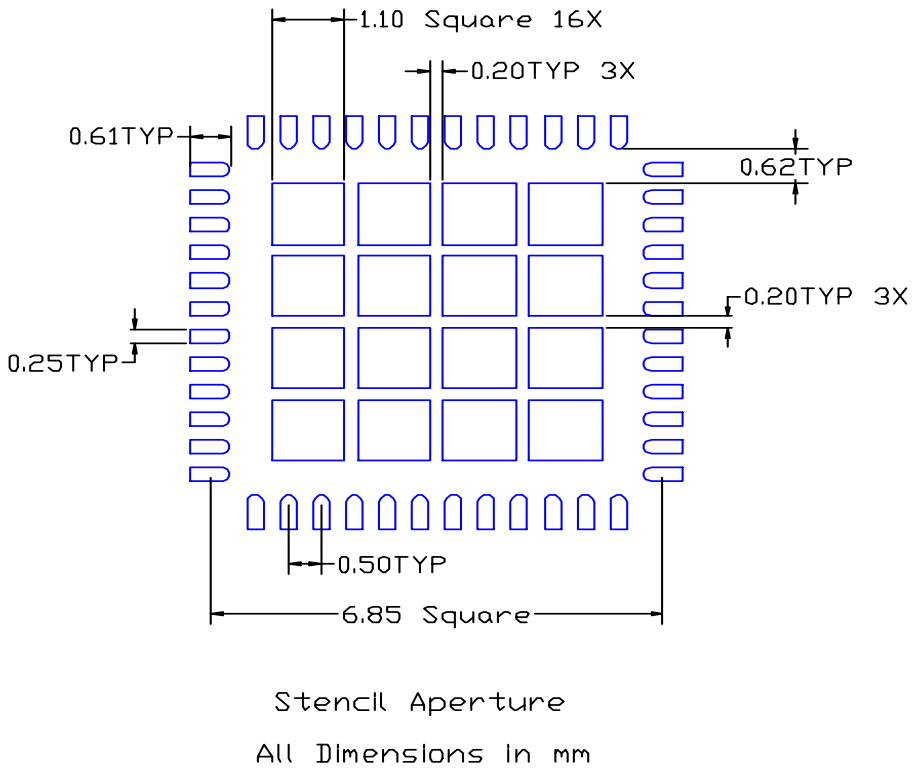


Figure 21: Stencil Design

* Contact International Rectifier to receive an electronic PCB Library file in your preferred format.

MARKING INFORMATION

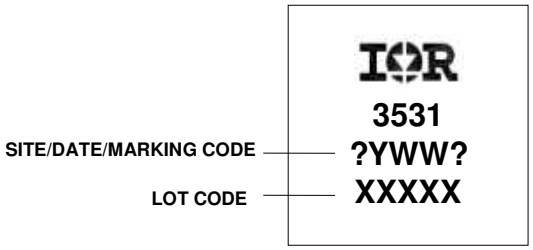
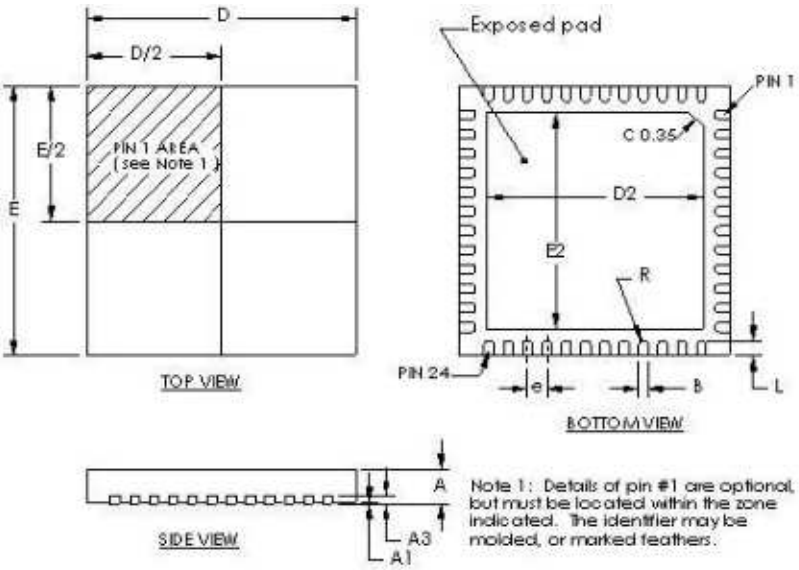


Figure 22: Package Marking

PACKAGE INFORMATION

48L MLPQ (7 x 7 mm Body) θ_{JA} = 23.5 ºC/W, θ_{JC} = 1 ºC/W



48L-7x7 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
e	0.50 TYP		
L	0.30	0.40	0.50
R	0.125 TYP		

Figure 23: Package Dimensions

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

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