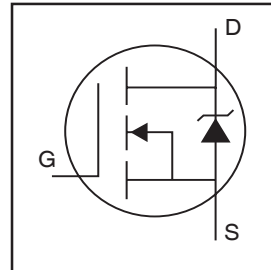


IRFIZ48VPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ®
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications
- Lead-Free

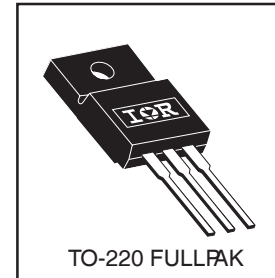


$V_{DSS} = 60V$
 $R_{DS(on)} = 12m\Omega$
 $I_D = 39A$

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	39	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	27	
I_{DM}	Pulsed Drain Current ① ②	290	
$P_D @ T_C = 25^\circ C$	Power Dissipation	43	W
	Linear Derating Factor	0.29	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current ① ②	72	A
E_{AR}	Repetitive Avalanche Energy ① ②	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ②	5.3	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	300 (1.6mm from case) 10 lbf•in (1.1N•m)	

Thermal Resistance

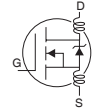
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	3.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	65	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.064	—	V/°C	Reference to 25°C , $I_D = 1\text{mA}$ ⑦
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	12.0	mΩ	$V_{GS} = 10V, I_D = 43A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	35	—	—	S	$V_{DS} = 25V, I_D = 43A$ ④ ⑦
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	110	nC	$I_D = 72A$
Q_{gs}	Gate-to-Source Charge	—	—	29		$V_{DS} = 48V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	36		$V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑦
$t_{d(on)}$	Turn-On Delay Time	—	7.6	—	ns	$V_{DD} = 30V$
t_r	Rise Time	—	200	—		$I_D = 72A$
$t_{d(off)}$	Turn-Off Delay Time	—	157	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	166	—		$R_D = 0.34\Omega$, See Fig. 10 ④ ⑦
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1985	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	496	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	91	—		$f = 1.0\text{MHz}$, See Fig. 5 ⑦
E_{as}	Single Pulse Avalanche Energy ② ⑦	—	780⑤	170⑥	mJ	$I_{AS} = 72A, L = 64\text{mH}$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	39	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ① ⑦	—	—	290		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 72A, V_{GS} = 0V$ ④ ⑦
t_{rr}	Reverse Recovery Time	—	70	100	ns	$T_J = 25^\circ\text{C}, I_F = 72A$
Q_{rr}	Reverse Recovery Charge	—	155	233	nC	$di/dt = 100A/\mu s$ ④ ⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 64\mu H$
 $R_G = 25\Omega$, $I_{AS} = 72A$. (See Figure 12)
- ③ $I_{SD} \leq 72A$, $di/dt \leq 151A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- ⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.
- ⑦ Uses IRFZ48V data and test conditions.
- ⑧ $t = 60s$, $f = 60\text{Hz}$

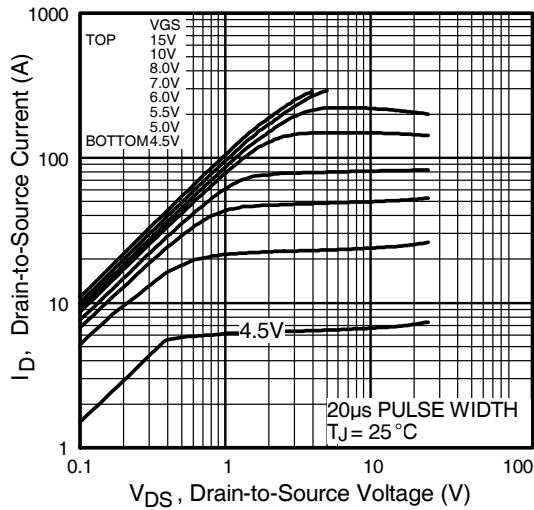


Fig 1. Typical Output Characteristics

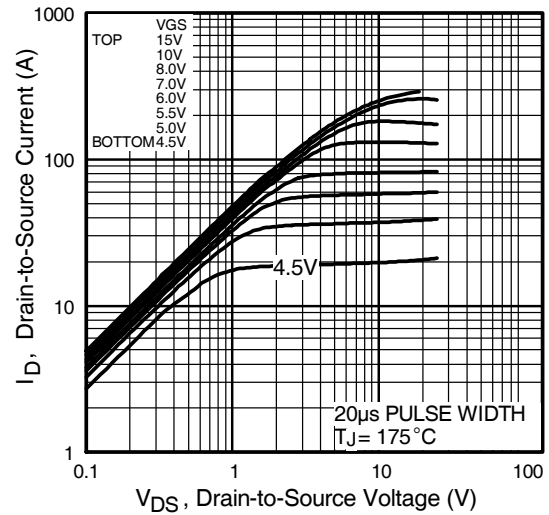


Fig 2. Typical Output Characteristics

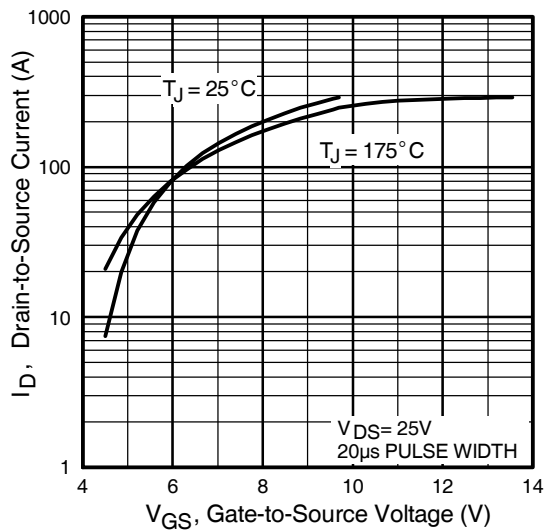


Fig 3. Typical Transfer Characteristics

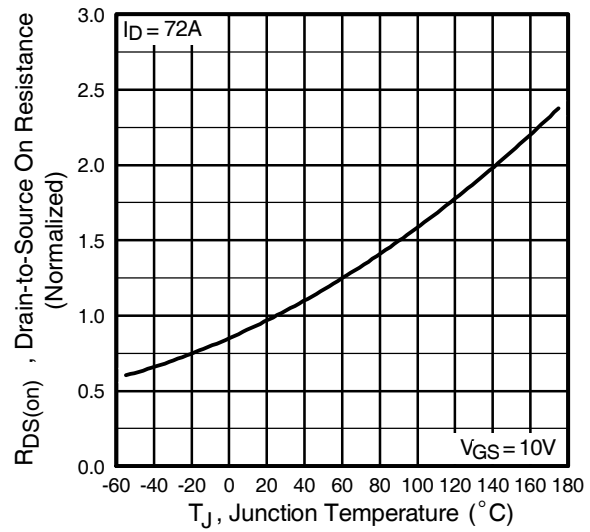


Fig 4. Normalized On-Resistance Vs. Temperature

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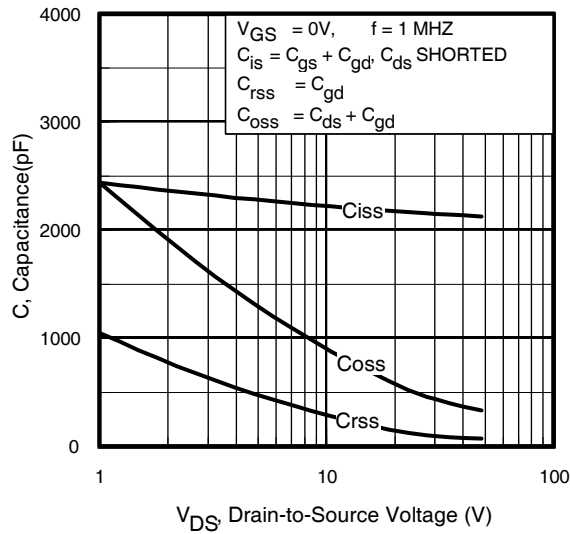


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

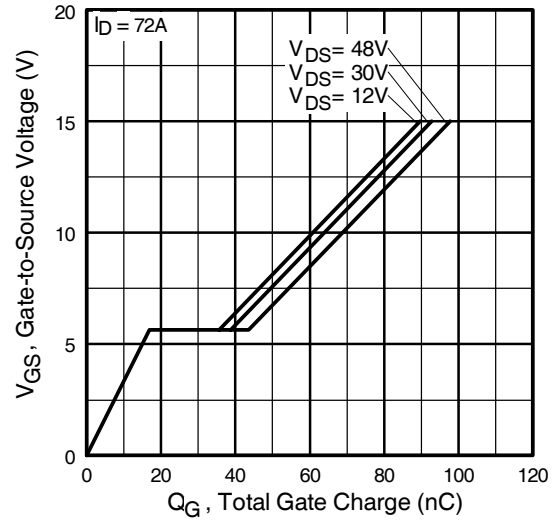


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

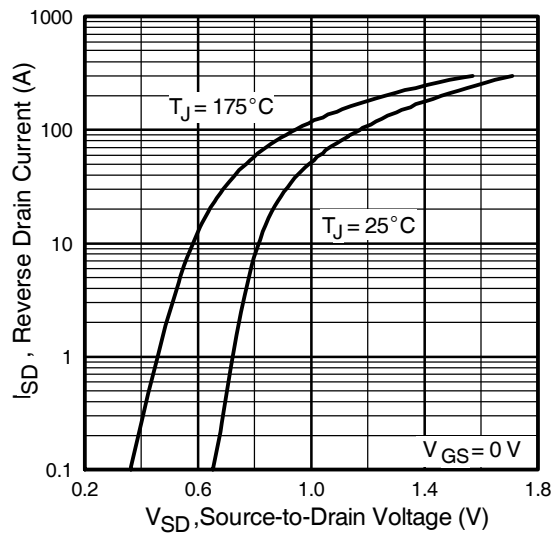


Fig 7. Typical Source-Drain Diode Forward Voltage

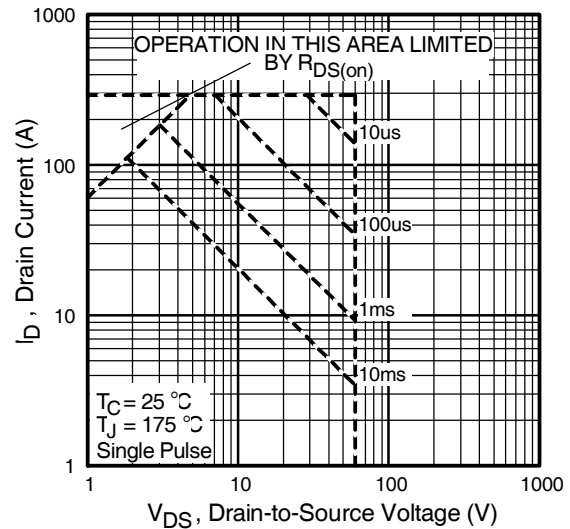


Fig 8. Maximum Safe Operating Area

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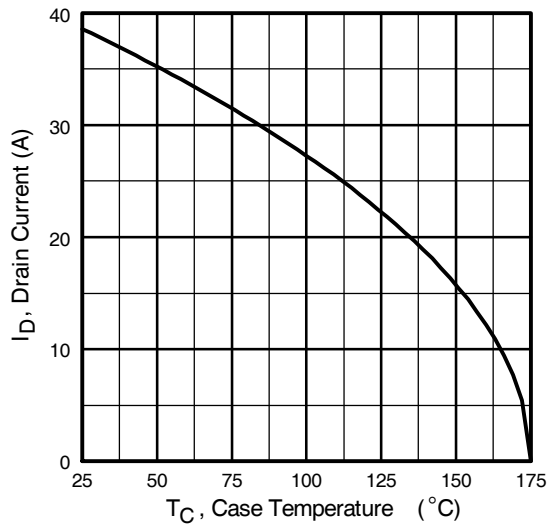


Fig 9. Maximum Drain Current Vs. Case Temperature

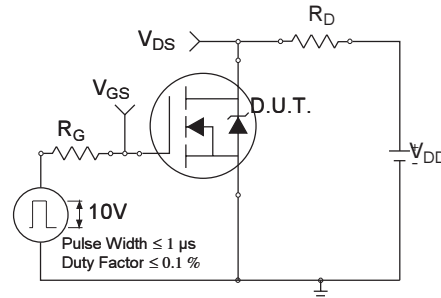


Fig 10a. Switching Time Test Circuit

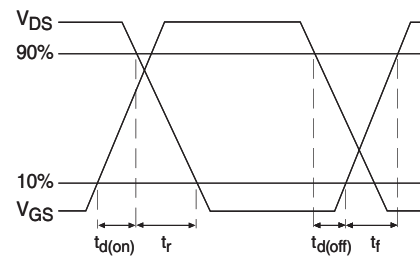


Fig 10b. Switching Time Waveforms

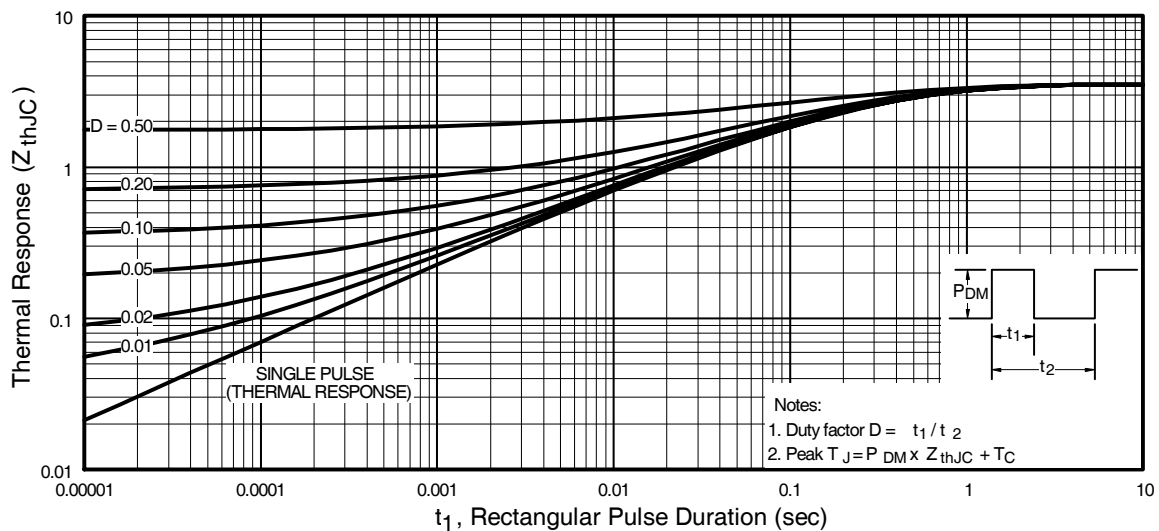


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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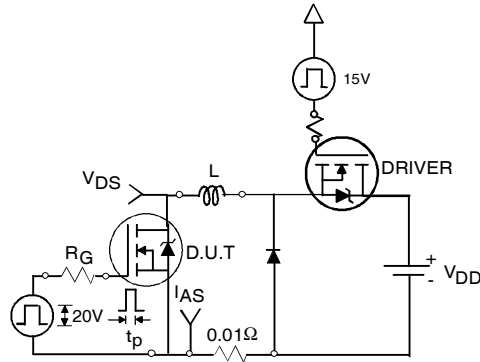


Fig 12a. Unclamped Inductive Test Circuit

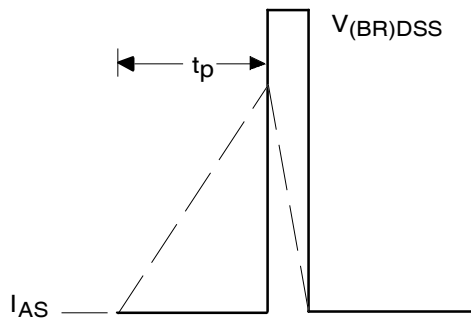


Fig 12b. Unclamped Inductive Waveforms

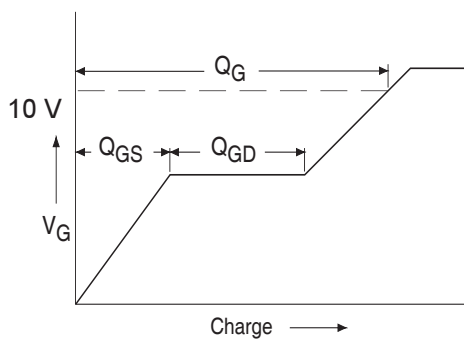


Fig 13a. Basic Gate Charge Waveform

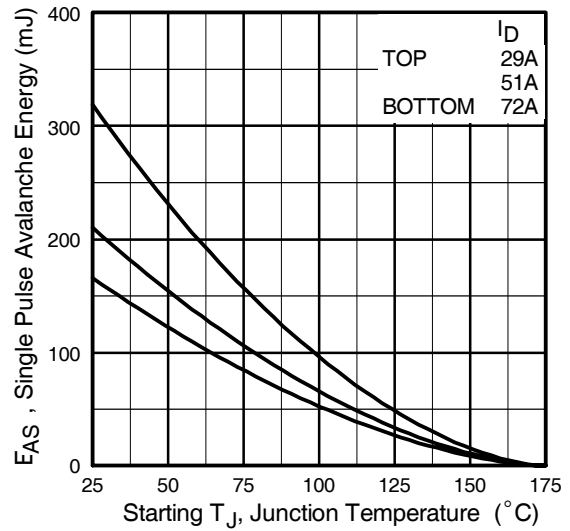


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

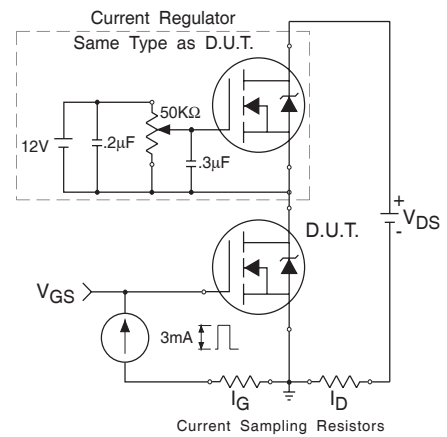


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

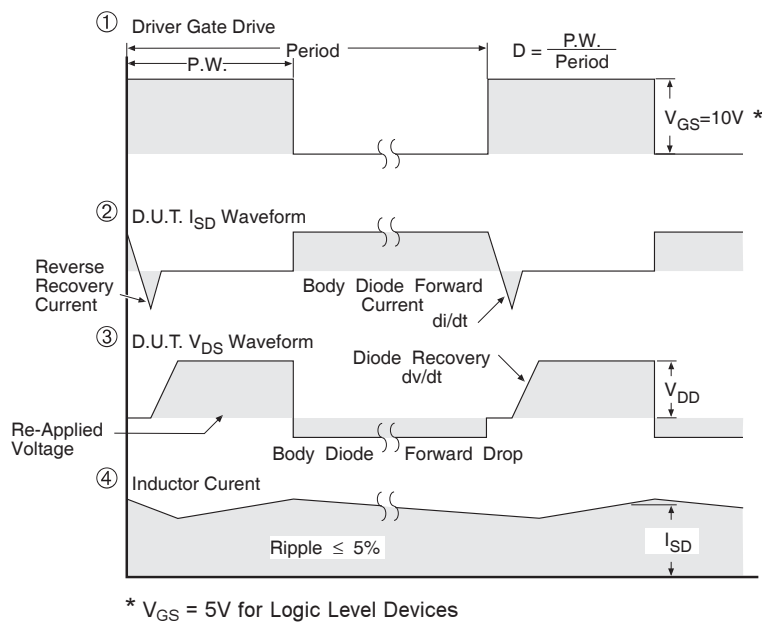
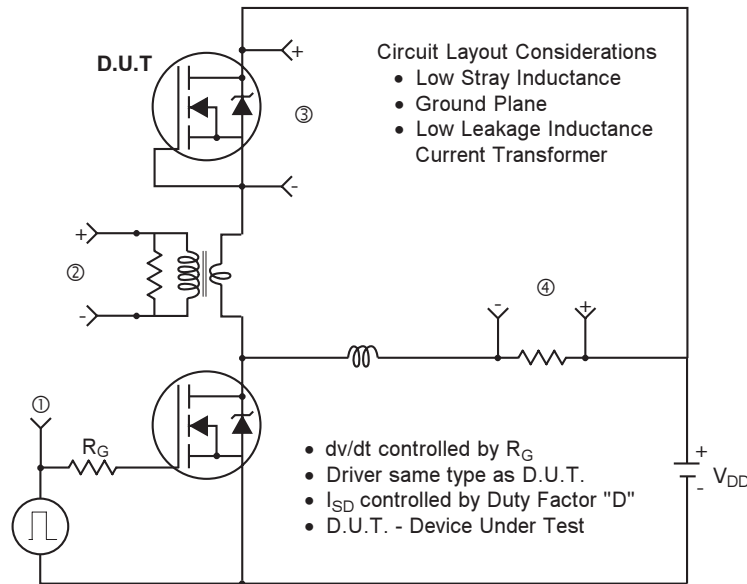
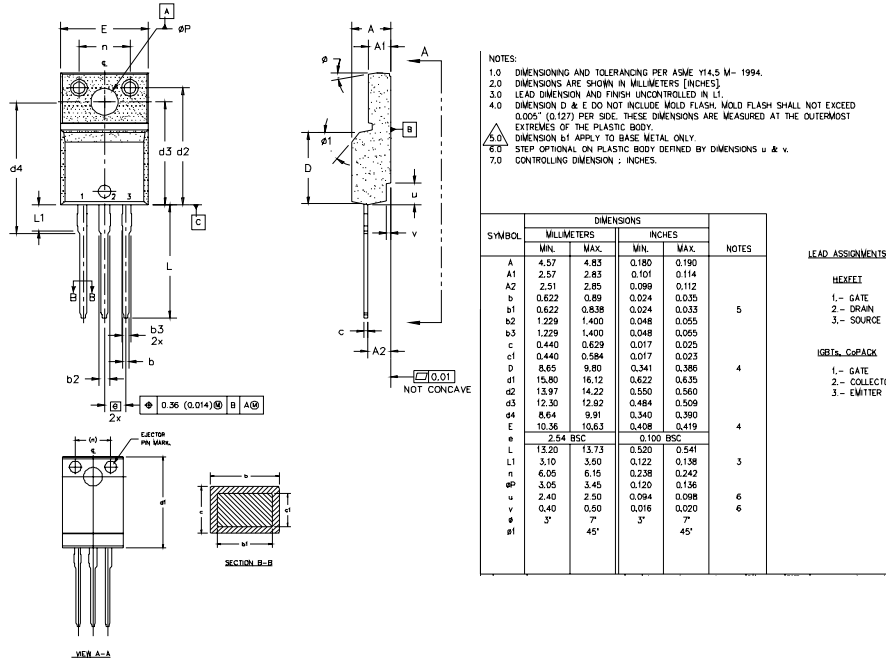


Fig 14. For N-Channel HEXFETS® Power MOSFETS

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TO-220 Full-Pak Package Outline

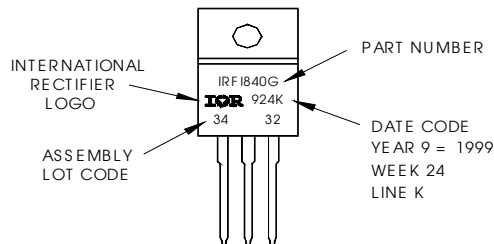
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TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.11/03

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>