International
IOR Rectifier

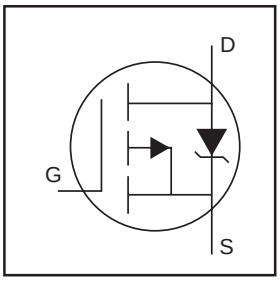
PD - 91749

PRELIMINARY

IRFR/U6215

HEXFET® Power MOSFET

- P-Channel
- 175°C Operating Temperature
- Surface Mount (IRFR6215)
- Straight Lead (IRFU6215)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = -150V

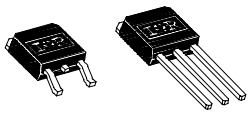
$R_{DS(on)}$ = 0.295Ω

I_D = -13A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



D-PAK TO-252AA I-PAK TO-251AA

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	-13	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	-9.0	
I_{DM}	Pulsed Drain Current ①⑥	-44	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑥	310	mJ
I_{AR}	Avalanche Current①⑥	-6.6	A
E_{AR}	Repetitive Avalanche Energy①⑥	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

5/11/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-150	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.295	Ω	V_{GS} = -10V, I_D = -6.6A ④
		—	—	0.58		V_{GS} = -10V, I_D = -6.6A ④T_J = 150°C
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	3.6	—	—	S	V_{DS} = -50V, I_D = -6.6A⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	µA	V_{DS} = -150V, V_{GS} = 0V
		—	—	-250		V_{DS} = -120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	66	nC	I_D = -6.6A
Q_{gs}	Gate-to-Source Charge	—	—	8.1		V_{DS} = -120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	35		V_{GS} = -10V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	V_{DD} = -75V
t_r	Rise Time	—	36	—		I_D = -6.6A
$t_{d(off)}$	Turn-Off Delay Time	—	53	—		R_G = 6.8Ω
t_f	Fall Time		37			R_D = 12Ω, See Fig. 10 ④⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑤
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	860	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	220	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-13	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	T_J = 25°C, I_S = -6.6A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	160	240	ns	T_J = 25°C, I_F = -6.6A
Q_{rr}	Reverse RecoveryCharge	—	1.2	1.7	µC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 14mH R_G = 25Ω, I_{AS} = -6.6A. (See Figure 12)

③ I_{SD} ≤-6.6A, di/dt ≤ -620A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

⑥ Uses IRF6215 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material)
For recommended footprint and soldering techniques refer to application note #AN-994

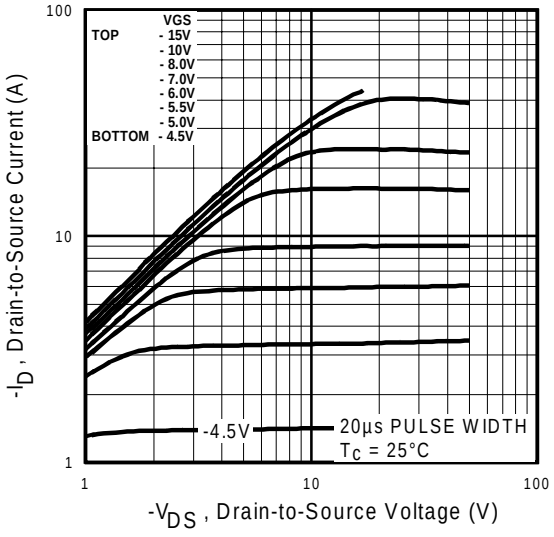


Fig 1. Typical Output Characteristics

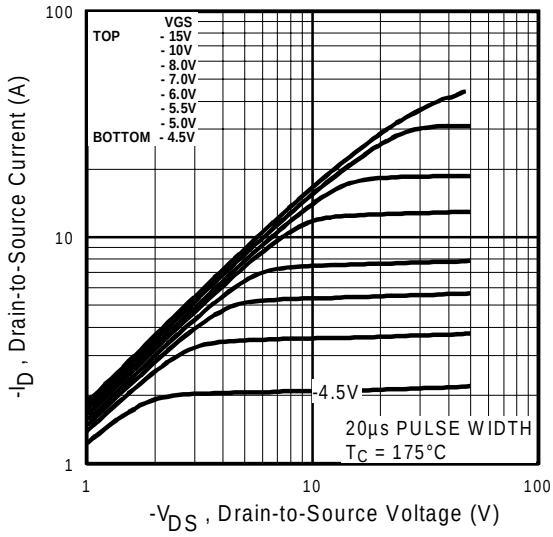


Fig 2. Typical Output Characteristics

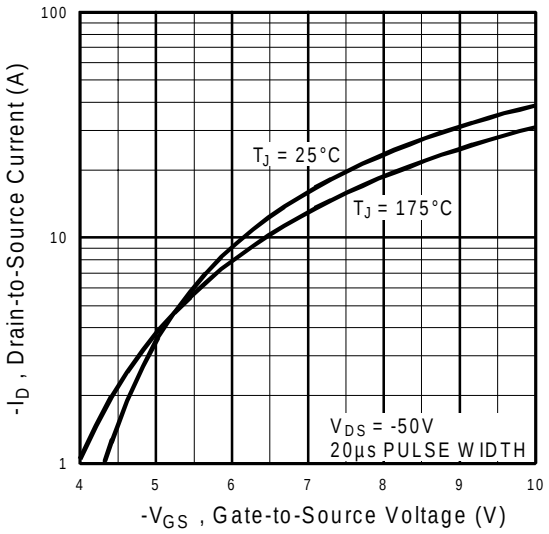


Fig 3. Typical Transfer Characteristics

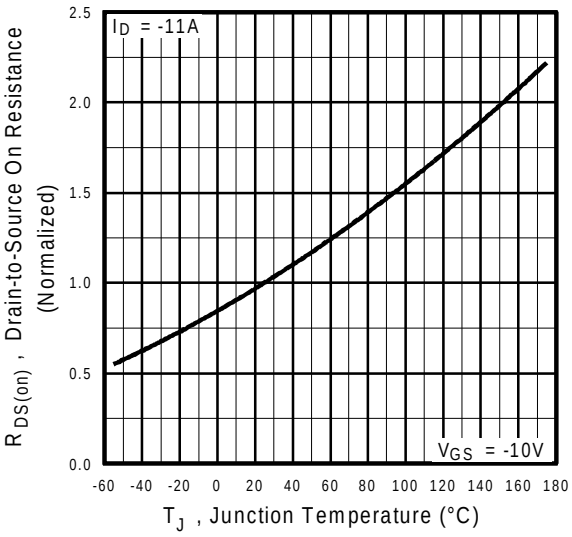


Fig 4. Normalized On-Resistance Vs. Temperature

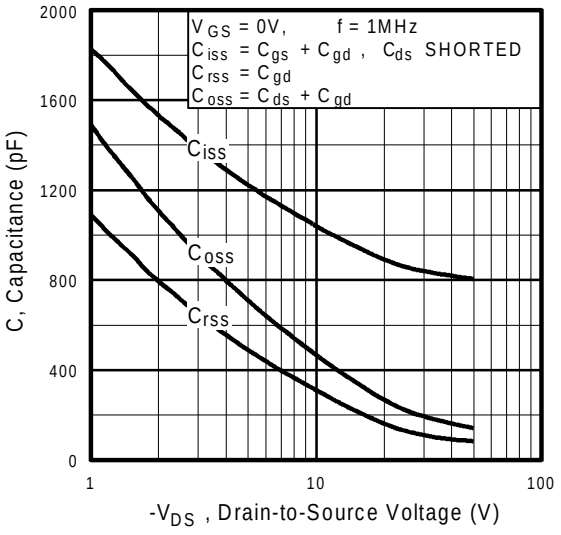


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

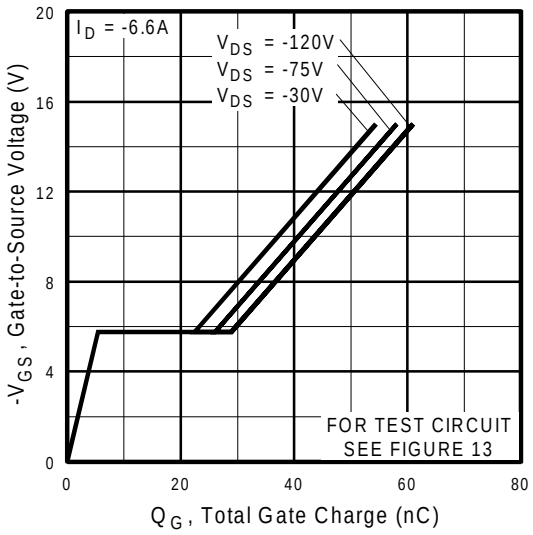


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

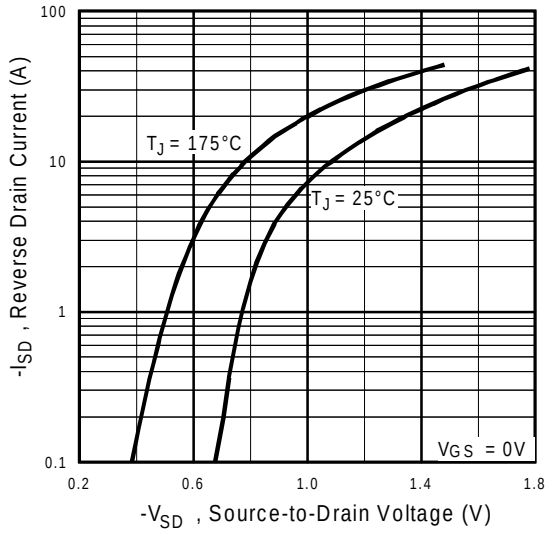


Fig 7. Typical Source-Drain Diode Forward Voltage

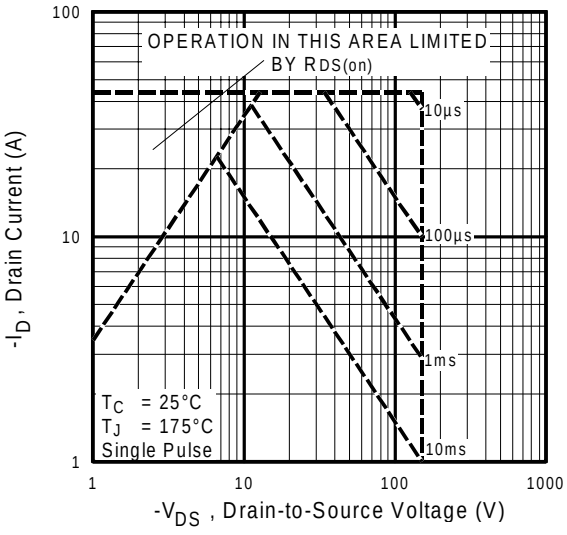


Fig 8. Maximum Safe Operating Area

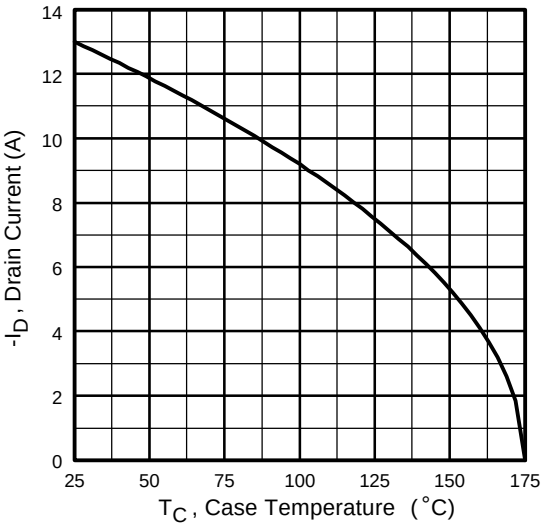


Fig 9. Maximum Drain Current Vs. Case Temperature

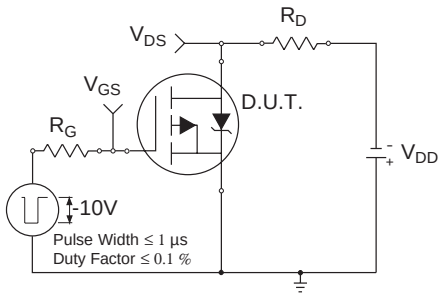


Fig 10a. Switching Time Test Circuit

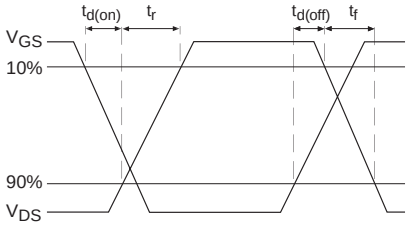


Fig 10b. Switching Time Waveforms

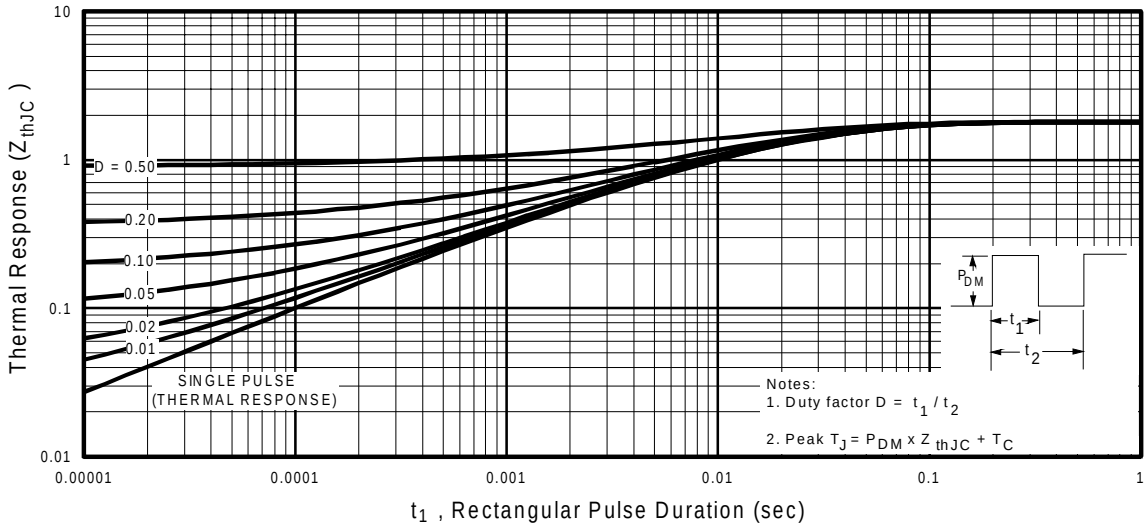


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

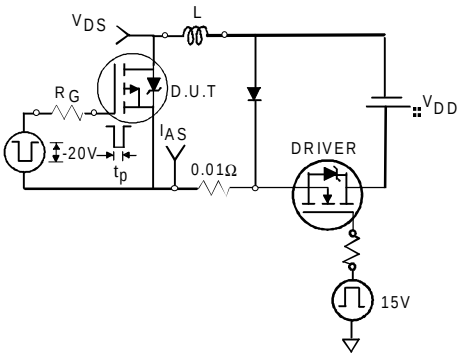


Fig 12a. Unclamped Inductive Test Circuit

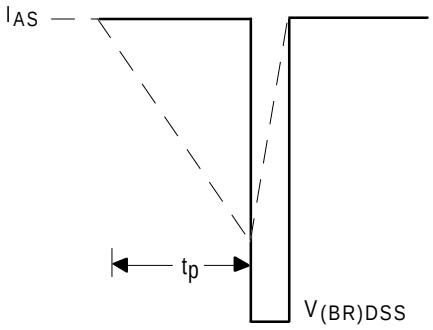


Fig 12b. Unclamped Inductive Waveforms

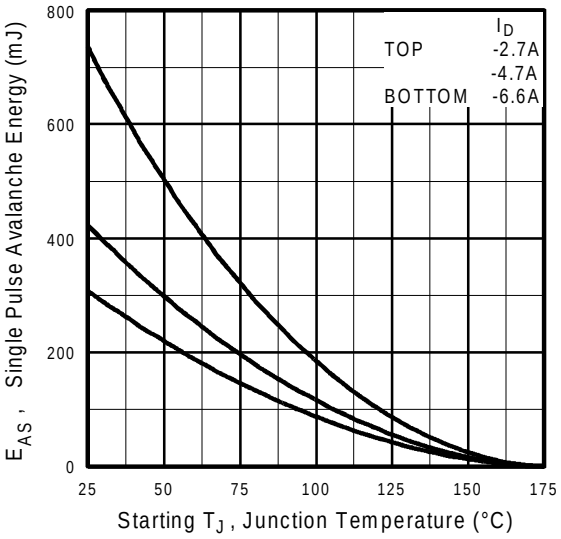


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

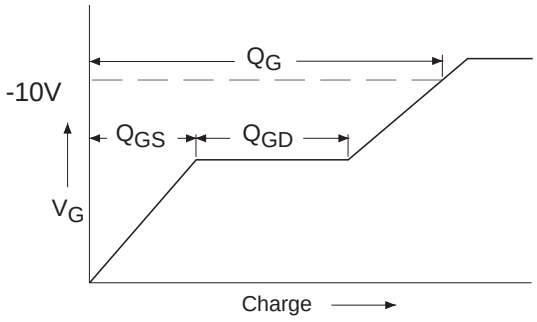


Fig 13a. Basic Gate Charge Waveform

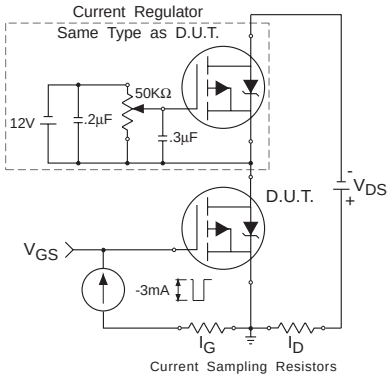
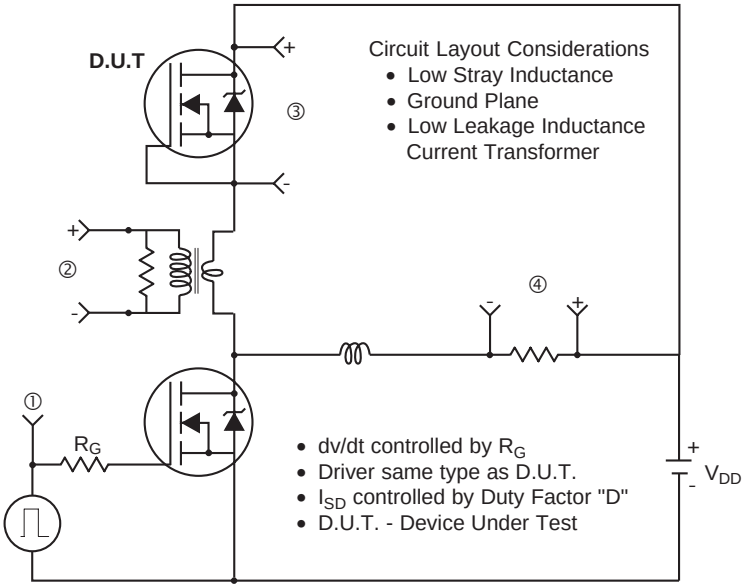
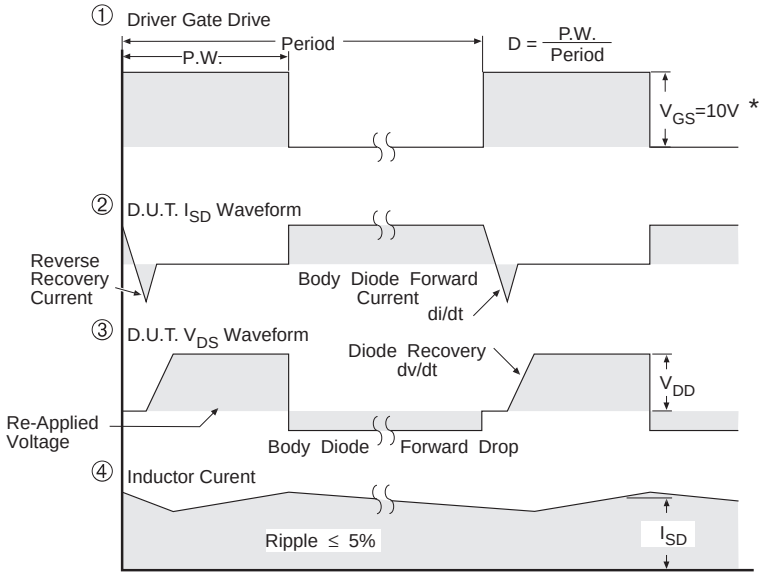


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

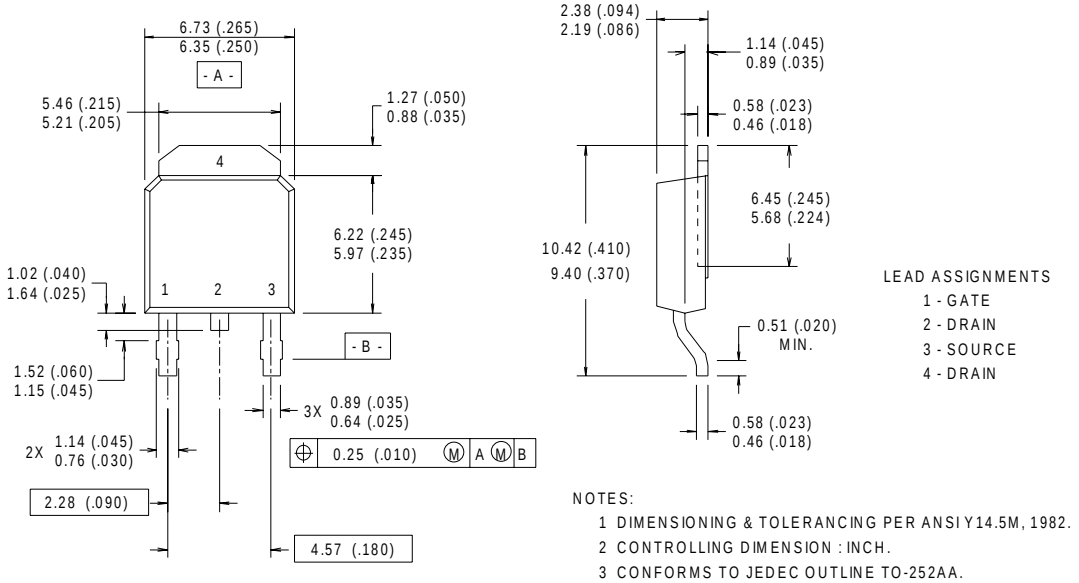


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-252AA Outline
Dimensions are shown in millimeters (inches)

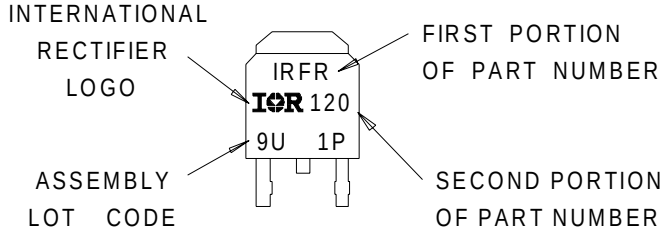


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

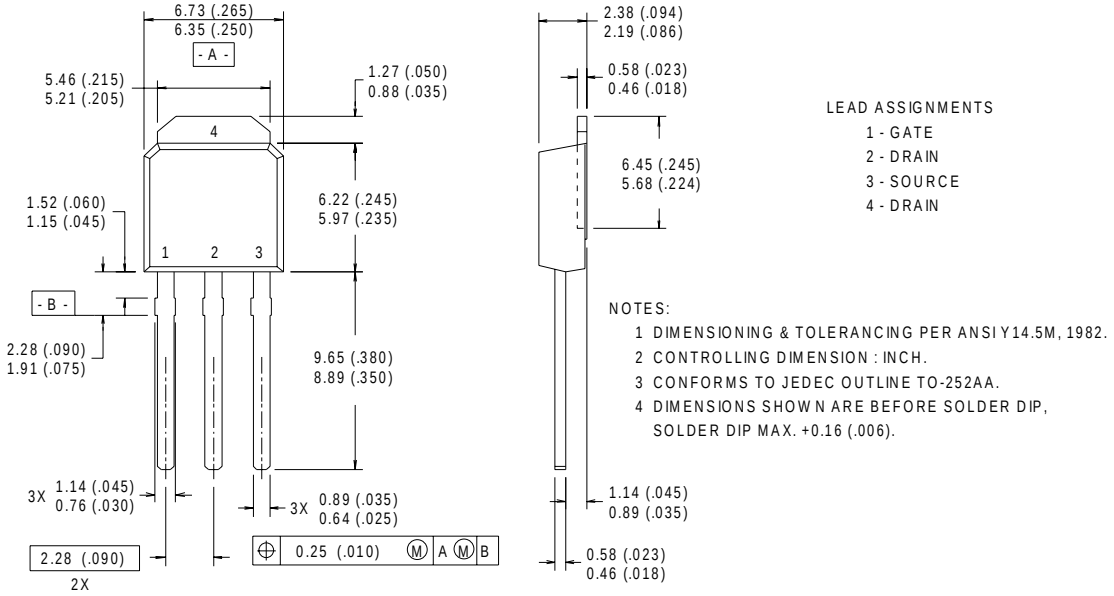
TO-252AA (D-PARK)

EXAMPLE : THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



Package Outline

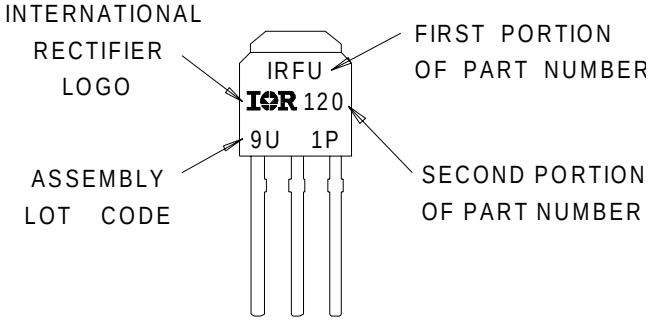
TO-251AA Outline
Dimensions are shown in millimeters (inches)



Part Marking Information

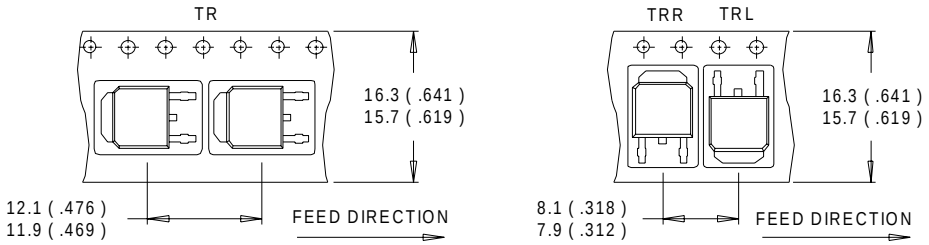
TO-251AA (I-PARK)

EXAMPLE : THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 9U1P

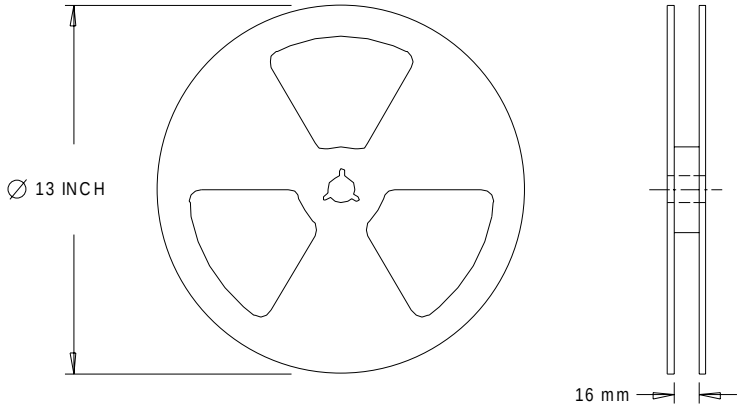


Tape & Reel Information

TO-252AA



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

International
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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR FAR EAST: 171 (K&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81 33 983 0086
IR SOUTHEAST ASIA: 315 Outram Road, #10-02 Tan Boon Liat Building, Singapore 16907 Tel: 65 221 8371

Data and specifications subject to change without notice.

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/