IS61LV2568L

256K x 8 HIGH-SPEED CMOS STATIC RAM

APRIL 2008

FEATURES

- High-speed access time: 8, 10 ns
- Operating Current: 50mA (typ.)
- Standby Current: 700µA (typ.)
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
  - 36-pin 400-mil SOJ
  - 44-pin TSOP (Type II)
- Lead-free available

DESCRIPTION

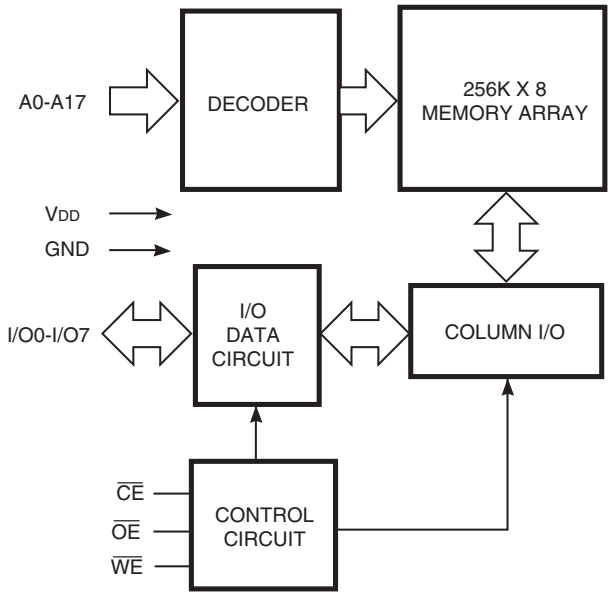
The *ISSI* IS61LV2568L is a very high-speed, low power, 262,144-word by 8-bit CMOS static RAM. The IS61LV2568L is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 36mW (max.) with CMOS input levels.

The IS61LV2568L operates from a single 3.3V power supply and all inputs are TTL-compatible.

The IS61LV2568L is available in 36-pin 400-mil SOJ and 44-pin TSOP (Type II) packages.

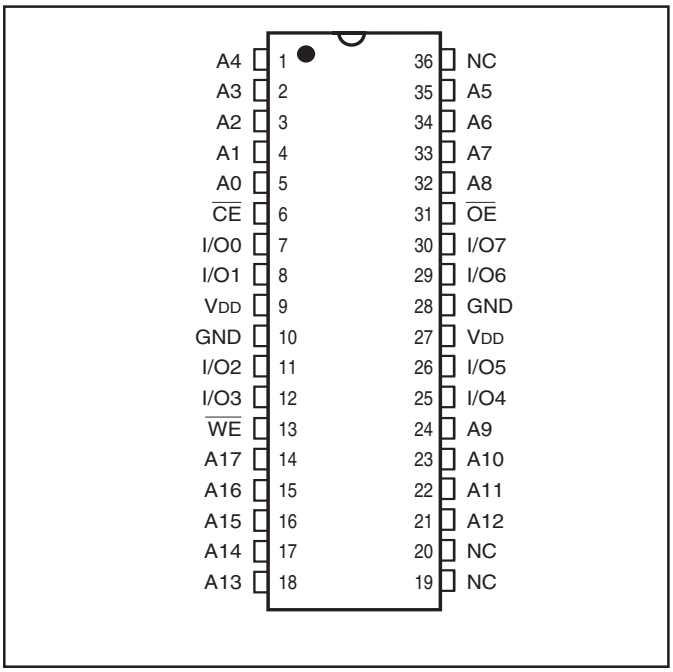
FUNCTIONAL BLOCK DIAGRAM



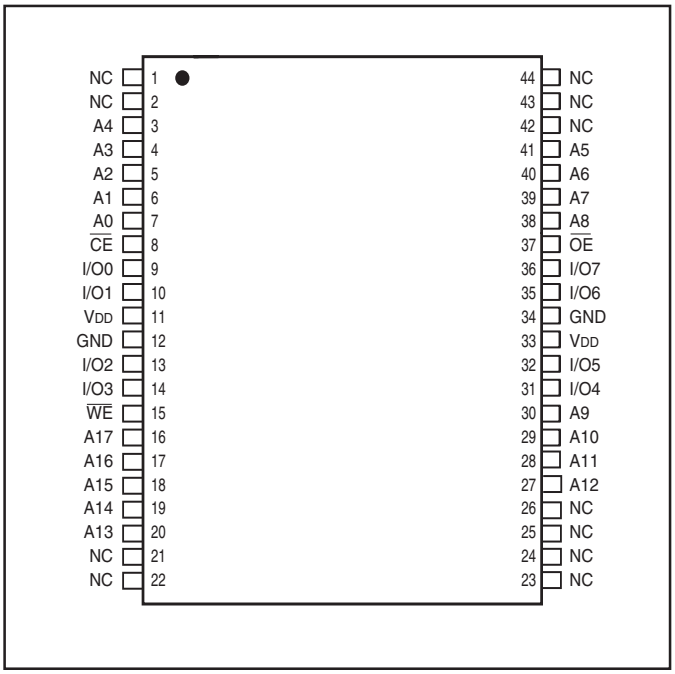
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PIN CONFIGURATION

36-Pin SOJ



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A17	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage with Respect to GND	–0.5 to +4.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_D	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V_{DD} (8ns)	V_{DD} (10 ns)
Commercial	0°C to +70°C	3.3V +10%,-5%	3.3V $\pm$ 10%
Industrial	–40°C to +85°C		3.3V $\pm$ 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL}(min) = –0.3V (DC); V_{IL}(min) = –2.0V (pulse width - 2.0 ns).
   V_{IH}(max) = V_{DD} + 0.3V (DC); V_{IH}(max) = V_{DD} + 2.0V (pulse width - 2.0 ns).

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	Unit
I_{CC}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL}	Com.	—	65	—	60	mA
		I_{OUT} = 0 mA, f = Max.	Ind.			—	65	
			typ.[2]	—	50	—	50	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max.,	Com.	—	30	—	25	mA
		V_{IN} = V_{IH} or V_{IL}	Ind.			—	30	
		$\overline{CE}$ ≥ V_{IH}, f = max						
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max.,	Com.	—	3	—	3	mA
		$\overline{CE}$ ≥ V_{DD} – 0.2V,	Ind.			—	4	mA
		V_{IN} ≥ V_{DD} – 0.2V, or	typ.[2]	—	700	—	700	µA
		V_{IN} ≤ 0.2V, f = 0						

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD}=3.3V, T_A=25^{0}C. Not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

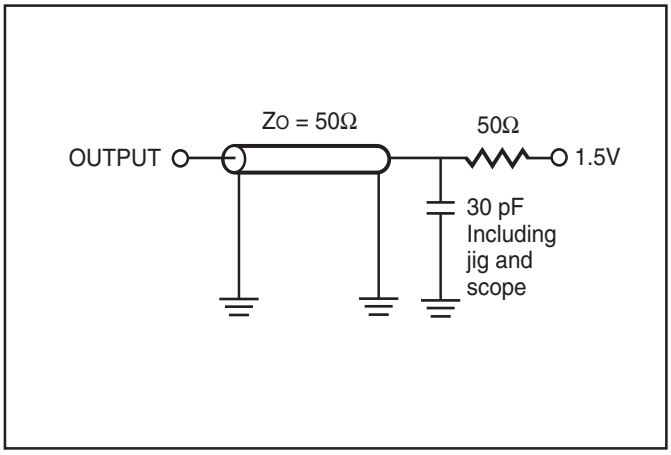


Figure 1

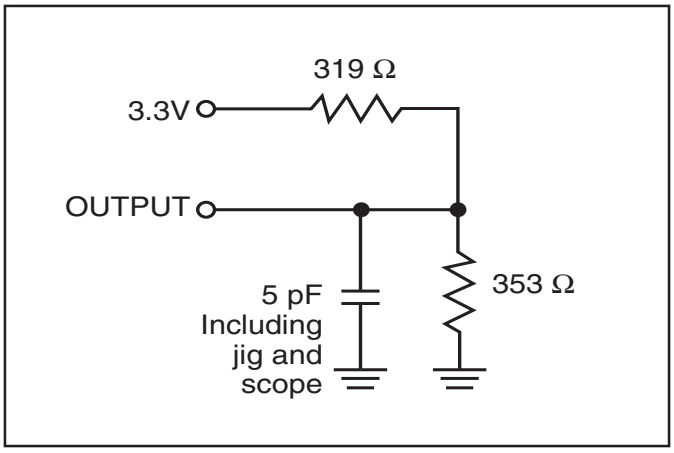


Figure 2

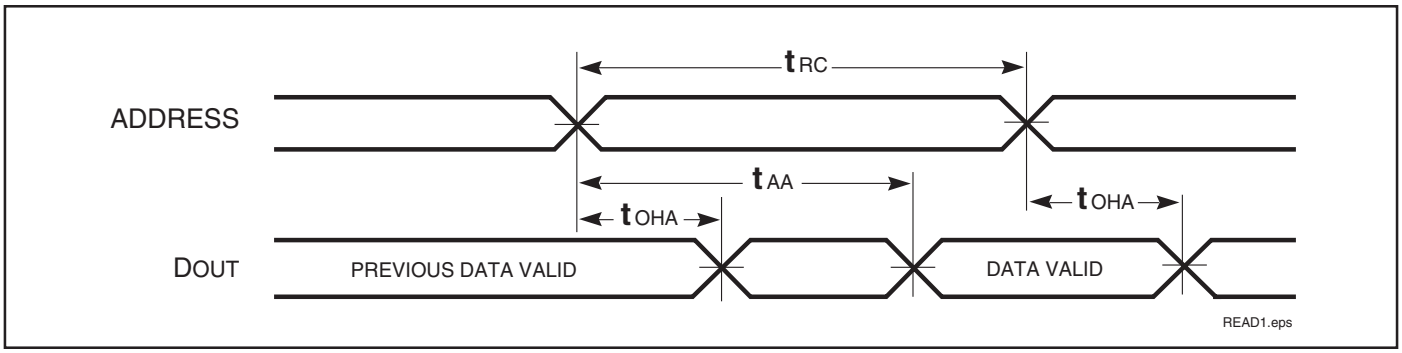
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		- 8 ns		-10 ns		
Symbol	Parameter	Min.	Max	Min.	Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	2.5	—	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	ns
t_{DOE}	$\overline{OE}$ Access Time	—	3.5	—	4	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	3.5	0	4	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3.5	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	3.5	0	4	ns

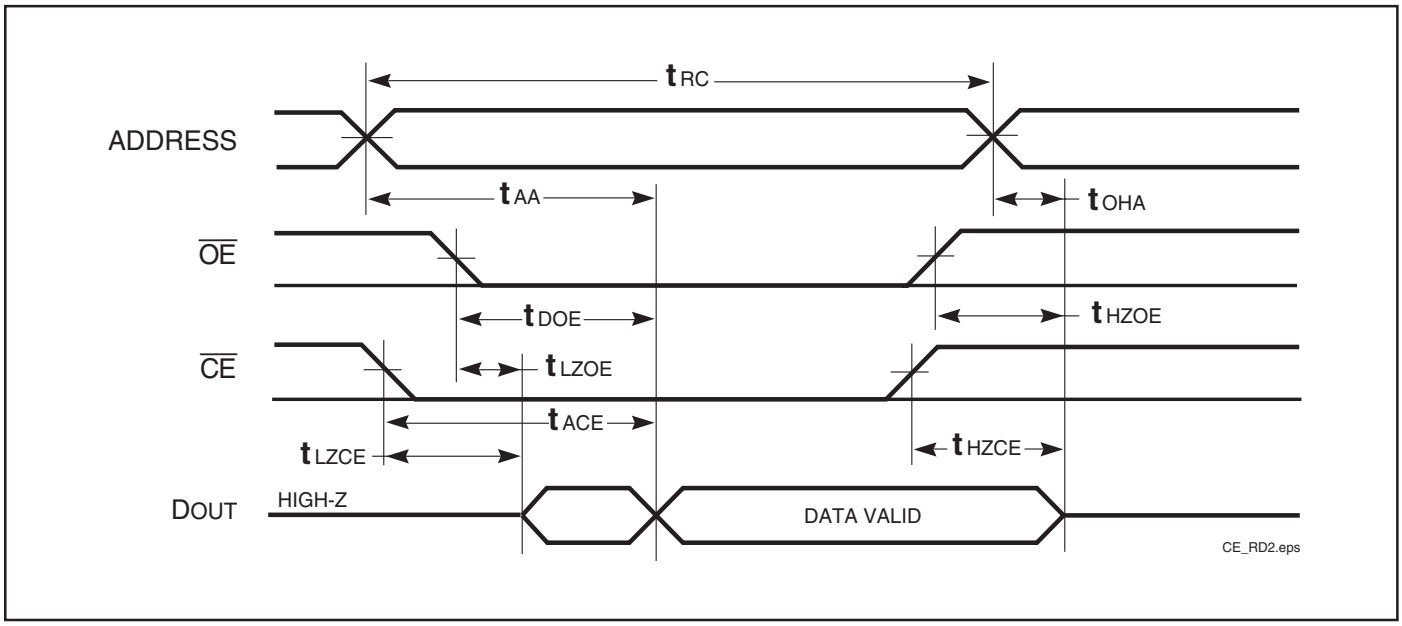
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL})



READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

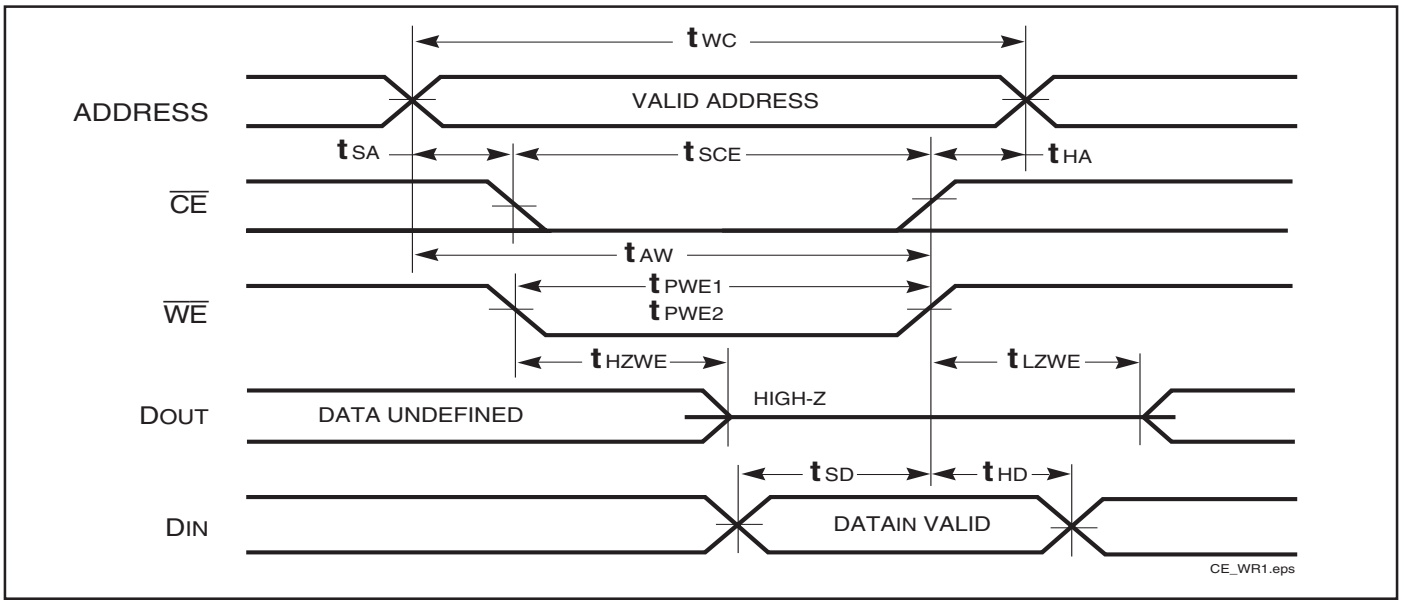
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

		- 8 ns		-10 ns		
Symbol	**Parameter**	**Min.**	**Max**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	8	—	ns
t_{AW}	Address Setup Time to Write End	7	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	6	—	7	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	6.5	—	8	—	ns
t_{SD}	Data Setup to Write End	4	—	5	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	3	—	4	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

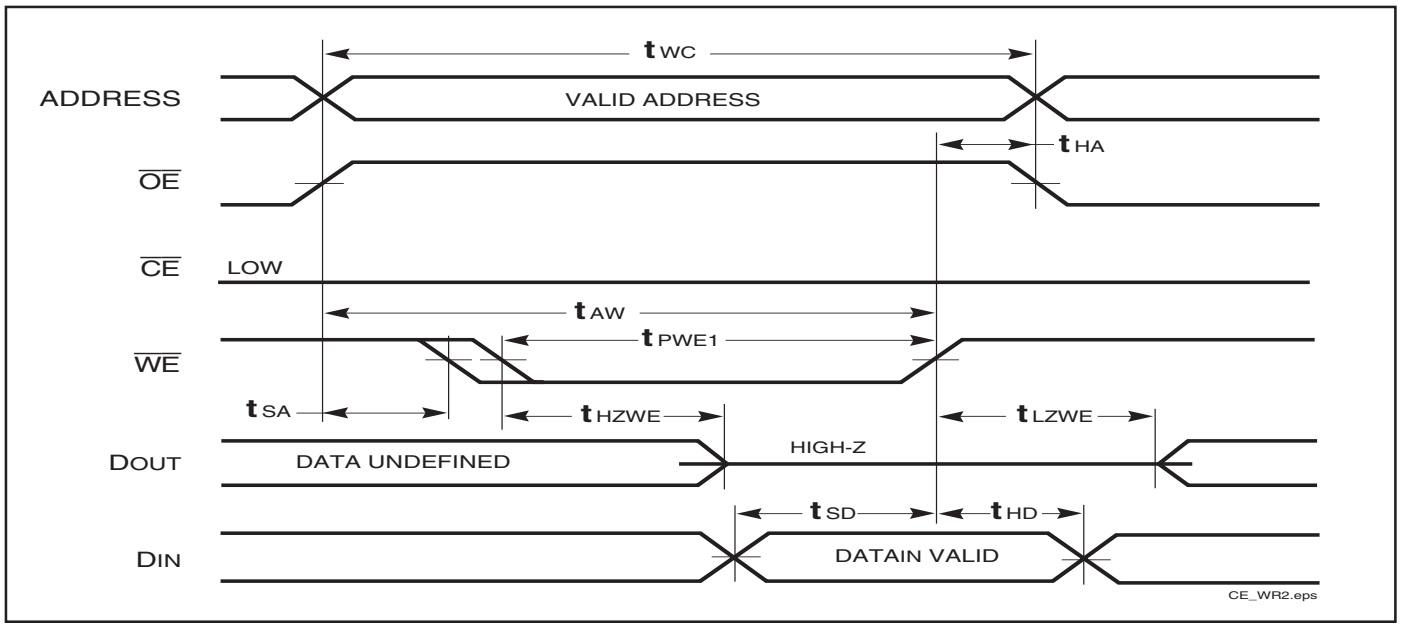


Note:

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

AC WAVEFORMS

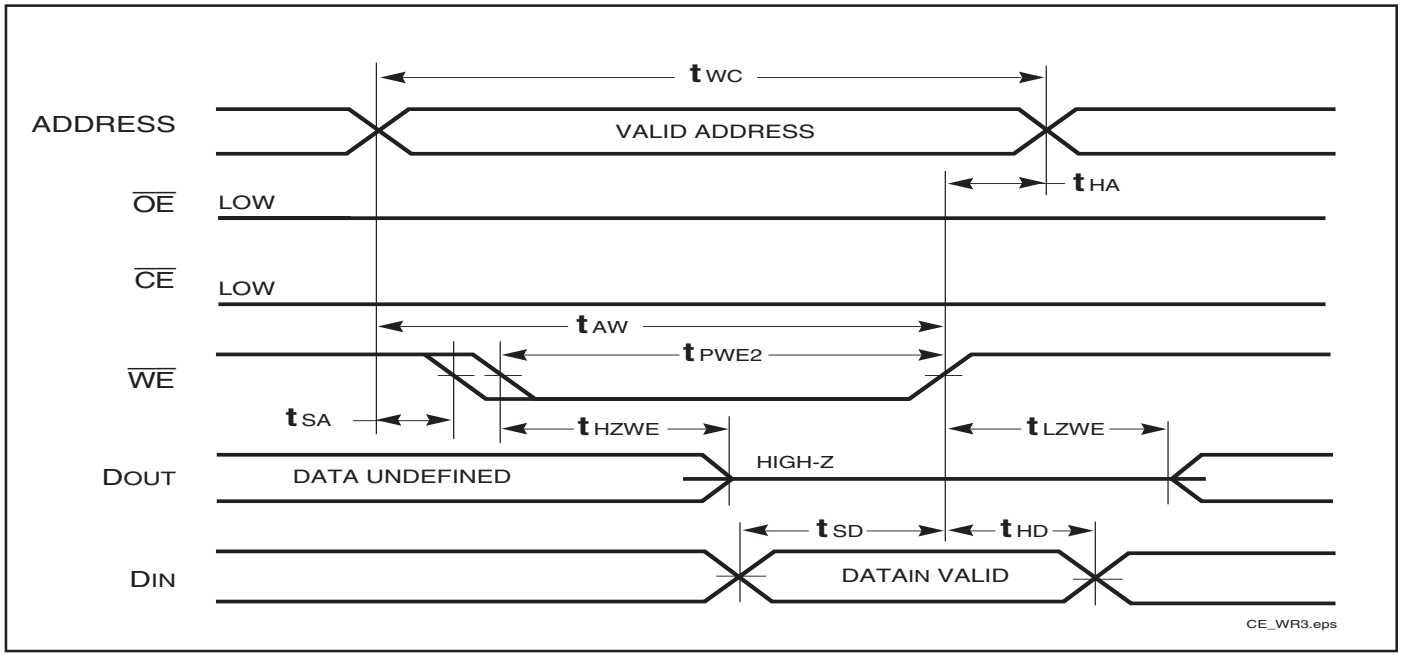
WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



Note:

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



Note:

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

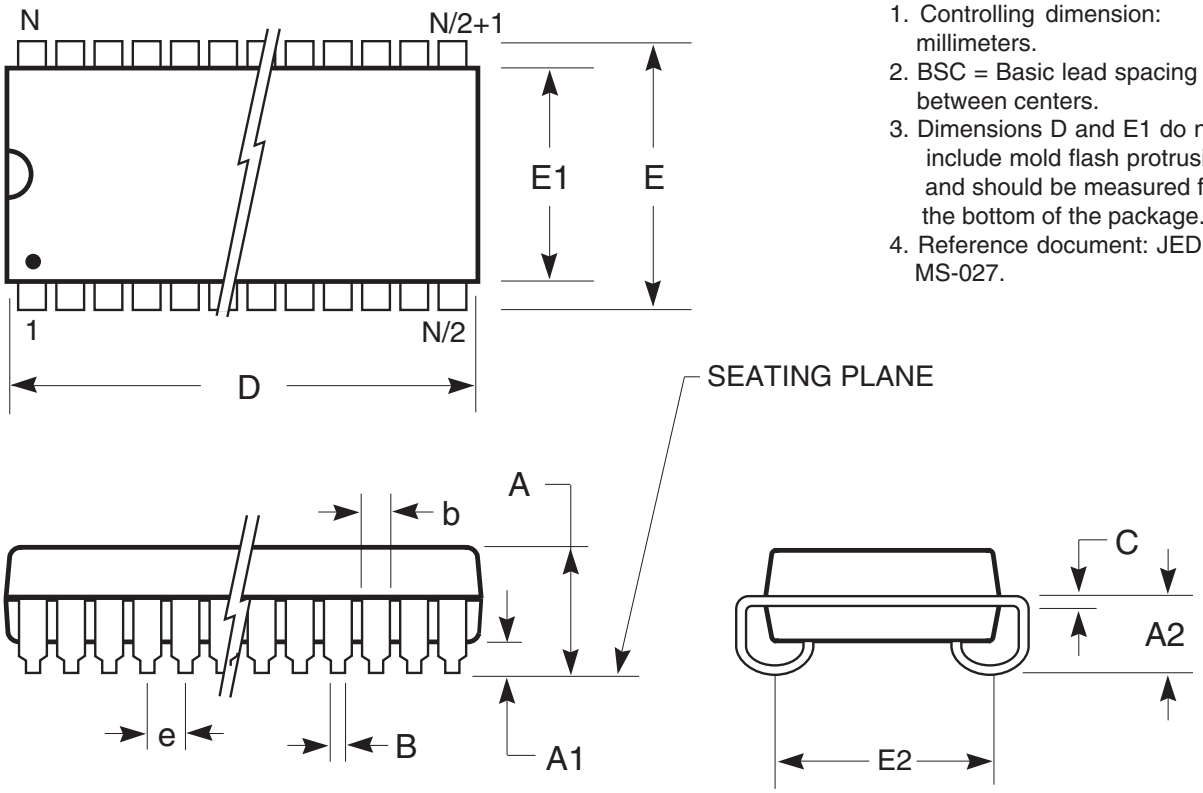
Speed (ns)	Order Part No.	Package
8	IS61LV2568L-8K	400-mil SOJ
	IS61LV2568L-8T	TSOP (Type II)
	IS61LV2568L-8TL	TSOP (Type II), Lead-free
10	IS61LV2568L-10T	TSOP (Type II)
	IS61LV2568L-10TL	TSOP (Type II), Lead-free

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61LV2568L-10KI	400-mil SOJ
	IS61LV2568L-10KLI	400-mil SOJ, Lead-free

PACKAGING INFORMATION

400-mil Plastic SOJ
Package Code: K



Notes:
1. Controlling dimension: millimeters.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Reference document: JEDEC MS-027.

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)		28				32				36		
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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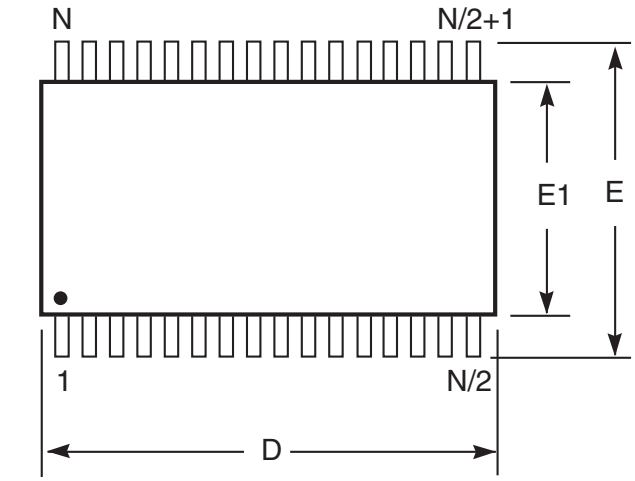
PACKAGING INFORMATION

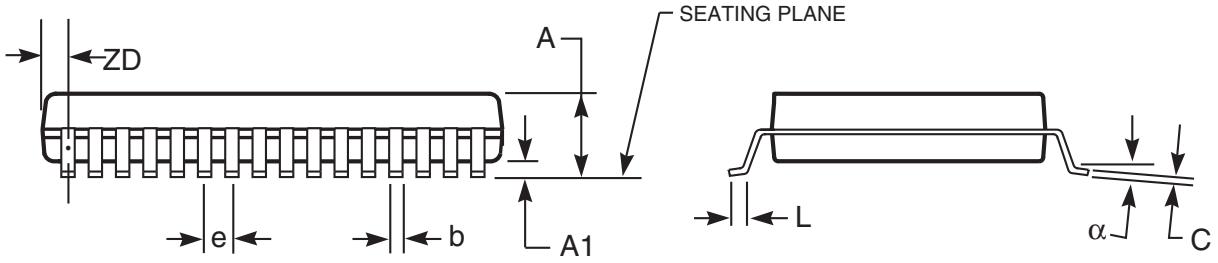
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)		40				42				44		
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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PACKAGING INFORMATION

Plastic TSOP
Package Code: T (Type II)





Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Ref. Std.												
No. Leads (N)		**32**				**44**				**50**		
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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