ITAxxB3

Bidirectional Transil™ array for data line protection

Features

- High surge capability Transil array: I_{PP} = 40 A (8/20 µs)
- Peak pulse power: 300 W (8/20 µs)
- Separated Input - Output
- Up to 9 bidirectional Transil functions
- Low clamping factor (V_{CL}/V_{BR}) at high current level
- Low leakage current
- ESD protection up to 15 kV

Complies with the following standards

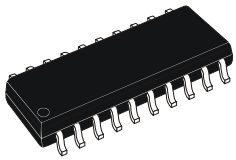
- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G- Method 3015-7: class 3B
  - 25 kV (human body model)

Applications

Differential data transmission lines protection, such as :

- RS-232
- RS-423
- RS-422
- RS-485

TM: Transil is a trademark of STMicroelectronics



SO-20

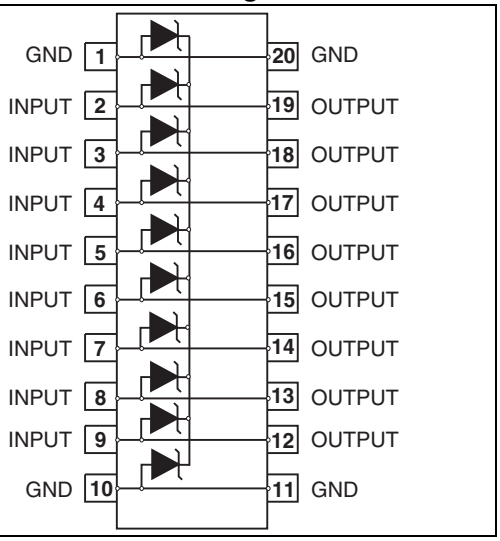
Description

Transil diode arrays provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages makes them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied IC's.

The ITA series combines high surge capability against energetic pulses with high voltage performance against ESD.

The separated input/output configuration of the device ensures improved protection against very fast transient overvoltage like ESD by elimination of the spikes induced by parasitic inductances created by external wiring.

Figure 1. Functional diagram



1 Characteristics

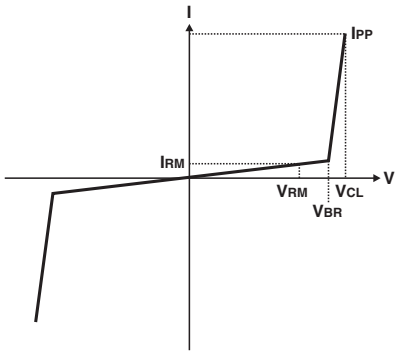
Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
P_{PP}	Peak pulse power (8/20 µs)(1)	T_j initial = T_{amb}	300	W
I_{PP}	Peak pulse current (8/20 µs)(1)	T_j initial = T_{amb}	40	A
I^2t	Wire I^2t value(1)		0.6	A^2s
T_j	Maximum operating junction temperature		125	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For surges greater than the specified maximum value, the I/O will first present a short-circuit and after an open circuit caused by the wire melting.

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop
C	Capacitance



Order code	V_{BR} @ I_R min. (1)		I_{RM} @ V_{RM} max.		V_{CL} @ I_{PP} 8/20 µs (1)		V_{CL} @ I_{PP} max. 8/20 µs (1)		αT max.	C max. (2)
	V	mA	µA	V	V	A	V	A	10^{-4}/°C	pF
ITA6V5B3	6.5	1	10	5	9.5	10	121	25	4	1100
ITA18B3	18	1	4	15	21	10	26	25	9	500
ITA25B3	25	1	4	24	31	10	36	25	12	420

1. Between I/O pin and ground.
2. Between two input pins at 0 V Bias, F = 1 MHz.

Figure 2. Pulse waveform

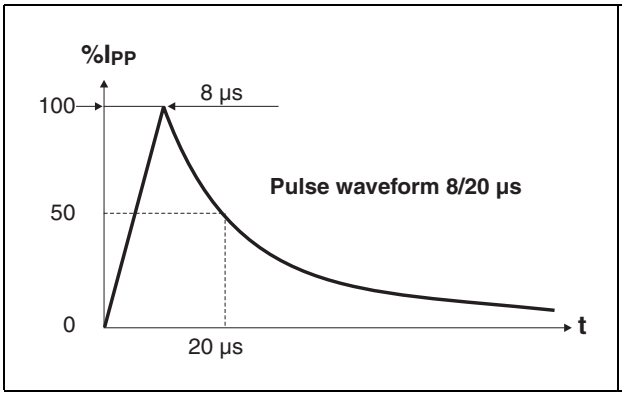


Figure 3. Typical peak pulse power versus exponential pulse duration

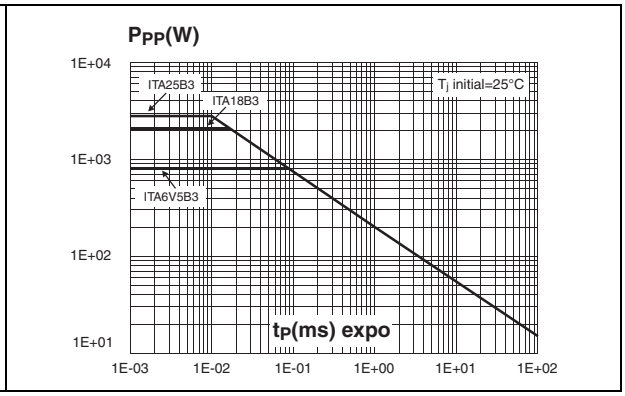


Figure 4. Clamping voltage versus peak pulse current (exponential waveform 8/20 µs)

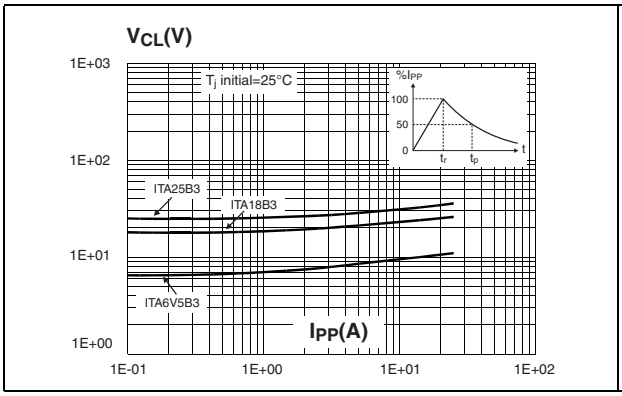


Figure 5. Peak current I_{DC} inducing open circuit of the wire for one input/output versus pulse duration (typical values)

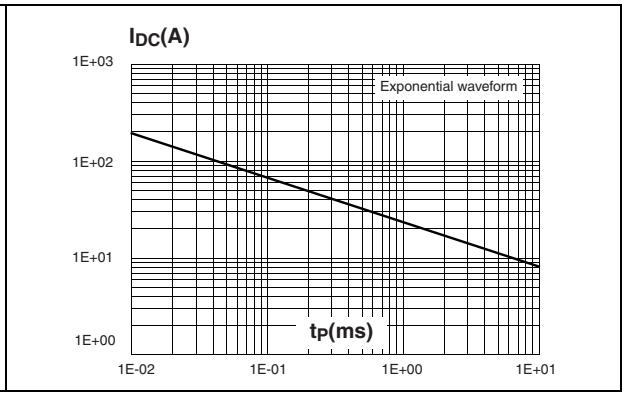


Figure 6. Junction capacitance versus reverse applied voltage for one input/output (typical values)

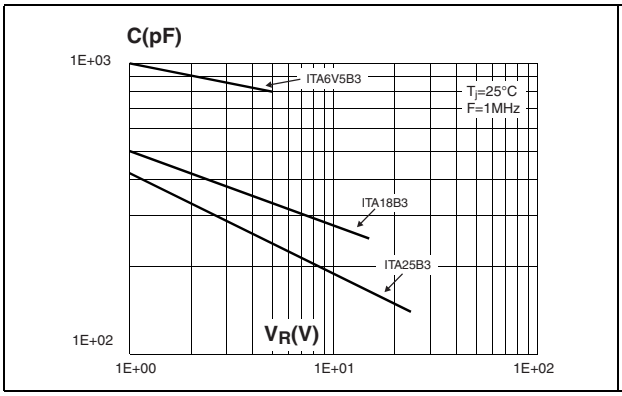
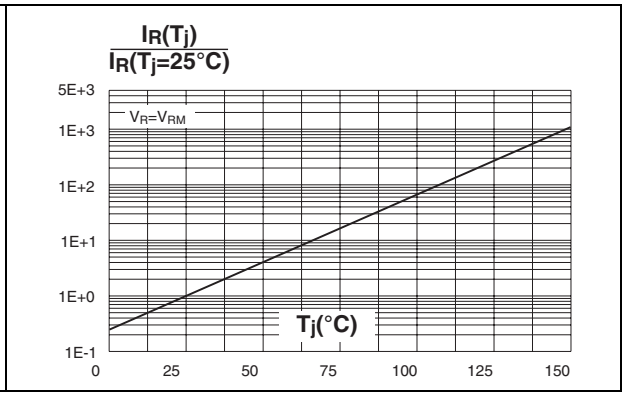


Figure 7. Relative variation of leakage current versus junction temperature



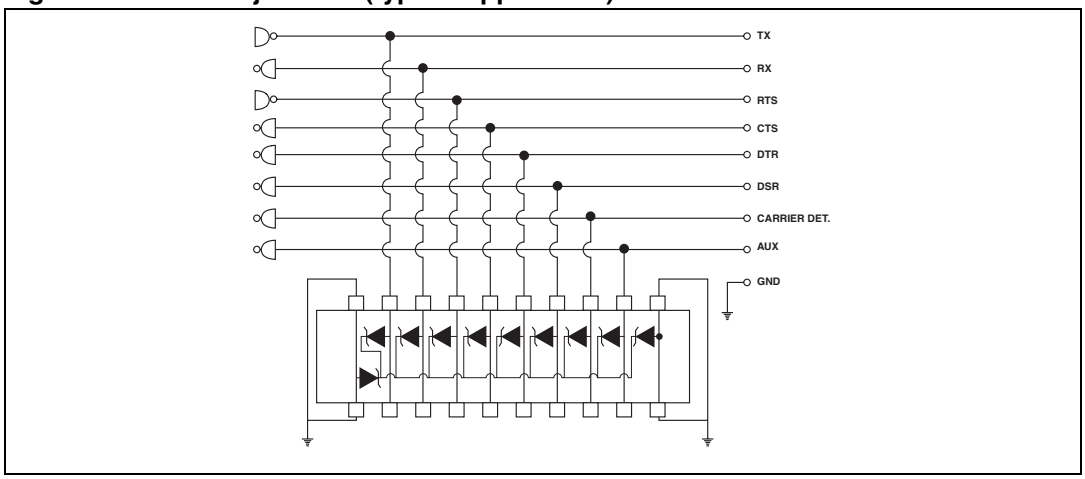
2 Application information

This monolithic Transil Array is based on 610 unidirectional Transils with a common cathode and can be configurated to offer up to 9 bidirectional functions. This imposes a maximum differential voltage between 2 input pins (see *Table 3*).

Table 3. Maximum differential voltages

Order code	Maximum differential voltage between two input pins at 25°C
ITA6V5B3	± 3.5 v
ITA18B3	± 9.0 v
ITA25B3	± 12.5 v

Figure 8. RS-232 junction (typical application)



2.1 Design advantage of ITAxxB3 used with 4-point structure

The ITAxxxB3 has been designed with a 4-point structure (separated Input/output) to efficiently protect against disturbances with very high di/dt rates, such as ESD.

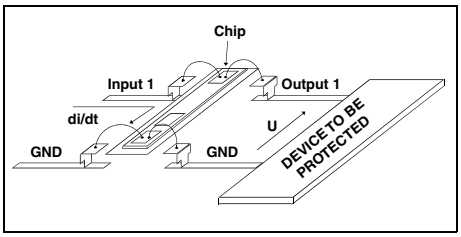
The purpose of this 4-point structure is to eliminate the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt).

Efficient protection depends not only on the component itself, but also on the circuit layout. The drawing given in figure 9 shows the layout to be used in order to take advantage of the 4-point structure of the ITAxxxB3.

With this layout, each line to be protected passes through the protection device.

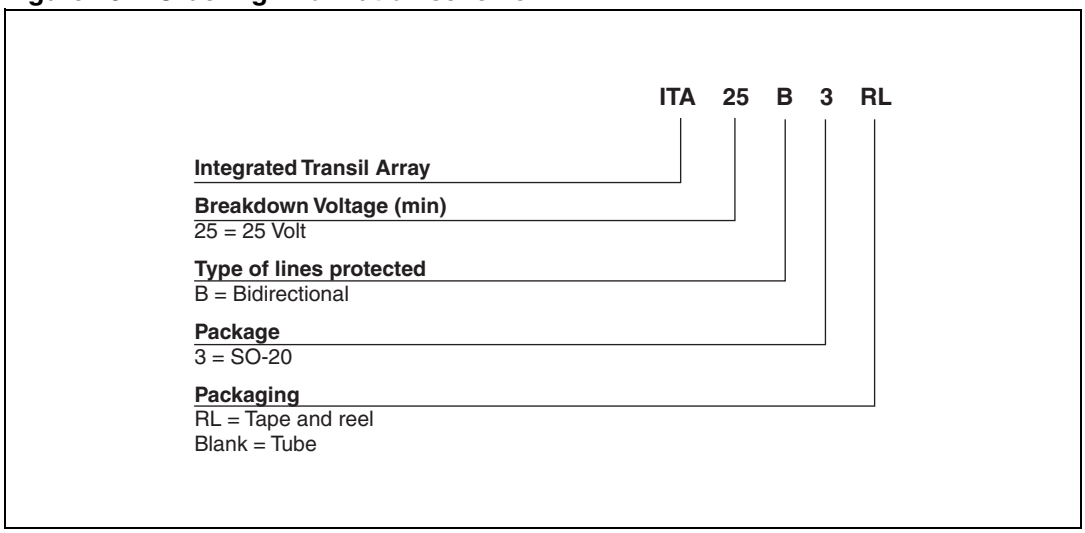
In this way, it realizes an interface between the data line and the circuit to be protected, guaranteeing an isolation between its inputs and outputs.

Figure 9. The 4 point structure



3 Ordering information scheme

Figure 10. Ordering information scheme

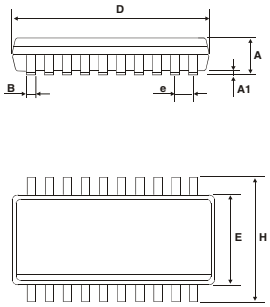


4 Package information

- Epoxy meets UL94, V0

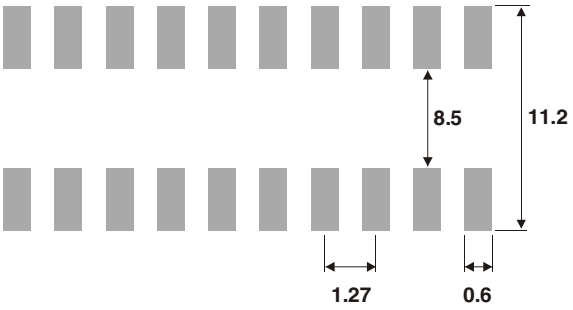
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 4. SO-20 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.092		0.104
A1	0.10		0.30	0.004		0.008
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13.0	0.484		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.029
L	0.40		1.27	0.016		0.050
K	8° (max)					

Figure 11. SO-20 footprint (dimensions in mm)



5 Ordering Information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ITA6V5B3	ITA6V5B3	SO-20	0.55 g	1000	Tube
ITA18B3	ITA18B3			1000	Tube
ITA18B3RL	ITA18B3			1000	Tape and reel
ITA25B3	ITA25B3			1000	Tube
ITA25B3RL	ITA25B3			1000	Tape and reel

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
13-Dec-2004	1	Initial release.
07-Nov-2007	2	Reformatted to current standards. Updated leakage current values in *Table 2* Updated pulse waveform parameters in *Figure 2*.

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