# EiceDRIVER™ APD 2ED4820-EM

## 48 V smart high-side MOSFET gate driver with SPI

## Features

- Extended supply voltage range: 20 - 70 V
- Two independent high-side gate driver outputs
- 1 A pull down, 0.3 A pull up for fast switch off/on
- Device control, configuration and diagnostic via SPI
- Low supply current in sleep mode $I_{BAT_Q}$ < 5 µA
- Supports back-to-back MOSFET topologies (common drain and common source)
- One bidirectional high or low-side analog current sense interface with configurable gain
- Configurable overcurrent/short circuit protection
- Gate undervoltage lock-out
- Safe state mode (both channels OFF) activated by direct input pin
- Ground loss detection



| Package | Marking |
|---|---|
| PG-TSDSO-24 | 2ED4820-EM |

## Potential applications

- 48 V battery protection switch
- 48 V input protection switch for DCDC converters, motor control unit etc.
- 48 V relay and fuse replacement

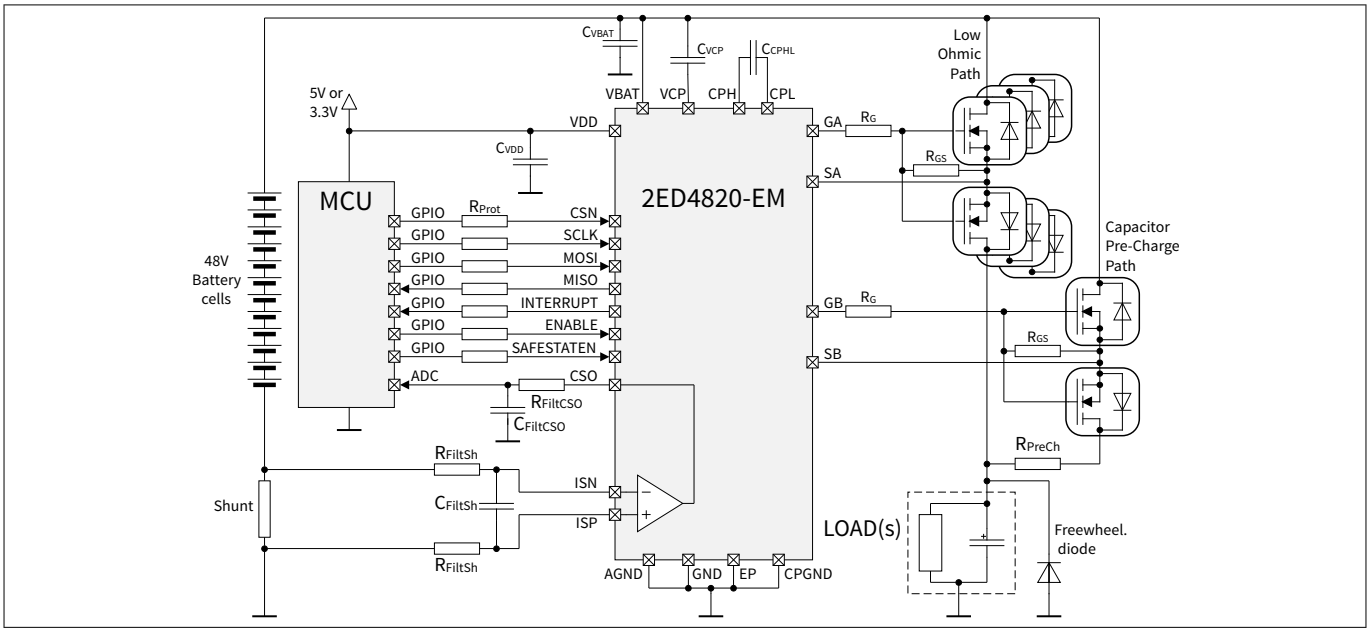



**Figure 1 48 V battery main switch application diagram**

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100 grade 1.

# Description

2ED4820-EM is a gate driver designed for high current 48 V automotive applications, with powerful gate outputs to drive many MOSFETs in parallel in order to minimize the conduction losses. It supports the back-to-back configuration, both common source and common drain structures, thanks to its two gate outputs.

In common source configuration, one gate output can be used to pre-charge highly capacitive loads.

2ED4820-EM generates the supply for the gate outputs based on an integrated one-stage charge pump with external pump and tank capacitors.

2ED4820-EM comes with an SPI interface, for easy configuration, diagnosis and control.

Several protection mechanisms are provided:

- Supply under- and overvoltage detection with configurable restart timer
- Charge pump undervoltage detection
- Gate to source undervoltage detection with immediate lock-out to prevent linear mode conduction of the MOSFETs
- Configurable drain to source overvoltage detection, which can also be deactivated
- Configurable overcurrent protection based on an analog current sense amplifier compatible for high-side or low-side shunt topologies
- Internal overtemperature warning and protection

An interrupt pin informs the MCU whenever one of these protections is triggered. Status registers can then be read by the MCU to understand what was the trigger for the notification.

The output of the current sense amplifier can be monitored by the MCU to implement additional protections, such as wire overtemperature.

In addition, 2ED4820-EM enables to implement an open load detection mechanism, checking the source voltage of the MOSFETs with respect to ground in the OFF state.

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# 1 Block diagram

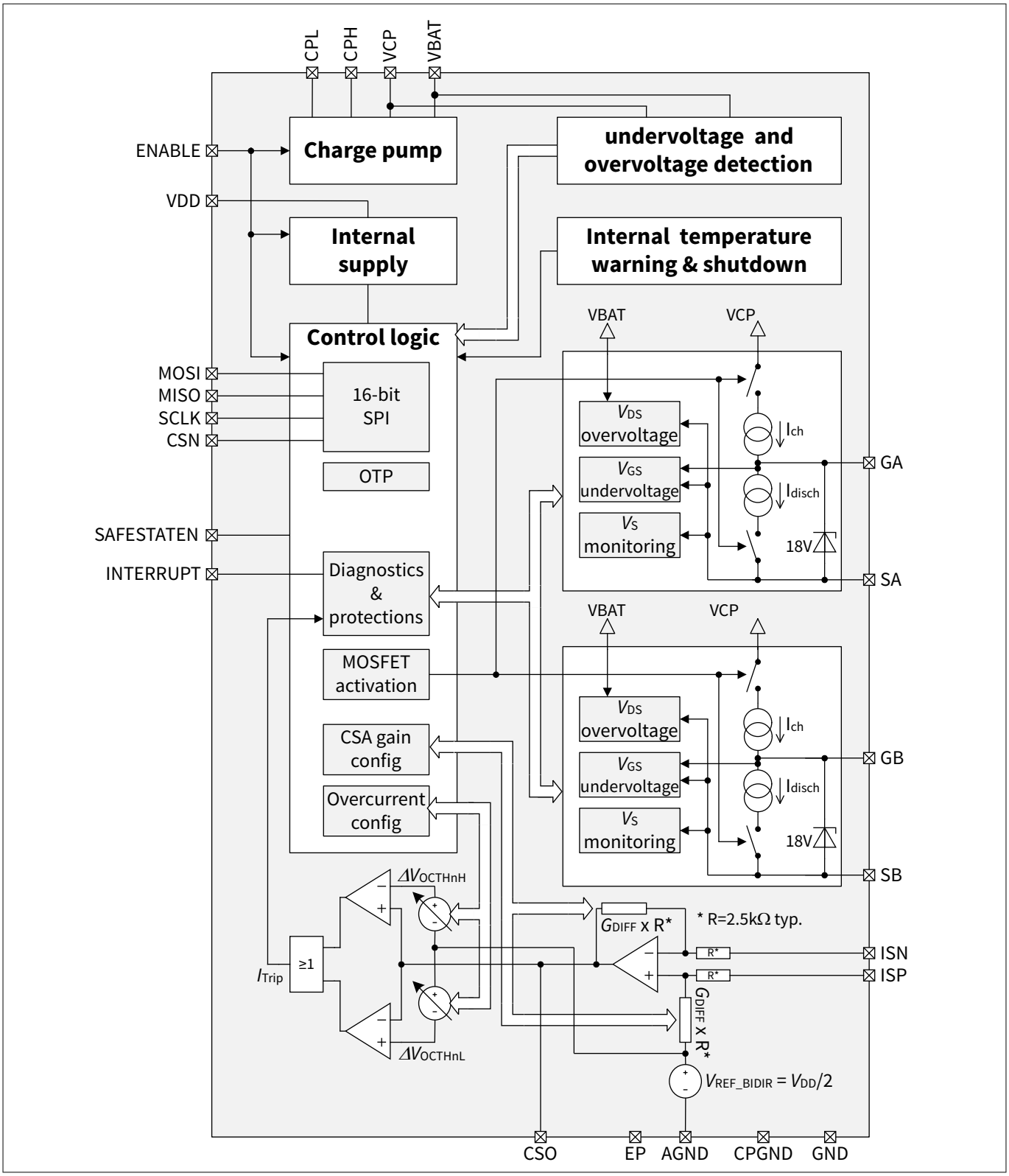



**Figure 2 Block diagram**

# 2 Pin configuration

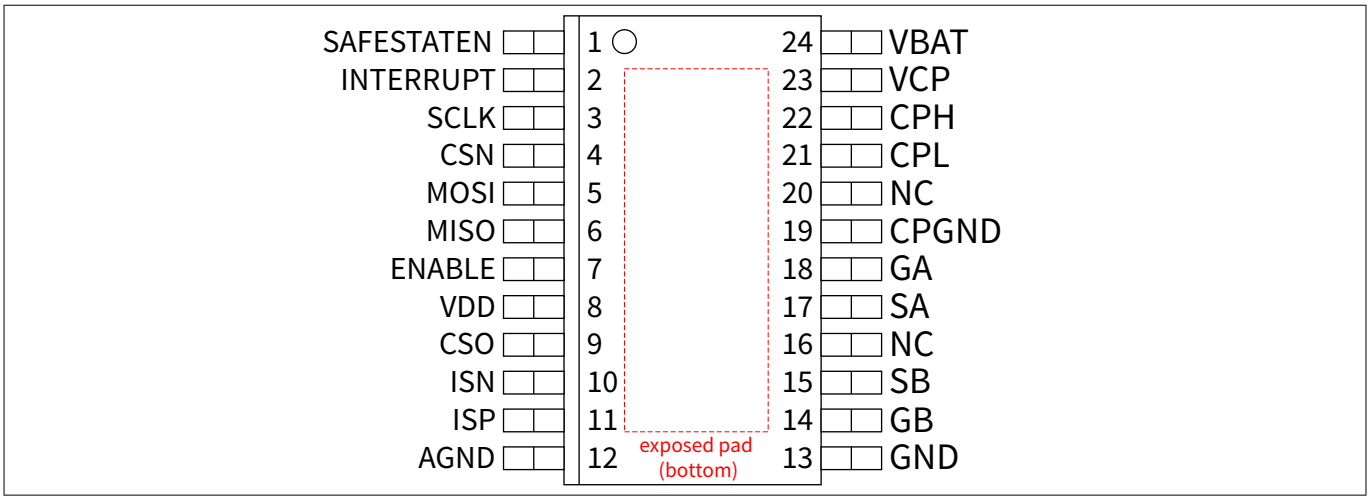



**Figure 3 Pin assignment**

**Table 1 Pin definitions and functions**

| Pin No. | Function | Symbol | Comment |
|---|---|---|---|
| 1 | µController | SAFESTATEN | Watchdog connection for safe state mode |
| 2 | µController | INTERRUPT | Interrupt signal output |
| 3 | SPI | SCLK | SPI clock input with internal pull-down |
| 4 | SPI | CSN | Chip select not with internal pull-up |
| 5 | SPI | MOSI | Master out slave in with internal pull-down |
| 6 | SPI | MISO | Master in slave out |
| 7 | µController | ENABLE | Switch device ON/OFF with internal pull-down |
| 8 | Supply | VDD | Main supply |
| 9 | µController | CSO | Current sense amplifier output |
| 10 | V-Sensing | ISN | Negative input for shunt voltage |
| 11 | V-Sensing | ISP | Positive input for shunt voltage |
| 12 | Supply | AGND | Analog GND |
| 13 | Supply | GND | Common usage ground |
| 14 | Gate connection | GB | Gate connection to channel B |
| 15 | Source connection | SB | Source connection to channel B |
| 16 | | NC | Not connected |
| 17 | Source connection | SA | Source connection to channel A |
| 18 | Gate connection | GA | Gate connection to channel A |
| 19 | Supply | CPGND | Charge pump GND |
| 20 | | NC | Not connected |
| 21 | ChargePump | CPL | Negative terminal of CP capacitor |
| 22 | ChargePump | CPH | Positive terminal of CP capacitor |

**(table continues...)**

**Table 1 (continued) Pin definitions and functions**

| Pin No. | Function | Symbol | Comment |
|---|---|---|---|
| 23 | ChargePump | VCP | Charge pump output / connection buffer capacitor |
| 24 | Supply | VBAT | 48 V supply |
| | | E.P. | Exposed pad (for cooling purpose only, do not use as electrical GND) |

# 3 General product characteristic

## 3.1 Absolute maximum ratings

Unless otherwise specified: $T_J$ = -40°C to +150°C; all voltages are referenced to GND.

**Table 2 Absolute maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| VBAT supply voltage | $V_{BAT}$ | -0.3 | – | 105 | V | 1) | PRQ-9 |
| Gate voltage with respect to Source | $V_{Gx_S}$ | -0.3 | – | 18 | V | 1) | PRQ-11 |
| Gate voltage with respect to VBAT | $V_{Gx_BAT}$ | -80 | – | 18 | V | 1) | PRQ-10 |
| Gate voltage | $V_{Gx}$ | -80 | – | $V_{CP}$ | V | 1) | PRQ-12 |
| Source voltage | $V_{Sx}$ | -90 | – | 105 | V | 1) | PRQ-199 |
| Source voltage with respect to VBAT | $V_{Sx_VBAT}$ | -90 | – | 2 | V | 1) | PRQ-92 |
| VDD logic supply voltage | $V_{DD}$ | -0.3 | – | 5.5 | V | 1) | PRQ-98 |
| **Current sense** | | | | | | | |
| ISP and ISN voltage | $V_{ISP}$, $V_{ISN}$ | -6 | – | 105 | V | 1) | PRQ-13 |
| ISP and ISN voltage with respect to VBAT | $V_{ISP_ISN_VBAT}$ | -105 | – | 2 | V | 1) | PRQ-542 |
| ISP and ISN differential voltage | $V_{ISP_ISN_DIFF}$ | -5 | – | 5 | V | 1) | PRQ-204 |
| CSO voltage | $V_{CSO}$ | -0.3 | – | $V_{DD}$+0.3 | V | 1) | PRQ-97 |
| **Logic** | | | | | | | |
| Logic input voltages (SCLK, CSN, MOSI, SAFESTATEN, ENABLE) | $V_{SCLK}$, $V_{CSN}$, $V_{MOSI}$, $V_{SAFESTATEN}$, $V_{ENABLE}$ | -0.3 | – | $V_{DD}$+0.3 | V | 1) | PRQ-94 |
| Logic output voltages (MISO, INTERRUPT) | $V_{MISO}$, $V_{INTERRUPT}$ | -0.3 | – | $V_{DD}$+0.3 | V | 1) | PRQ-96 |
| **Charge pump** | | | | | | | |
| Charge pump voltage (VCP) | $V_{CP}$ | -0.3 | – | 105 | V | 1) | PRQ-337 |
| Charge pump voltage (VCP) with respect to VBAT | $V_{CP_VBAT}$ | -0.3 | – | 18 | V | 1) | PRQ-400 |
| Charge pump voltage (CPL) | $V_{CPL}$ | -0.3 | – | $V_{BAT}$ | V | 1) | PRQ-95 |
| Charge pump voltage (CPH) | $V_{CPH}$ | $V_{BAT}$-0.3 | – | $V_{CP}$+0.3 | V | 1) | PRQ-261 |

**(table continues...)**

**Table 2 (continued) Absolute maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Charge pump ground and analog ground voltage | $V_{CPGND}$, $V_{AGND}$ | -0.3 | – | 0.3 | V | 1) | PRQ-205 |
| **Temperature** | | | | | | | |
| Junction temperature | $T_J$ | -40 | – | 150 | °C | 1) | PRQ-17 |
| Storage temperature | $T_{STG}$ | -55 | – | 150 | °C | 1) | PRQ-19 |
| **ESD susceptibility** | | | | | | | |
| ESD susceptibility at all pins (HBM) | $V_{ESD_HBM1}$ | -2 | – | 2 | kV | 1) 2) HBM | PRQ-20 |
| ESD susceptibility of VBAT pin versus GND (HBM) | $V_{ESD_HBM2}$ | -4 | – | 4 | kV | 1) 2) HBM | PRQ-100 |
| ESD susceptibility at all pins (CDM) | $V_{ESD_CDM}$ | -500 | – | 500 | V | 1) 3) CDM | PRQ-401 |
| ESD susceptibility at corner pins (CDM) (pins 1, 12, 13, 24) | $V_{ESD_CDM}$ | -750 | – | 750 | V | 1) 3) CDM | PRQ-414 |

1) Not subject to production test, specified by design.
2) ESD susceptibility, human body model "HBM", according to AEC Q100-002
3) ESD susceptibility, charged device model "CDM", according to AEC Q100-011

## 3.2 Functional range

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; all voltages are referenced to GND; positive current flowing into pin.

**Table 3 Functional range**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| VBAT supply voltage range for normal operation | $V_{BAT(NORM)}$ | 24 | – | 54 | V | – | PRQ-101 |
| VBAT extended supply voltage range | $V_{BAT(EXT)}$ | 20 | – | 70 | V | Parameter deviations possible | PRQ-102 |
| VBAT supply transients slew rate | $dV_{BAT}/dt$ | -10 | – | 10 | V/µs | 1) | PRQ-397 |
| Logic supply voltage (VDD) | $V_{DD}$ | 3.0 | – | 5.5 | V | – | PRQ-105 |
| VDD logic supply transients slew rate | $dV_{DD}/dt$ | -10 | – | 10 | V/µs | 1) | PRQ-398 |
| SPI logic input voltage | $V_{SCLK}$, $V_{CSN}$, $V_{MOSI}$ | 0 | – | $V_{DD}$ | V | – | PRQ-106 |

**(table continues...)**

**Table 3 (continued) Functional range**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Source voltage transients slew rate | $dV_{Sx}/dt$ | -70 | – | 70 | V/µs | 1) | PRQ-399 |
| Logic input voltage | $V_{SAFESTATEN}$, $V_{ENABLE}$ | 0 | – | $V_{DD}$ | V | – | PRQ-107 |
| CSO output current | $I_{CSO}$ | -4 | – | 0 | mA | – | PRQ-355 |
| ISP, ISN input voltage | $V_{ISP}$, $V_{ISN}$ | -2 | – | VBAT + 2 | V | – | PRQ-508 |
| ISP, ISN common mode slew rate | $V_{SENSE_COMMON}$ | -70 | – | 70 | V/µs | 1) | PRQ-491 |
| ISP, ISN differential mode slew rate | $V_{SENSE_DIFFERENTIAL}$ | -5 | – | 5 | V/µs | 1) | PRQ-492 |
| Junction temp | $T_J$ | -40 | – | 150 | °C | – | PRQ-18 |

1) Not subject to production test, specified by design.

## 3.3 Thermal resistance

$T_J$ = -40°C to +150°C.

**Table 4 Thermal resistance**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to case, TA = -40°C | $R_{thJC_cold}$ | – | 4 | – | K/W | 1) | PRQ-99 |
| Junction to case, TA = 85°C | $R_{thJC_hot}$ | – | 5 | – | K/W | 1) | PRQ-71 |
| Junction to ambient, TA = -40°C | $R_{thJA_cold_2s2p}$ | – | 38 | – | K/W | 1) 2) | PRQ-72 |
| Junction to ambient, TA = 85°C | $R_{thJA_hot_2s2p}$ | – | 31 | – | K/W | 1) 2) | PRQ-73 |

1) Not subject to production test, specified by design.
2) Specified RthJA value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. The device is dissipating 1 W power.

# 4 General product description

## 4.1 Power supply

The device is externally supplied by two pins: VDD and VBAT.

The gate driver requires multiple power supplies:

- VBAT supplies the charge pump and parts of the gate control block
- VDD supplies SPI interface, internal logic, protection functions as well as the current sense interface
- Internally generated charge pump voltage VCP supplies the gate control block, $V_{DS}$ and $V_{GS}$ detection blocks and current sense amplifier

## 4.2 Operation mode

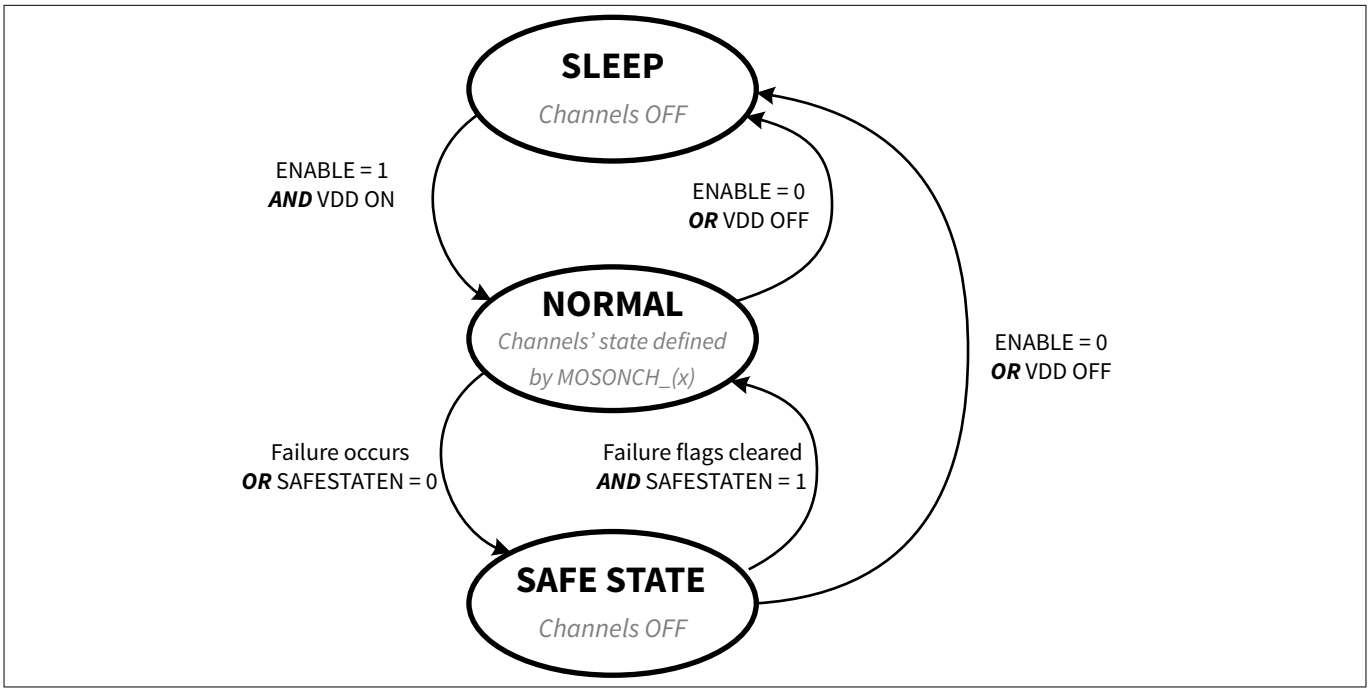



**Figure 4 Operation modes overview**

### 4.2.1 Normal mode

The device enters normal mode after the SPI setup time $t_{SET_SPI}$, if the microcontroller sets the pin ENABLE to high.

In normal mode, the MOSFET gate driver is enabled and can be configured through the SPI interface, provided that the voltages applied to VBAT and VDD are within the operating range.

### 4.2.2 Sleep mode

The device enters sleep mode if the microcontroller sets the ENABLE pin to low.

In sleep mode, most of the internal circuitry is deactivated: the current consumption of VBAT and VDD is reduced respectively to $I_{VBAT_Q}$ and $I_{VDD_Q}$.

### 4.2.3 Safe state mode

The device will enter safe state if the pin SAFESTATEN is set to low.

In safe state the external MOSFETs of both channels are deactivated (e.g. switched off).

To bring the device from safe state back to normal mode, the pin SAFESTATEN has to be set to high and the failure flag SAFESTATE must be cleared via SAFESTATE_CL or FAIL_RST_0 together with FAIL_RST_1.

If the microcontroller sets the ENABLE pin to low, the device enters the sleep mode.

### 4.2.4 Reset behavior

After the ENABLE pin is pulled high or after an undervoltage event at VDD, the logic content is reset.

In both cases, the failure flag VDD_UV is set to high to indicate that a reset was performed.

## 4.3 Charge pump

The charge pump generates the positive supply for the gate control block, for the $V_{GS}$ and $V_{DS}$ comparators and for the current sense amplifier.

$V_{CP_PUMP}$ thresholds define hysteresis control of the charge pump output voltage by activating/deactivating charge pumping.

$V_{CP_READY}$ thresholds flag the microcontroller that the charge pump output voltage is high enough to activate a channel.

$V_{CP_UV}$ thresholds flag a charge pump output under voltage failure. In this case, turning on and protecting a channel cannot be ensured any more, so the channels are switched off.

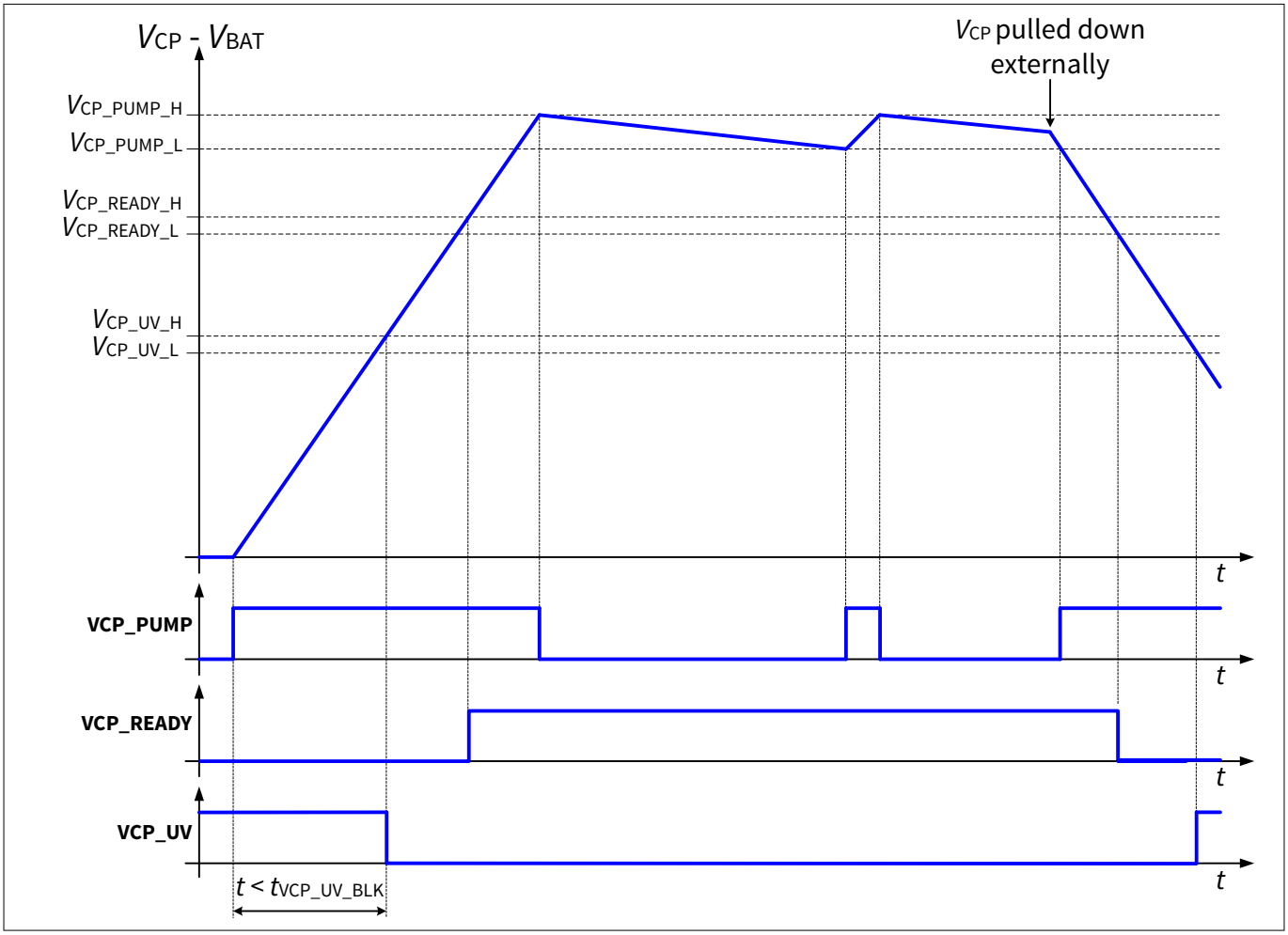



**Figure 5 Charge pump operating**

The charge pump is ready to operate according the VCP_PUMP signal when the following condition is fulfilled:

ENABLE = high **AND** TSD = low **AND** VBAT_OV = low **AND** VCP_UV = low.

At the first activation of the charge pump, the VCP_UV diagnostic will be blanked for the $t_{VCP_UV_BLK}$ duration in order to operate a safe start.

Note that a triggering of VCP_UV will therefore switch off the charge pump in a latched way.

The VCP_PUMP signal is controlling the charge pump activity:

- When the charge pump is enabled it is pumping as long as the VCP_PUMP signal is high
- As soon as the $V_{CP}$ - $V_{BAT}$ voltage gets above the $V_{CP_PUMP_H}$ threshold, the VCP_PUMP signal is turned low and the charge pump stops pumping
- As soon as the $V_{CP}$ - $V_{BAT}$ voltage gets below the $V_{CP_PUMP_L}$ threshold, the VCP_PUMP signal is turned high and the charge pump is pumping

The VCP_READY bit is set to 1 once the $V_{CP}$ - $V_{BAT}$ voltage gets higher than the $V_{CP_READY_H}$ threshold.

The VCP_READY bit is set to 0 once the $V_{CP}$ - $V_{BAT}$ voltage gets lower than the $V_{CP_READY_L}$ threshold.

The VCP_UV bit is set to 0 once the $V_{CP}$ - $V_{BAT}$ voltage gets higher than the $V_{CP_UV_H}$ threshold.

The VCP_UV bit is set to 1 once the $V_{CP}$ - $V_{BAT}$ voltage gets lower than the $V_{CP_UV_L}$ threshold.

VCP_UV is blanked for a duration of $t_{VCP_UV_BLK}$ after charge pump gets enabled (e.g.: after device enable or after clearing VCP_UV failure flag).

## 4.4 Electrical characteristics: supply

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; CSO pin left open; all voltages are referenced to GND; positive current flowing into pin.

**Table 5 Electrical characteristics: supply**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Quiescent current consumption, ENABLE = LOW** | | | | | | | |
| VBAT supply quiescent current | $I_{BAT_Q}$ | – | – | 5 | µA | 1) $T_A \le 85°C$ | PRQ-112 |
| VDD logic supply quiescent current | $I_{DD_Q}$ | – | – | 7 | µA | 1) $T_A \le 85°C$ | PRQ-114 |
| **Current consumption, ENABLE = HIGH** | | | | | | | |
| VBAT supply current | $I_{BAT_SUP}$ | – | – | 10 | mA | 1) MOSONCH_A = 1; MOSONCH_B = 1; $R_{GS} \ge 1$ MΩ; $C_{VCP}$ = 2.2 µF | PRQ-27 |
| VDD logic supply current | $I_{DD_SUP}$ | – | – | 10 | mA | CSA_HSS = 0; CSA_COUTSEL = 0 | PRQ-118 |
| VDD logic supply current | $I_{DD_SUP}$ | – | – | 15 | mA | 1) CSA_HSS = 1; CSA_COUTSEL = 1 | PRQ-543 |

1) Not subject to production test, specified by characterization.

## 4.5 Electrical characteristics: digital IOs

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; all voltages are referenced to GND; positive current flowing into pin; pull-up resistors connected to VDD, pull-down resistors connected to GND.

**Table 6 Electrical characteristics: digital IOs**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Logic input voltage** | | | | | | | |
| Logic high input voltage | $V_{IH}$ | 0.7*$V_{DD}$ | – | $V_{DD}$ | V | – | PRQ-30 |
| Logic low input voltage | $V_{IL}$ | 0 | – | 0.7 | V | – | PRQ-31 |
| Logic input threshold hysteresis | $V_{IHY}$ | 100 | – | – | mV | – | PRQ-32 |
| **Logic output voltage** | | | | | | | |
| Logic high output voltage level | $V_{OH}$ | $V_{DD}$ - 0.4 | $V_{DD}$ - 0.2 | $V_{DD}$ | V | $I_O$ = -1.6 mA | PRQ-415 |
| Logic low output voltage level | $V_{OL}$ | 0 | 0.2 | 0.4 | V | $I_O$ = 1.6 mA | PRQ-416 |
| **Pull-up / -down resistors** | | | | | | | |
| ENABLE pull-down resistor | $R_{PD_ENABLE}$ | 30 | 40 | 50 | kΩ | – | PRQ-126 |
| SCLK pull-down resistor | $R_{PD_SCLK}$ | 30 | 40 | 50 | kΩ | – | PRQ-410 |
| SAFESTATEN pull-down resistor | $R_{PD_SAFESTATEN}$ | 30 | 40 | 50 | kΩ | – | PRQ-409 |
| MOSI pull-down resistor | $R_{PD_MOSI}$ | 30 | 40 | 50 | kΩ | – | PRQ-411 |
| INTERRUPT pull-down resistor | $R_{PD_INTERRUPT}$ | 30 | 40 | 50 | kΩ | – | PRQ-479 |
| CSN pull-up resistor | $R_{PU_CSN}$ | 30 | 40 | 50 | kΩ | – | PRQ-412 |
| **SPI interface setup time** | | | | | | | |
| SPI interface setup time | $t_{SET_SPI}$ | – | – | 150 | µs | – | PRQ-413 |

## 4.6 Electrical characteristics: charge pump

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; all voltages are referenced to GND; positive current flowing into pin.

**Table 7 Electrical characteristics: charge pump**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Charge pump frequency | $f_{CP}$ | 140 | 156 | 172 | kHz | – | PRQ-127 |
| **VCP_PUMP** | | | | | | | |
| VCP_PUMP_H threshold | $V_{CP_PUMP_H}$ | 12.7 | 14 | 15 | V | – | PRQ-343 |
| VCP_PUMP_L threshold | $V_{CP_PUMP_L}$ | 11.7 | 13 | 14 | V | – | PRQ-344 |
| VCP_PUMP hysteresis | $V_{CP_PUMP_HY}$ | 0.5 | 1 | 1.5 | V | – | PRQ-402 |

**(table continues...)**

**Table 7 (continued) Electrical characteristics: charge pump**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **VCP_READY** | | | | | | | |
| VCP_READY_H threshold | $V_{CP_READY_H}$ | 10 | 11 | 11.7 | V | – | PRQ-345 |
| VCP_READY_L threshold | $V_{CP_READY_L}$ | 9.5 | 10.5 | 11.2 | V | – | PRQ-346 |
| VCP_READY hysteresis | $V_{CP_READY_HY}$ | 0.38 | 0.5 | 0.62 | V | – | PRQ-403 |
| **VCP_UV** | | | | | | | |
| VCP_UV_H threshold | $V_{CP_UV_H}$ | 5.7 | 6.5 | 7 | V | – | PRQ-347 |
| VCP_UV_L threshold | $V_{CP_UV_L}$ | 5.2 | 6 | 6.5 | V | – | PRQ-348 |
| VCP_UV hysteresis | $V_{CP_UV_HY}$ | 0.25 | 0.5 | 0.75 | V | – | PRQ-404 |
| VCP_UV Blanking time | $t_{VCP_UV_BLK}$ | 2.4 | 3 | 4 | ms | – | PRQ-494 |
| **Charge pump output current** | | | | | | | |
| Charge pump output current capability at VCP | $I_{CPO}$ | – | – | -10 | mA | $C_{CPHL}$ = 220 nF; | PRQ-349 |
| CPL pulsed current | $\lvert I_{CPL_PULSE} \rvert$ | 60 | 80 | 110 | mA | – | PRQ-487 |

# 5 High-side gate driver

The high-side gate driver is capable to drive multiple external MOSFETs for high current capability. Two independent channels are available, and they can be switched on and off by the SPI register commands. The gate drivers are supplied by an internal one-stage charge pump with external capacitors.

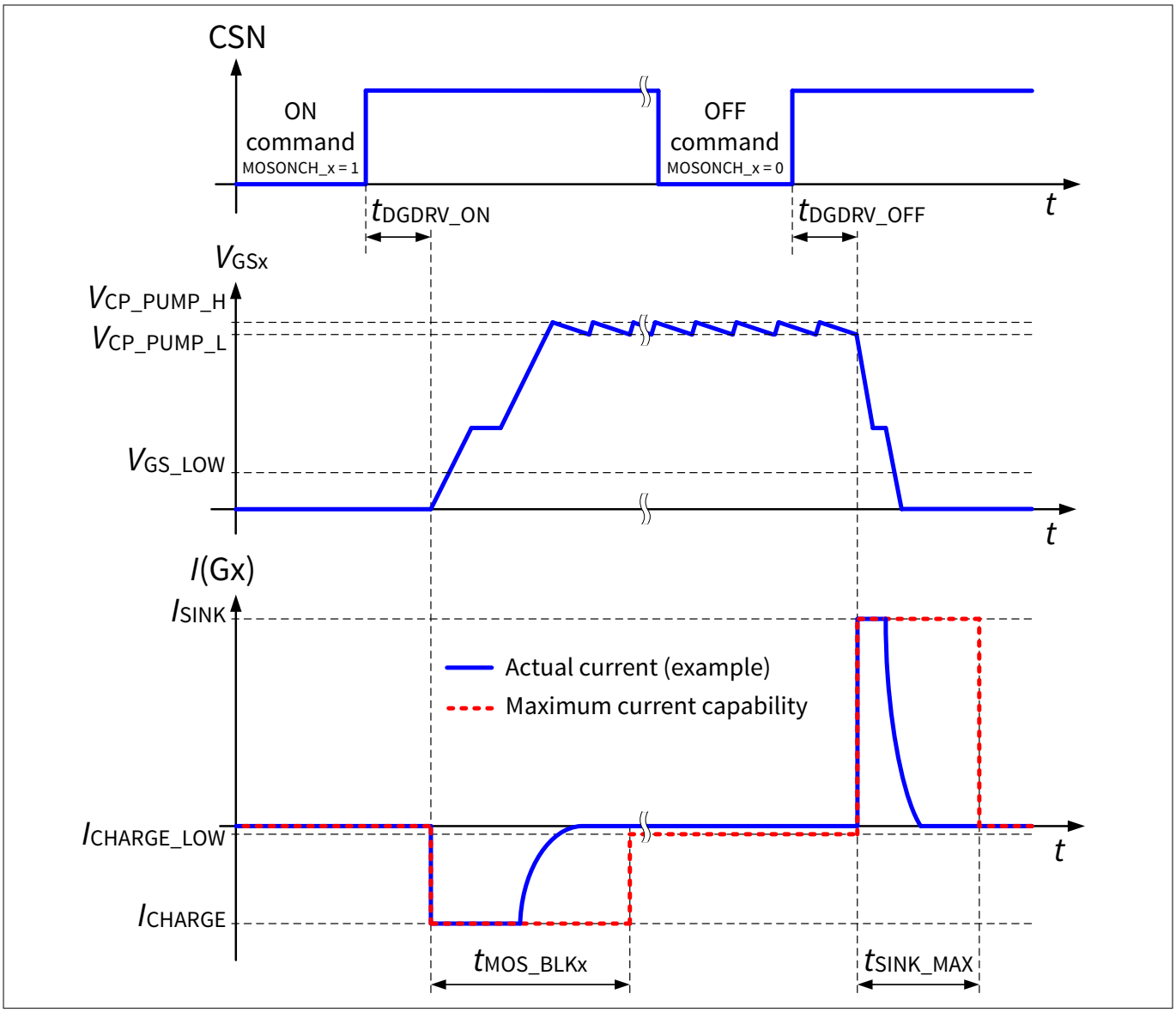



**Figure 6 Maximum gate driving capability**

## 5.1 Channel activation

The selected channel is activated under the following condition:
ENABLE = high **AND** MOSONCH_(x) = high **AND** SAFESTATEN = high.

**Table 8 MOSFET activation**

| MOSONCH_(x)[0] | MOSFET activation state |
|---|---|
| 0 | MOSFET channel not activated (default) |
| 1 | MOSFET channel activated |

When a channel is activated through the SPI interface, its output gate current capability is set to $I_{CHARGE}$ for a duration of maximum $t_{MOS_BLKx}$ (MOS blanking time). $I_{CHARGE}$ is active until $V_{GS}$ reaches $V_{CP}$, so the actual time depends on the MOSFETs gate capacitance.

Once the $t_{MOS_BLKx}$ time expires, the output gate current capability is reduced to maximum $I_{CHARGE_LOW}$ ; the actual current delivered by the driver depends on external leakages, coming for example from an external pull-down resistor added between gate and source of the MOSFETs.

## 5.2 Channel deactivation

The channel is deactivated by discharging the external MOSFET's gate if one of the following conditions are met:

- MOSONCH_(x) set from high to low
- Pin ENABLE set from high to low
- SAFESTATEN set from high to low

*Note: In case of a failure, MOSONCH_(x) is automatically set from high to low, which immediately triggers a channel deactivation.*

When a channel is deactivated either due to MOSONCH_(x) or pin SAFESTATEN set from high to low, the output gate control pulls a high discharge current, set to $I_{SINK}$ for a duration of maximum $t_{SINK_MAX}$. $I_{SINK}$ is active until $V_{GS}$ is zero, so the actual time depends on the MOSFETs gate capacitance.

Once $t_{SINK_MAX}$ expires, the output gate control changes to a voltage clamping structure, which limits the gate to source voltage ($V_{GS}$) to maximum $V_{GS_LOW}$. This clamping structure ensures that the MOSFETs' $V_{GS}$ is below $V_{GS(th)}$ to keep them OFF.

When MOSONCH_(x) is low while ENABLE pin is high, there is a leakage current flowing out of the Sx pins: $I_{Sx_OFF}$.

When the channels are deactivated due to pin ENABLE set from high to low, the output gate control does not pull the high discharge current ($I_{SINK}$), it immediately changes to the voltage clamping structure with very low leakage current on the Sx pins.

## 5.3 MOSFET driver output

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; all voltages are referenced to GND; positive current flowing into pin.

**Table 9 MOSFET driver output**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Gate charge current high | $I_{CHARGE}$ | – | – | -300 | mA | $V_{Gx} = V_{Sx} = 0$ V | PRQ-133 |
| Gate charge current low | $I_{CHARGE_LOW}$ | -5 | -4 | -2.5 | mA | – | PRQ-488 |
| Gate discharge current | $I_{SINK}$ | 0.9 | 1.1 | 1.3 | A | $V_{Gx}$ - $V_{Sx}$ = 13 V | PRQ-134 |
| Gate discharge current maximum active time | $t_{SINK_MAX}$ | 8 | 10 | 12 | µs | 1) | PRQ-539 |
| Source current in OFF mode | $I_{Sx_OFF}$ | – | 40 | – | µA | 1) MOSONCH_(x) = 0; ENABLE = HIGH | PRQ-544 |
| High level output voltage Gx vs. Sx | $V_{GS}$ | $V_{CP_PUMP_L}$ | – | $V_{CP_PUMP_H}$ | V | Current between Gx and Sx = 1 mA | PRQ-135 |

**(table continues...)**

**Table 9 (continued) MOSFET driver output**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Low level output voltage Gx vs. Sx | $V_{GS_LOW}$ | – | – | 1.7 | V | $T_J$ < 25°C<br>Current beween Gx and Sx = 100 mA<br>0 V ≤ $V_{BAT}$ ≤ $V_{BAT(EXT)_MAX}$<br>0 V ≤ $V_{DD}$ ≤ $V_{DD_MAX}$ | PRQ-498 |
| Low level output voltage Gx vs. Sx | $V_{GS_LOW}$ | – | – | 1.5 | V | $T_J$ ≥ 25°C<br>Current between Gx and Sx = 100 mA<br>0 V ≤ $V_{BAT}$ ≤ $V_{BAT(EXT)_MAX}$<br>0 V ≤ $V_{DD}$ ≤ $V_{DD_MAX}$ | PRQ-524 |
| **Gate driver dynamic parameter** | | | | | | | |
| Gate turn-on delay time | $t_{DGDRV_ON}$ | – | – | 3 | µs | Duration between CSN goes from low to high and gate charge current is activated | PRQ-137 |
| Gate turn-off delay time | $t_{DGDRV_OFF}$ | – | – | 3 | µs | Duration between CSN goes from low to high and gate dicharge current is activated | PRQ-139 |
| Delay time for gate turn-off triggered by SAFESTATEN | $t_{DGOFF_SFSTN}$ | – | – | 3 | µs | Duration between SAFESTATEN goes from high to low and gate dicharge current is activated | PRQ-527 |
| Gate to source clamped voltage | $V_{GS_TH}$ | 15.5 | – | 19.5 | V | – | PRQ-476 |
| **Active zener clamping** | | | | | | | |
| Gate zener clamping with respect to VBAT | $V_{CLAMP_G_VBAT}$ | 78 | 82 | 87 | V | $I_{_G}$ = -2.5 mA | PRQ-489 |
| Gate zener clamping with respect to GND | $V_{CLAMP_G_GND}$ | 78 | 82 | 87 | V | $I_{_G}$ = -2.5 mA | PRQ-490 |

*1)* Not subject to production test, specified by design.

# 6 Protection and monitoring

The device provides three sets of features to protect and monitor:

- Monitorings, which give a status to the MCU
- Warnings, which inform the MCU of critical events with limited impact
- Failure detections, which trigger internal actions (channel deactivation mainly) and notify immediately the MCU

## 6.1 Monitorings

### 6.1.1 Source voltage monitoring in OFF state

If the source voltage $V_{Sx}$ of a deactivated channel rises above $V_{S_TH}$, and ENABLE is high, then the appropriate flag VSOURCE_(x) is set to 1.

This warning allows to implement an "open load detection in OFF state", since the voltage on the source pin Sx would be pulled up by the leakage of the gate driver if there is no load connected.

### 6.1.2 Charge pump voltage monitoring

If the charge pump voltage VCP is above $V_{CP_READY_H}$, then the VCP_READY flag is set to 1.

### 6.1.3 SPI address monitoring

If the MCU tries to read or write a register with an address which is not available, then the ADD_NOT_AVAIL flag is set to 1.

## 6.2 Warnings

In order to inform the MCU about any warning on the driver, the warning flags will be used and updated by the device, which notifies the MCU by setting the INTERRUPT pin to high.

The warnings are not latched and will be reset, if the condition no longer applies.

The warnings do not change the state of the output channels.

### 6.2.1 Temperature warning

The OT_WARNING is set to 1 if the overtemperature warning threshold $T_{JW}$ is reached and exceeded.

### 6.2.2 One time programmable (OTP) memory data corruption

The device embeds an OTP to store internal settings, used to trim internal blocks for full specification compliance. These settings are written during manufacturing and this memory cannot be accessed by SPI.

The MEM_FAIL flag is set to 1 if OTP data is corrupted or if OTP readout failed. In this case all affected trimmings are set to default values, therefore parameter deviations are possible. OTP is checked and read out right after the device is enabled.

*Note: OTP cannot be read in case of a not connected ground pin.*

### 6.2.3 Ground loss

In case of a voltage difference between 2 ground pins (whether GND, AGND or CPGND) higher than $V_{GND_LOSS}$, the corresponding LOG_(x) warning flags will be set to 1. This is typically the case for not connected ground pins.

- Disconnecting AGND will trigger LOG_A and LOG_CP flags

- Disconnecting CPGND will trigger LOG_CP and LOG_D flags
- Disconnecting DGND will trigger LOG_A and LOG_D flags

## 6.3 Failures detection

Failures detection is provided to implement protections for the external MOSFETs and eventually for the load.

There are two types of failures detected by the gate driver:

- Latching failures, which require to be cleared before the gate driver can operate again. This category is split into two sub-categories:
  - Latching failures for which clearing the flag will automatically turn the channel on again. They include:
    - Undervoltage on the charge pump
    - Undervoltage on gate-source voltage ( $V_{GS} = [V_{Gx}\text{-}V_{Sx}]$ )
    - Overvoltage on drain-source voltage ( $V_{DS} = [V_{BAT}\text{-}V_{Sx}]$ ), when VDS(x)_SS_[0] = 0 to enable the protection
  - Latching failures for which an SPI command has to follow the flag clearing in order to turn the channel on again. They include :
    - Undervoltage on $V_{DD}$
    - SAFESTATEN pin activation
    - Overtemperature shut down
    - Overcurrent
- Non-latching failures, which do not need to be cleared: once the failure source is gone, the gate driver can operate again after a configurable delay. They include:
  - Overvoltage on $V_{BAT}$
  - Undervoltage on $V_{BAT}$

### 6.3.1 Failure notification and clearing

In case of failure detection, the FAILURE flag is set to high, the INTERRUPT pin is set to high and the corresponding channel(s) is (are) deactivated automatically by setting register bit MOSONCH_(x) to 0 (except for drain-source failure detection when it is disabled through the VDS(x)_SS register).

A latching failure can only be cleared when the failure is not present anymore, except for VCP_UV, VGSTH_(x) and VDSTRIP_(x).

### 6.3.2 Non-latching failures

The non-latching failures do not need to be reset: the gate driver activates the MOSFET again, if the failure does not exist anymore.

#### 6.3.2.1 VBAT overvoltage

If $V_{BAT}$ exceeds $V_{BAT_OV_OFF}$, the FAILURE bit and VBAT_OV flag are set to 1.

If the $V_{BAT}$ gets lower than $V_{BAT_OV_ON}$, then the restart will be done after $t_{OV_RESTART}$.

While the device is in auto-restart duration, none of the channels can be activated by the µC.

**Table 10 VBAT overvoltage auto-restart time**

| VBATOVARST[1:0] | VBAT overvoltage auto-restart time (typical): $t_{OV_RESTART}$ |
|---|---|
| 00 | 10 µs (default) |
| 01 | 50 µs |
| 10 | 200 µs |
| 11 | 1 ms |

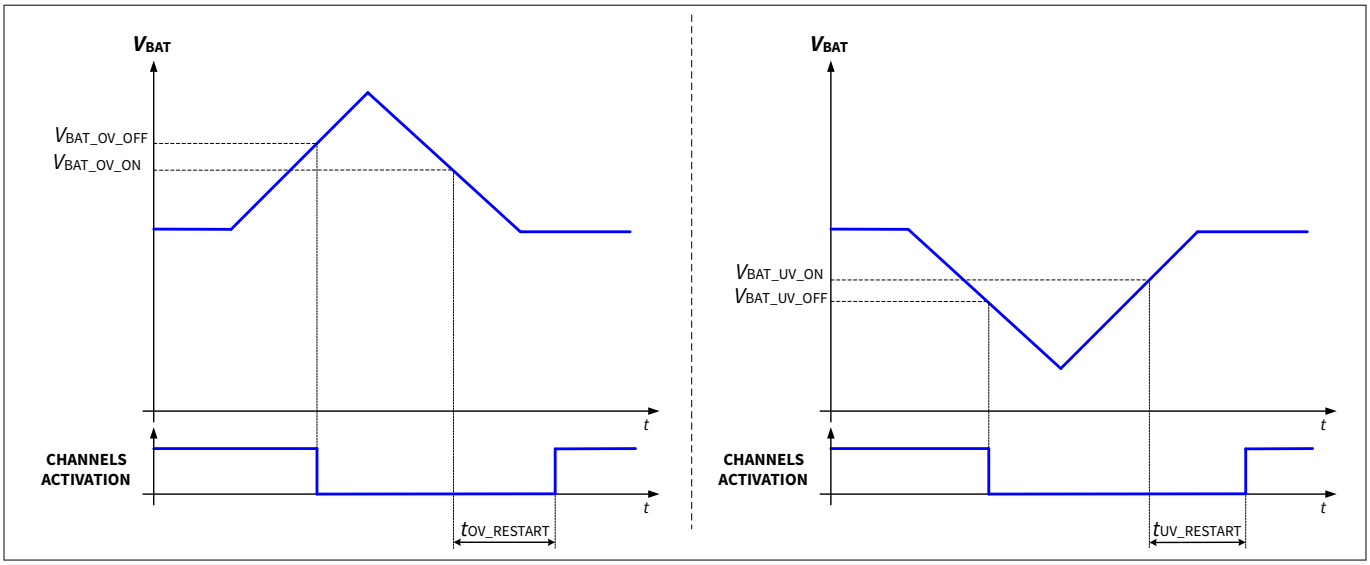



**Figure 7 VBAT overvoltage and undervoltage auto-restart time diagrams**

### 6.3.2.2 VBAT undervoltage

If $V_{BAT}$ gets lower than $V_{BAT_UV_OFF}$, the FAILURE bit and VBAT_UV flag are set to 1.

If the $V_{BAT}$ gets higher than $V_{BAT_UV_ON}$, then the restart will be done after $t_{UV_RESTART}$.

While the device is in auto-restart duration, none of the channels can be activated by the µC.

**Table 11 VBAT undervoltage auto-restart time**

| VBATUVARST[1:0] | VBAT undervoltage auto-restart time $t_{UV_RESTART}$ (typical) |
|---|---|
| 00 | 1 ms (default) |
| 01 | 5 ms |
| 10 | 20 ms |
| 11 | 50 ms |

## 6.3.3 Latching failures

Once a latching failure (except VDD_UV) has been detected, a reset can be operated either by toggling ENABLE, VDD (Chapter 4.2.4), or by an SPI command.

### 6.3.3.1 Blank time and filter time for failures detections

#### 6.3.3.1.1 Blank time

Both drain-source and gate-source failure detections are inherently triggered at the turn-on of a channel. Turning on a MOSFET implies a transient phase where the gate-source voltage is rising and drain-source voltage is decreasing before they reach their steady state.

Both failure detections have therefore to be temporary blanked at turn-on, which is the purpose of the configurable blank time: $t_{MOS_BLKx}$. Its value is configured for each channel independently, based on the MOSFETs characteristics (total $C_{GS}$ mainly).

*Note: As described in Chapter 5.1, $t_{MOS_BLKx}$ also defines the maximum duration of the $I_{CHARGE}$ current.*

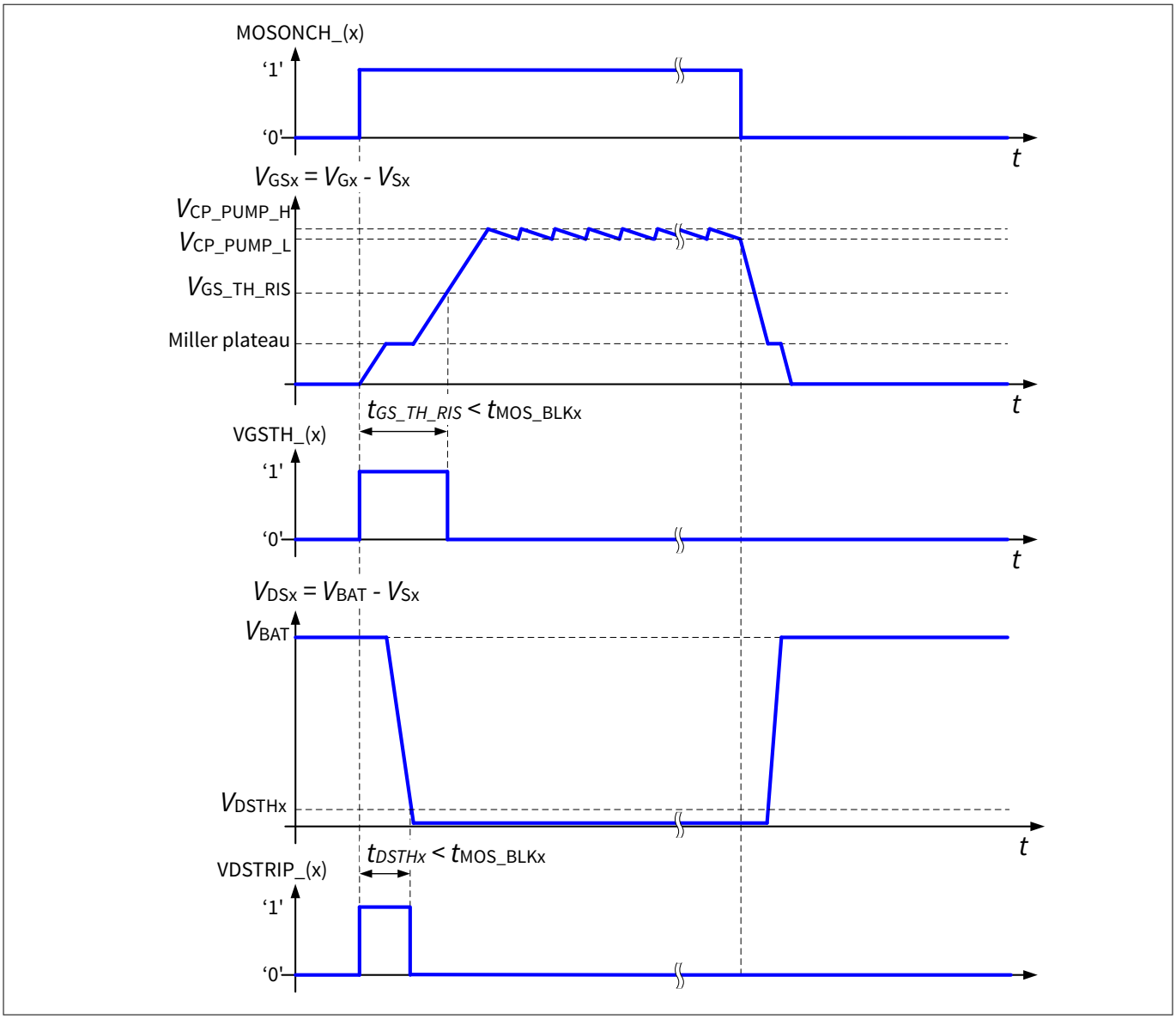



**Figure 8 Blank time at MOSFET turn-on**

A configurable blank time for the drain-source and gate-source failure detections is applied at the turn-on of the selected channel. During the blank time $t_{MOS_BLKx}$, a drain-source or gate-source overvoltage failure is masked.

**Table 12 MOSFET voltage blank time**

| MOSBLK_(x)_[1:0] | MOSFET voltage blank time (typical) $t_{MOS_BLKx}$ |
|---|---|
| 00 | 10 µs (default) |
| 01 | 20 µs |
| 10 | 50 µs |
| 11 | 100 µs |

#### 6.3.3.1.2 Filter time

Both drain-source and gate-source failure detections may be wrongly triggered due to noisy signals on the monitored pins. A configurable filter time is therefore provided for each channel independently, which applies for the two failure detections: $t_{MOS_FLTx}$.

**Table 13 MOSFET voltage filter time**

| MOSFLT_(x)_[1:0] | MOSFET voltage filter time (typical) $t_{MOS_FLTx}$ |
|---|---|
| 00 | 0.5 µs |
| 01 | 1 µs (default) |
| 10 | 2 µs |
| 11 | 5 µs |

### 6.3.3.2 Drain-source overvoltage

The drain to source voltage of activated channel(s) is continuously monitored in order to protect high-side MOSFETs against a short circuit to ground during ON-state.

If a channel is activated and the $V_{BAT}$ (drain) to $V_{Sx}$ (source) voltage $V_{DS}$ exceeds $V_{DSTHx}$ for longer than the filter time $t_{MOS_FLTx}$ after the blanking time $t_{MOS_BLKx}$, the bit FAILURE and the VDSTRIP_(x) bit are set to 1 and the register bit MOSONCH_(x) is set to 0 if the VDS(x)_SS bit is set to 0.

Otherwise (VDS(x)_SS bit is set to 1) only the bit FAILURE and the VDSTRIP_(x) bit are set to 1 and the register bit MOSONCH_(x) is still set to 1.

Each channel has a dedicated threshold that can be selected by the register VDSTH_(x).

When VDS(x)_SS bit is set to 0 and the VDSTRIP_(x) failure flag is cleared, the selected channel immediately turns on again. If the $V_{DS}$ of the channel is still above $V_{DSTHx}$ for longer than the filter time $t_{MOS_FLTx}$ after the blanking time $t_{MOS_BLKx}$ (e.g. the failure cause is still present), the channel is disabled again.

**Table 14 Drain-source overvoltage threshold**

| VDSTH_(x)_[2:0] | Positive drain-source overvoltage threshold (typical) $V_{DSTHx}$ | Negative drain-source overvoltage threshold |
|---|---|---|
| 000 | 100 mV | -100 mV |
| 001 | 150 mV | -150 mV |
| 010 | 200 mV (default) | - 200 mV (default) |
| 011 | 250 mV | -250 mV |
| 100 | 300 mV | -300 mV |
| 101 | 400 mV | - 400 mV |
| 110 | 500 mV | - 500 mV |
| 111 | 600 mV | - 600 mV |

**Table 15 Drain-source channel de-activation condition**

| VDS(x)_SS_[0] | Drain-source channel condition |
|---|---|
| 0 | Channel is de-activated in case of drain-source overvoltage |
| 1 | Channel is not de-activated in case of drain-source overvoltage (default) |

### 6.3.3.3 Gate-source undervoltage

The device reports a gate-source undervoltage failure if the following conditions are both met:

- After expiration of the configured blank time $t_{MOS_BLKx}$
- If the gate-source voltage is less than the threshold $V_{GS_TH(x)}$ for the selected channel for a duration longer than the configured filter time $t_{MOS_FLTx}$

In case of gate-source undervoltage failure, the bit FAILURE and the bit VGSTH_(x) are set to 1.

When the VGSTH_(x) flag is cleared, the selected channel automatically turns on again. If the $V_{GS}$ of the channel is still below VGS_TH_RIS for longer than the filter time $t_{MOS_FLTx}$ after the blanking time $t_{MOS_BLKx}$ (e.g. the failure cause is still present), the channel is disabled again.

### 6.3.3.4 Channel cross-control

While activating both channels, VGSTH_(x) and VDSTRIP_(x) failures related to one channel may or may not affect the other channel. This cross-control between the 2 channels is programmable by SPI.

While the CHCRCTRL bit is set to 1, any of the following failures will deactivate the channels A (CHA) and B (CHB) according this overview:

- In case of VGSTH_(x) = 1 -> CHA = OFF and CHB = OFF
- In case of VDSTRIP_A = 1, VDSA_SS = 0 and VDSB_SS = 0 -> CHA = OFF and CHB = OFF
- In case of VDSTRIP_A = 1, VDSA_SS = 1 and VDSB_SS = 0 -> CHA = **Keep previous state (ON)** and CHB = OFF
- In case of VDSTRIP_A = 1, VDSA_SS = 0 and VDSB_SS = 1 -> CHA = OFF and CHB = **Keep previous state**
- In case of VDSTRIP_A = 1, VDSA_SS = 1 and VDSB_SS = 1 -> CHA = **Keep previous state (ON)** and CHB = **Keep previous state**
- In case of VDSTRIP_B = 1, VDSA_SS = 0 and VDSB_SS = 0 -> CHA = OFF and CHB = OFF
- In case of VDSTRIP_B = 1, VDSA_SS = 1 and VDSB_SS = 0 -> CHA = **Keep previous state** and CHB = OFF
- In case of VDSTRIP_B = 1, VDSA_SS = 0 and VDSB_SS = 1 -> CHA = OFF and CHB = **Keep previous state** (ON)
- In case of VDSTRIP_B = 1, VDSA_SS = 1 and VDSB_SS = 1 -> CHA = **Keep previous state** and CHB = **Keep previous state** (ON)

If the CHCRCTRL bit is set to 0, only the faulty channel will be treated.

**Table 16 Channel cross-control**

| CHCRCTRL[0] | Channel cross-control status |
|---|---|
| 0 | Cross-control deactivated |
| 1 | Cross-control activated (default) |

### 6.3.3.5 VDD undervoltage

If the VDD voltage falls below the $V_{DD_UV_ON}$ threshold, the device is reset. When $V_{DD}$ comes back above the $V_{DD_UV_ON}$ threshold, VDD_UV bit is set to 1.

### 6.3.3.6 VCP undervoltage

The VCP_UV bit and the FAILURE bit are set to 1 as soon as the ($V_{CP}$ - $V_{BAT}$) voltage gets lower than the $V_{CP_UV_L}$ threshold. The charge pump is immediately disabled.

When the failure flag VCP_UV is cleared, the charge pump immediately restarts. If the ($V_{CP}$ - $V_{BAT}$) voltage is still below $V_{CP_UV_H}$ after the startup blanking time $t_{VCP_UV_BLK}$, (e.g. the failure cause is still present), the charge pump is disabled again.

### 6.3.3.7 SAFESTATEN activation

Once the SAFESTATEN signal is set to low, the FAILURE bit is set to 1.

### 6.3.3.8 Overtemperature

If the internal temperature sensor reaches $T_{JSD}$, the gate drivers are latched off, the charge pump and the current sense amplifier are deactivated and the TSD and FAILURE flags are set to 1.

### 6.3.3.9 Current sense amplifier and overcurrent comparator

Current sense amplifier is used for monitoring the voltage drop across the shunt resistor as a sensor for the load current. If overcurrent is detected, this will switch off both channels.

Current sense comparator and amplifier are active under the following condition:

ENABLE = high **AND** VCP_UV = low **AND** VBAT_UV = low **AND** VBAT_OV = low **AND** TSD = low **AND** $V_{DD} > V_{DD_UV_ON}$.

#### 6.3.3.9.1 Gain configuration

The differential gain of the current sense amplifier is configurable by the configuration bits CSAG_(x).

**Table 17 Configuration of the current sense amplifier gain**

| CSAG[2:0] | Current sense amplifier gain $G_{DIFF}$ (typical) |
|---|---|
| 000 | 10 V/V |
| 001 | 15 V/V |
| 010 | 20 V/V |
| 011 | 25 V/V |
| 100 | 31.5 V/V |
| 101 | 35 V/V (default) |
| 110 | 40 V/V |
| 111 | 47.7 V/V |

#### 6.3.3.9.2 Current sense position

In order to adjust the internal circuitry to the proper shunt position (high-side or low-side), the CSA_HSS needs to be set.

While the CSA_HSS bit is set to 0, the internal circuitry is optimized for a current sense in low-side position.

If the CSA_HSS bit is set to 1, the internal circuitry is optimized for a current sense in high-side position.

**Table 18 Current sense position adjustment**

| CSA_HSS[0] | Current sense position |
|---|---|
| 0 | Shunt is in low-side position (default) |
| 1 | Shunt is in high-side position |

#### 6.3.3.9.3 Current sense output load

In order to adjust to the amount of output charge connected to the CSO pin, some internal circuitry can be activated.

While the CSA_COUTSEL bit is set to 1, the internal circuitry is optimized for an external load capacitance higher than 100 pF.

If the CSA_COUTSEL bit is set to 0, the internal circuitry is optimized for an external load capacitance lower than 100 pF.

**Table 19 Current sense output load adjustment**

| CSA_COUTSEL[0] | Current sense output charge |
|---|---|
| 0 | Output load < 100 pF (default) |
| 1 | Output load > 100 pF |

### 6.3.3.9.4 Overcurrent detection

A comparator at CSO detects overcurrent conditions.

If the CSA output is out of the range between threshold voltages ΔVOCTHxL and ΔVOCTHxH configured in OCTH, all channels are switched off and the bits FAILURE and ITRIP are set to 1 if at least one channel was in ON state.

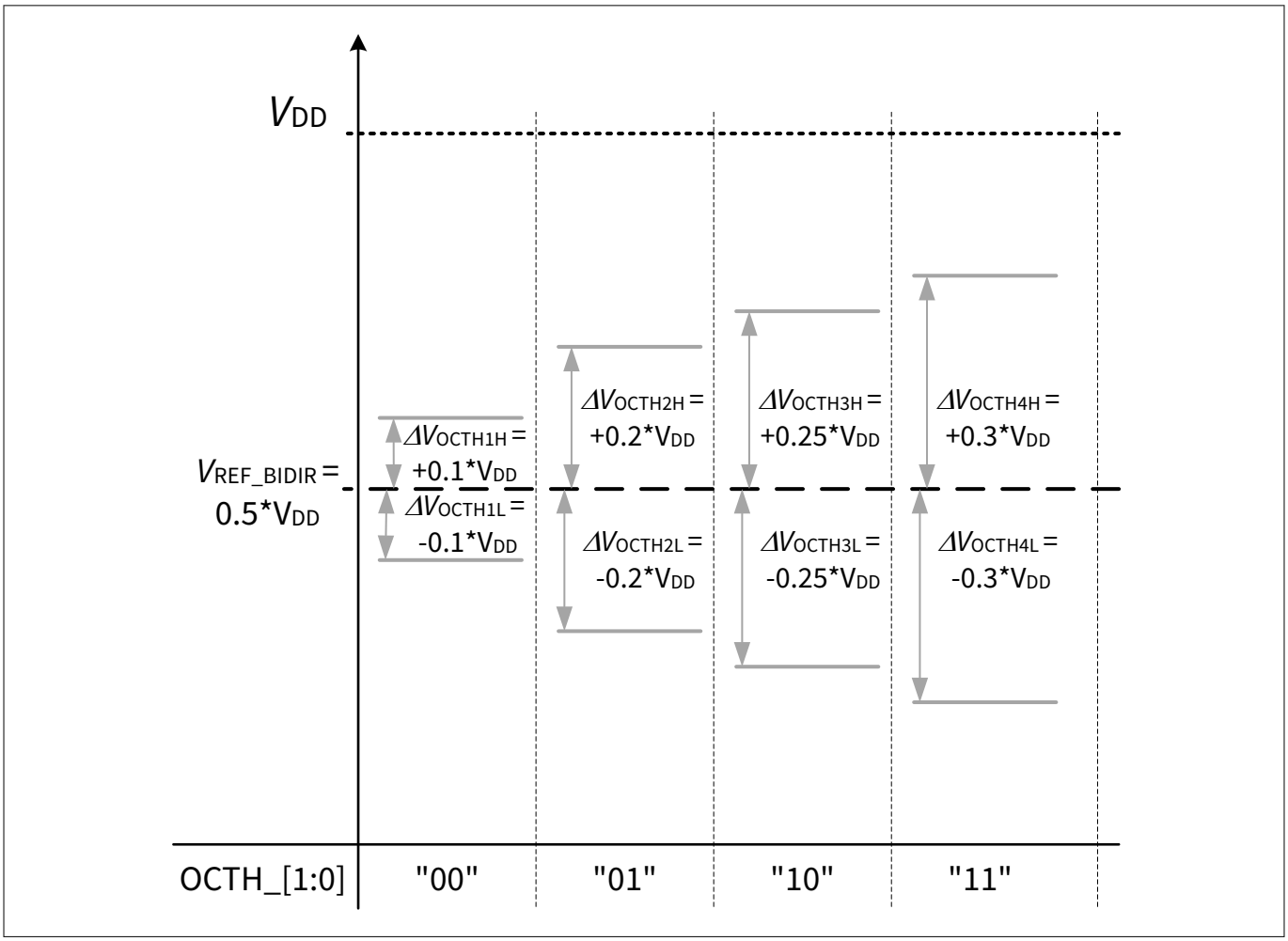



**Figure 9 Overcurrent detection thresholds**

### 6.3.3.9.5 Electrical characteristics: current sense

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; all voltages are referenced to GND; positive current flowing into pin.

**Table 20 Electrical characteristics: current sense**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input offset voltage | $V_{OFFSET}$ | -1.4 | 0 | 1.4 | mV | – | PRQ-52 |
| Integrated output noise voltage at CSO pin | $V_{CSO_NOISE}$ | – | – | 5 | $mV_{rms}$ | [1] ISP shorted to ISN; all gain settings; output open (no load at CSO) | PRQ-262 |
| PSRR - Power supply rejection ratio VCP | $P_{SRR}$ | 60 | – | – | dB | DC up to 1 kHz | PRQ-63 |
| Settling time to 98% | $t_{SET}$ | – | – | 7 | µs | Duration between CSN goes from low to high and signal at CSO pin is settled (98% of final value) | PRQ-222 |
| Reference voltage for bidirectional CSA | $V_{REF_BIDIR}$ | -2% | $V_{DD}/2$ | +2% | V | – | PRQ-228 |
| Digital glitch filter time for ITRIP | $t_{ITRIP_FLT}$ | 1.2 | 1.5 | 1.8 | µs | [1] | PRQ-505 |
| ISP, ISN leakage current while off | $I_{SP_OFF}$, $I_{SN_OFF}$ | -5 | – | 5 | µA | ENABLE = 0; $V_{ISP} = V_{ISN}$; 0 V ≤ $V_{ISN}$,$V_{ISP}$ ≤ $V_{BAT}$ | PRQ-392 |
| **Common mode rejection ratio** | | | | | | | |
| CMRR - common mode rejection ratio @ Gain = 10 V/V | $C_{MRR10}$ | 75 | – | – | dB | DC up to 1 kHz | PRQ-64 |
| CMRR - common mode rejection ratio @ Gain = 15 V/V | $C_{MRR15}$ | 77 | – | – | dB | DC up to 1 kHz | PRQ-148 |
| CMRR - common mode rejection ratio @ Gain = 20 V/V | $C_{MRR20}$ | 81 | – | – | dB | DC up to 1 kHz | PRQ-149 |
| CMRR - common mode rejection ratio @ Gain = 25 V/V | $C_{MRR25}$ | 83 | – | – | dB | DC up to 1 kHz | PRQ-150 |
| CMRR - common mode rejection ratio @ Gain = 31.5 V/V | $C_{MRR31.5}$ | 83 | – | – | dB | DC up to 1 kHz | PRQ-210 |
| CMRR - common mode rejection ratio @ Gain = 35 V/V | $C_{MRR35}$ | 85.5 | – | – | dB | DC up to 1 kHz | PRQ-211 |
| CMRR - common mode rejection ratio @ Gain = 40 V/V | $C_{MRR40}$ | 86 | – | – | dB | DC up to 1 kHz | PRQ-212 |

**(table continues...)**

**Table 20 (continued) Electrical characteristics: current sense**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| CMRR - common mode rejection ratio @ Gain = 47.7 V/V | $C_{MRR47.7}$ | 88.5 | – | – | dB | DC up to 1 kHz | PRQ-213 |
| **Current sense amplifier differential gain** | | | | | | | |
| Current sense amplifier differential gain 10 V/V | $G_{DIFF10}$ | 9.8 | 10 | 10.2 | V/V | Test condition: CSAG = (000) | PRQ-53 |
| Current sense amplifier differential gain 15 V/V | $G_{DIFF15}$ | 14.7 | 15 | 15.3 | V/V | Test condition: CSAG = (001) | PRQ-77 |
| Current sense amplifier differential gain 20 V/V | $G_{DIFF20}$ | 19.6 | 20 | 20.4 | V/V | Test condition: CSAG = (010) | PRQ-78 |
| Current sense amplifier differential gain 25 V/V | $G_{DIFF25}$ | 24.5 | 25 | 25.5 | V/V | Test condition: CSAG = (011) | PRQ-79 |
| Current sense amplifier differential gain 31.5 V/V | $G_{DIFF31.5}$ | 30.87 | 31.5 | 32.13 | V/V | Test condition: CSAG = (100) | PRQ-206 |
| Current sense amplifier differential gain 35 V/V | $G_{DIFF37.7}$ | 34.3 | 35 | 35.7 | V/V | Test condition: CSAG = (101) | PRQ-207 |
| Current sense amplifier differential gain 40 V/V | $G_{DIFF40}$ | 39.2 | 40 | 40.8 | V/V | Test condition: CSAG = (110) | PRQ-208 |
| Current sense amplifier differential gain 47.7 V/V | $G_{DIFF47.7}$ | 46.75 | 47.7 | 48.65 | V/V | Test condition: CSAG = (111) | PRQ-209 |
| **Current sense bandwidth** | | | | | | | |
| Low gain current sense bandwidth | $f_{BW_LOW}$ | 200 | – | – | kHz | Max output current capability = 4 mA, cload between 10 pF and 400 pF, CSAG[2:0] from '000' to '110' | PRQ-388 |
| High gain current sense bandwidth | $f_{BW_HIGH}$ | 150 | – | – | kHz | Max output current capability = 4 mA, cload between 10 pF and 400 pF, CSAG[2:0]='111' | PRQ-389 |
| **Overcurrent thresholds** | | | | | | | |
| Overcurrent threshold 1 high relative to VREF_BIDIR | $\Delta V_{OCTH1H}$ | 0.095* $V_{DD}$ | 0.105* $V_{DD}$ | 0.115* $V_{DD}$ | V | OCTH = (00) | PRQ-531 |
| Overcurrent threshold 1 low relative to VREF_BIDIR | $\Delta V_{OCTH1L}$ | -0.115* $V_{DD}$ | -0.105* $V_{DD}$ | -0.095* $V_{DD}$ | V | OCTH = (00) | PRQ-532 |

**(table continues...)**

**Table 20 (continued) Electrical characteristics: current sense**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Overcurrent threshold 2 high relative to VREF_BIDIR | $\Delta V_{OCTH2H}$ | 0.199* $V_{DD}$ | 0.210* $V_{DD}$ | 0.221* $V_{DD}$ | V | OCTH = (01) | PRQ-533 |
| Overcurrent threshold 2 low relative to VREF_BIDIR | $\Delta V_{OCTH2L}$ | -0.214* $V_{DD}$ | -0.203* $V_{DD}$ | -0.192* $V_{DD}$ | V | OCTH = (01) | PRQ-534 |
| Overcurrent threshold 3 high relative to VREF_BIDIR | $\Delta V_{OCTH3H}$ | 0.243* $V_{DD}$ | 0.254* $V_{DD}$ | 0.265* $V_{DD}$ | V | OCTH = (10) | PRQ-535 |
| Overcurrent threshold 3 low relative to VREF_BIDIR | $\Delta V_{OCTH3L}$ | -0.265* $V_{DD}$ | -0.254* $V_{DD}$ | -0.243* $V_{DD}$ | V | OCTH = (10) | PRQ-536 |
| Overcurrent threshold 4 high relative to VREF_BIDIR | $\Delta V_{OCTH4H}$ | 0.293* $V_{DD}$ | 0.304* $V_{DD}$ | 0.315* $V_{DD}$ | V | OCTH = (11) | PRQ-537 |
| Overcurrent threshold 4 low relative to VREF_BIDIR | $\Delta V_{OCTH4L}$ | -0.315* $V_{DD}$ | -0.304* $V_{DD}$ | -0.293* $V_{DD}$ | V | OCTH = (11) | PRQ-538 |

*1)* Not subject to production test, specified by design.

## 6.4 INTERRUPT pin control

The INTERRUPT pin is set high and latched if one of the following occurs:

- FAILURE bit is set to 1
- OT_WARNING is set to 1
- GEN_INTERRUPT flag is set to 1 (for testing the interrupt signal connection to controller)
- GND_LOSS bit is set to 1
- MEM_FAIL bit is set to 1

Once the INTERRUPT signal has been set high due to a failure or a warning flag, it can be cleared either by:

- Reading the corresponding failure bit via SPI
- Setting the INT_CLEAN bit to 1

If the INTERRUPT signal has been set high via the GEN_INTERRUPT bit, it can be cleared only by setting GEN_INTERRUPT back to 0. INT_CLEAN will not remove that interrupt in this case.

## 6.5 Electrical characteristics: protection and monitoring

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C; all voltages are referenced to GND; positive current flowing into pin.

**Table 21 Electrical characteristics: protection and monitoring**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **MOS voltage blank time** | | | | | | | |
| MOS voltage blank time 1 | $t_{MOS_BLK1}$ | 8 | 10 | 12 | µs | 1) Start: gate charge current is activated | PRQ-152 |
| MOS voltage blank time 2 | $t_{MOS_BLK2}$ | 16 | 20 | 24 | µs | 1) Start: gate charge current is activated | PRQ-153 |
| MOS voltage blank time 3 | $t_{MOS_BLK3}$ | 40 | 50 | 60 | µs | 1) Start: gate charge current is activated | PRQ-154 |
| MOS voltage blank time 4 | $t_{MOS_BLK4}$ | 80 | 100 | 120 | µs | 1) Start: gate charge current is activated | PRQ-155 |
| **MOS voltage monitoring filter time** | | | | | | | |
| MOS voltage filter time 1 | $t_{MOS_FLT1}$ | 0.4 | 0.5 | 0.6 | µs | 1) | PRQ-295 |
| MOS voltage filter time 2 | $t_{MOS_FLT2}$ | 0.8 | 1 | 1.2 | µs | 1) | PRQ-296 |
| MOS voltage filter time 3 | $t_{MOS_FLT3}$ | 1.6 | 2 | 2.4 | µs | 1) | PRQ-297 |
| MOS voltage filter time 4 | $t_{MOS_FLT4}$ | 4 | 5 | 6 | µs | 1) | PRQ-298 |
| **Drain to source monitoring threshold** | | | | | | | |
| Positive drain to source monitoring threshold 1 | $V_{DSTH_1_POS}$ | 80 | 100 | 120 | mV | – | PRQ-82 |
| Negative drain to source monitoring threshold 1 | $V_{DSTH_1_NEG}$ | -120 | -100 | -80 | mV | – | PRQ-417 |
| Positive drain to source monitoring threshold 2 | $V_{DSTH_2_POS}$ | 120 | 150 | 180 | mV | – | PRQ-83 |
| Negative drain to source monitoring threshold 2 | $V_{DSTH_2_NEG}$ | -180 | -150 | -120 | mV | – | PRQ-418 |
| Positive drain to source monitoring threshold 3 | $V_{DSTH_3_POS}$ | 160 | 200 | 240 | mV | – | PRQ-84 |
| Negative drain to source monitoring threshold 3 | $V_{DSTH_3_NEG}$ | -240 | -200 | -160 | mV | – | PRQ-419 |
| Positive drain to source monitoring threshold 4 | $V_{DSTH_4_POS}$ | 200 | 250 | 300 | mV | – | PRQ-85 |
| Negative drain to source monitoring threshold 4 | $V_{DSTH_4_NEG}$ | -300 | -250 | -200 | mV | – | PRQ-420 |
| Positive drain to source monitoring threshold 5 | $V_{DSTH_5_POS}$ | 240 | 300 | 360 | mV | – | PRQ-86 |
| Negative drain to source monitoring threshold 5 | $V_{DSTH_5_NEG}$ | -360 | -300 | -240 | mV | – | PRQ-421 |
| Positive drain to source monitoring threshold 6 | $V_{DSTH_6_POS}$ | 320 | 400 | 480 | mV | – | PRQ-87 |

**(table continues...)**

**Table 21 (continued) Electrical characteristics: protection and monitoring**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Negative drain to source monitoring threshold 6 | $V_{DSTH_6_NEG}$ | -480 | -400 | -320 | mV | – | PRQ-422 |
| Positive drain to source monitoring threshold 7 | $V_{DSTH_7_POS}$ | 400 | 500 | 600 | mV | – | PRQ-88 |
| Negative drain to source monitoring threshold 7 | $V_{DSTH_7_NEG}$ | -600 | -500 | -400 | mV | – | PRQ-423 |
| Positive drain to source monitoring threshold 8 | $V_{DSTH_8_POS}$ | 480 | 600 | 720 | mV | – | PRQ-89 |
| Negative drain to source monitoring threshold 8 | $V_{DSTH_8_NEG}$ | -720 | -600 | -480 | mV | – | PRQ-424 |
| **Gate to source monitoring threshold** | | | | | | | |
| Gate to source undervoltage threshold rising | $V_{GS_TH_RIS}$ | 5.8 | 7 | 8.5 | V | – | PRQ-144 |
| Gate to source undervoltage threshold falling | $V_{GS_TH_FAL}$ | 5.65 | 6.6 | 7.4 | V | – | PRQ-495 |
| Gate to source undervoltage threshold hysteresis | $V_{GS_UV_HYS}$ | 100 | 400 | 900 | mV | – | PRQ-496 |
| **Source overvoltage threshold** | | | | | | | |
| VSx overvoltage threshold | $V_{S_TH}$ | 3.5 | 5 | 6.5 | V | – | PRQ-145 |
| **VBAT undervoltage** | | | | | | | |
| VBAT_UV switch OFF voltage | $V_{BAT_UV_OFF}$ | 17.5 | 18.5 | 19.5 | V | – | PRQ-23 |
| VBAT_UV switch ON voltage | $V_{BAT_UV_ON}$ | 18 | 19 | 20 | V | – | PRQ-24 |
| VBAT_UV hysteresis | $V_{BAT_UV_HYS}$ | 0.3 | 0.5 | 0.7 | V | – | PRQ-431 |
| **VBAT overvoltage** | | | | | | | |
| VBAT_OV switch ON voltage | $V_{BAT_OV_ON}$ | 70 | 72 | 74 | V | – | PRQ-119 |
| VBAT_OV switch OFF voltage | $V_{BAT_OV_OFF}$ | 71 | 73 | 75 | V | – | PRQ-26 |
| VBAT_OV hysteresis | $V_{BAT_OV_HYS}$ | 0.5 | 1 | 2 | V | – | PRQ-432 |
| **VBAT undervoltage auto-restart duration** | | | | | | | |
| Undervoltage auto-restart time 1 | $t_{UV_RESTART1}$ | 0.8 | 1 | 1.2 | ms | 1) | PRQ-309 |

**(table continues...)**

**Table 21 (continued) Electrical characteristics: protection and monitoring**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Undervoltage auto-restart time 2 | $t_{UV_RESTART2}$ | 4 | 5 | 6 | ms | 1) | PRQ-310 |
| Undervoltage auto-restart time 3 | $t_{UV_RESTART3}$ | 16 | 20 | 24 | ms | 1) | PRQ-311 |
| Undervoltage auto-restart time 4 | $t_{UV_RESTART4}$ | 40 | 50 | 60 | ms | 1) | PRQ-312 |
| **VBAT overvoltage auto-restart duration** | | | | | | | |
| Overvoltage auto-restart time 1 | $t_{OV_RESTART1}$ | 10 | 13 | 16 | µs | 1) | PRQ-299 |
| Overvoltage auto-restart time 2 | $t_{OV_RESTART2}$ | 40 | 50 | 60 | µs | 1) | PRQ-301 |
| Overvoltage auto-restart time 3 | $t_{OV_RESTART3}$ | 160 | 200 | 240 | µs | 1) | PRQ-302 |
| Overvoltage auto-restart time 4 | $t_{OV_RESTART4}$ | 0.8 | 1 | 1.2 | ms | 1) | PRQ-303 |
| **Temperature warning and shutdown** | | | | | | | |
| Thermal warning junction temperature | $T_{JW}$ | 110 | 130 | 150 | °C | 1) | PRQ-48 |
| Thermal shutdown junction temperature | $T_{JSD}$ | 155 | 175 | 195 | °C | 1) | PRQ-49 |
| Thermal warning hysteresis | $T_{JW_HYS}$ | – | 10 | – | K | 1) | PRQ-405 |
| Thermal shutdown hysteresis | $T_{JSD_HYS}$ | – | 10 | – | K | 1) | PRQ-406 |
| **VDD undervoltage** | | | | | | | |
| VDD_UV switch ON voltage | $V_{DD_UV_ON}$ | – | – | 2.8 | V | – | PRQ-120 |
| **Ground loss** | | | | | | | |
| Ground loss | $\lvert V_{GND_LOSS}\rvert$ | 0.18 | 0.3 | 0.5 | V | – | PRQ-507 |

1) Not subject to production test, specified by design.

# 7 SPI

The device provides a SPI communication slave which uses the input lines SCLK, CSN and MOSI and the output line MISO.

The SPI uses a 16-bit protocol which transfers the MSB first and provides a daisy chain capability with other 16-bit SPI devices.

Any 16-bit data transfer starts by a falling edge on CSN.

While CSN is low, the incoming data on MOSI is sampled on the falling edge of SCLK while the outgoing data on MISO is shifted out on the rising edge of SCLK.

Each 16-bit data transfer is terminated by a rising edge on CSN.

The SPI includes a modulo 16 counter ensuring that data is taken only when a multiple of 16 bit has been transferred.

In case a wrong number of bit is transferred, or a wrong number of clock cycles is propagated, the SPI interface will generate a transmission error and it will not accept the data that has been just sent.

The system microcontroller selects the device by means of the CSN pin.

If CSN is high, the SPI ignores any signals at the SCLK and MOSI pins and forces the pin MISO into a high impedance state.

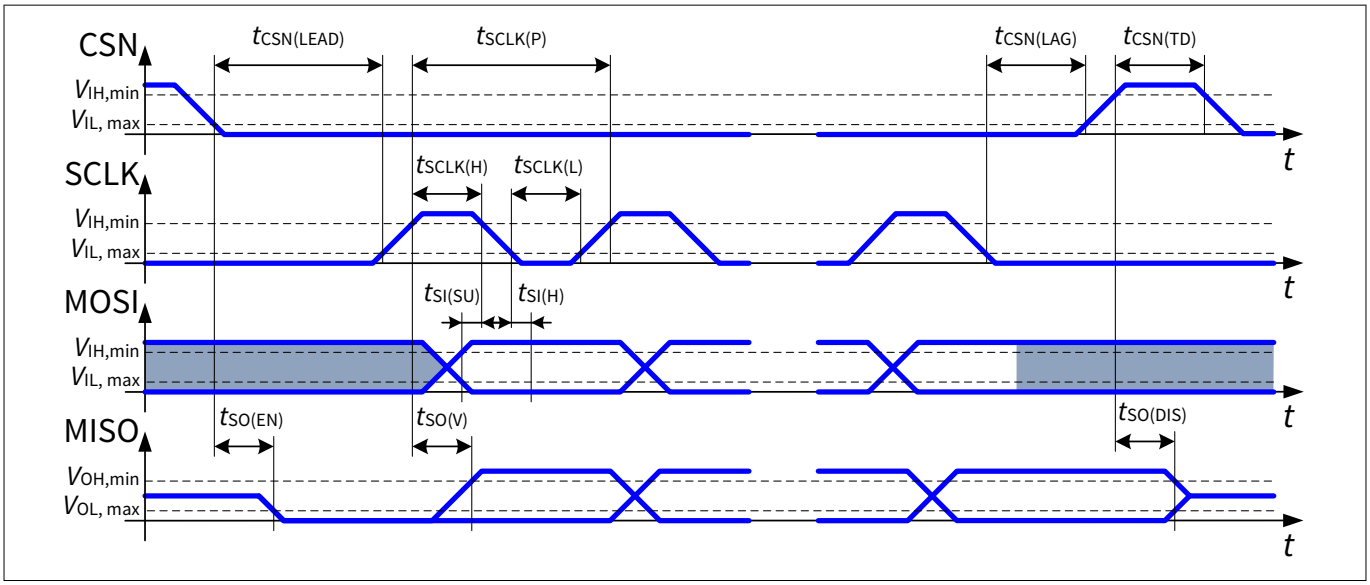



**Figure 10 SPI timings**

## 7.1 Communication start

While CSN is low, data transfer can take place.

If CSN changes from high to low and SCLK is low for $t_{CSN\ LEAD}$ or longer:

- The SPI transfers the information requested in the previous communications into the shift buffer
- The pin MISO changes from high impedance state to low state within $t_{SO(EN)}$
- The modulo16 counter starts counting SCLK clocks

*Note: CSN has to be kept low during the transfer of the whole communication frame.*

If SCLK changes from low to high while CSN is low:

- The MISO signals the bit shifted out of the shift buffer (first clock the MSB) after $t_{SO(V)}$

If SCLK changes from high to low while CSN is low:

- The data bits are shifted for one position to the MSB direction

- The MOSI signal is read into the shift buffer (at the LSB position) within $t_{SI(H)}$
- The modulo 16 counter is increased by 1

The SPI MOSI input has to be valid $t_{SI(SU)}$ before the falling edge of SCLK.

The clock circles with write, read and shift function have to be repeated, until the whole frame is read into the shift buffer (e.g. 16 repetitions for one SPI buffer).

## 7.2 Communication end

If CSN rises from low to high and the SCLK is low since $t_{CSN(LAG)}$, the value of the modulo 16 counter is checked.

If the modulo 16 counter signals a multiple (1,2,3...) of 16 SCLK clocks, the shift buffer data is executed as command (e.g. writing into the addressed register) within $t_{CSN(TD)}$.

MISO signals switches to high impedance within $t_{SO(DIS)}$ after CSN went high.

The SPI interface is ready to start a new transfer with a CSN to low transition if the time $t_{CSN(TD)}$ elapsed after the CSN went high.

## 7.3 SPI: electrical characteristics: timings

Unless otherwise specified: VBAT and VDD inside the normal operation range; $T_J$ = -40°C to +150°C.

**Table 22 SPI electrical characteristics: timings**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Transfer delay time | $t_{CSN(TD)}$ | 400 | – | – | ns | 1) | PRQ-370 |
| Enable lead time | $t_{CSN(LEAD)}$ | 200 | – | – | ns | 1) | PRQ-371 |
| Enable lag time | $t_{CSN(LAG)}$ | 200 | – | – | ns | 1) | PRQ-372 |
| Output enable time | $t_{SO(EN)}$ | – | 100 | 150 | ns | 1) $C_{load}$ = 100 pF | PRQ-373 |
| Output disable time | $t_{SO(DIS)}$ | – | 100 | 150 | ns | 1) $C_{load}$ = 100 pF | PRQ-374 |
| Serial clock high time | $t_{SCLK(H)}$ | 90 | – | – | ns | 1) | PRQ-375 |
| Serial clock low time | $t_{SCLK(L)}$ | 90 | – | – | ns | 1) | PRQ-376 |
| **SPI frequency** | | | | | | | |
| Serial clock frequency | $f_{SCLK}$ | 0.5 | – | 5 | MHz | 1) | PRQ-377 |
| Serial input setup time | $t_{SI(SU)}$ | 20 | – | – | ns | 1) | PRQ-426 |
| Serial input hold time | $t_{SI(H)}$ | 20 | – | – | ns | 1) | PRQ-427 |
| Serial output valid time | $t_{SO(V)}$ | – | 100 | 150 | ns | 1) $C_{load}$ = 100 pF | PRQ-428 |
| SCLK duty cycle | $DC_{SCLK}$ | 47 | 50 | 53 | % | 1) | PRQ-478 |

1) Not subject to production test, specified by design.

## 7.4 Daisy Chain

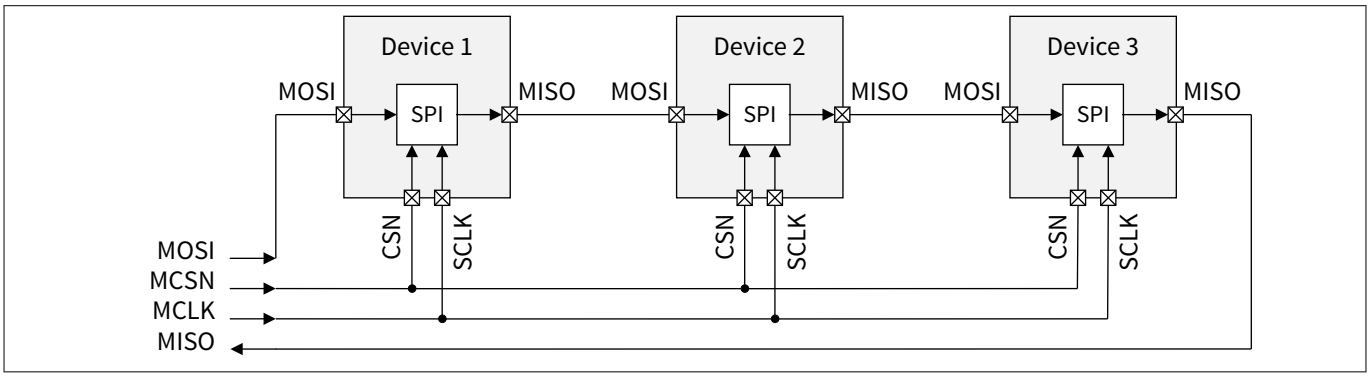



**Figure 11 Daisy chain capability**

The SPI of the device provides daisy chain capability for modulo 16 bit SPI devices. In this configuration several devices are activated by the same CSN signal, called MCSN. The MOSI line of one device is connected with the MISO line of another device (see Figure 11), in order to build a chain. The end of the chain is connected to the input of the microcontroller, the output of the microcontroller to the beginning of the chain. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

The microcontroller must set the MCSN to low and start the communication with a multiple of 16 bit data, the multiplier is the number of chained devices. The first data sent goes to the last devices (device 3 in Figure 11) with the last bit transferred. After the communication is finished the MCSN must go to high again.

*Note: A wrong number of master serial clocks will generate a transmission error from all devices in the chain.*

## 7.5 SPI Protocol

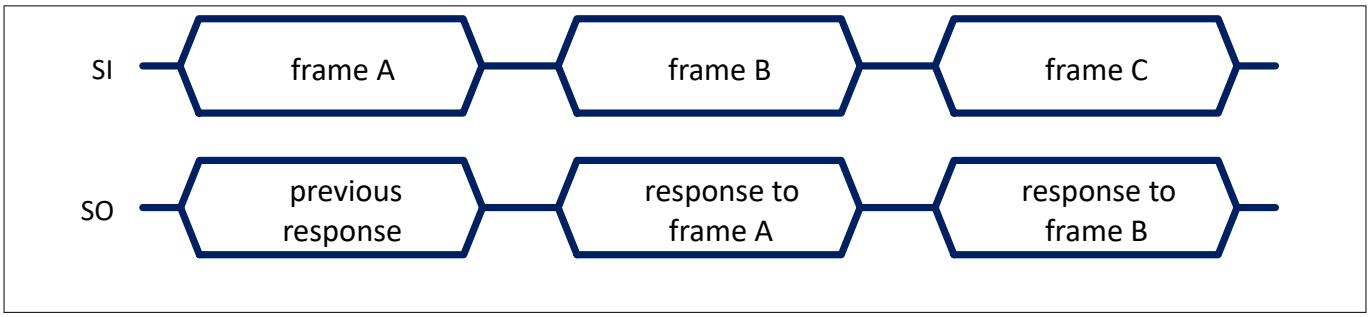



**Figure 12 Command response sequence**

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the microcontroller.

The relationship between MOSI and MISO content during SPI communication is shown in Figure 12.

MOSI line represents the frame sent from the microcontroller and MISO line is the answer provided by the gate driver SPI. The “previous response” means that the frame sent back depends on the command frame sent from the microcontroller before.

The responses of write commands are deterministic and are reporting the default diagnosis register.

The responses of a read command are the required register.

In case of transmission error the default response is the diagnosis register with the transmission error bit set to 1.

The SPI word is 16 bit wide and is structured according to the following tables.

Word from microcontroller:

| Read/Write | Address | | | | | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R/W | A6/nu | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Response from SPI interface :

| Trans ERROR | Address | | | | | | | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TER | A6/nu | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

A6..A0 are used to address a register, D7..D0 are data.

*Note: Bit A6 is reserved for future use (default value 0).*

The microcontroller can access to the SPI registers using the 16 bit word as described below.
Write procedure :

- Set MSB to 1 (read/write bit)
- Addressing the register using A [6...0]
- Preparing the data in Data [7 ... 0]

Read procedure:

- Set MSB to 0 (read/write bit)
- Addressing the register using A [6...0]
- Data bits are don't care

Any communication of the microcontroller with the SPI interface is responded by the SPI interface.
In any case the response will report the transmission error bit TER as MSB representing the validity of the previous communication.

**Table 23 TER bit**

| TER bit | Communication status |
|---|---|
| 1 | Error in the previous communication |
| 0 | No error in the previous communication |

After a reset as described in Chapter 4.2.4, the TER bit in the response to the first command is set high, to inform the master that this is the first communication.

Beside the TER bit, the response to a microcontroller communication contains:

- In case of a write command: the standard diagnosis (address 00000b).
- In case of a read command: the data in the addressed register. In this case, the answer will contain both the address of the register and the data there contained.

The answer is on the next frame, as explained in Figure 12.

The first response after power on is by default the standard diagnosis register content. Within the information the $V_{DD_UV}$ is set to 1 in order to inform about the power off situation before the communication.

# 8 Register specification

## 8.1 Control registers

| Address | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register Name | Register Functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | R | FAILURE | VCP_READY | MEM_FAIL | OT_WARNING | TSD | VDD_UV | VBAT_UV | VBAT_OV | **STDIAG** | General diagnosis (battery voltage status, VDD undervoltage, overtemperature, warning temperature, overcurrent, cp_ready, power management ok) |
| 1 | R | VCP_UV | ITRIP | VGSTH_B | VDSTRIP_B | VSOURCE_B | VGSTH_A | VDSTRIP_A | VSOURCE_A | **CHDIAG** | Channel specific diagnosis (gate source voltage, drain source voltage, source overvoltage) |
| 2 | R | | | | LOG_A | LOG_D | LOG_CP | ADD_NOT_AV | SAFESTATEN | **DIAG** | Diagnosis |
| 3 | WR | CHCRCTRL | ITRIP_CL | VGSTH_B_CL | VDSB_CL | MOSONCH_B | VGSTH_A_CL | VDSA_CL | MOSONCH_A | **MOS_CHS_CTRL** | Channels A and B activation and cleaning related failure |
| 4 | W | VCP_UV_CL | | SAFESTATE_CL | INT_CLEAN | TSD_CL | VDD_UV_CL | VBATUV_CL | VBATOV_CL | **FAILURE CLEAN** | Clean failures |
| 5 | WR | VDSB_SS | VDSTH_B | | | VDSA_SS | VDSTH_A | | | **VDSTHA_B** | Drain-source overvoltage threshold - channel A and channel B |
| 6 | WR | MOSBLK_B | | MOSFLT_B | | MOSBLK_A | | MOSFLT_A | | **MOSFLTBLKA_B** | MOS voltage filter and blank time - channel A and channel B |
| 7 | WR | | CSA_OUTSEL | CSA_HSS | OCTH | | CSAG | | | **CSAG_OCTH** | Current sense amplifier gain $G_{DIFF}$ and overcurrent detection thresholds |
| 8 | WR | | | | | VBATUVARST | | VBATOVARST | | **VBATOVUVRST** | VBAT overvoltage and undervoltage auto-restart time |
| 9 | W | | | FAIL_RST_1 | SFT_RST_1 | | GEN_INTERRUPT | FAIL_RST_0 | SFT_RST_0 | **RESETS** | Reset Register |
| 10 | WR | SPARE_7 | SPARE_6 | SPARE_5 | SPARE_4 | SPARE_3 | SPARE_2 | SPARE_1 | SPARE_0 | **SPARE_REG** | Spare Register |

**Figure 13 Registers overview**

**Table 24 Bit descriptions**

| Register Name | Bit | Bit name | Description |
|---|---|---|---|
| STDIAG | 7 | FAILURE | Main failure indication, 1 when there is a failure |
| | 6 | VCP_READY | Charge pump is ready |
| | 5 | MEM_FAIL | Error in the memory, trimming not possible (flag cannot be cleaned) |
| | 4 | OT_WARNING | Temperature warning |
| | 3 | TSD | Chip in overtemperature (latched) |
| | 2 | VDD_UV | VDD undervoltage propagated in the first command and indicates an under voltage event |
| | 1 | VBAT_UV | VBAT undervoltage failure (not latched) |
| | 0 | VBAT_OV | VBAT overvoltage failure (not latched) |
| CHDIAG | 7 | VCP_UV | Charge pump undervoltage |
| | 6 | ITRIP | Overcurrent failure (latched) |
| | 5 | VGSTH_B | Gate-source undervoltage - channel B (latched) |
| | 4 | VDSTRIP_B | Drain to source overvoltage - channel B (latched) |
| | 3 | VSOURCE_B | Source overvoltage - channel B |
| | 2 | VGSTH_A | Gate-source undervoltage - channel A (latched) |
| | 1 | VDSTRIP_A | Drain to source overvoltage - channel A (latched) |
| | 0 | VSOURCE_A | Source overvoltage - channel A |
| DIAG | 4 | LOG_A | Loss of ground connection on AGND |
| | 3 | LOG_D | Loss of ground connection on GND |
| | 2 | LOG_CP | Loss of ground connection on CPGND |
| | 1 | ADD_NOT_AVAIL | Address not available |
| | 0 | SAFESTATEN | Reflection of the SAFESTATEN pin |
| MOS_CHS_CTRL | 7 | CHCRCTRL | Channel cross control activation |
| | 6 | ITRIP_CL | Clear ITRIP flag |
| | 5 | VGSTH_B_CL | Clear VGS flag channel B |
| | 4 | VDSB_CL | Clear VDS flag channel B |
| | 3 | MOSONCH_B | Switch on channel B |
| | 2 | VGSTH_A_CL | Clear VGS flag channel A |
| | 1 | VDSA_CL | Clear VDS flag channel A |
| | 0 | MOSONCH_A | Switch on channel A |
| FAILURE CLEAN | 7 | VCP_UC_CL | Clear charge pump undervoltage failure |
| | 5 | SAFESTATE_CL | Clear Safestate failure |
| | 4 | INT_CLEAN | Clear interrupt |
| | 3 | TSD_CL | Clear overtemperature failure |
| | 2 | VDD_UV_CL | Clear VDD undervoltage failure |

**(table continues...)**

**Table 24 (continued) Bit descriptions**

| Register Name | Bit | Bit name | Description |
|---|---|---|---|
| | 1 | VBATUV_CL | Clear VBAT overvoltage failure |
| | 0 | VBATOV_CL | Clear VBAT undervoltage failure |
| VDSTHA_B | 7 | VDSB_SS | VDS channel B safe state on when 1. VDS safe state off when 0. |
| | [6:4] | VDSTH_B | Drain-source overvoltage threshold channel B |
| | 3 | VDSA_SS | VDS channel A safe state on when 1. VDS safe state off when 0. |
| | [2:0] | VDSTH_A | Drain-source overvoltage threshold channel A |
| MOSFLTBLKA_B | [7:6] | MOSBLK_B | MOS voltage blank time channel B |
| | [5:4] | MOSFLT_B | MOS voltage filter time channel B |
| | [3:2] | MOSBLK_A | MOS voltage blank time channel A |
| | [1:0] | MOSFLT_A | MOS voltage filter time channel A |
| CSAG_OCTH | 6 | CSA_COUTSEL | Configures the current sense amplifier output stage depending on the output capacitor |
| | 5 | CSA_HSS | Control signal to select the CSA configuration LSS or HSS (or bidirectional) |
| | [4:3] | OCTH | Overcurrent detection thresholds |
| | [2:0] | CSAG | Current sense amplifier gain $G_{DIFF}$ |
| VBATOVUVRST | [3:2] | VBATUVARST | VBAT undervoltage auto-restart time |
| | [1:0] | VBATOVARST | VBAT overvoltage auto-restart time |
| RESETS | 5 | FAIL_RST_1 | Reset Fails registers 1 |
| | 4 | SFT_RST_1 | Software Reset 1 |
| | 2 | GEN_INTERRUPT | Generate interrupt signal |
| | 1 | FAIL_RST_0 | Reset Fails registers 0 |
| | 0 | SFT_RST_0 | Software Reset 0 |
| SPARE_REG | 7 | SPARE_7 | Spare register bit 7 |
| | 6 | SPARE_6 | Spare register bit 6 |
| | 5 | SPARE_5 | Spare register bit 5 |
| | 4 | SPARE_4 | Spare register bit 4 |
| | 3 | SPARE_3 | Spare register bit 3 |
| | 2 | SPARE_2 | Spare register bit 2 |
| | 1 | SPARE_1 | Spare register bit 1 |
| | 0 | SPARE_0 | Spare register bit 0 |

# 9 Application information

## 9.1 48 V battery protection switch with low-side current sense and capacitive pre-charge

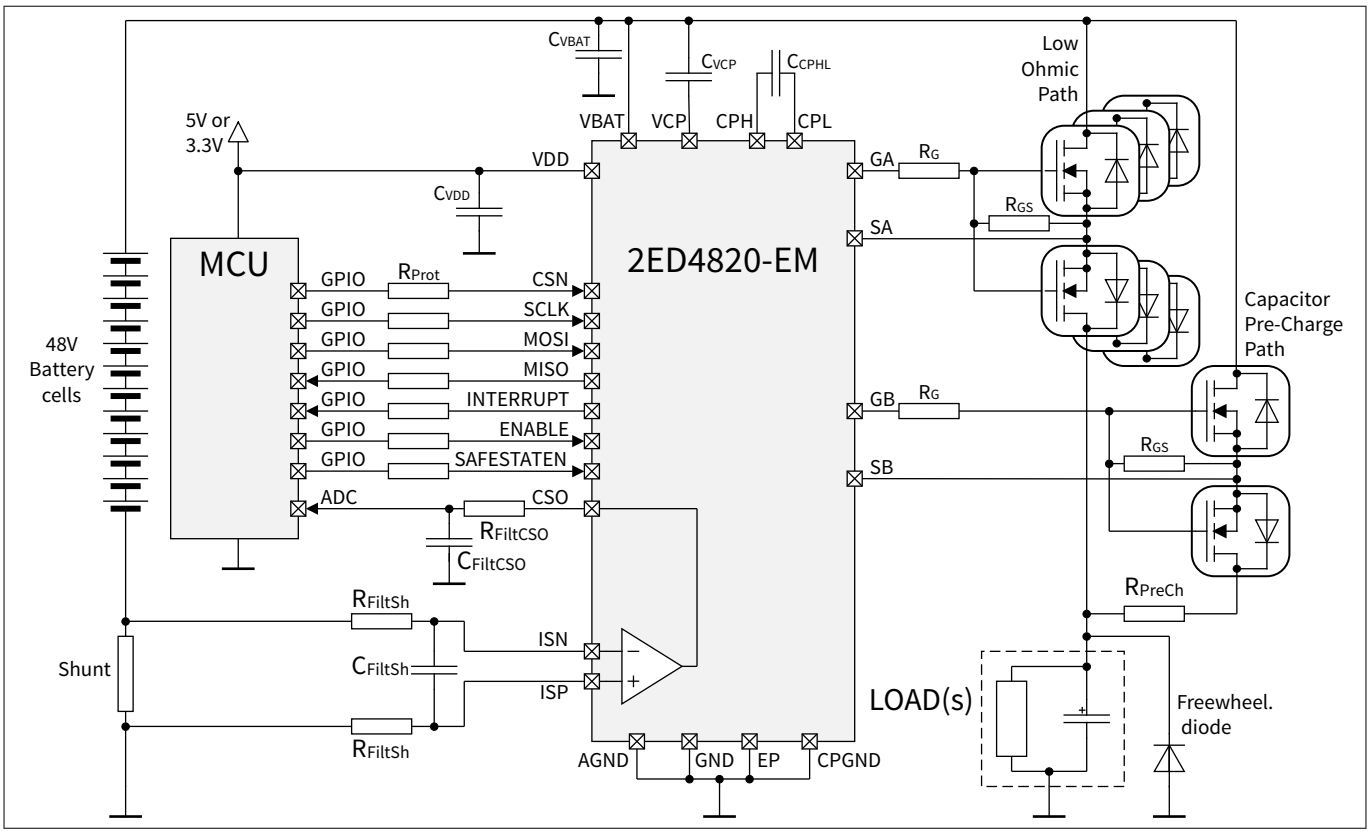



**Figure 14 48 V battery protection switch application diagram**

## 9.2 Common drain with high-side current sense

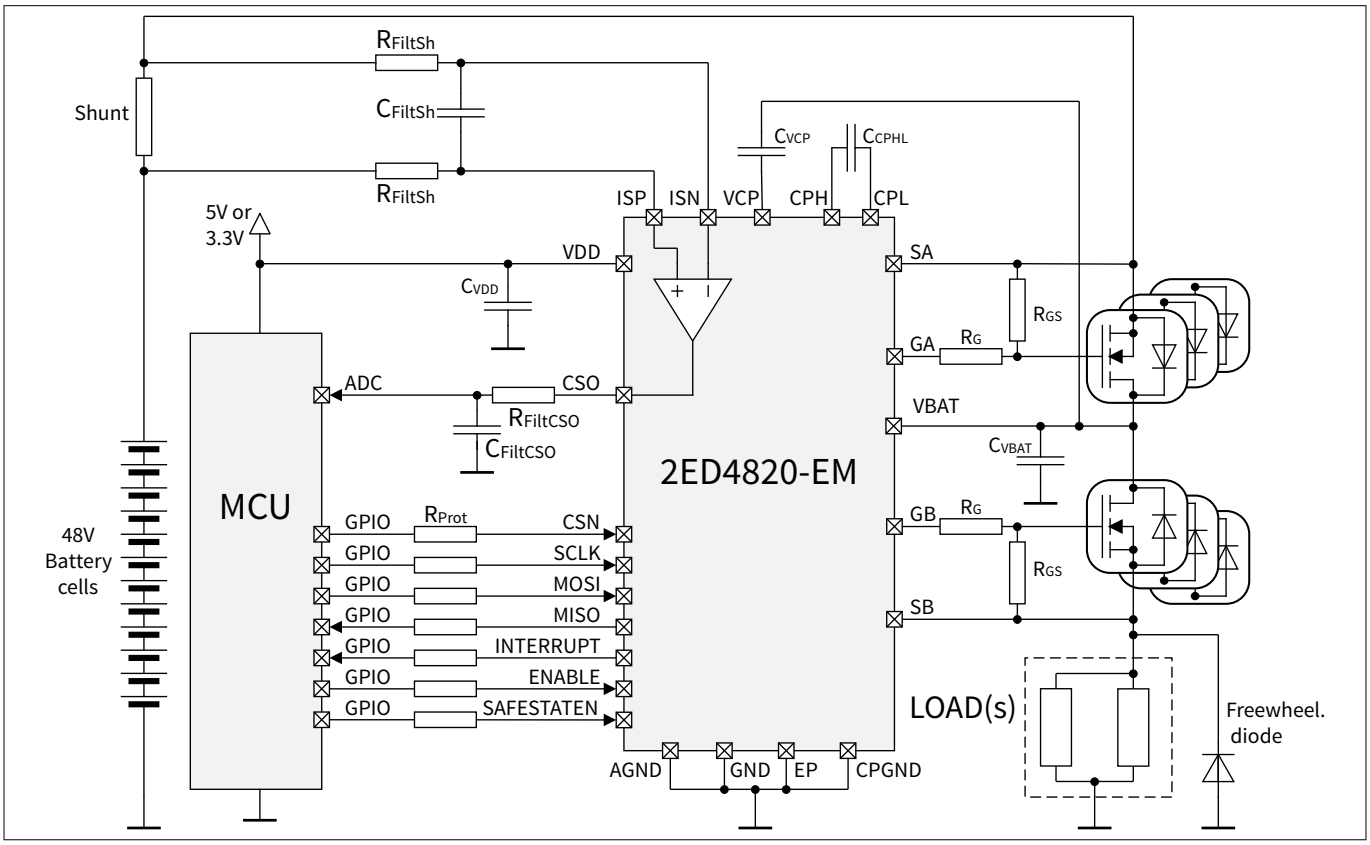



**Figure 15 Common drain with high-side current sense application diagram**

## 9.3 Bill of material

Supply pins have to be decoupled with ceramic capacitors, positioned as follows:

- $C_{VBAT}$ close to VBAT and AGND pins
- $C_{VDD}$ close to VDD and GND pins
- $C_{VCP}$ close to VCP and VBAT pins

**Table 25 Bill of material**

| Reference | Value | Purpose |
|---|---|---|
| $R_{Prot}$ | 1.0 kΩ | Protection of the microcontroller |
| $C_{VDD}$ | 1.0 µF | Supply decoupling; on layout, located close to the VDD & GND pins |
| $C_{VBAT}$ | 4.7 µF + 220 nF | Supply decoupling; on layout, located close to the VBAT & AGND pins |
| $C_{VCP}$ | 2.2 µF | Charge pump output capacitor - value depends on number of MOSFETs to drive |
| $C_{CPHL}$ | 220 nF | Charge pump capacitor |
| $R_G$ | 10.0 Ω | Gate protection resistor |
| $R_{GS}$ | 150.0 kΩ | Gate to source pull-down resistor |
| $R_{PreCh}$ | 10.0 Ω | Power resistor limiting the capacitor pre-charge current |

**(table continues...)**

**Table 25 (continued) Bill of material**

| | | |
|---|---|---|
| $R_{FiltCSO}$ | 10.0 kΩ | Protection of the microcontroller and low pass filter on current sense output |
| $C_{FiltCSO}$ | 10 nF | Low pass filter on current sense output - value depends on bandwidth required |
| $R_{FiltSh}$ | 4.7 Ω | Filter to cancel the inductive part of the shunt - value depends on Shunt |
| $C_{FiltSh}$ | 1 µF | Filter to cancel the inductive part of the shunt - value depends on Shunt |

# 10 Package

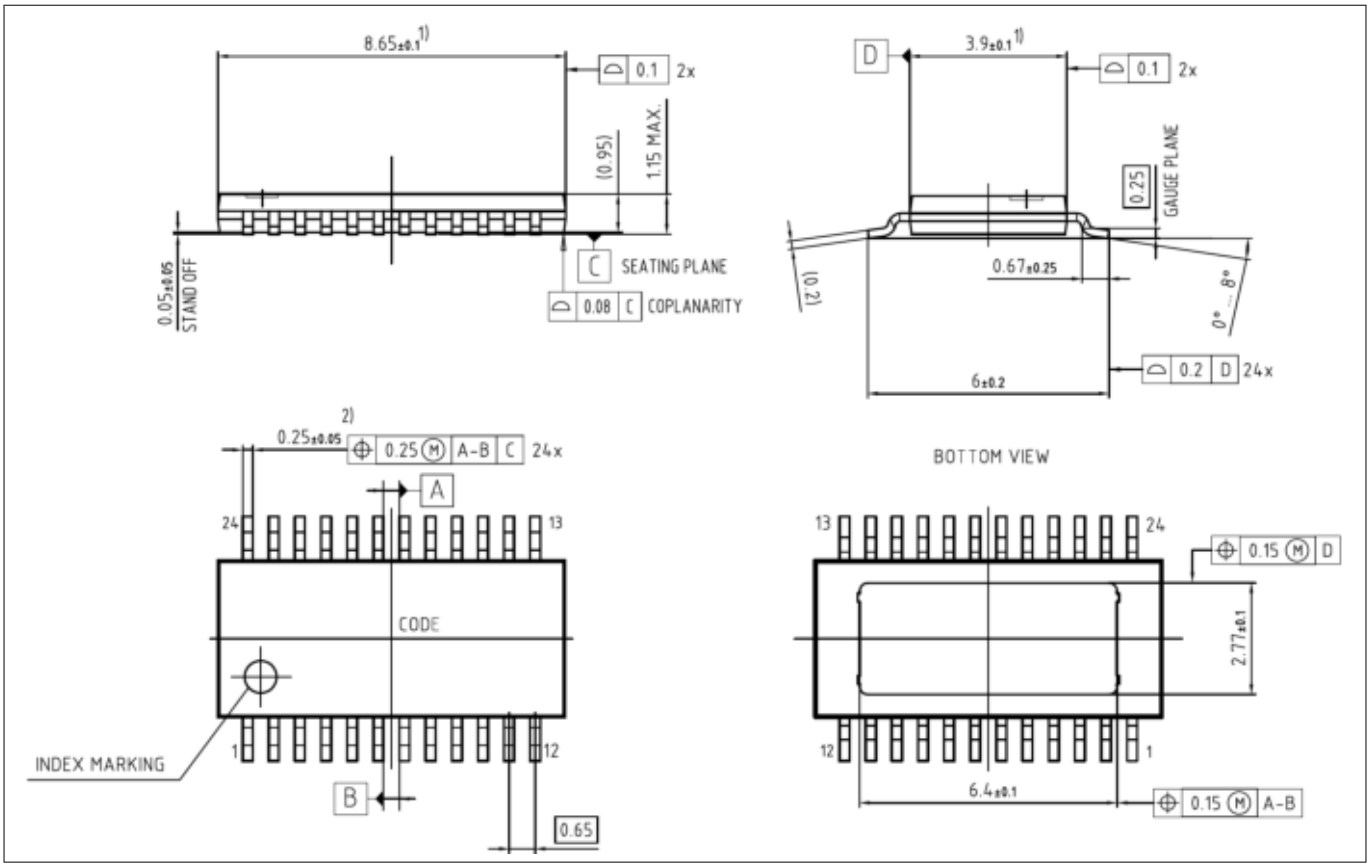



**Figure 16 Package dimensions**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| Rev.1.10 | 2022-12-20 | • Updated Block diagram, Figure 2<br>• Added PRQ-544 in Chapter 5.3<br>• Improved CMRR performance Chapter 6.3.3.9.5 → PRQ-64, PRQ-148, PRQ-149, PRQ-150, PRQ-210, PRQ-211, PRQ-212, PRQ-213 |
| Rev.1.00 | 2021-07-23 | • Datasheet creation |

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