

MOSFET

OptiMOS™ 3 Power-Transistor, 120 V

Features

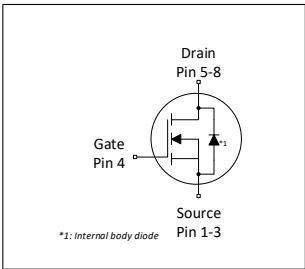
- N-channel, logic level
- 100% avalanche tested
- Excellent gate charge x RDS(on) product (FOM)
- Very low on-resistance RDS(on)
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	120	V
$R_{DS(on),max}$	12	mΩ
I_D	68	A
Q_{oss}	51	nC
$Q_G(0V..10V)$	51	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC0303LS	PG-TDSON-8	0303LS	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	68 53 10	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=45\text{ °C/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	274	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	155	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	114	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.64	1.1	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	18	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁽²⁾	R_{thJA}	-	-	45	°C/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.85	2.4	V	$V_{DS}=V_{GS}$, $I_D=72\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.01 10	1 100	μA	$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	9.8 11.7	12.0 14.2	m Ω	$V_{GS}=10\text{ V}$, $I_D=34\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=17\text{ A}$
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance	g_{fs}	42	81	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=34\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	3700	4900	pF	$V_{GS}=0\text{ V}$, $V_{DS}=60\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	380	495	pF	$V_{GS}=0\text{ V}$, $V_{DS}=60\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	19	25	pF	$V_{GS}=0\text{ V}$, $V_{DS}=60\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	5	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	22	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	6	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=17\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	11.4	-	nC	$V_{DD}=60\text{ V}$, $I_D=17\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	8.4	-	nC	$V_{DD}=60\text{ V}$, $I_D=17\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	13.1	-	nC	$V_{DD}=60\text{ V}$, $I_D=17\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	51	-	nC	$V_{DD}=60\text{ V}$, $I_D=17\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.1	-	V	$V_{DD}=60\text{ V}$, $I_D=17\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	51	-	nC	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	79	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	274	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.87	1.2	V	$V_{GS}=0\text{ V}$, $I_F=34\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	85	-	ns	$V_R=60\text{ V}$, $I_F=17\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	220	-	nC	$V_R=60\text{ V}$, $I_F=17\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

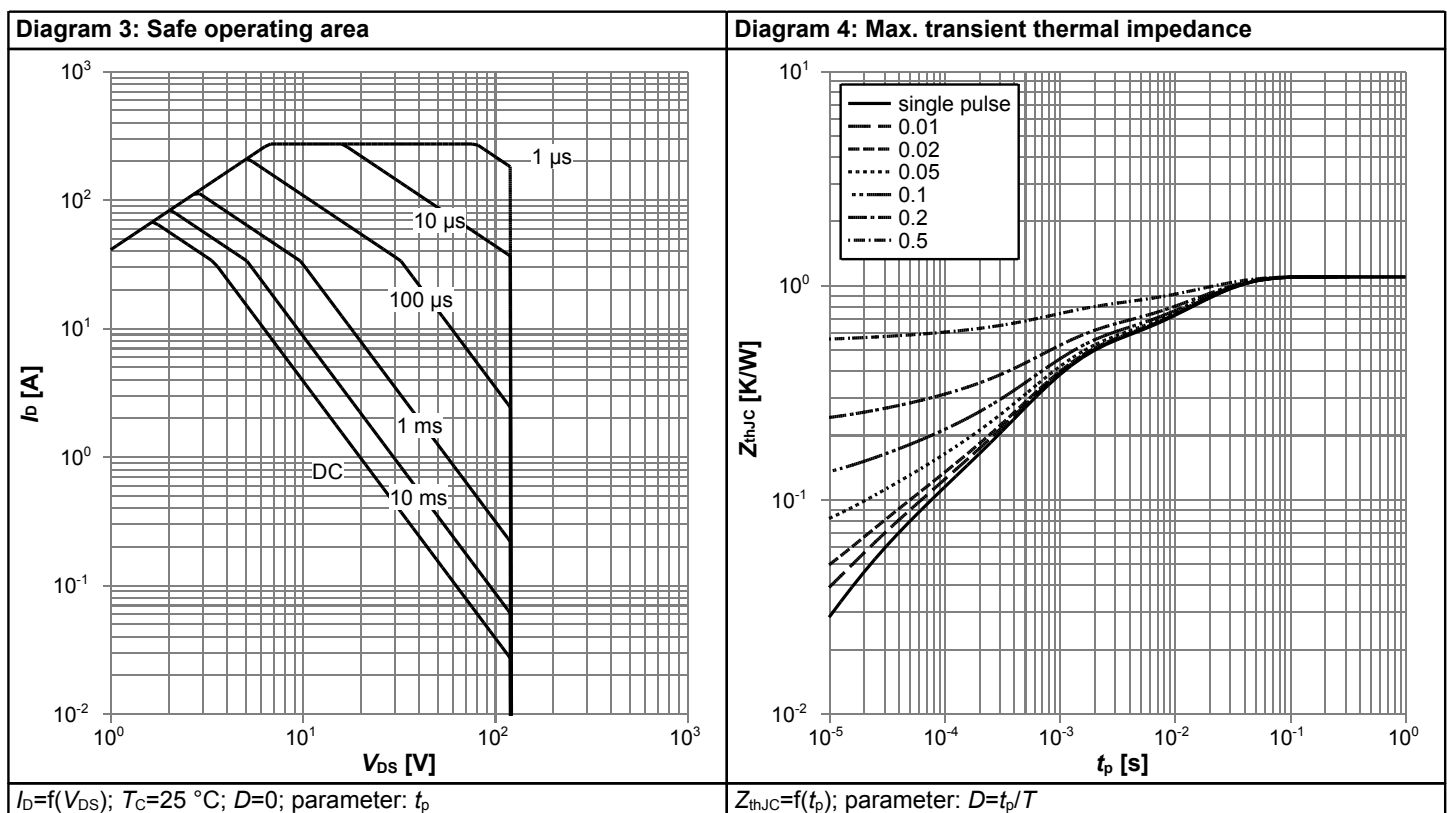
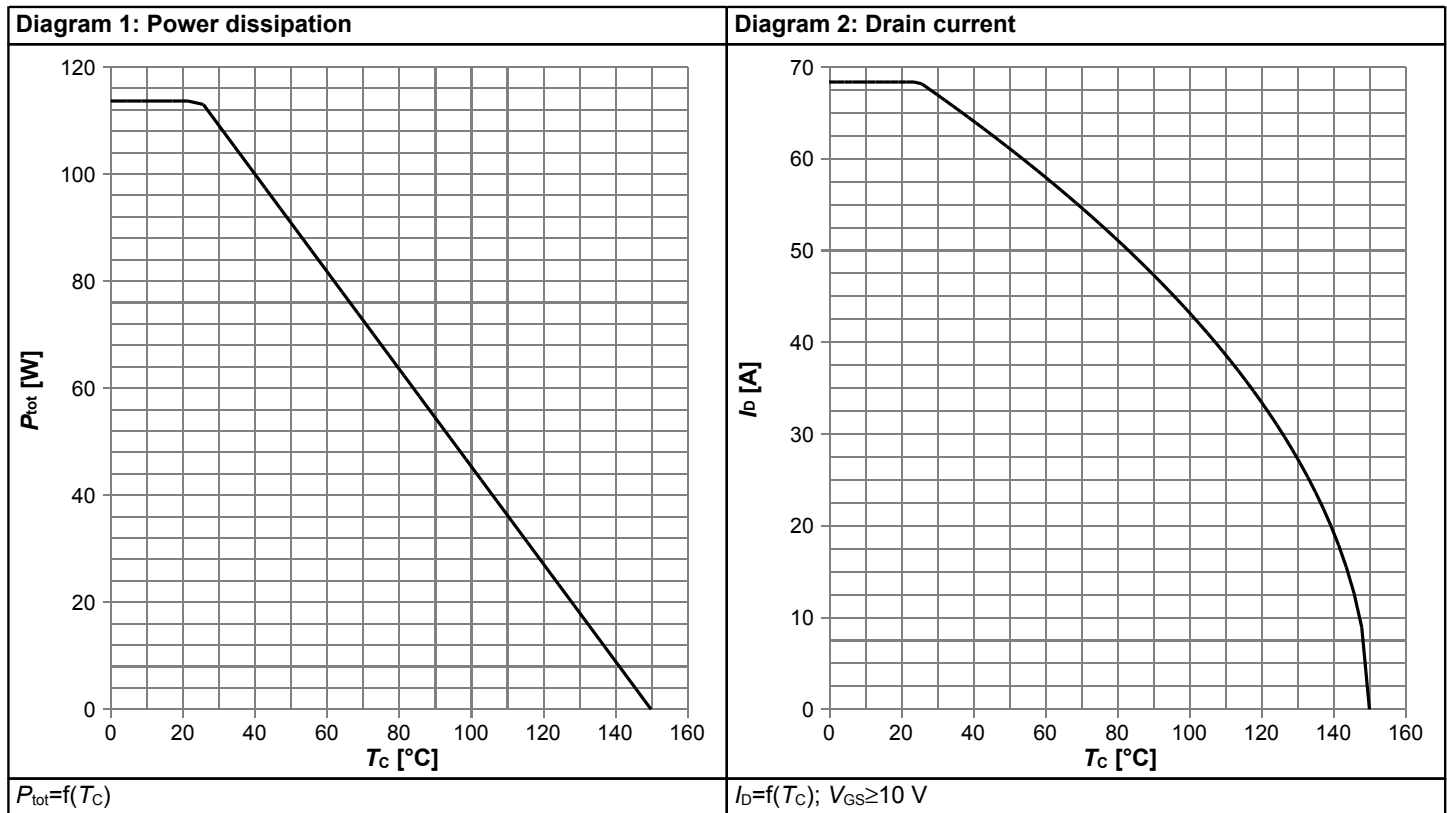
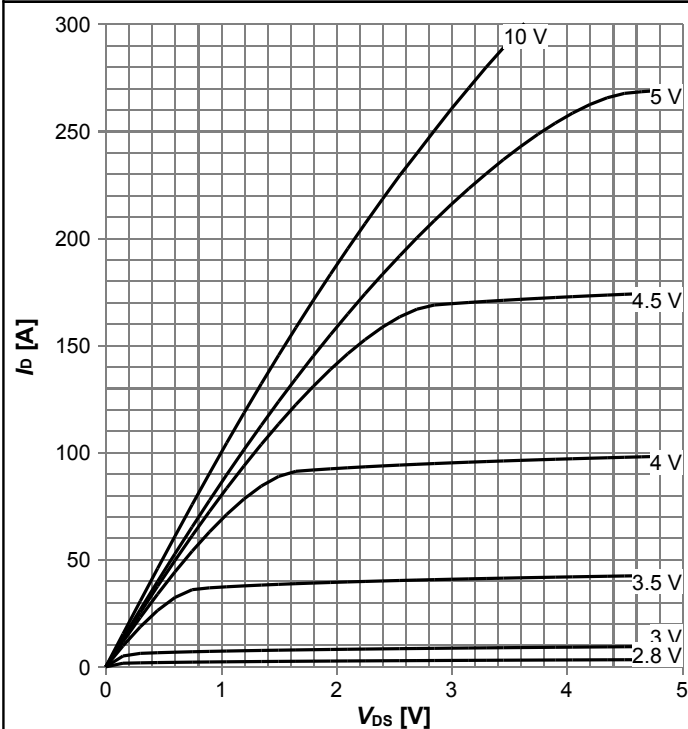
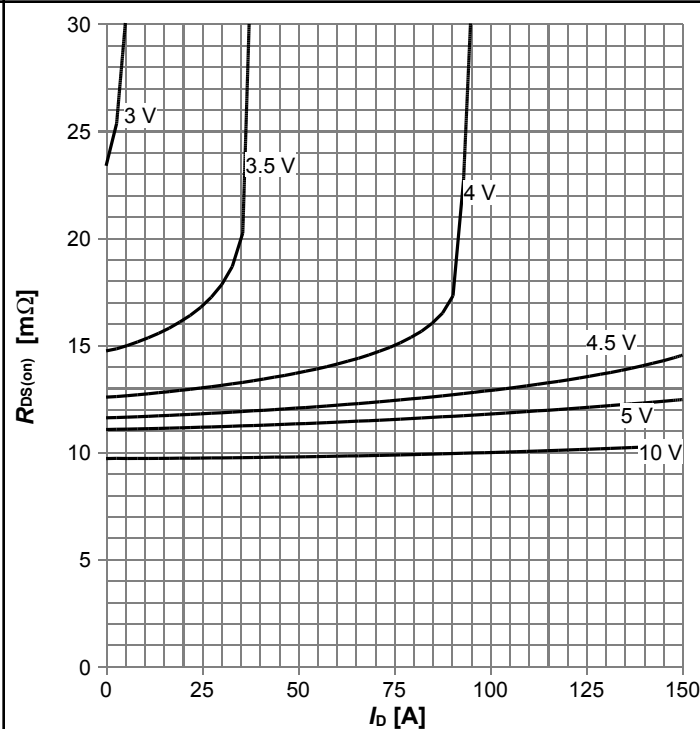


Diagram 5: Typ. output characteristics



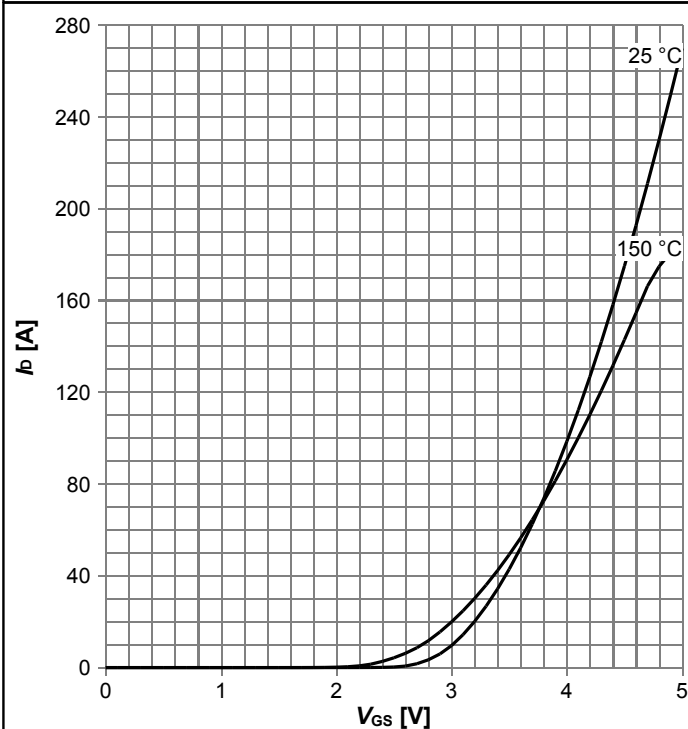
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



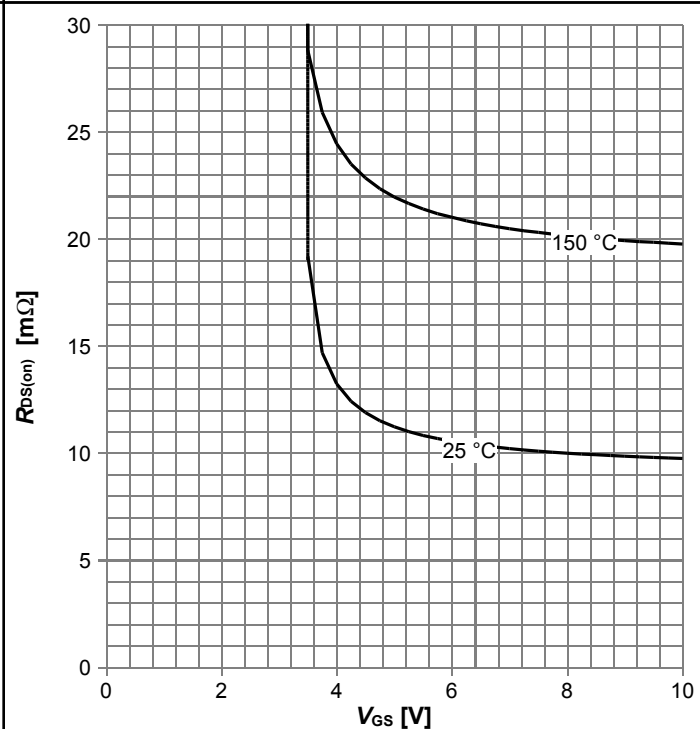
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



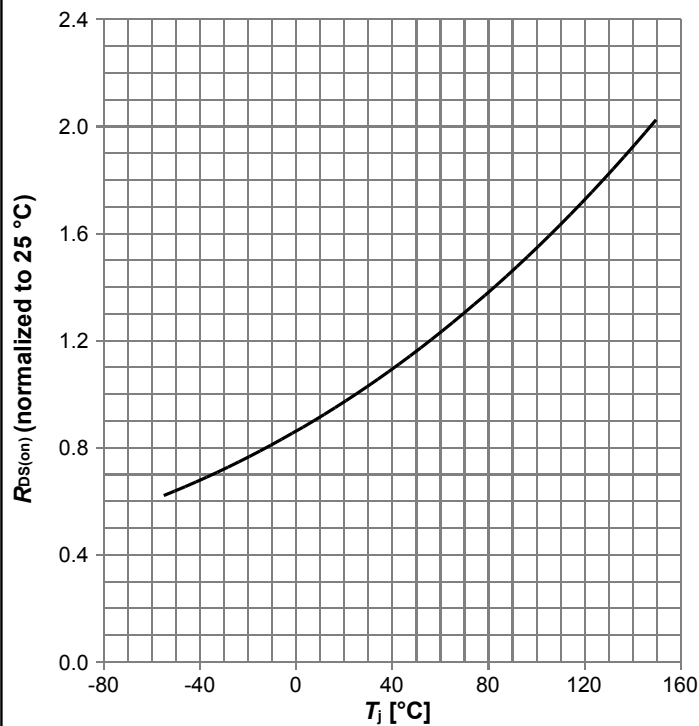
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



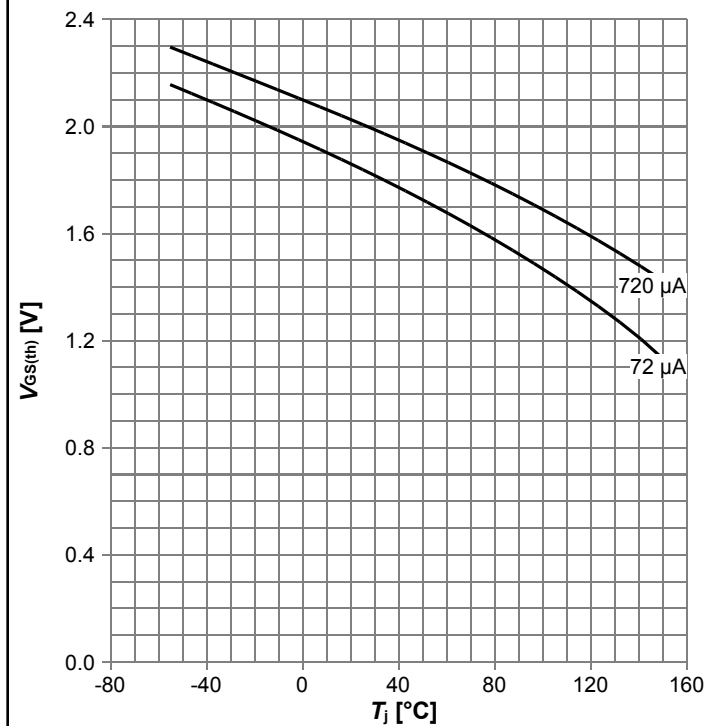
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



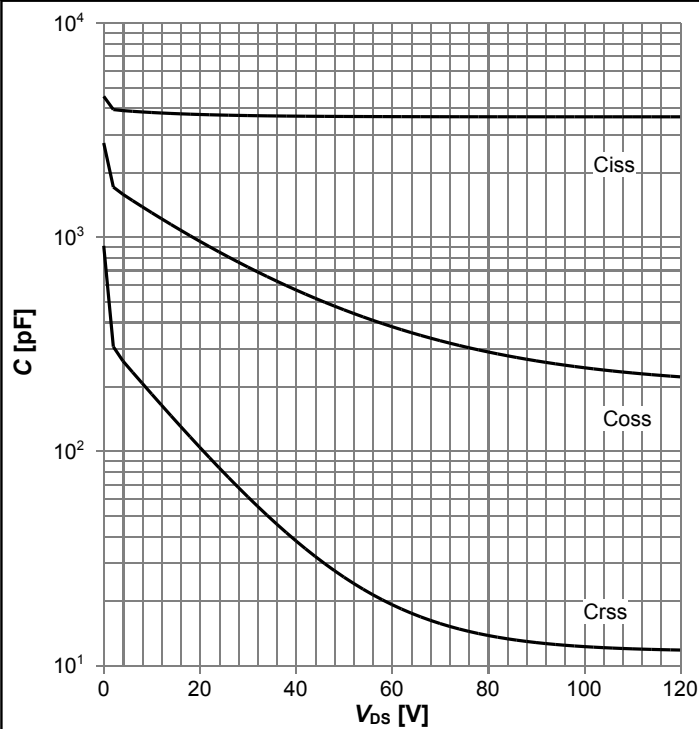
$$R_{DS(on)} = f(T_j), I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



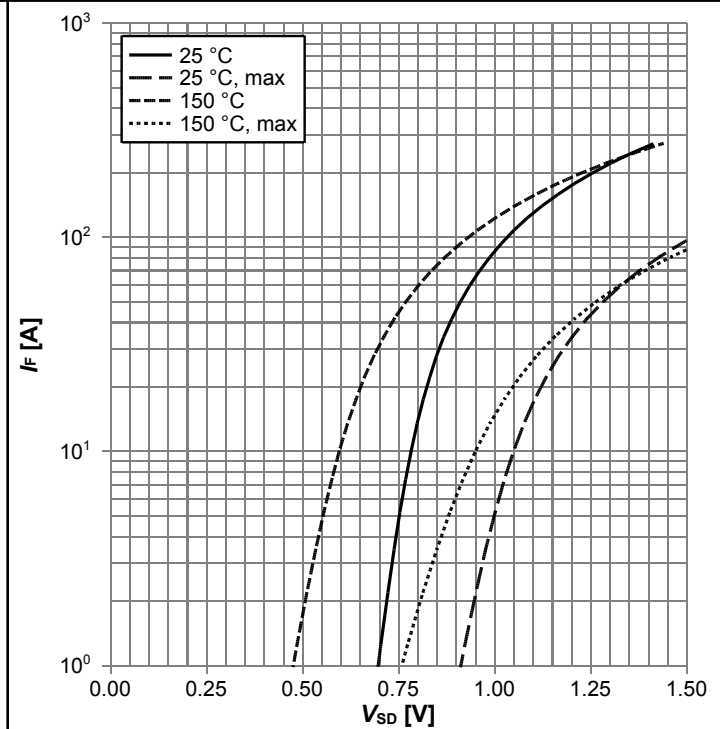
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



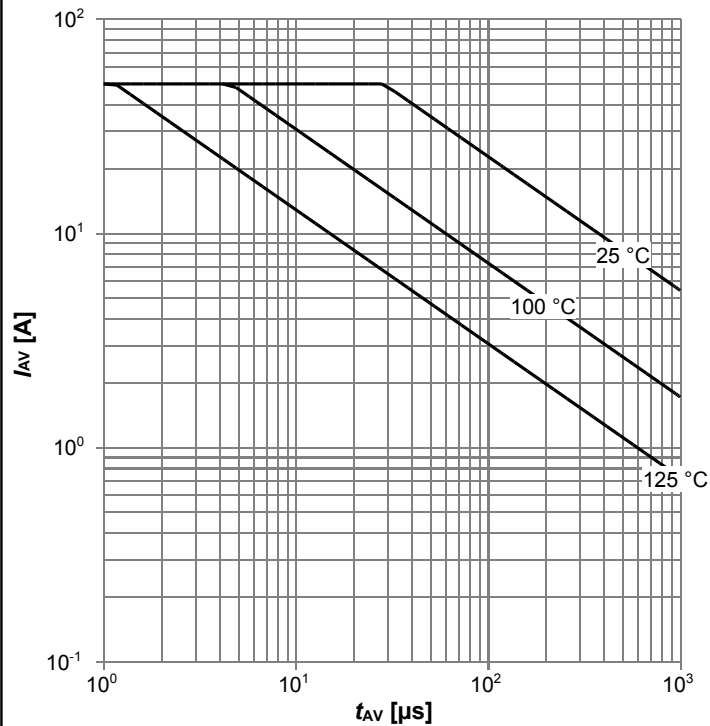
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



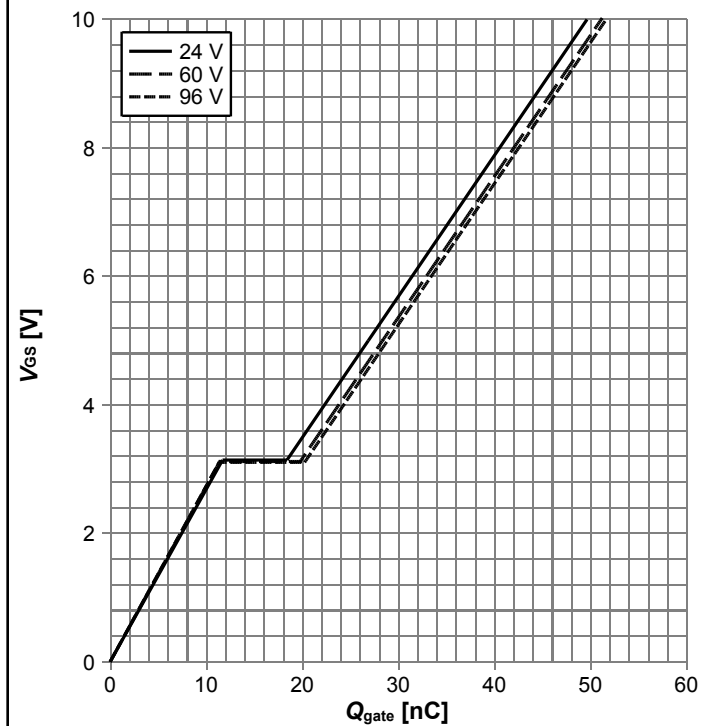
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



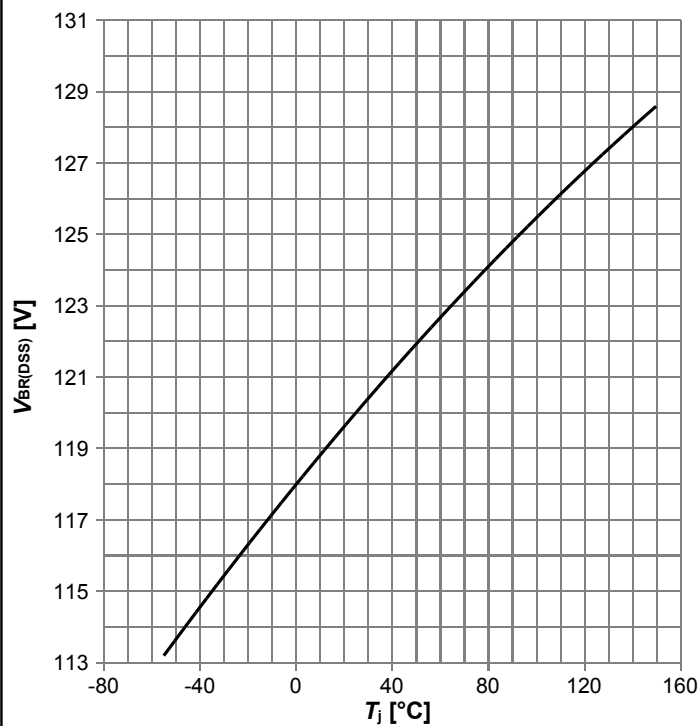
$I_{AS}=f(t_{AV})$; $R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



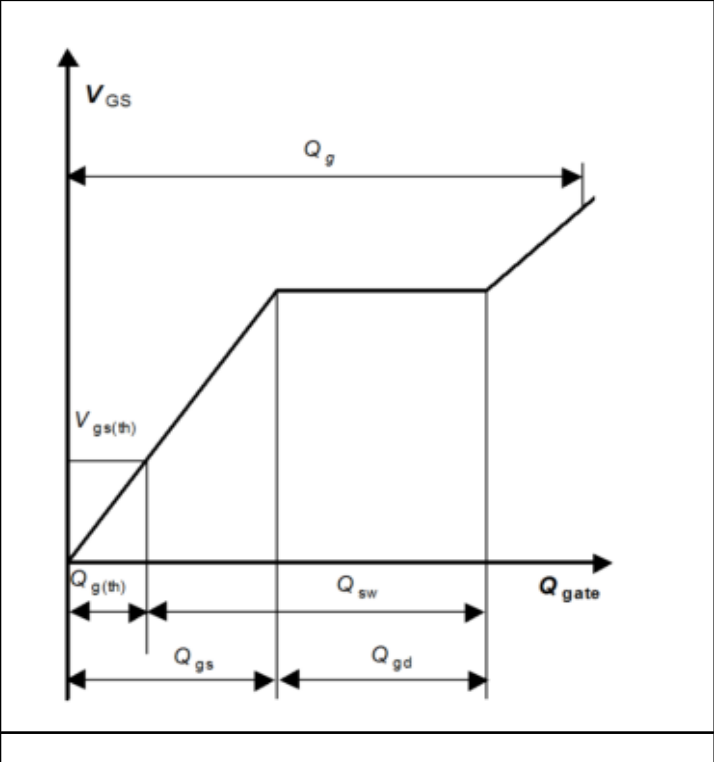
$V_{GS}=f(Q_{gate})$, $I_D=25 A$ pulsed, $T_j=25 \text{ }^\circ\text{C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines

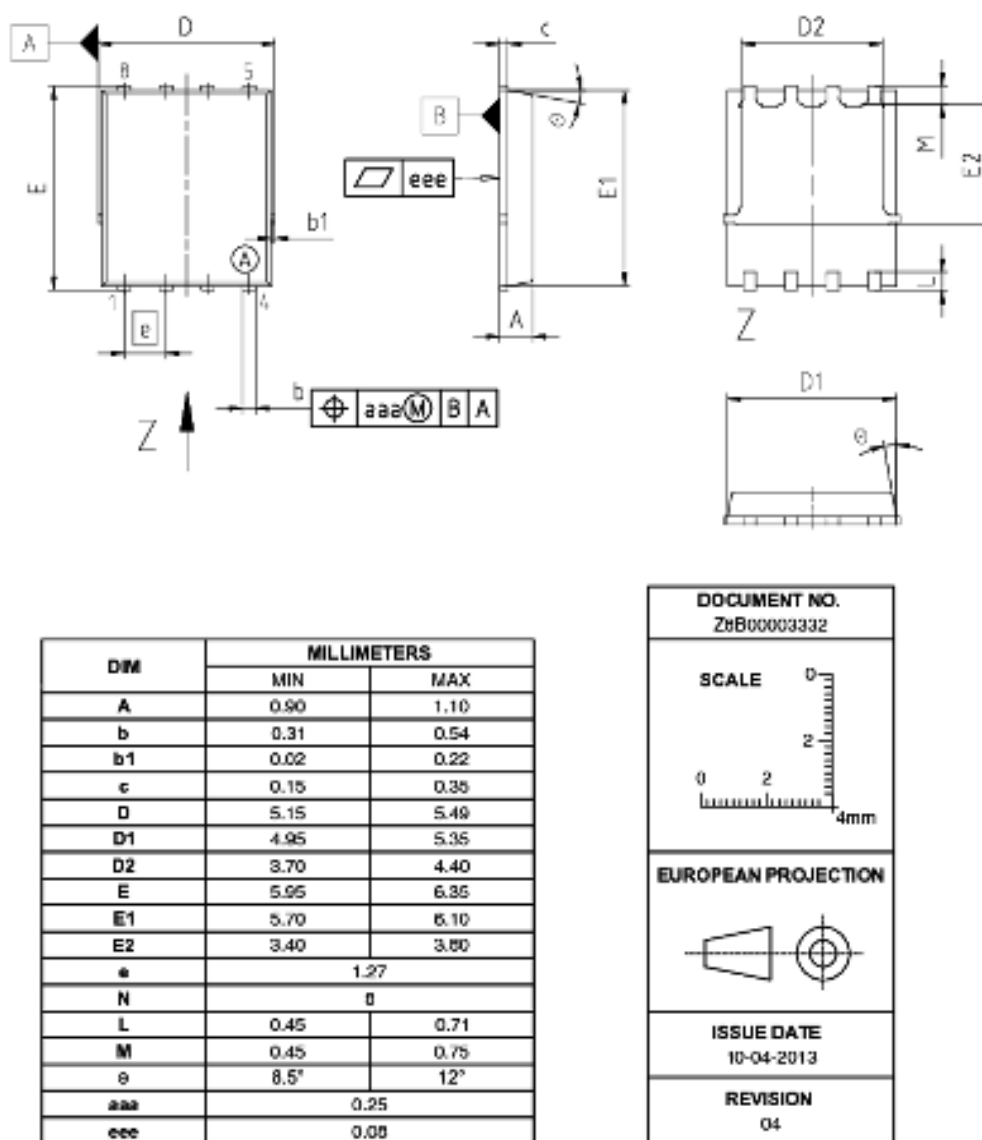


Figure 1 Outline PG-TDSON-8, dimensions in mm

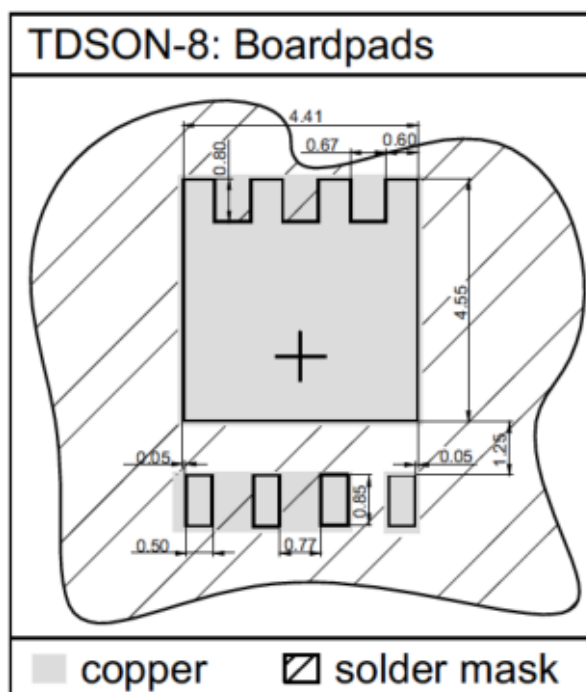


Figure 2 Outline Footprint (TDSON-8)



Rev. 2.1, 2022-08-09

Revision History

BSC0303LS

Revision: 2022-08-09, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-12-02	Release of final version
2.1	2022-08-09	Update "Features", qualification, footnotes and fix bug.

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