# CY62137EV30 MoBL®

# 2-Mbit (128 K × 16) Static RAM

## Features

- Very high speed: 45 ns
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62137CV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Byte power-down feature
- Offered in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP II) package

## Functional Description

The CY62137EV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can also be put into standby mode reducing power consumption when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input and output pins ($I/O_0$ through $I/O_{15}$) are placed in a high impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

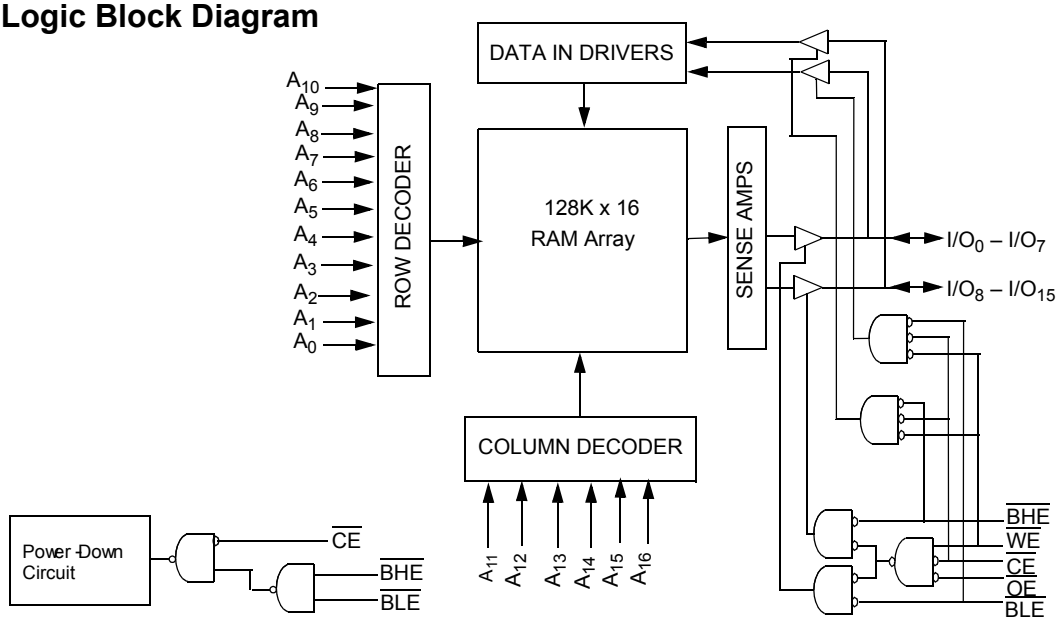
Writing to the device is accomplished by asserting Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$), is written into the location specified on the address pins ($A_0$ through $A_{16}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{16}$).

Reading from the device is accomplished by asserting Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $I/O_8$ to $I/O_{15}$. See the Truth Table on page 11 for a complete description of read and write modes.

The CY62137EV30 is available in 48-ball VFBGA and 44-pin TSOPII packages.

For a complete list of related documentation, click here.

## Logic Block Diagram



## Contents

**Pin Configurations** ..... **3**
**Product Portfolio** ..... **3**
**Maximum Ratings** ..... **4**
**Operating Range** ..... **4**
**Electrical Characteristics** ..... **4**
**Capacitance** ..... **5**
**Thermal Resistance** ..... **5**
**AC Test Loads and Waveforms** ..... **5**
**Data Retention Characteristics** ..... **6**
**Data Retention Waveform** ..... **6**
**Switching Characteristics** ..... **7**
**Switching Waveforms** ..... **8**
**Truth Table** ..... **11**
**Ordering Information** ..... **12**
Ordering Code Definitions ..... 12
**Package Diagrams** ..... **13**
**Acronyms** ..... **15**
**Document Conventions** ..... **15**
Units of Measure ..... 15
**Document History Page** ..... **16**
**Sales, Solutions, and Legal Information** ..... **18**
Worldwide Sales and Design Support ..... 18
Products ..... 18
PSoC® Solutions ..... 18
Cypress Developer Community ..... 18
Technical Support ..... 18

## Pin Configurations

**Figure 1. 48-ball VFBGA pinout (Top View)** [1, 2]

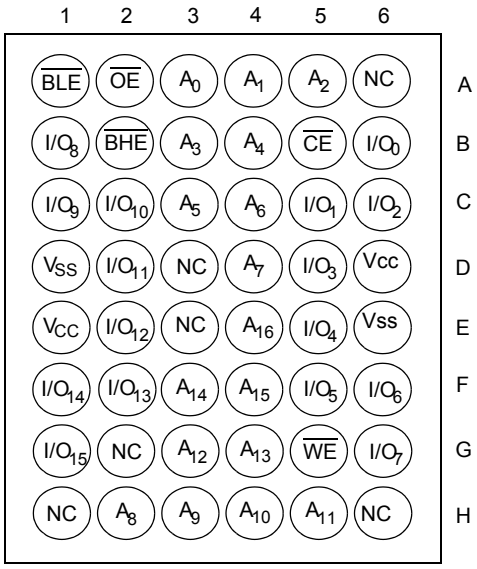
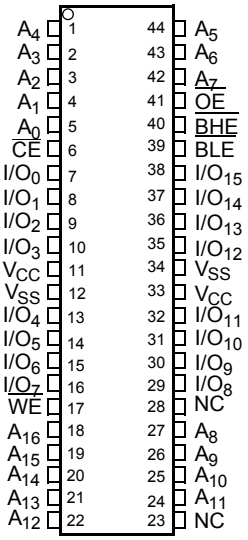



**Figure 2. 44-pin TSOP II pinout (Top View)** [1]




## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$ (mA) | | | | Standby $I_{SB2}$ (µA) | |
| | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | Min | Typ [3] | Max | | Typ [3] | Max | Typ [3] | Max | Typ [3] | Max |
| CY62137EV30-45LL | 2.2 V | 3.0 V | 3.6 V | 45 ns | 2 | 2.5 | 15 | 20 | 1 | 7 |

**Notes**
1. NC pins are not connected on the die.
2. Pins D3, H1, G2, H6 and H3 in the 48-ball VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential [4, 5] .....–0.3 V to ($V_{CC(MAX)}$ + 0.3 V)

DC voltage applied to outputs in High Z state [4, 5] .....–0.3 V to ($V_{CC(MAX)}$ + 0.3 V)

DC input voltage [4, 5] .....–0.3 V to ($V_{CC(MAX)}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$[6] |
|---|---|---|---|
| CY62137EV30-45LL | Industrial | –40 °C to +85 °C | 2.2 V to 3.6 V |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [7] | Max | |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –0.1 mA | $V_{CC}$ = 2.20 V | 2.0 | – | – | V |
| | | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 2.70 V | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 0.1 mA | $V_{CC}$ = 2.20 V | – | – | 0.4 | V |
| | | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 2.70 V | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ = 2.2 V to 2.7 V | | 1.8 | – | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | 2.2 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | $V_{CC}$ = 2.2 V to 2.7 V | | –0.3 | – | 0.6 | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | –0.3 | – | 0.8 | V |
| $I_{IX}$ | Input leakage current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_O$ ≤ $V_{CC}$, Output disabled | | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating supply current | f = $f_{max}$ = 1/$t_{RC}$ | $V_{CC}$ = $V_{CCmax}$ $I_{OUT}$ = 0 mA CMOS levels | – | 15 | 20 | mA |
| | | f = 1 MHz | | – | 2.0 | 2.5 | |
| $I_{SB1}$[8] | Automatic CE power-down current — CMOS inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≤ 0.2 V, f = $f_{max}$ (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC}$ = 3.60 V | | – | 1 | 7 | µA |
| $I_{SB2}$ [8] | Automatic CE power-down current — CMOS inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V or $V_{IN}$ ≤ 0.2 V, f = 0, $V_{CC}$ = 3.60 V | | – | 1 | 7 | µA |

**Notes**

4. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = $V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after $V_{CC}$ stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ.)}$, $T_A$ = 25 °C.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ specification. Other inputs can be left floating.

## Capacitance

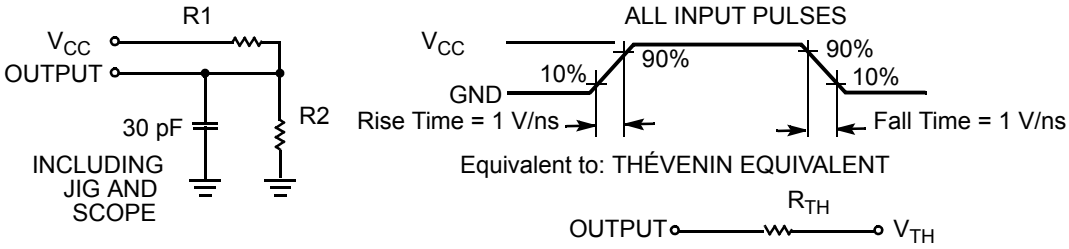
| Parameter [9] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [9] | Description | Test Conditions | 48-ball BGA | 44-pin TSOP II | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 54 | 57 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 12 | 17 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**




| Parameters | 2.50 V | 3.0 V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

**Note**
9. Tested initially and after any design or process changes that may affect these parameters.

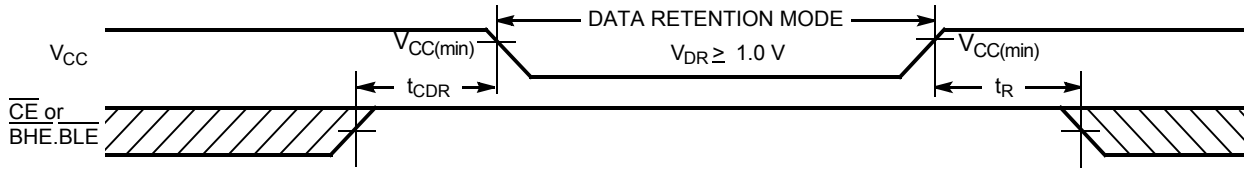
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ [10] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | 1 | – | – | V |
| $I_{CCDR}$ [11] | Data retention current | $V_{CC}$= 1 V,<br>$\overline{CE} \geq V_{CC} - 0.2$ V or<br>($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 0.8 | 3 | µA |
| $t_{CDR}$[12] | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R$[13] | Operation recovery time | | 45 | – | – | ns |

## Data Retention Waveform

**Figure 4. Data Retention Waveform** [14]




**Notes**

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A$ = 25 °C.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ specification. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
14. BHE.BLE is the AND of both $\overline{BHE}$ and $\overline{BLE}$. The chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range

| Parameter [15, 16] | Description | 45 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 45 | – | ns |
| $t_{AA}$ | Address to data valid | – | 45 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [17] | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [17, 18] | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z [17] | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z [17, 18] | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 45 | ns |
| $t_{DBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to data valid | – | 45 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low Z [17] | 5 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to High Z [17, 18] | – | 18 | ns |
| **Write Cycle** [19, 20] | | | | |
| $t_{WC}$ | Write cycle time | 45 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 35 | – | ns |
| $t_{AW}$ | Address setup to write end | 35 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 35 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 35 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [17, 18] | – | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [17] | 10 | – | ns |

**Notes**

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in Figure 3 on page 5.
16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
17. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
18. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. The minimum pulse width for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

**Figure 5. Read Cycle 1: Address Transition Controlled** [21, 22]

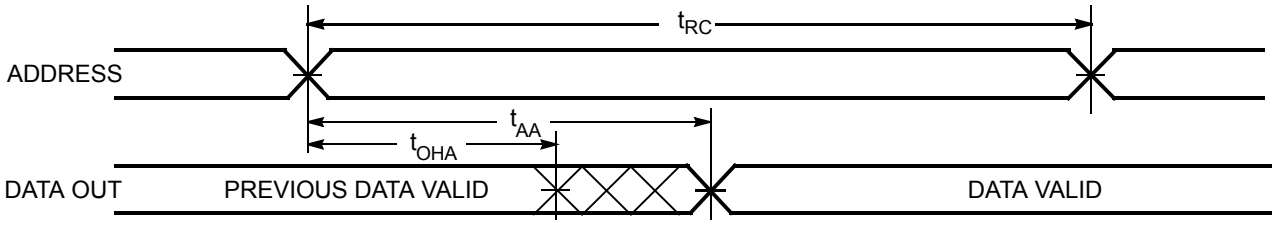
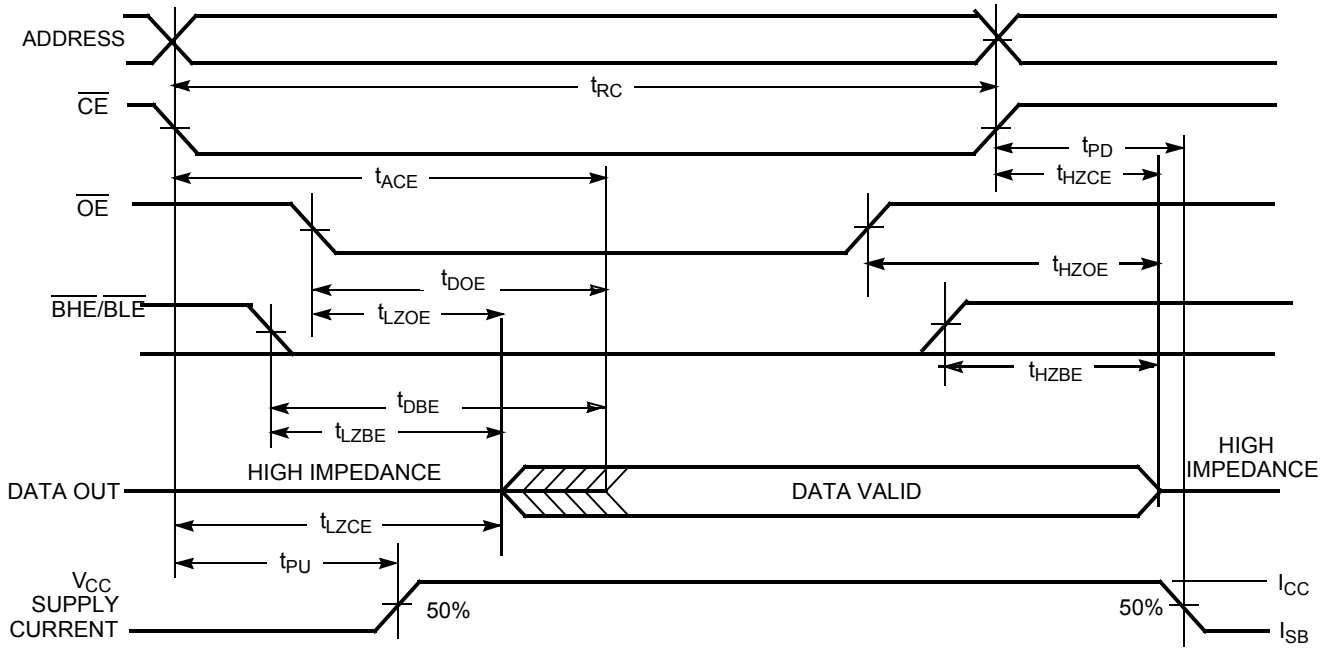



**Figure 6. Read Cycle No. 2: $\overline{OE}$ Controlled** [22, 23]




**Notes**
21. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and $\overline{BLE}$ = $V_{IL}$.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid prior to or coincident with $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1: $\overline{WE}$ Controlled** [24, 25, 26]

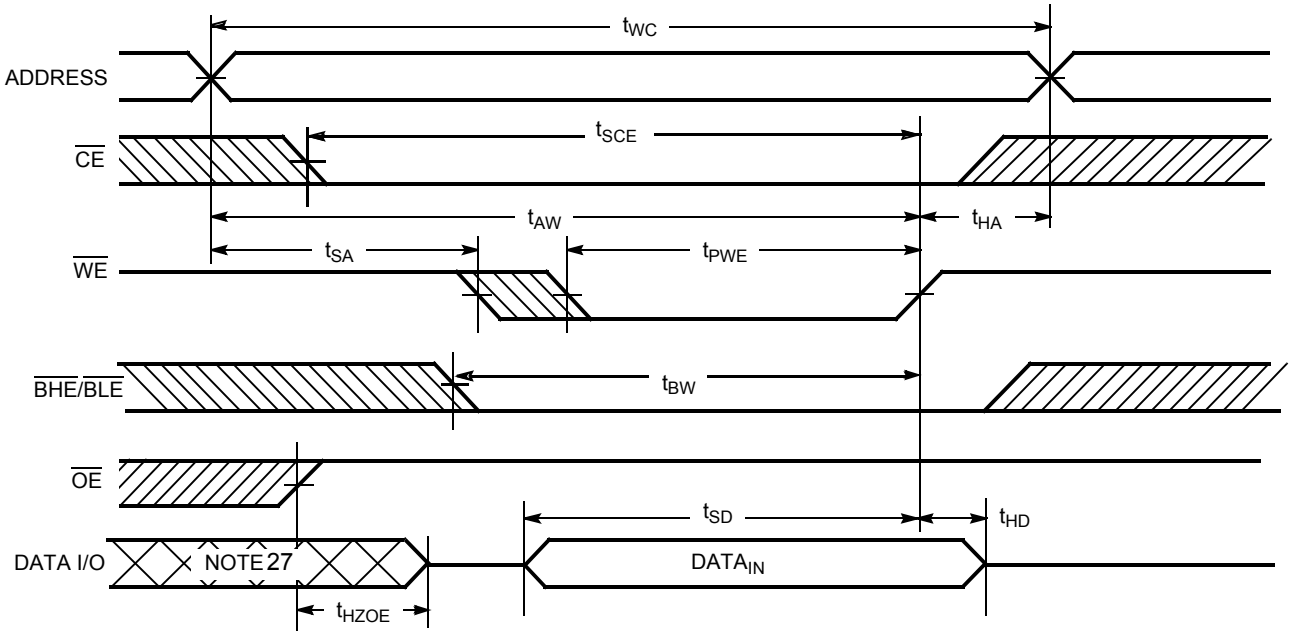
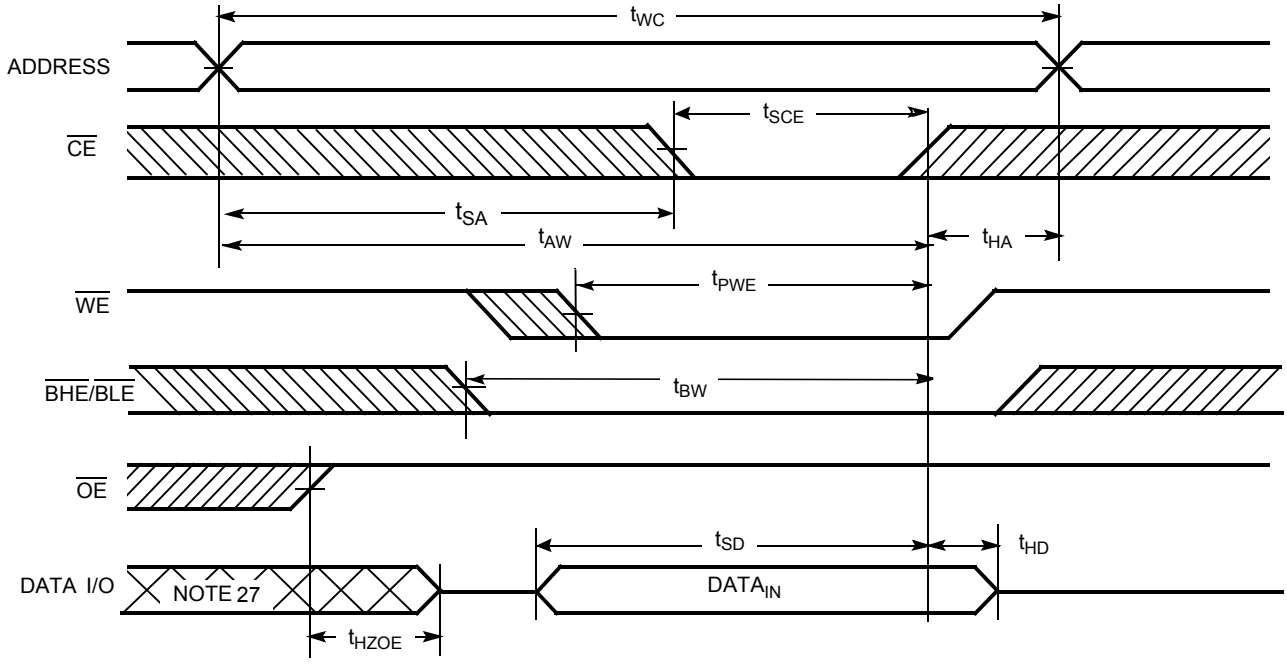



**Figure 8. Write Cycle No. 2: $\overline{CE}$ Controlled** [24, 25, 26]




**Notes**

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write
25. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
27. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 3: $\overline{WE}$ Controlled, $\overline{OE}$ LOW [28]**

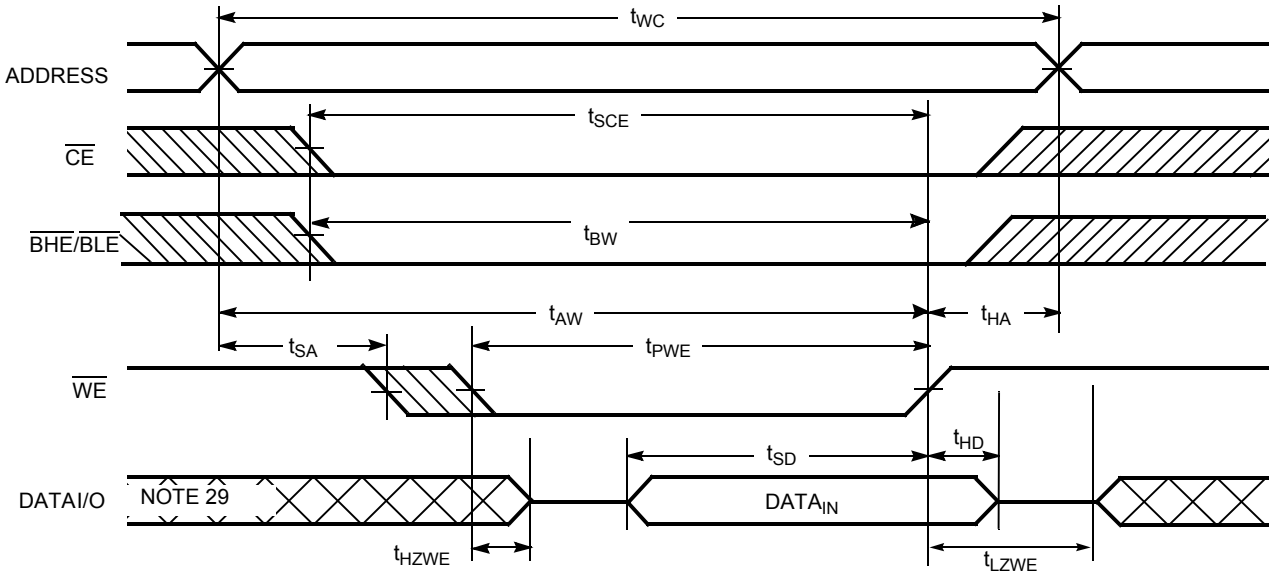
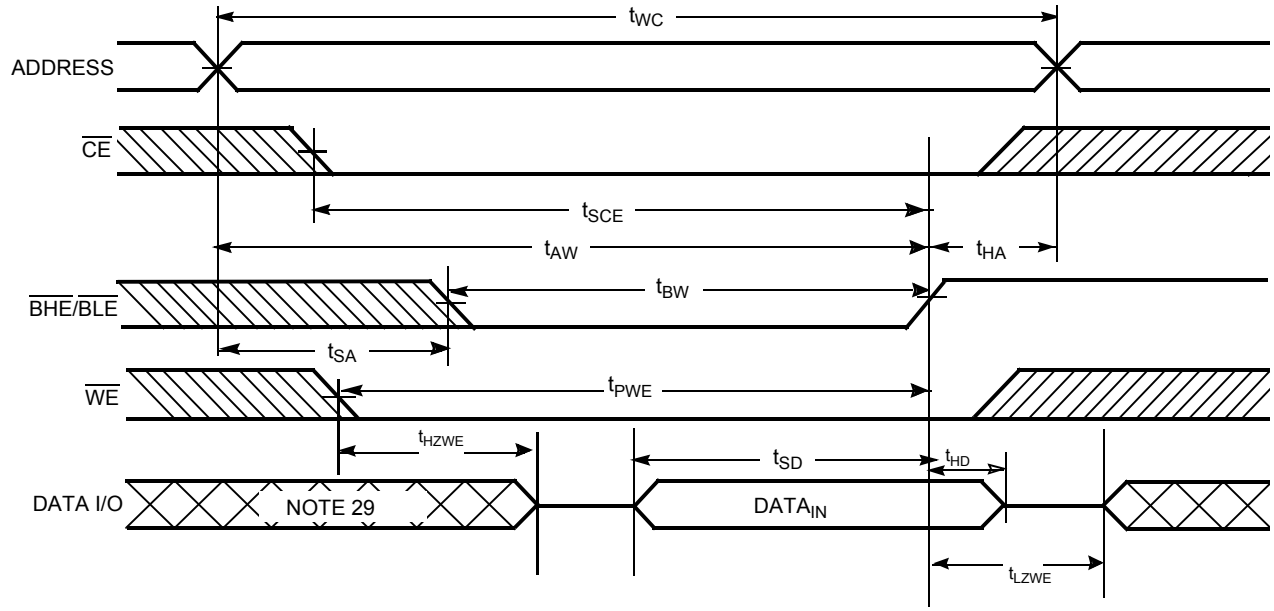



**Figure 10. Write Cycle No. 4: $\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW [28]**




**Notes**
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high impedance state.
29. During this period, the I/Os are in output state and input signals should not be applied.

## Truth Table

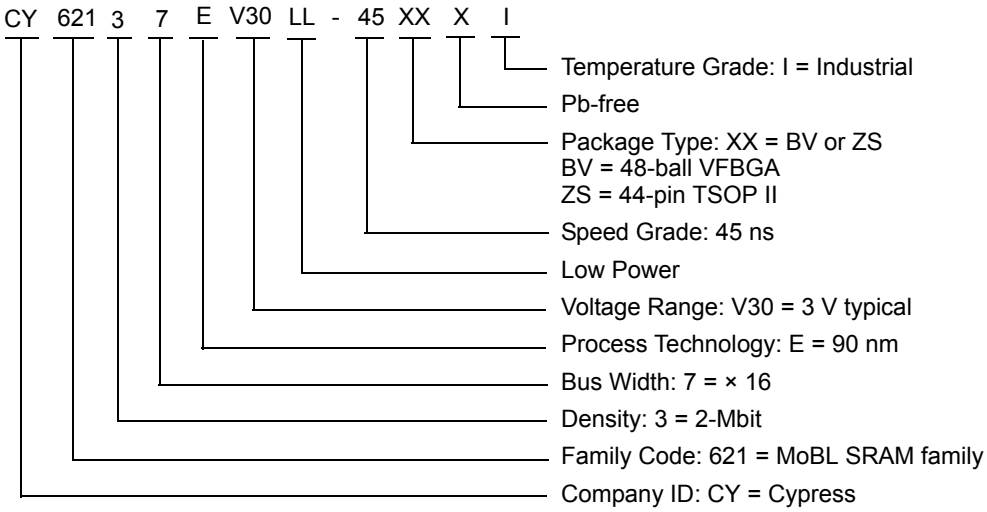
| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X[30] | X[30] | High Z | Deselect/power-down | Standby ($I_{SB}$) |
| X[30] | X | X | H | H | High Z | Deselect/power-down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data out ($I/O_O$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data out ($I/O_O$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | L | H | High Z | Output disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data in ($I/O_O$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data in ($I/O_O$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Write | Active ($I_{CC}$) |
| L | L | X | L | H | Data in ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Write | Active ($I_{CC}$) |

**Note**
30. Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ / $\overline{BLE}$) must be at fixed CMOS levels (not floating). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

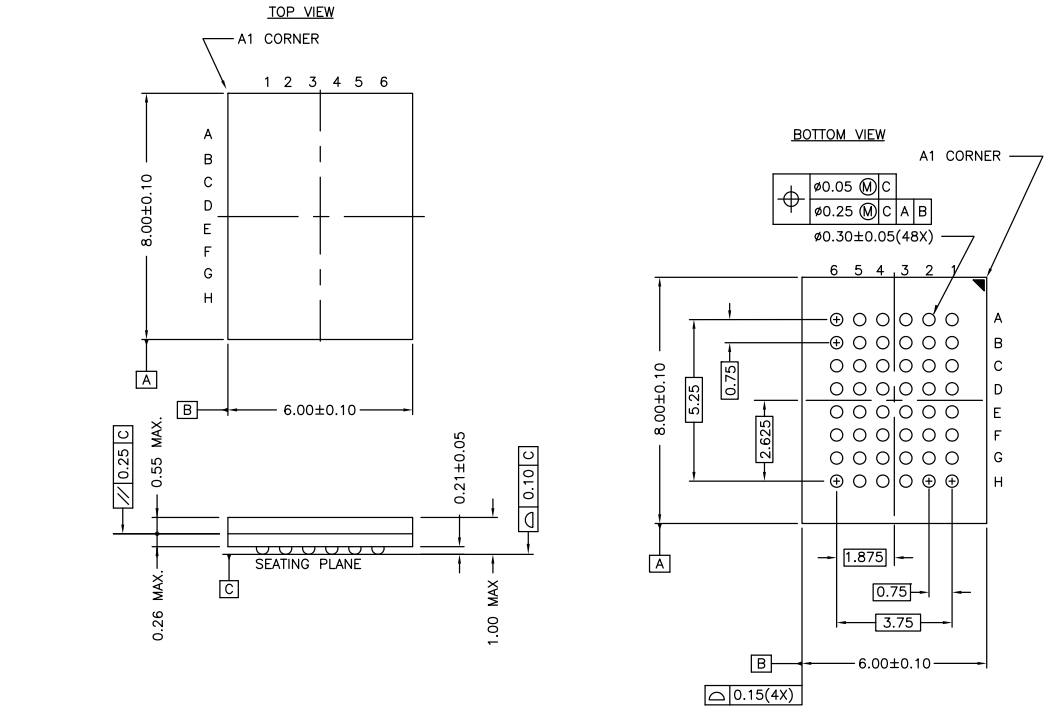
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62137EV30LL-45BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | Industrial |
| 45 | CY62137EV30LL-45ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | |

### Ordering Code Definitions



## Package Diagrams

**Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**

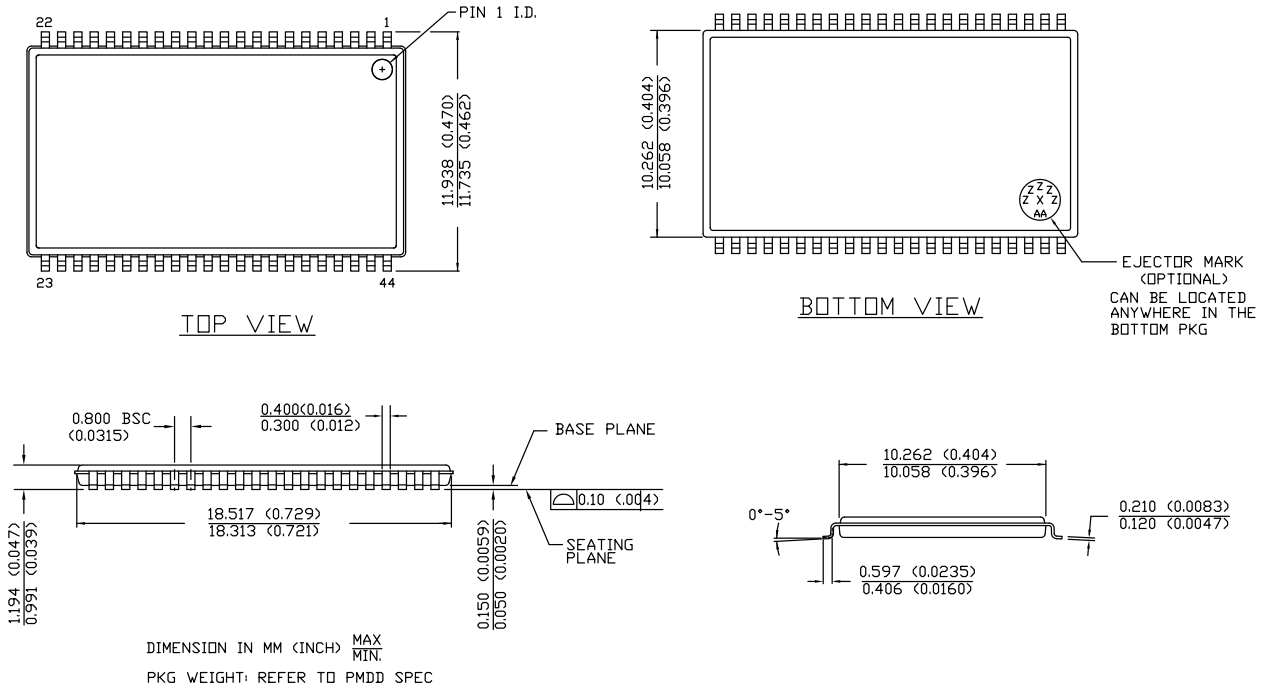



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

## Package Diagrams (continued)

**Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087**




51-85087 *E

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{BLE}$ | Byte Low Enable |
| $\overline{BHE}$ | Byte High Enable |
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| % | percent |
| pF | picofarad |
| Ω | ohm |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62137EV30 MoBL®, 2-Mbit (128 K × 16) Static RAM<br>Document Number: 38-05443 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 203720 | AJU | See ECN | New data sheet |
| *A | 234196 | AJU | See ECN | Changed $I_{CC}$ MAX at f=1MHz from 1.7 mA to 2.0 mA<br>Changed $I_{CC}$ TYP from 12 mA (35 ns speed bin) and 10 mA (45 ns speed bin) to 15 mA and 12 mA respectively<br>Changed $I_{CC}$ MAX from 20 mA (35 ns speed bin) and 15 mA (45 ns speed bin) to 25 mA and 20 mA respectively<br>Changed $I_{SB1}$ and $I_{SB2}$ TYP from 0.6 μA to 0.7 μA<br>Changed $I_{SB1}$ and $I_{SB2}$ MAX from 1.5 μA to 2.5 μA<br>Changed $I_{CCDR}$ from 1 μA to 2 μA<br>Fixed typos on TSOP II pinout:<br>Pin 18-22: address lines<br>Pin 23: NC<br>Added Pb-free information |
| *B | 427817 | NXR | See ECN | Converted from Advanced Information to Final.<br>Removed 35 ns Speed Bin<br>Removed “L” version<br>Changed ball E3 from DNU to NC.<br>Removed the redundant footnote on DNU.<br>Moved Product Portfolio from Page # 3 to Page #2.<br>Changed $I_{CC}$ (Max) value from 2 mA to 2.5 mA and $I_{CC}$ (Typ) value from 1.5 mA to 2 mA at f=1 MHz<br>Changed $I_{CC}$ (Typ) value from 12 mA to 15 mA at f = $f_{max}$=1/$t_{RC}$<br>Changed $I_{SB1}$ and $I_{SB2}$ Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA.<br>Changed $V_{CC}$ stabilization time in footnote #7 from 100 μs to 200 μs<br>Changed the AC test load capacitance from 50pF to 30pF on Page# 4<br>Changed $V_{DR}$ from 1.5V to 1V on Page# 4.<br>Changed $I_{CCDR}$ from 2 μA to 3 μA.<br>Added $I_{CCDR}$ typical value.<br>Corrected $t_R$ in Data Retention Characteristics from 100 μs to $t_{RC}$ ns<br>Changed $t_{OHA}$, $t_{LZCE}$ and $t_{LZWE}$ from 6 ns to 10 ns<br>Changed $t_{LZBE}$ from 6 ns to 5 ns<br>Changed $t_{LZOE}$ from 3 ns to 5 ns<br>Changed $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$ and $t_{HZWE}$ from 15 ns to 18 ns<br>Changed $t_{SCE}$,$t_{AW\ and}$ $t_{BW}$ from 40 ns to 35 ns<br>Changed $t_{PWE}$ from 30 ns to 35 ns<br>Changed $t_{SD}$ from 20 ns to 25 ns<br>Updated the Ordering Information table and replaced the Package Name column with Package Diagram. |
| *C | 2604685 | VKN / PYRS | 11/12/08 | Added footnote 8 related to $I_{SB2}$ and $I_{CCDR}$<br>Added footnote 13 related to AC timing parameters |
| *D | 3143896 | RAME | 01/17/2011 | Converted all tablenote to footnotes.<br>Added Ordering Code Definitions.<br>Added Acronyms and Units of Measure.<br>Updated Package Diagrams:<br>spec 51-85150 – Changed revision from *D to *F. |
| *E | 3283711 | AJU | 06/15/2011 | Updated Functional Description:<br>Removed the Note “For best practice recommendations, refer to the Cypress application note “SRAM System Design Guidelines” on http://www.cypress.com website.” and its reference.<br>Updated to new template. |

## Document History Page (continued)

| Document Title: CY62137EV30 MoBL®, 2-Mbit (128 K × 16) Static RAM<br>Document Number: 38-05443 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *F | 3806123 | TAVA | 11/08/2012 | Updated Data Retention Waveform (Updated Figure 4 (Changed "$V_{DR} \geq 1.5$ V" to "$V_{DR} \geq 1.0$ V")).<br>Updated Package Diagrams (spec 51-85150 (Changed revision from *F to *H), spec 51-85087 (Changed revision from *C to *E)). |
| *G | 4101224 | VINI | 08/21/2013 | Updated Switching Characteristics:<br>Updated Note 16.<br>Updated to new template.<br>Completing Sunset Review. |
| *H | 4574264 | VINI | 11/19/2014 | Updated Functional Description:<br>Added "For a complete list of related documentation, click here." at the end.<br>Updated Maximum Ratings:<br>Referred Notes 4 and 5 In "Supply voltage to ground potential".<br>Updated Switching Characteristics:<br>Added Note 20 and referred the same note in "Write Cycle". |
| *I | 5025363 | VINI | 11/24/2015 | Updated Thermal Resistance:<br>Changed value of $\Theta_{JA}$ parameter corresponding to 48-ball BGA package from 75 °C/W to 54 °C/W.<br>Changed value of $\Theta_{JA}$ parameter corresponding to 44-pin TSOP II package from 77 °C/W to 57 °C/W.<br>Changed value of $\Theta_{JC}$ parameter corresponding to 48-ball BGA package from 10 °C/W to 12 °C/W.<br>Changed value of $\Theta_{JC}$ parameter corresponding to 44-pin TSOP II package from 13 °C/W to 17 °C/W.<br>Updated to new template.<br>Completing Sunset Review. |

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