EZ-USB™ SD3 USB and Mass Storage Peripheral Controller

USB 3.0

Features

- Latest-generation storage support
  - SD3.0/SDXC – UHS1 SDR50 / DDR50 Master
  - eMMC 4.4 Master
  - SDIO 3.0 Master
- USB integration
  - Certified USB 3.0 and USB 2.0 peripheral: SuperSpeed (SS), Hi-Speed (HS), and Full-Speed (FS) only.
  - Thirty-two physical endpoints
  - Integrated transceiver
- Ultra low-power in core power-down mode
  - Less than 60 µA with VBATT on and 20 µA with VBATT off
- I^2C master controller at 1 MHz
- Selectable input clock frequencies
  - 19.2, 26, 38.4, and 52 MHz
  - 19.2-MHz crystal input support
- Independent power domains for core and I/O
- 10 × 10 mm, 0.8-mm pitch ball grid array (BGA) package

Applications

- USB thumb drives
- Card readers
- Laptop with SD slots
- SD slot in TV/STB
- WIFI Dongles
- USB SDIO Bridge
- Raid on-Chip Controller

Errata: For information on silicon errata, see **"Errata"** on page 39. Details include trigger conditions, devices affected, and proposed workaround.

Logic block diagram

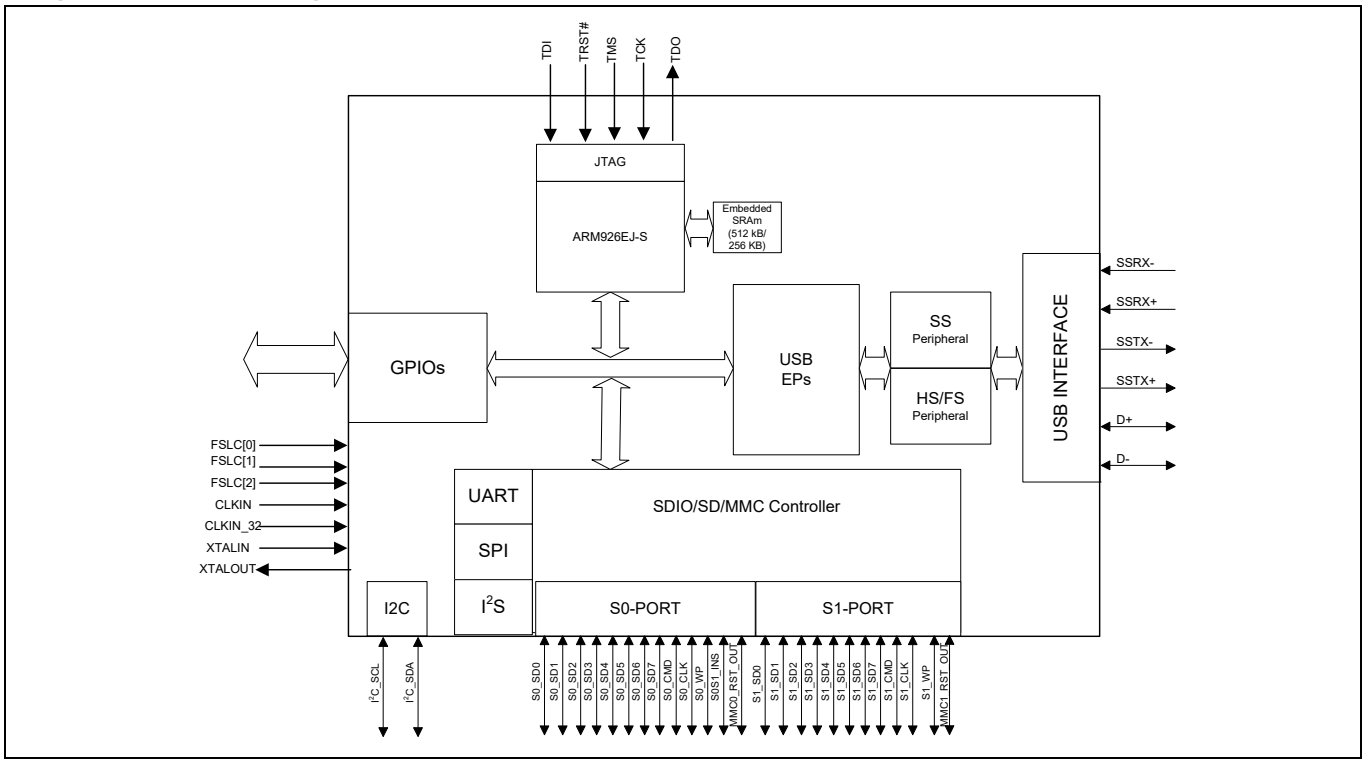


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1 Functional overview

SD3™ is a USB 3.0 SuperSpeed mass-storage controller providing the latest SD/MMC support. SD3 complies with the SD Specification, Version 3.0, and the MMC Specification, Version 4.41.

SD3 offers the following access paths among USB and mass storage ports:

- A USB-port (U-Port) supporting USB 3.0 peripheral
- Two mass-storage ports (S0-Port and S1-Port) supporting mass-storage devices. Following are the possible configurations for the two mass-storage ports:
  - SD and MMC
  - SD and SD
  - MMC and MMC
  - SD and SDIO
  - MMC and SDIO
  - SDIO and SDIO

Combinations of these accesses can happen independently or in an interleaved manner.

The SD3 complies with the USB 3.0 v1.0 specification and is also backward compatible with USB 2.0.

1.1 USB interface (U-Port)

SD3 offers the following features:

- Supports USB peripheral functionality compliant with the USB 3.0 Specification Revision 1.0 and is backward-compatible with the USB 2.0 Specification
- Supports up to 16 IN and 16 OUT endpoints.
- Supports USB Attached SCSI (UAS) device class to optimize mass-storage access performance.
- As a USB peripheral, SD3 supports UAS and Mass Storage Class (MSC) peripheral classes.
- When the USB port is not in use, the PHY and transceiver may be disabled for power savings.

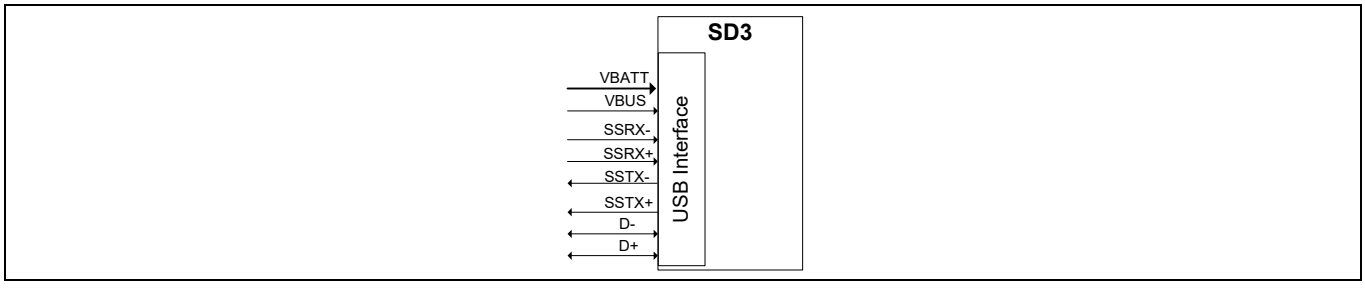


Figure 1 USB interface signals

1.2 Mass-storage support (S-Port)

The SD3 storage interface port supports the following specifications:

- SD Specification, Version 3.0
- Multimedia Card-System Specification, MMCA Technical Committee, Version 4.4
- SDIO Host controller compliant with SDIO Specification Version 3.00

1.3 I²C interface

SD3 has an I²C interface compatible with the I²C Bus Specification Revision 3. Because SD3's I²C interface is capable of operating only as I²C master, it may be used to communicate with other I²C slave devices. For example, SD3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option.

SD3's I²C master controller also supports multi-master mode functionality.

The power supply for the I²C interface is VIO5, which is a separate power domain from the other serial peripherals. This is to allow the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I²C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I²C controller supports the clock stretching feature to enable slower devices to exercise flow control.

Both SCL and SDA signals of the I²C interface require external pull-up resistors. These resistors must be connected to VIO5.

1.4 UART interface

The UART interface of SD3 supports full-duplex communication. It includes the signals noted in **Table 1**.

Table 1 UART interface signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then SD3's UART only transmits data when the CTS input is asserted. In addition to this, SD3's UART asserts the RTS output signal, when it is ready to receive data.

1.5 I²S interface

SD3 has an I²S port to support external audio codec devices. SD3 functions as I²S Master as transmitter only. The I²S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). SD3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I2S interface are 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz and 192 kHz.

1.6 SPI interface

SD3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see **"SPI timing specification"** on page 32 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from 4 bits to 32 bits.

2 Boot options

SD3 can load boot images from various sources, selected by the configuration of the PMODE pins. The boot options for the SD3 are as follows:

- Boot from USB
- Boot from I^2C
- Boot from eMMC on S0-Port
- Boot from SPI
  - Infineon SPI Flash parts supported are S25FS064S (64-Mbit), S25FS128S (128-Mbit) and S25LFL064L (64-Mbit).
  - W25Q32FW (32-Mbit) and equivalent parts are also supported.

Table 2 Booting options for SD3

PMODE[2:0][1]	Boot from
FF1	USB Boot
FFF	I^2C On Failure, USB Boot is enabled
0FF	I^2C only
0F1	SPI On Failure, USB Boot is enabled

3 Reset

A reset is initiated by asserting the Reset# pin on SD3. The specific reset sequence and timing requirements are detailed in **Figure 3** and **Table 15**. All I/Os are tristated during a hard reset.

4 Clocking

SD3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

SD3 has an on-chip oscillator circuit that uses an external 19.2 MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal option/clock frequency option. The configuration options are shown in **Table 3**.

Clock inputs to SD3 must meet the phase noise and jitter requirements specified in **Table 4**.

The input clock frequency is independent of the clock/data rate of SD3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3 Crystal/clock frequency selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/clock frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 4 Input clock specifications for SD3

Parameter	Description	Specification		Unit
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	dB
	10-kHz offset	–	–120	dB
	100-kHz offset	–	–128	dB
	1-MHz offset	–	–130	dB
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	%
Undershoot	–	–	–3	%
Rise time/fall time	–	–	3	ns

4.1 32-kHz watchdog timer clock input

SD3 includes a watchdog timer that can be used to interrupt the core, automatically wake up SD3 in Standby mode, and reset the core. The watchdog timer runs off a 32-kHz clock, which may optionally be supplied from an external source on a dedicated pin of SD3.

The watchdog timer can be disabled by firmware.

Requirements for the optional 32-kHZ clock input are listed in **Table 5**.

Table 5 32-kHz clock input requirements

Parameter	Min	Max	Unit
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise Time/fall Time	–	200	ns

Note

5 Power

SD3 has the following main groups of power supply domains:

- **IO_VDDQ:** This refers to a group of independent supply domains for digital I/Os. The voltage level on these supplies are 1.8 V to 3.3 V. SD3 provides six independent supply domains for digital I/Os listed as follows:
  - S0VDDQ: S0-Port (for SD/MMC) I/O Power Supply Domain
  - S1VDDQ: S1-Port (for SD/MMC) I/O Power Supply Domain
  - S2VDDQ: S2-Port (GPIO) Power Supply Domain
  - VIO4: S1-Port GPIO[53:57]/O Power Supply Domain (these pins support MMC's high nibble data line - D[7:4] on S1-Port)
  - VIO5: I2C Power Supply Domain (supports 1.2 V to 3.3 V)
  - CVDDQ: Clock Power Supply Domain
- **VDD:** This is the supply voltage for the logic core. The nominal supply voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
  - **AVDD**: This is the 1.2-V supply for the PLL, crystal oscillator and other core analog circuits
  - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS:** This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through SD3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Note: No specific power-up sequence required for SD3 power domains. Minimum power on reset time of 1 ms should be met and the power domains must be stable for SD3 operation.

5.1 Power modes

SD3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. In this mode the internal CPU clock and the internal PLLs are enabled.

Normal operating power consumption does not exceed the sum of ICC_CORE max and ICC_USB max (see **Table 8** for current consumption specifications).

The I/O power supplies (S0VDDQ, S1VDDQ, VIO4, and VIO5) may be turned off when the corresponding interface is not in use. S2VDDQ cannot be turned off at any time if the S2-Port is used in the application.

- SD3 supports four low-power modes (see **Table 6**):
  - Suspend mode with USB 3.0 PHY enabled (L1 mode)
  - Suspend mode with USB 3.0 PHY disabled (L2 mode)
  - Standby mode (L3 mode)
  - Core power-down mode (L4 mode)

Table 6 Entry and Exit methods for Low-Power modes

Low Power mode	Characteristics	Methods of Entry	Methods of Exit
Suspend mode with USB 3.0 PHY Enabled (L1 mode)	• The power consumption in this mode does not exceed ISB_1 • USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone operates with its internal clock while all other clocks are shut down • All I/Os maintain their previous state • Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually • The states of the configuration registers, buffer memory and all internal RAM are maintained • All transactions must be completed before SD3 enters Suspend mode (state of outstanding transactions are not preserved) • The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	• Firmware executing on the core can put SD3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SD3 into suspend mode	• D+ transitioning to low or high • D– transitioning to low or high • Resume condition on SSRX +/- • Detection of VBUS • Assertion of GPIO[17] • Assertion of RESET#
Suspend mode with USB 3.0 PHY disabled (L2 mode)	• The power consumption in this mode does not exceed ISB_2 • USB 3.0 PHY is disabled and the USB interface is in suspend mode • The clocks are shut off. The PLLs are disabled • All I/Os maintain their previous state • USB interface maintains the previous state • Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually • The states of the configuration registers, buffer memory, and all internal RAM are maintained • All transactions must be completed before SD3 enters Suspend mode (state of outstanding transactions are not preserved) • The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	• Firmware executing on the core can put SD3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SD3 into suspend mode	• D+ transitioning to low or high • D– transitioning to low or high • Detection of VBUS • Assertion of GPIO[17] • Assertion of RESET#

Note
2. The power consumption depends on how the SD3 IOs are utilized in the application. Refer to **KBA85505** to estimate the current consumption by different power domains (VIO1–VIO5).

Table 6 Entry and Exit methods for Low-Power modes (continued)

Low Power mode	Characteristics	Methods of Entry	Methods of Exit
Standby Mode (L3 mode)	• The power consumption in this mode does not exceed ISB3 • All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that needed data is read before putting SD3 into this Standby Mode • The program counter is reset after waking up from Standby • GPIO pins maintain their configuration • Crystal oscillator is turned off • Internal PLL is turned off • USB transceiver is turned off • Core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM • Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	• Firmware executing on the core or external processor configures the appropriate register	• Detection of VBUS • Assertion of GPIO[17] • Assertion of RESET#
Core Power Down Mode (L4 mode)	• The power consumption in this mode does not exceed ISB_4 • Core power is turned off • All buffer memory, configuration registers and the program RAM do not maintain state. It is necessary to reload the firmware on exiting from this mode • In this mode, all other power domains can be turned on/off individually	• Turn off VDD	• Reapply VDD • Assertion of RESET#

Note
2. The power consumption depends on how the SD3 IOs are utilized in the application. Refer to **KBA85505** to estimate the current consumption by different power domains (VIO1–VIO5).

6 Configuration fuse

Fuse options are available for specific usage models. Contact Infineon Applications/Marketing for details.

7 Digital I/Os

SD3 provides firmware controlled pull-up or pull-down resistors internally on all digital I/O pins. The pins can be pulled high through an internal 50-kΩ resistor or can be pulled low through an internal 10-kΩ resistor to prevent the pins from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (through internal 50 kΩ)
- Pull down (through internal 10 kΩ)
- Hold (I/O hold its value) when in low power modes

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured based on each interface.

8 EMI

SD3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. SD3 can tolerate reasonable EMI, conducted by aggressor, outlined by these specifications and continue to function as expected.

9 System level ESD

SD3 has built-in ESD protection on the D+, D–, GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-KV human body model (HBM) based on JESD22-A114 Specification
- ±6-KV contact discharge and ±8-KV air gap discharge based on IEC61000-4-2 level 3A
- ±8-KV contact discharge and ±15-KV air gap discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated.

The SuperSpeed USB signals (SSRX+, SSRX-, SSTX+, SSTX-) and S0/S1_INS have up to ±2.2 KV HBM internal ESD protection.

10 Pinout

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	NC
E	GPIO[47]	VSS	S1VDDQ	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	S0VDDQ	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	S2VDDQ
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	NC	S2VDDQ	GPIO[11]	VSS

Figure 2 SD3 BGA ball map (top view)

11 Pin description

Table 7 Pin list

Pin #	Power domain	I/O	Name	Description		
S2-PORT (GPIO)						
F10	VI01	I/O	GPIO[0]	GPIO		
F9	VI01	I/O	GPIO[1]	GPIO		
F7	VI01	I/O	GPIO[2]	GPIO		
G10	VI01	I/O	GPIO[3]	GPIO		
G9	VI01	I/O	GPIO[4]	GPIO		
F8	VI01	I/O	GPIO[5]	GPIO		
H10	VI01	I/O	GPIO[6]	GPIO		
H9	VI01	I/O	GPIO[7]	GPIO		
J10	VI01	I/O	GPIO[8]	GPIO		
J9	VI01	I/O	GPIO[9]	GPIO		
K11	VI01	I/O	GPIO[10]	GPIO		
L10	VI01	I/O	GPIO[11]	GPIO		
K10	VI01	I/O	GPIO[12]	GPIO		
K9	VI01	I/O	GPIO[13]	GPIO		
J8	VI01	I/O	GPIO[14]	GPIO		
G8	VI01	I/O	GPIO[15]	GPIO		
J6	VI01	I/O	GPIO[16]	GPIO		
K8	VI01	I/O	GPIO[17]	GPIO		
K7	VI01	I/O	GPIO[18]	GPIO		
J7	VI01	I/O	GPIO[19]	GPIO		
H7	VI01	I/O	GPIO[20]	GPIO		
G7	VI01	I/O	GPIO[21]	GPIO		
G6	VI01	I/O	GPIO[22]	GPIO		
K6	VI01	I/O	GPIO[23]	GPIO		
H8	VI01	I/O	GPIO[24]	GPIO		
G5	VI01	I/O	GPIO[25]	GPIO		
H6	VI01	I/O	GPIO[26]	GPIO		
K5	VI01	I/O	GPIO[27]	GPIO		
J5	VI01	I/O	GPIO[28]	GPIO		
H5	VI01	I/O	GPIO[29]	GPIO		
G4	VI01	I/O	GPIO[30]	PMODE[0]		
H4	VI01	I/O	GPIO[31]	PMODE[1]		
L4	VI01	I/O	GPIO[32]	PMODE[2]		
L8			NC	No Connect		
C5	CVDDQ	I	RESET#	Active Low. Hardware Reset.		
				8b MMC configuration	**SD+GPIO configuration**	**GPIO configuration**
K2	VI02	I/O	GPIO[33]	S0_SD0	S0_SD0	GPIO
J4	VI02	I/O	GPIO[34]	S0_SD1	S0_SD1	GPIO
K1	VI02	I/O	GPIO[35]	S0_SD2	S0_SD2	GPIO

Pin description

Table 7 Pin list(continued)

Pin #	Power domain	I/O	Name	Description							
J2	VI02	I/O	GPIO[36]	S0_SD3			S0_SD3			GPIO	
J3	VI02	I/O	GPIO[37]	S0_SD4			GPIO			GPIO	
J1	VI02	I/O	GPIO[38]	S0_SD5			GPIO			GPIO	
H2	VI02	I/O	GPIO[39]	S0_SD6			GPIO			GPIO	
H3	VI02	I/O	GPIO[40]	S0_SD7			GPIO			GPIO	
F4	VI02	I/O	GPIO[41]	S0_CMD			S0_CMD			GPIO	
G2	VI02	I/O	GPIO[42]	S0_CLK			S0_CLK			GPIO	
G3	VI02	I/O	GPIO[43]	S0_WP			S0_WP			GPIO	
F3	VI02	I/O	GPIO[44]	S0S1_INS			S0S1_INS			GPIO	
F2	VI02	I/O	GPIO[45]	MMC0_RST_OUT			GPIO			GPIO	
				8b MMC	**SD + UART**	**SD + SPI**	**SD + GPIO**	**GPIO**	**GPIO + UART + I2S**	**SD + I2S**	**UART + SPI + I2S**
F5	VI03	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
E1	VI03	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E5	VI03	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
E4	VI03	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D1	VI03	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
D2	VI03	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
D3	VI03	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D4	VIO4	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
C9			NC	No Connect							
A3	U3RXVDDQ	I	SSRXM	USB 3.0 SuperSpeed Receive Minus							
A4	U3RXVDDQ	I	SSRXP	USB 3.0 SuperSpeed Receive Plus							
A6	U3TXVDDQ	O	SSTXM	USB 3.0 SuperSpeed Transmit Minus							
A5	U3TXVDDQ	O	SSTXP	USB 3.0 SuperSpeed Transmit Plus							
A9	VBATT/ VBUS	I/O	D+	USB (HS/FS) Data Plus							
A10	VBATT/ VBUS	I/O	D-	USB (HS/FS) Data Minus							
A11			NC	No Connect							
B2	CVDDQ	I	FSLC[0]	FSLC[0]							
C6	AVDD	I/O	XTALIN	XTALIN							

Table 7 Pin list(continued)

Pin #	Power domain	I/O	Name	Description
C7	AVDD	I/O	XTALOUT	XTALOUT
B4	CVDDQ	I	FSLC[1]	FSLC[1]
E6	CVDDQ	I	FSLC[2]	FSLC[2]
D7	CVDDQ	I	CLKIN	CLKIN
D6	CVDDQ	I	CLKIN_32	CLKIN_32
D9	VIO5	I/O	I^2C_GPIO[58]	SCL (Serial Clock) for I^2C Bus Interface
D10	VIO5	I/O	I^2C_GPIO[59]	SDA (Serial Data) for I^2C Bus Interface
E7	VIO5	I	TDI	TDI
C10	VIO5	O	TDO	TDO
B11	VIO5	I	TRST#	TRST#
E8	VIO5	I	TMS	TMS
F6	VIO5	I	TCK	TCK
D11	VIO5	O	O[60]	GPIO
E10		PWR	VBATT	
B10		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	S2VDDQ	
E2		PWR	VSS	
L9		PWR	S2VDDQ	
G1		PWR	VSS	
F1		PWR	S0VDDQ	
G11		PWR	VSS	
E3		PWR	S1VDDQ	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	

Table 7 Pin list(continued)

Pin #	Power domain	I/O	Name	Description
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/ VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ+/-1% resistor between this pin and GND)
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω+/-1% resistor between this pin and GND)

12 Electrical specifications

12.1 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature	–65°C to +150°C
Ambient temperature with power supplied (Industrial)	–40°C to +85°C
Supply voltage to ground potential V_{DD}, A_{VDDQ}	1.25 V
$S2_{VDDQ}$,$S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, V_{IO5}	3.6 V
$U3TX_{VDDQ}$, $U3RX_{VDDQ}$	1.25 V
DC input voltage to any input pin	VCC + 0.3
DC voltage applied to outputs in High-Z state (VCC is the corresponding I/O voltage)	VCC + 0.3
Latch-up current	> 200 mA
Maximum output short circuit current for all I/O configurations. (Vout = 0 V)	–100 mA

Static discharge voltage ESD protection levels:

- ±2.2-KV human body model (HBM) based on JESD22-A114
- Additional ESD Protection levels on D+, D–, VBUS, GND pins U-port and GPIO pins LPP-Port
- ±6-KV contact discharge, ±8-KV air gap discharge based on IEC61000-4-2 level 3A, ±8-KV contact discharge, and ±15-KV air gap discharge based on IEC61000-4-2 level 4C

12.2 Operating conditions

Parameter	**Range**
TA (ambient temperature under bias) Industrial	–40°C to +85°C
V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$ supply voltage	1.15 V to 1.25 V
V_{BATT} supply voltage	3.2 V to 6 V
$S2_{VDDQ}$, $S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, C_{VDDQ} supply voltage	1.7 V to 3.6 V
V_{IO5} supply voltage	1.15 V to 3.6 V

12.3 DC specifications

Table 8 DC specifications

Parameter	Description	Min	Max	Unit	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
$S0_{VDDQ}$	SD/ MMC/ CF I/O power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
$S1_{VDDQ}$	SD/MMC I/O power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
$S2_{VDDQ}$	GPIO/ CF I/O power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
V_{IO4}	GPIO/ I/O power supply domain	1.7	3.6	V	1.8-V, 2.5-V, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-V, 3.3-V typical
V_{IO5}	I^2C voltage supply	1.2	3.3	V	1.2-V,1.8-V, 2.5-V, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port).VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC - 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	0.9 × VCC	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply. Refer to **Table 9** for values of I_{OH} at various drive strength and V_{CC}.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply. Refer to **Table 9** for values of I_{OL} at various drive strength and V_{CC}.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os that have a pull-up/down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at VDDQ
I_{CC} Core	Core and Analog Voltage Operating Current	–	200	mA	Total current through AVDD, VDD
I_{CC} USB	USB voltage supply operating current	–	60	mA	
I_{SB1}	Total suspend current during Suspend Mode with USB 3.0 PHY enabled (L1 mode)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)

Table 8 DC specifications(continued)

Parameter	Description	Min	Max	Unit	Notes
I_{SB2}	Total suspend current during Suspend Mode with USB 3.0 PHYdisabled (L2 mode)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total Standby Current during Standby Mode (L3 mode)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total Standby Current during Core Power Down Mode (L4 mode)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage Ramp Rate on Core and I/O Supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise Level Permitted on VDD and I/O Supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise Level Permitted on AVDD Supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

Table 9 I_{OH}/I_{OL} values for different drive strength and V_{DDIO} values

V_{DDIO} (V)	V_{OH} (V)	V_{OL} (V)	Drive Strength	$I_{OH\ max}$ (mA)	$I_{OL\ min}$ (mA)
1.7	1.53	0.17	Quarter	1.02	2.21
			Half	1.51	3.28
			Three-Quarters	1.83	3.85
			Full	2.28	4.73
2.5	2.25	0.25	Quarter	5.03	3.96
			Half	7.38	5.84
			Three-Quarters	8.89	6.89
			Full	11.07	8.61
3.6	3.24	0.36	Quarter	7.80	5.74
			Half	11.36	8.64
			Three-Quarters	13.64	10.15
			Full	16.92	12.67

13 Thermal characteristics

Table 10 Thermal characteristics

Parameter	Description	Value	Unit
$T_{J\ MAX}$	Maximum Junction Temperature	125	°C
Θ_{JA}	Thermal resistance (junction to ambient)	34.66	°C/W
Θ_{JB}	Thermal resistance (junction to board)	27.03	°C/W
Θ_{JC}	Thermal resistance (junction to case)	13.57	°C/W

14 AC timing parameters

14.1 Storage port timing

The S0-Port and S1-Port support the MMC Specification Version 4.4 and SD Specification Version 3.0.

Table 11 lists the timing parameters for S0-Port and S1-Port of SD3.

Table 11 S-Port timing parameters[3]

Parameter	Description	Min	Max	Unit
MMC-20				
tSDIS CMD	Host input setup time for CMD	4.8	–	ns
tSDIS DAT	Host input setup time for DAT	4.8	–	ns
tSDIH CMD	Host input hold time for CMD	4.4	–	ns
tSDIH DAT	Host input hold time for DAT	4.4	–	ns
tSDOS CMD	Host output setup time for CMD	5	–	ns
tSDOS DAT	Host output setup time for DAT	5	–	ns
tSDOH CMD	Host output hold time for CMD	5	–	ns
tSDOH DAT	Host output hold time for DAT	5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	50	–	ns
SDFREQ	Clock frequency		20	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MMC-26				
tSDIS CMD	Host input setup time for CMD	10	–	ns
tSDIS DAT	Host input setup time for DAT	10	–	ns
tSDIH CMD	Host input hold time for CMD	9	–	ns
tSDIH DAT	Host input hold time for DAT	9	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	3	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	38.5	–	ns
SDFREQ	Clock frequency		26	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MC-HS				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	4	–	ns
tSDIH CMD	Host input hold time for CMD	3	–	ns
tSDIH DAT	Host input hold time for DAT	3	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	3	–	ns

Table 11 S-Port timing parameters[3] (continued)

Parameter	Description	Min	Max	Unit
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	19.2	–	ns
SDFREQ	Clock frequency	–	52	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MMC-DDR52				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	0.56	–	ns
tSDIH CMD	Host input hold time for CMD	3	–	ns
tSDIH DAT	Host input hold time for DAT	2.58	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	2.5	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	2.5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	19.2	–	ns
SDFREQ	Clock frequency		52	MHz
tSDCLKOD	Clock duty cycle	45	55	%
SD-Default Speed (SDR12)				
tSDIS CMD	Host input setup time for CMD	24	–	ns
tSDIS DAT	Host input setup time for DAT	24	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	5	–	ns
tSDOS DAT	Host output setup time for DAT	5	–	ns
tSDOH CMD	Host output hold time for CMD	5	–	ns
tSDOH DAT	Host output hold time for DAT	5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	40	–	ns
SDFREQ	Clock frequency		25	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-High-Speed (SDR25)				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	4	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	6	–	ns
tSDOS DAT	Host output setup time for DAT	6	–	ns
tSDOH CMD	Host output hold time for CMD	2	–	ns
tSDOH DAT	Host output hold time for DAT	2	–	ns

Table 11 S-Port timing parameters[3] (continued)

Parameter	Description	Min	Max	Unit
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	20	–	ns
SDFREQ	Clock frequency	–	50	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-SDR50				
tSDIS CMD	Host input setup time for CMD	1.5	–	ns
tSDIS DAT	Host input setup time for DAT	1.5	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	0.8	–	ns
tSDOH DAT	Host output hold time for DAT	0.8	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	10	–	ns
SDFREQ	Clock frequency		100	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-DDR50				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	0.92	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	6	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	0.8	–	ns
tSDOH DAT	Host output hold time for DAT	0.8	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	20	–	ns
SDFREQ	Clock frequency		50	MHz
tSDCLKOD	Clock duty cycle	45	55	%

Note
3. All parameters guaranteed by design and validated through characterization.

14.2 I²C interface timing

14.2.1 I²C timing

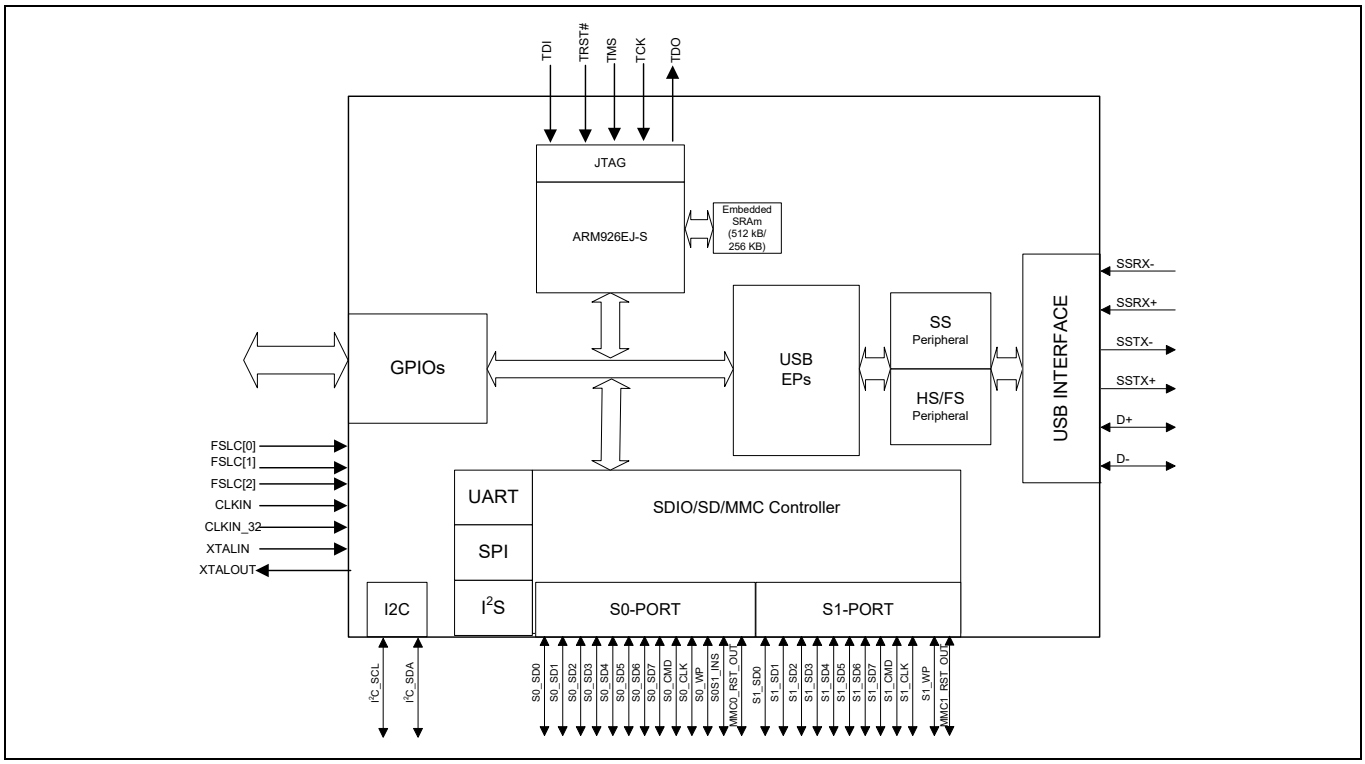


Figure 3 I²C timing definition

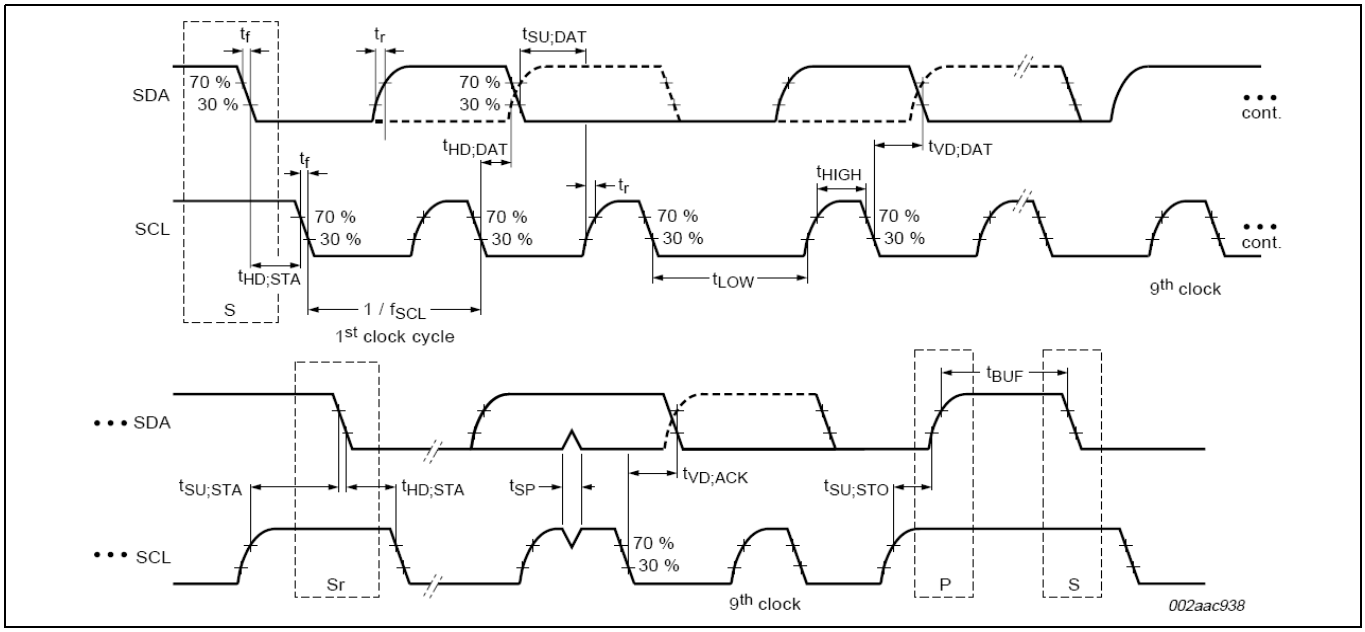


Table 12 I²C timing parameters[4]

Parameter	Description	Min	Max	Unit
I²C Standard Mode parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I²C Fast Mode parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus-free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns
I²C Fast Mode Plus parameters (Not supported at I2C_VDDQ = 1.2V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs
tHD:DAT	Data hold time	0	–	µs

Note
4. All parameters guaranteed by design and validated through characterization.

Table 12 I^2C timing parameters[4] (continued)

Parameter	Description	Min	Max	Unit
tSU:DAT	Data setup time	50	–	µs
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

Note
4. All parameters guaranteed by design and validated through characterization.

14.2.2 I^2S timing diagram

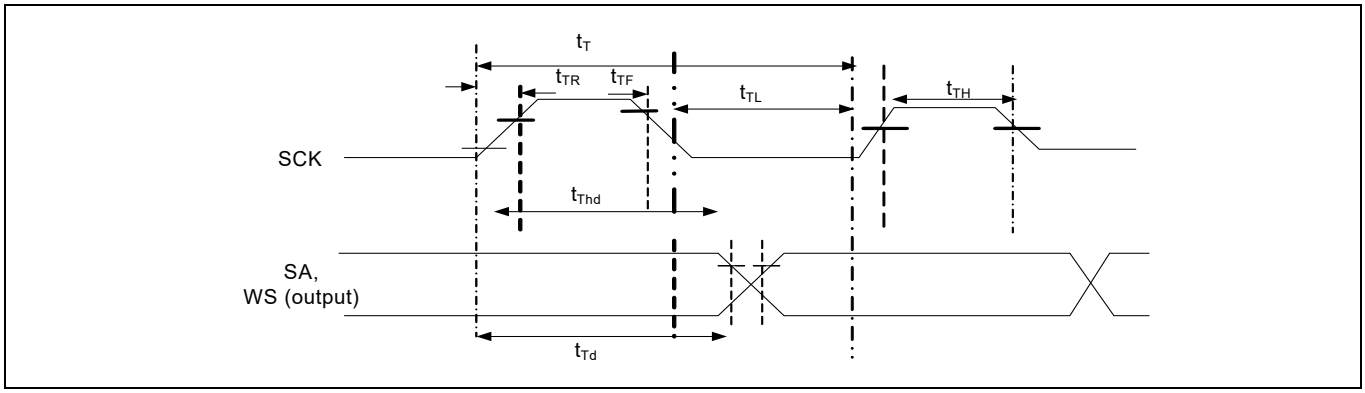


Figure 4 I^2S transmit cycle

Table 13 I^2S timing parameters[6]

Parameter	Description	Min	Max	Unit
tT	I^2S transmitter clock cycle	Ttr	–	ns
tTL	I^2S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I^2S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I^2S transmitter rise time	–	0.15 Ttr	ns
tTF	I^2S transmitter fall time	–	0.15 Ttr	ns
tThd	I^2S transmitter data hold time	0	–	ns
tTd	I^2S transmitter delay time	–	0.8tT	ns

Note
5. tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).

Note
6. All parameters guaranteed by design and validated through characterization.

14.2.3 SPI timing specification

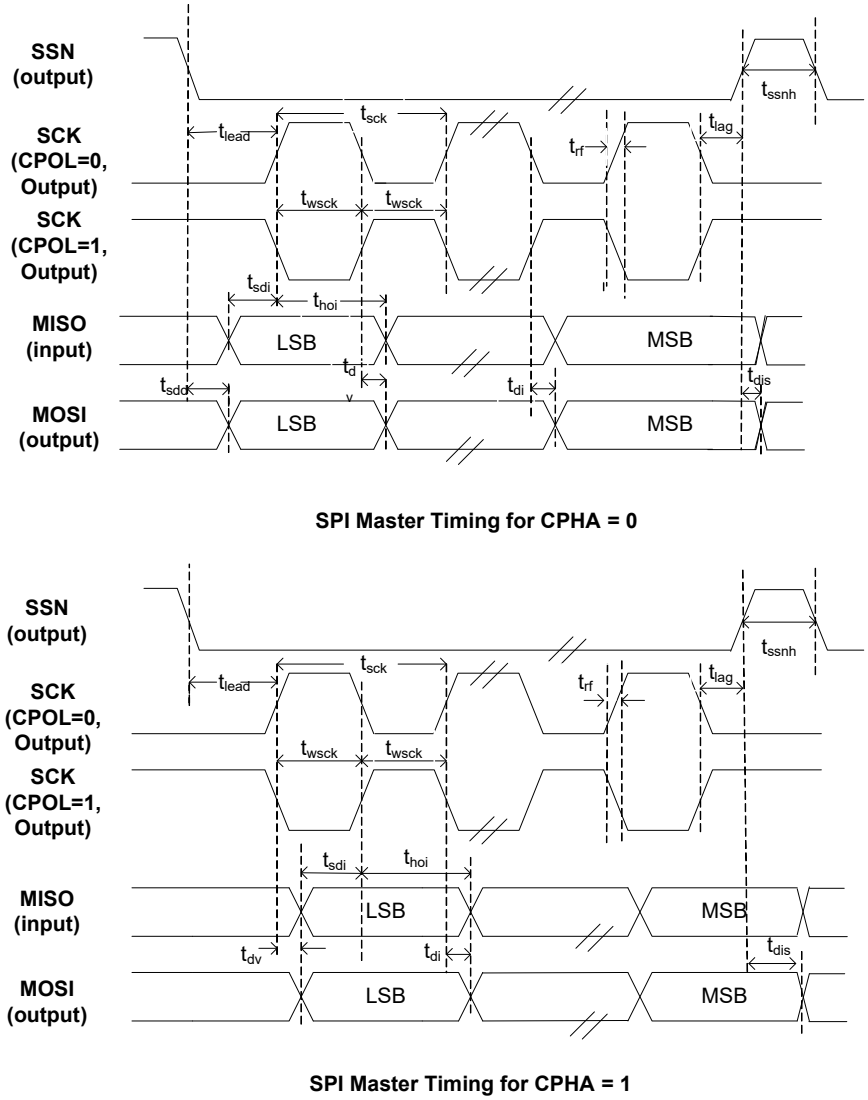


Figure 5 SPI timing

AC timing parameters

Table 14 SPI timing parameters[7]

Parameter	Description	Min	Max	Unit
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[8]-5	1.5 tsck[8]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[8]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes
7. All parameters guaranteed by design and validated through characterization.
8. Depends on LAG and LEAD setting in the SPI_CONFIG register.

14.3 Reset sequence

Table 15 provides the hard reset sequence requirements for SD3.

Table 15 Reset and standby timing parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
tRH	Minimum high on RESET#	–	5	–
tRR	Reset Recovery Time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
tSBY	Time to enter Standby/Suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
tWU	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted	–	5	–

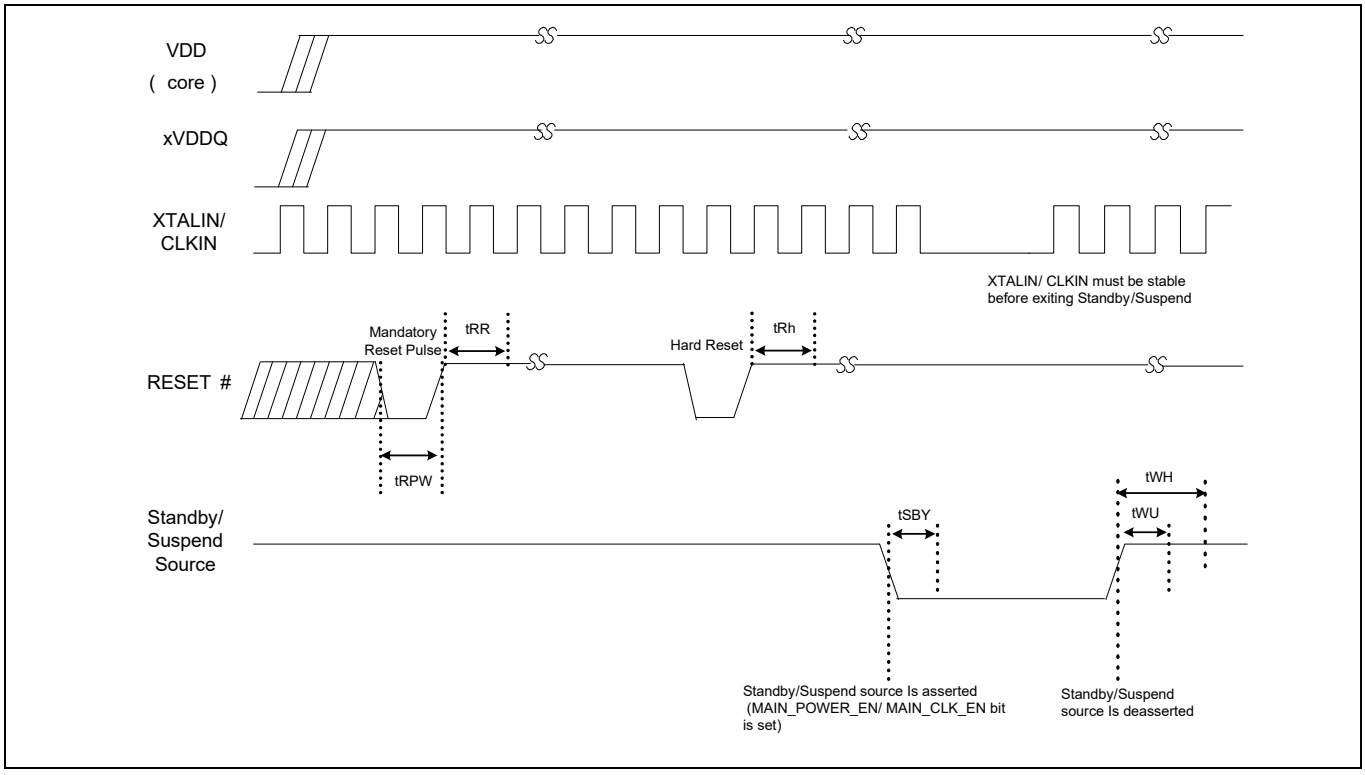
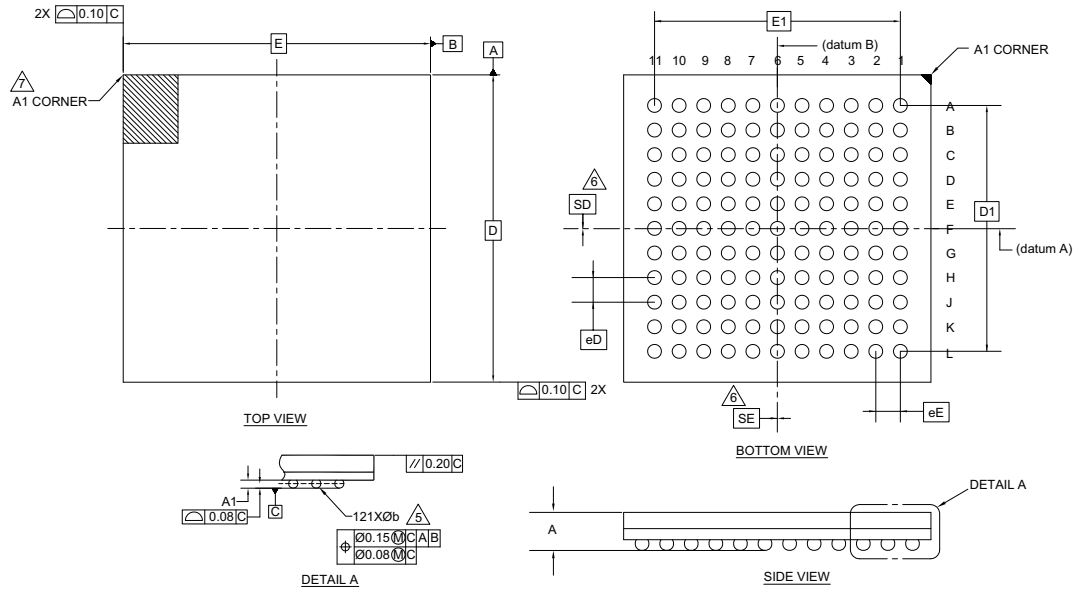


Figure 6 Reset sequence

15 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.15	-	-
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		
E1	8.00 BSC		
MD	11		
ME	11		
N	121		
∅ b	0.25	0.30	0.35
eD	0.80 BSC		
eE	0.80 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

001-54471 *F

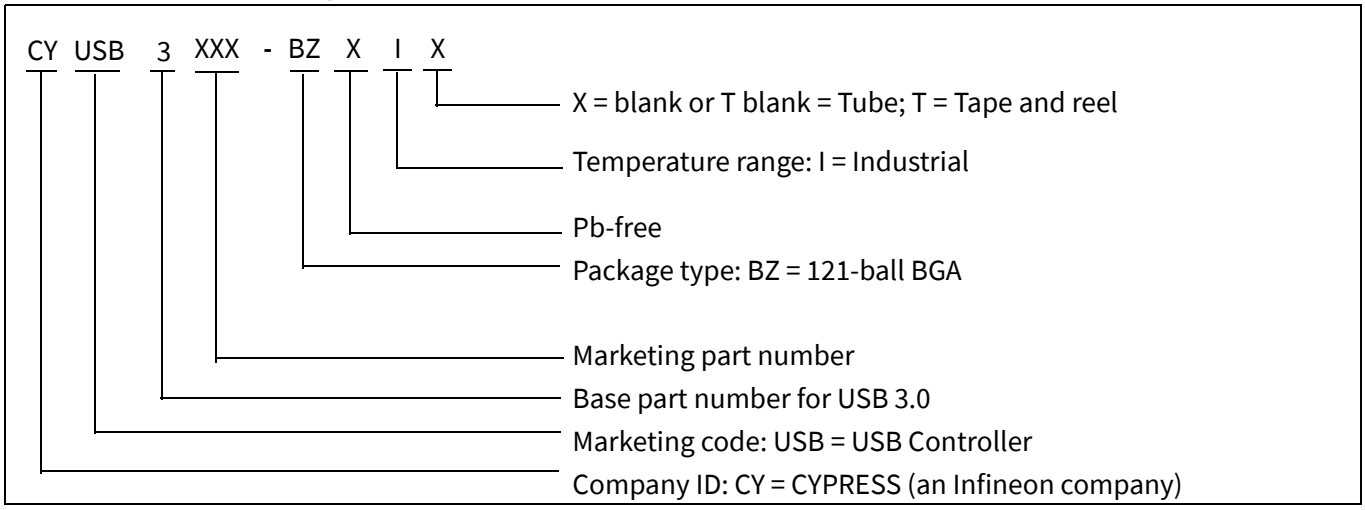
Figure 7 121-ball FBGA (10 × 10 × 1.20 mm) package outline, 001-54471

16 Ordering information

Table 16 Ordering information

Ordering code	SD/eMMC SDIO ports	SRAM (KB)	Package type
CYUSB3025-BZXI	2	512	121-ball BGA

16.1 Ordering code definitions



17 Acronyms

Table 17 Acronyms used in this document

Acronym	Description
BGA	ball grid array
MMC	multimedia card
PLL	phase locked loop
SD	secure digital
SDIO	secure digital input / output
SLC	single-level cell
USB	universal serial bus

18 Document conventions

18.1 Units of measure

Table 18 Units of measure

Symbol	Unit of measure
°C	degree Celsius
MBps	Megabytes per second
MHz	mega hertz
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt

19 Errata

This section describes the errata for the SD3 CYUSB3025-BZXI. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description. Contact your local Infineon Sales Representative if you have questions.

Part numbers affected

Part number	Device characteristics
CYUSB3025-BZXI	All Variants

SD3 USB and Mass Storage Peripheral Controller qualification status

Product status: Sampling

SD3 USB and Mass Storage Peripheral Controller errata summary

The following table defines the errata applicability to available SD3 USB and Mass Storage Peripheral Controller family devices.

Items	Part number	Silicon revision	Fix status
1. **Turning off VIO1 during Normal, Suspend, and Standby modes causes the SD3 to stop working.**	CYUSB3025-BZXI	All	Workaround provided
2. **USB enumeration failure in USB boot mode when SD3 is self-powered.**	CYUSB3025-BZXI	All	Workaround provided
3. **Bus collision is seen when the I2C block is used as a master in the I2C Multi-master configuration.**	CYUSB3025-BZXI	All	Use SD3 in single-master configuration
4. **Low Power U1 Fast-Exit Issue with USB3.0 host controller.**	CYUSB3025-BZXI	All	Workaround provided
5. **USB data corruption when operating on hosts with poor link quality.**	CYUSB3025-BZXI	All	Workaround provided
6. **Device treats Rx Detect sequence from the USB 3.0 host as a valid U1 exit LFPS burst.**	CYUSB3025-BZXI	All	Workaround provided
7. **I2C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle.**	CYUSB3025-BZXI	All	No workaround needed
8. **ISD3 Device does not respond correctly to Port Capability Request from Host after multiple power cycles.**	CYUSB3025-BZXI	All	Workaround provided

1. Turning off VIO1 during Normal, Suspend, and Standby modes causes the SD3 to stop working.	
Problem definition	Turning off the VIO1 during Normal, Suspend, and Standby modes will cause the SD3 to stop working.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the VIO1 is turned off during Normal, Suspend, and Standby modes.
Scope of impact	SD3 stops working.
Workaround	VIO1 must stay on during Normal, Suspend, and Standby modes.
Fix status	No fix. Workaround is required.

2. USB enumeration failure in USB boot mode when SD3 is self-powered.	
Problem definition	When SD3 is self-powered and not connected to the USB host, it enters low-power mode and does not wake up when connected to USB host afterwards. This is because the bootloader does not check the VBUS pin on the connector to detect USB connection. It expects that the USB bus is connected to the host when it is powered on.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when SD3 is self-powered in USB boot mode.
Scope of impact	Device does not enumerate.
Workaround	Reset the device after connecting to USB host.
Fix status	No fix. Workaround is required.

3. Bus collision is seen when the I^2C block is used as a master in the I^2C Multi-master configuration.	
Problem definition	When SD3 is used as a master in the I^2C multi-master configuration, there can be occasional bus collisions.
Parameters affected	NA
Trigger condition(s)	This condition is triggered only when the SD3 I^2C block operates in Multi-master configuration.
Scope of impact	The SD3 I^2C block can transmit data when the I^2C bus is not idle leading to bus collision.
Workaround	Use SD3 as a single master.
Fix status	No fix.

4. Low Power U1 Fast-Exit Issue with USB3.0 host controller.	
Problem definition	When SD3 device transitions from Low power U1 state to U0 state within 5 µs after entering U1 state, the device sometimes fails to transition back to U0 state, resulting in USB Reset.
Parameters affected	NA
Trigger condition(s)	This condition is triggered during low power transition mode.
Scope of impact	Unexpected USB warm reset during data transfer.
Workaround	This problem can be worked around in the FW by disabling LPM (Link Power Management) during data transfer.
Fix status	FW workaround is proven and reliable.

5. USB data corruption when operating on hosts with poor link quality.	
Problem definition	If SD3 is operating on a USB 3.0 link with poor signal quality, the device could send corrupted data on any of the IN endpoints (including the control endpoint).
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the USB3.0 link signal quality is very poor.
Scope of impact	Data corruption in any of the IN endpoints (including the control endpoint).
Workaround	The application firmware should perform an error recovery by stalling the endpoint on receiving CYU3P_USBEPSS_RESET_EVT event, and then stop and restart DMA path when the CLEAR_FEATURE request is received. Note: SDK versions 1.3.3 and above internally manages the DMA transfers and performs the endpoint reset when potential error conditions are seen. For more details in application firmware, please refer to **GpiftoUsb** example available with SDK.
Fix status	FW Work-around is proven and reliable.

6. Device treats Rx Detect sequence from the USB 3.0 host as a valid U1 exit LFPS burst.	
Problem definition	The USB 3.0 PHY in the SD3 device uses an electrical idle detector to determine whether LFPS is being received. The duration for which the receiver does not see an electrical idle condition is timed to detect various LFPS bursts. This implementation causes the device to treat an Rx Detect sequence from the USB host as a valid U1 exit LFPS burst.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the USB host is initiating an Rx Detect sequence while the USB 3.0 Link State Machine on the SD3 is in the U1 state. Since the host will only perform Rx Detect sequence in the RX Detect and U2 states, the error condition is seen only in cases where the USB link on the host has moved into the U2 state while the link on SD3 is in the U1 state.
Scope of impact	SD3 moves into Recovery prematurely leading to a Recovery failure followed by Warm Reset and USB re-enumeration. This sequence can repeat multiple times resulting in data transfer failures.
Workaround	SD3 can be configured to transition from U1 to U2 a few microseconds before the host does so. This will ensure that the link will be in U2 on the device side before the host attempts any Rx Detect sequence; thereby preventing a false detection of U1 exit.
Fix status	Workaround is implemented in FX3 SDK library 1.3.4 and above.

7. I^2C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle.	
Problem definition	I^2C Data Valid (tVD:DAT) parameter at 400 kHz with a 40/60 duty cycle is 1.0625 µs, which exceeds the I^2C specification limit of 0.9 µs.
Parameters affected	NA
Trigger condition(s)	This violation occurs only at 400 kHz with a 40/60 duty cycle of the I^2C clock.
Scope of impact	Setup time (t_{SUDAT}) is met with a huge margin for the transmitted data for 400 kHz and so $t_{vd:DAT}$ violation will not cause any data integrity issues.
Workaround	No workaround needed.
Fix status	No fix needed.

8. ISD3 Device does not respond correctly to Port Capability Request from Host after multiple power cycles.	
Problem definition	During multiple power cycles, sometimes the SD3 device does not respond correctly to the Port Capability request (Link Packet) from the USB Controller. In view of this, SD3 does not get the subsequent Port Configuration request from the USB controller, resulting in SS.Disabled state. The device fails to recover from this state and finally results in enumeration failure.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the SD3 provides an incorrect response to the Port Capability request from the host.
Scope of impact	Device fails to enumerate after multiple retries.
Workaround	Since the host does not send the Port Configuration request to the SD3 device, it causes a Port Configuration request timeout interrupt to be triggered in the device. This interrupt is handled in the FX3 SDK 1.3.4 onwards to generate and signal CY_U3P_USB_EVENT_LMP_EXCH_FAIL event to the application. This event should be handled in the user application such that it does a USB Interface Block Restart. Refer the Knowledge Base Article (**KBA225778**) for more details and the firmware workaround example project.
Fix status	Suggested firmware work-around is proven and reliable.

Revision history

Document revision	Date	Description of changes
*O	2023-04-27	Release to web.

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Email:
erratum@infineon.com

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