MOSFET

StrongIRFET™

PG-TO 247-3



Features

- Very low $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ (FOM)
- Optimized Q_{rr}
- 175°C operating temperature
- Product validation according to JEDEC standard
- Optimized for broadest availability from distribution partners

Benefits

- Reduced conduction losses
- Ideal for high switching frequency
- Lower overshoot voltage
- Increased reliability versus 150°C rated parts
- Halogen-free according to IEC61249-2-21

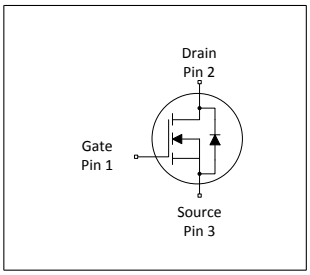


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),typ}$	1.1	mΩ
$R_{DS(on),max}$	1.28	mΩ
$I_{D(Silicon\ Limited)}$	483	A
$I_{D(Package\ Limited)}$	209	A
$Q_G(0V..10V)$	330	nC

Type / Ordering Code	Package	Marking	Related Links
IRF100P218	PG-TO 247-3	IRF100P218	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	209 483 341	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=25 °C (silicon limited) V_{GS}=10 V, T_C=100 °C (silicon limited)[1]
Pulsed drain current[1]	$I_{D,pulse}$	-	-	836	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	1050	mJ	I_D=100 A, R_{GS}=50 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	556 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W[3]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case[4]	R_{thJC}	-	-	0.27	°C/W	-
Thermal resistance, junction -Ambient	R_{thJA}	-	-	40	°C/W	-
Case-to-Sink, Flat Greased Surface	R_{thCS}	-	0.24	-	°C/W	-

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[4] R_{thJC} is measured at T_J approximately 90°C.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	40	-	mV/°C	I_D=2 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	2.2	-	3.8	V	V_{DS}=V_{GS}, I_D=278 µA
Zero gate voltage drain current	I_{DSS}	- -	- -	5 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.1 1.3	1.28 1.5	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=6 V, I_D=50 A
Gate resistance[1)]	R_G	-	0.6	-	Ω	-
Transconductance	g_{fs}	-	350	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	24000	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	3500	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	150	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	50	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, R_G=2.7 Ω
Rise time	t_r	-	110	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, R_G=2.7 Ω
Turn-off delay time	$t_{d(off)}$	-	170	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, R_G=2.7 Ω
Fall time	t_f	-	120	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, R_G=2.7 Ω

[1)] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	100	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	71	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge[2)]	Q_{gd}	-	65	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	95	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total[2)]	Q_g	-	330	412	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	265	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	411	-	nC	V_{DD}=50 V, V_{GS}=0 V

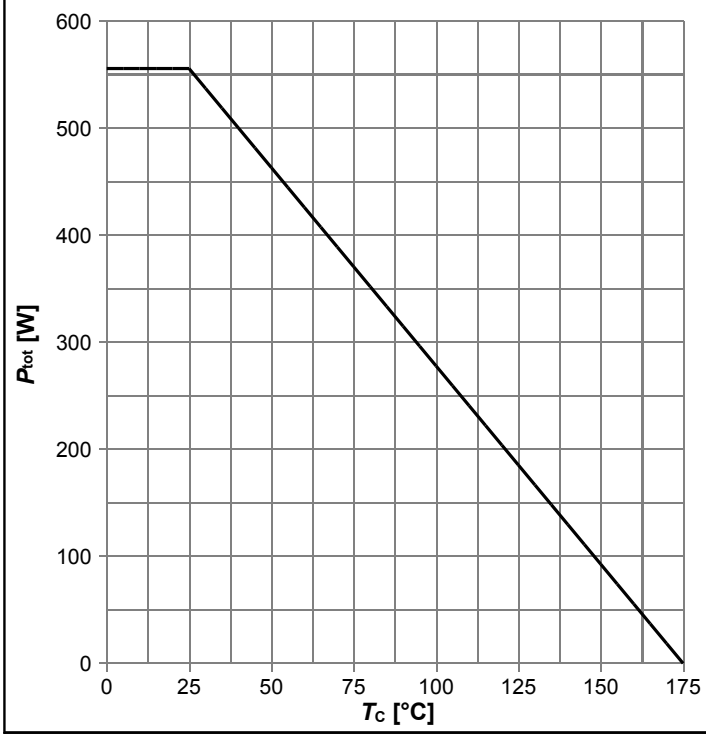
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	209	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	836	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time[2)]	t_{rr}	-	110	-	ns	V_R=85 V, I_F=100 A, di_F/dt=100 A/µs, Tj=25 °C
Reverse recovery charge[2)]	Q_{rr}	-	280	-	nC	V_R=85 V, I_F=100 A, di_F/dt=100 A/µs, Tj=25 °C

[1)] See "Gate charge waveforms" for parameter definition
[2)] Defined by design. Not subject to production test.

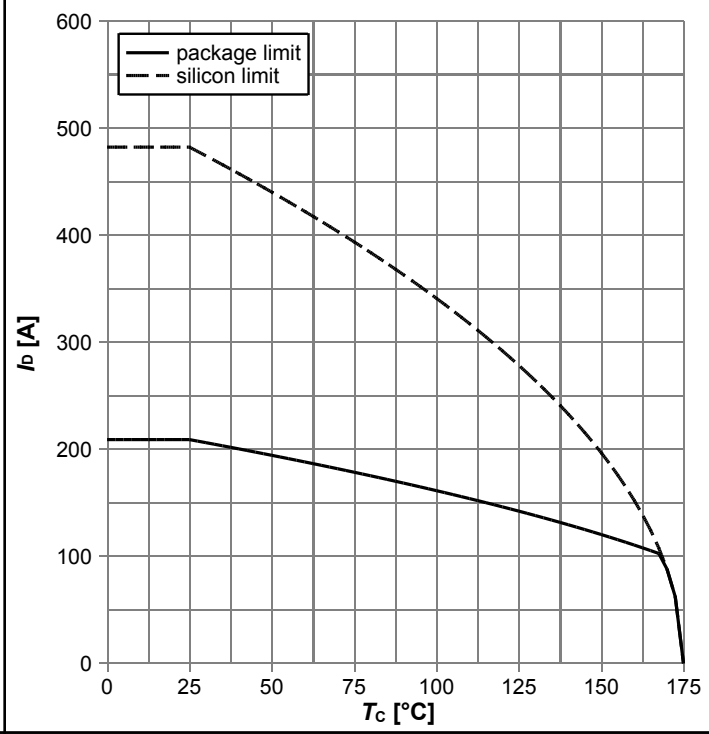
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



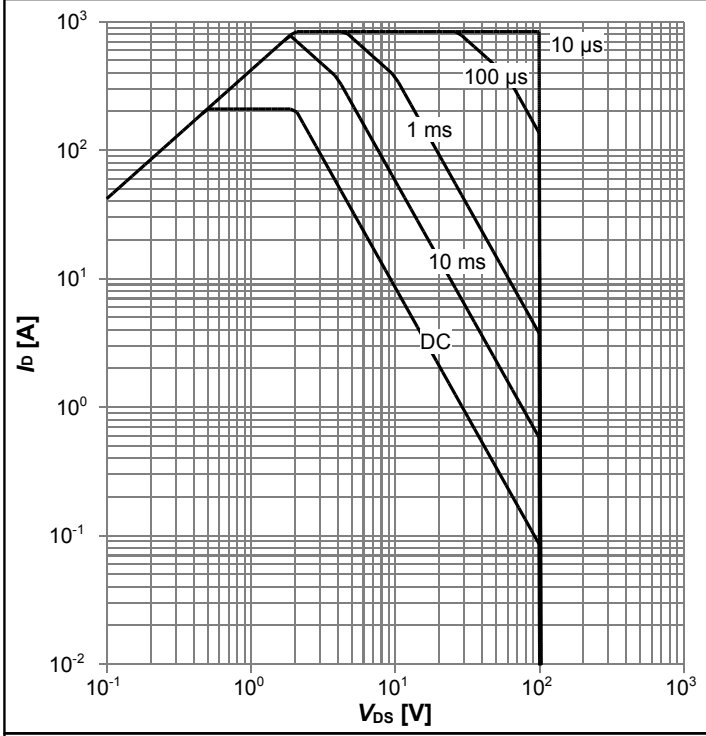
$P_{tot}=f(T_C)$

Diagram 2: Drain current



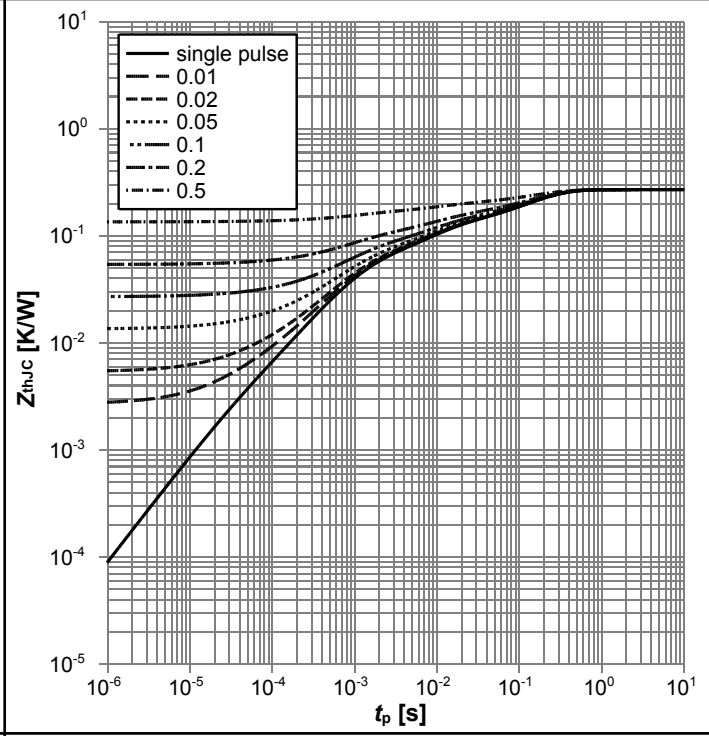
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



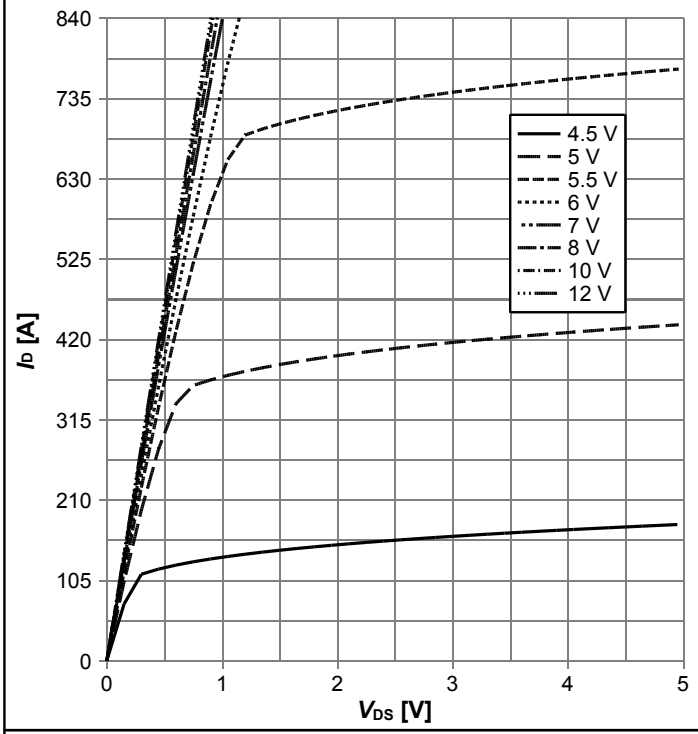
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



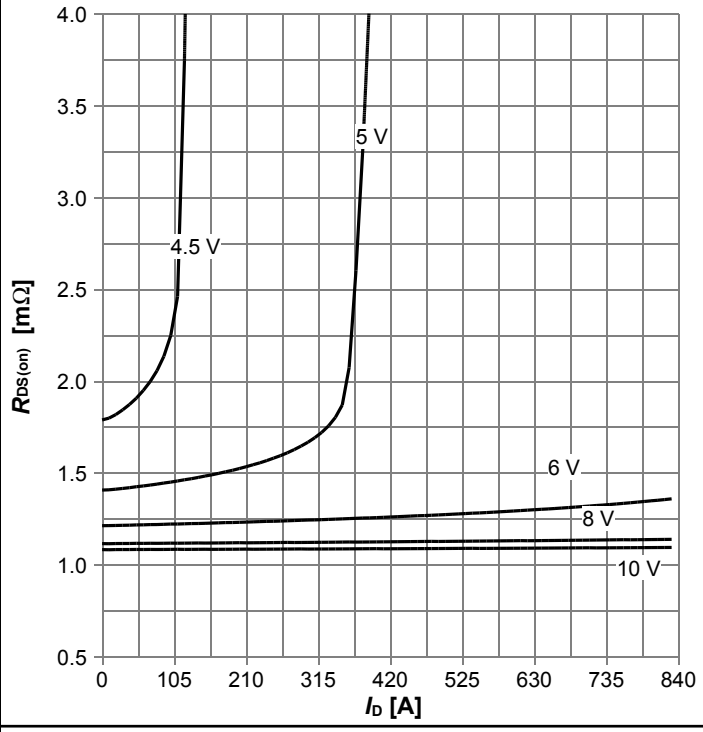
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



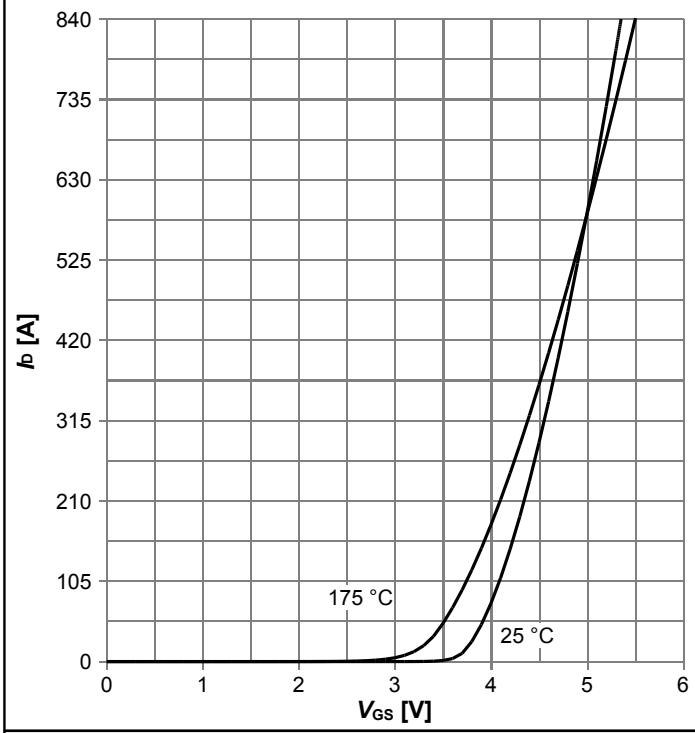
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



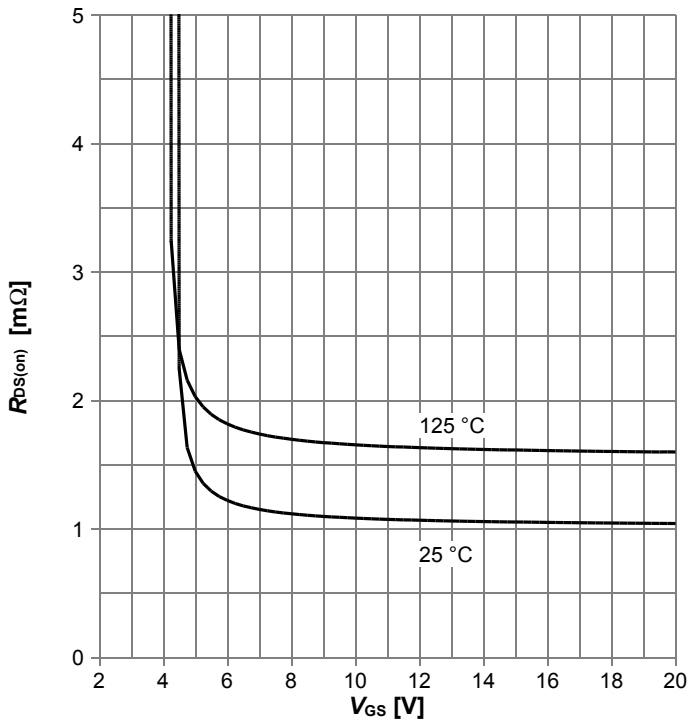
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



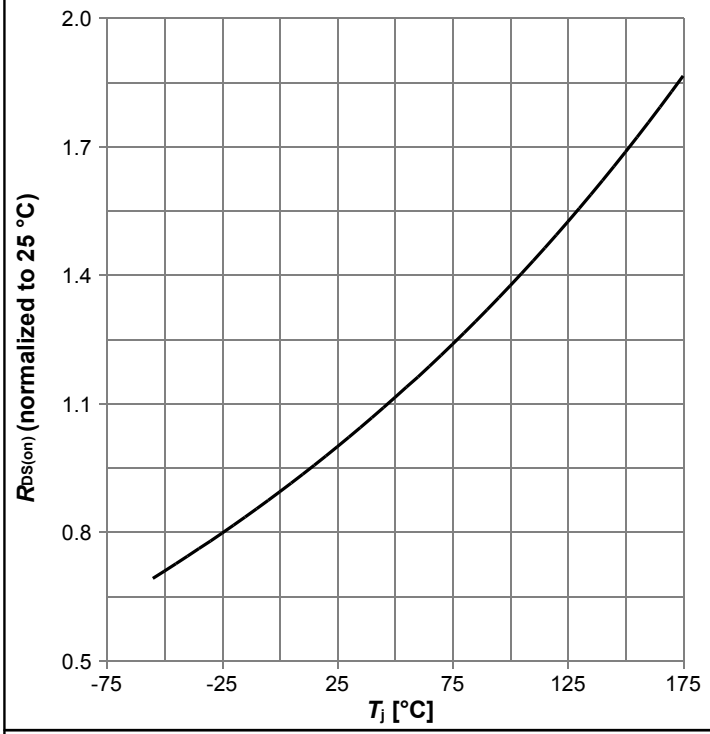
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



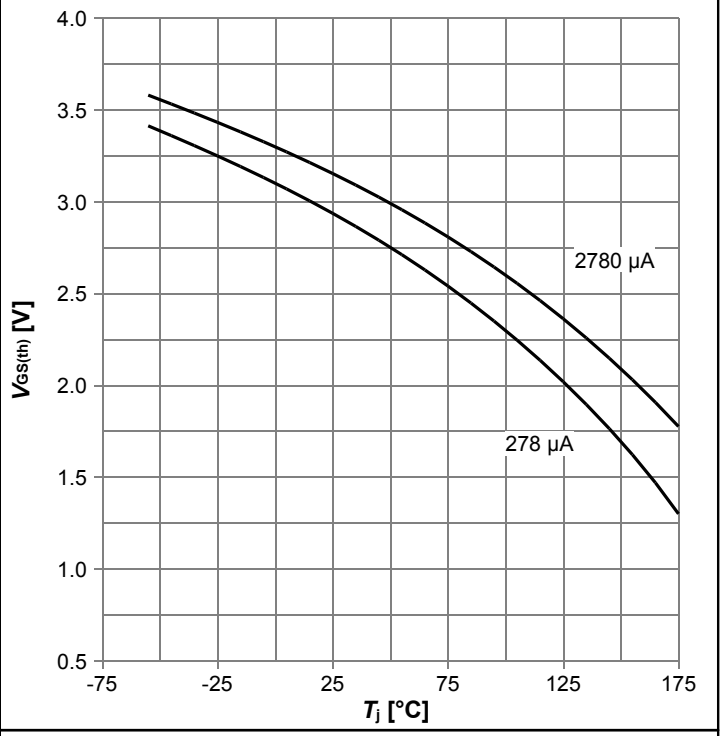
$R_{DS(on)}=f(V_{GS})$, $I_D=100$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



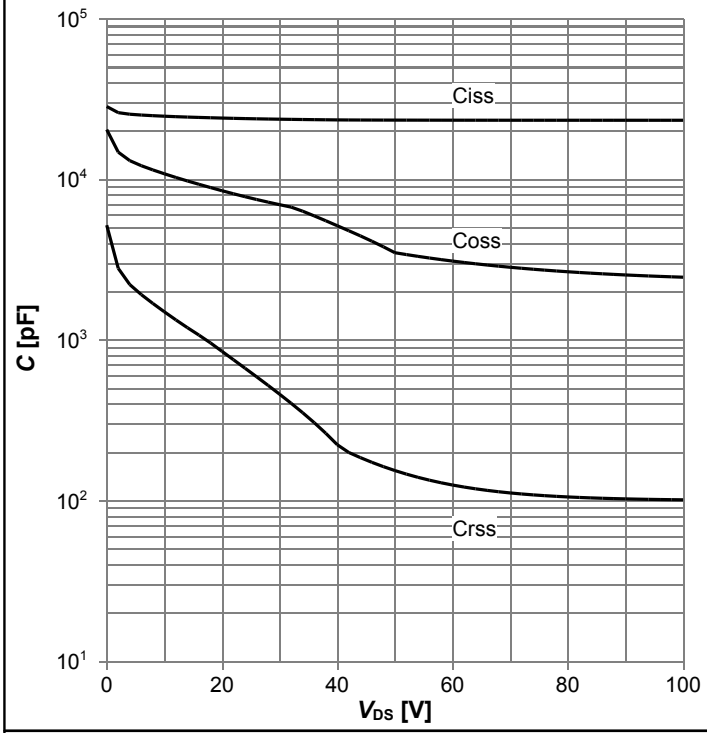
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



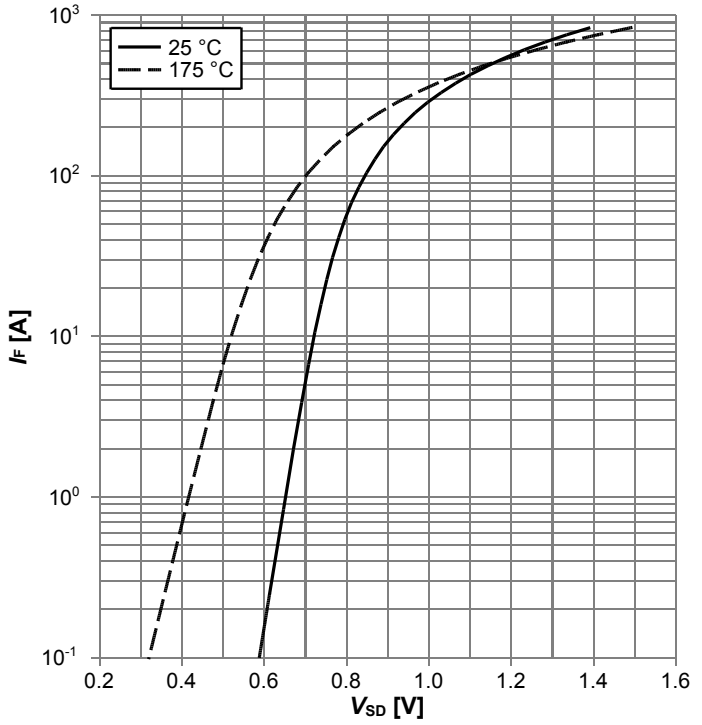
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



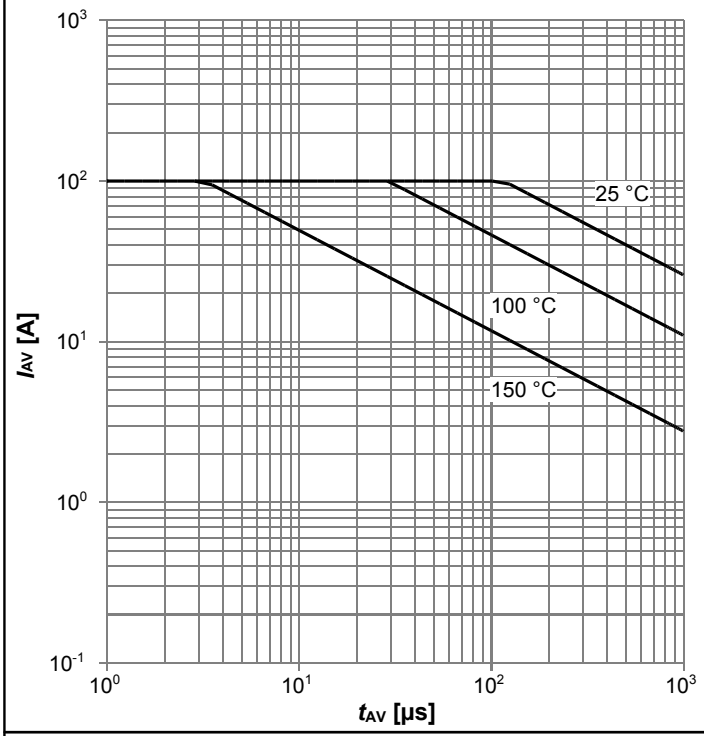
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



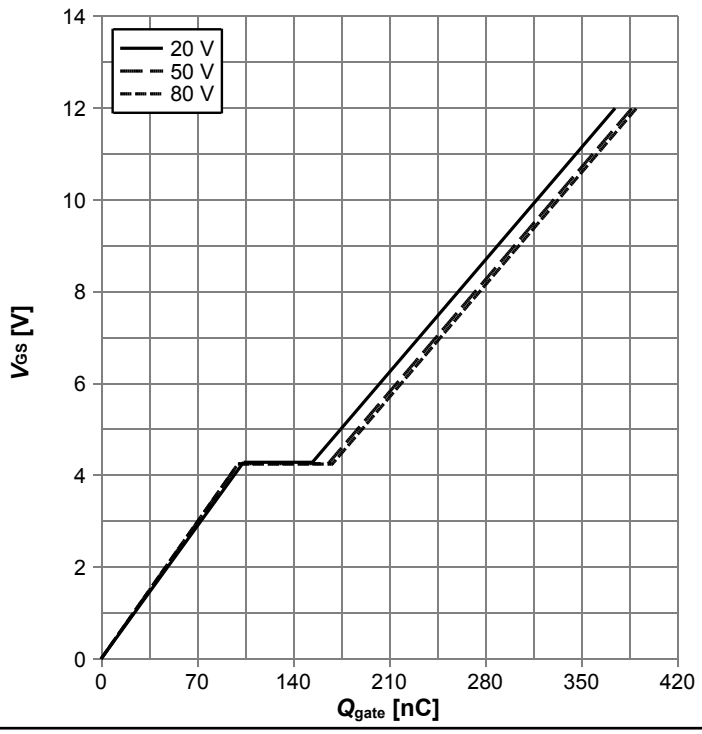
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



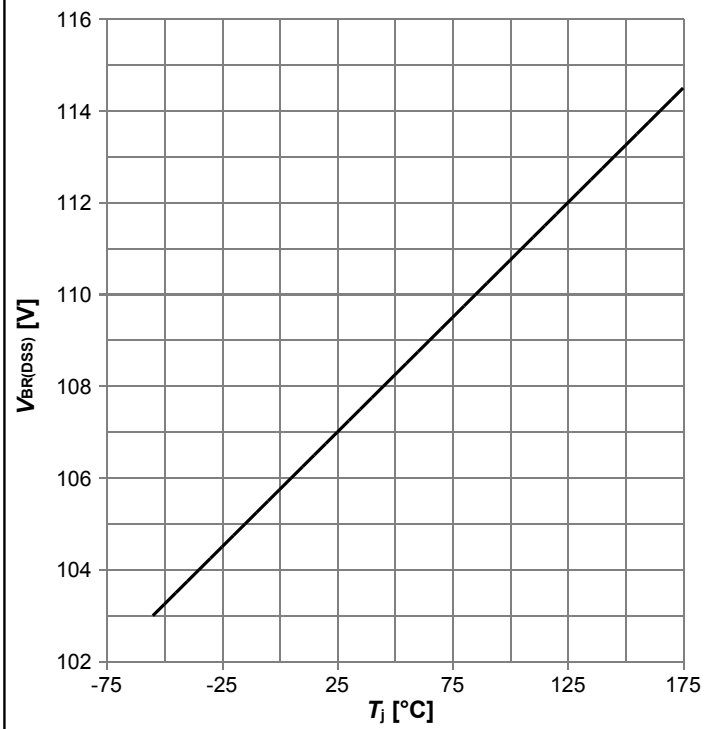
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



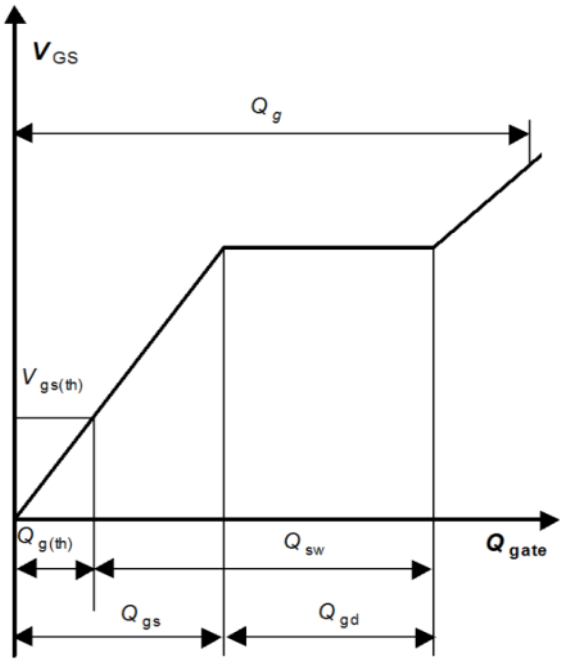
V_{GS}=f(Q_{gate}), I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

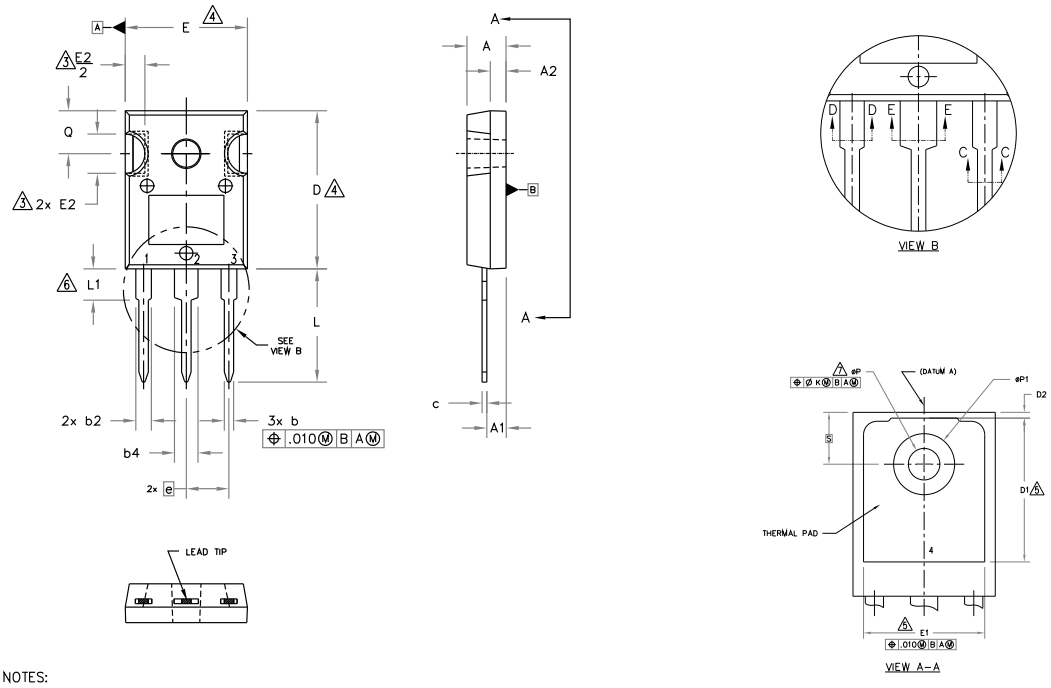


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

Figure 1 Outline PG-TO 247-3, dimensions in mm/inches

Revision History

IRF100P218

Revision: 2020-01-20, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
1.0	2018-09-25	Release of preliminary version
2.0	2018-10-16	Release of final version
2.1	2020-01-20	Update from IR MOSFT/StrongIRFET™ to StrongIRFET™

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81726 München, Germany
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