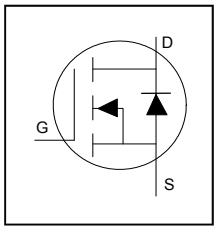
International
IOR Rectifier

# StrongIRFET™
# IRL40B209

HEXFET® Power MOSFET

**Application**
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters




| | |
|---|---|
| $V_{DSS}$ | 40V |
| $R_{DS(on)}$ typ. | 1.0mΩ |
| max | 1.25mΩ |
| $I_{D\ (Silicon\ Limited)}$ | 414A① |
| $I_{D\ (Package\ Limited)}$ | 195A |




TO-220AB
IRL40B209

**Benefits**
- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- RoHS Compliant, Halogen-Free

| G | D | S |
|---|---|---|
| Gate | Drain | Source |

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRL40B209 | TO-220 | Tube | 50 | IRL40B209 |

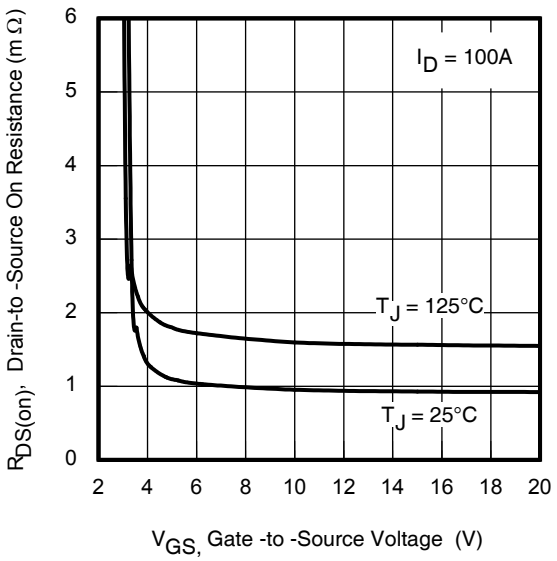



**Fig 1.** Typical On-Resistance vs. Gate Voltage

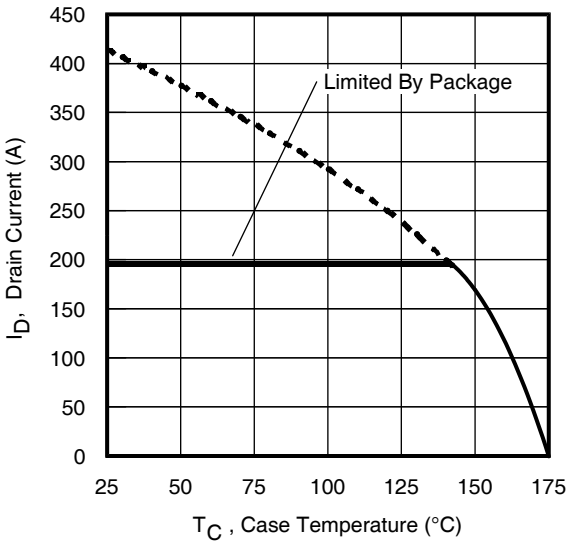



**Fig 2.** Maximum Drain Current vs. Case Temperature

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**Absolute Maximum Rating**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 414① | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 293① | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited) | 195 | |
| $I_{DM}$ | Pulsed Drain Current ② | 1707 ⑩ | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 375 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |
| | Mounting Torque, 6-32 or M3 Screw | 10 lbf·in (1.1 N·m) | |

**Avalanche Characteristics**

| | | | |
|---|---|---|---|
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ③ | 730 | mJ |
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ⑨ | 1420 | |
| $I_{AR}$ | Avalanche Current ② | See Fig 15, 16, 23a, 23b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ② | | mJ |

**Thermal Resistance**

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑧ | — | 0.4 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 62 | |

**Static @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.031 | — | V/°C | Reference to 25°C, $I_D$ = 5mA ② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 1.0 | 1.25 | mΩ | $V_{GS}$ = 10V, $I_D$ = 100A⑤ |
| | | — | 1.2 | 1.6 | | $V_{GS}$ = 4.5V, $I_D$ = 50A ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 2.4 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 1.0 | µA | $V_{DS}$ =40 V, $V_{GS}$ = 0V |
| | | — | — | 150 | | $V_{DS}$ =40V,$V_{GS}$ = 0V,$T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Gate Resistance | — | 2.1 | — | Ω | |

**Notes:**

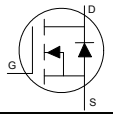
① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
② Repetitive rating; pulse width limited by max. junction temperature.
③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.15mH,$R_G$ = 50Ω, $I_{AS}$ = 100A, $V_{GS}$ =10V.
④ $I_{SD} \le$ 100A, di/dt ≤ 930A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C.
⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.
⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.
⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$
⑧ $R_\theta$ is measured at $T_J$ approximately 90°C.
⑨ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 1mH, $R_G$ = 50Ω, $I_{AS}$ = 53A, $V_{GS}$ =10V.
⑩ Pulse drain current is limited at 780A by source bonding technology.

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**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 270 | — | — | S | $V_{DS}$ = 10V, $I_D$ =100A |
| $Q_g$ | Total Gate Charge | — | 180 | 270 | nC | $I_D$ = 100A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 51 | — | | $V_{DS}$ = 20V |
| $Q_{gd}$ | Gate-to-Drain Charge | — | 88 | — | | $V_{GS}$ = 4.5V⑤ |
| $Q_{sync}$ | Total Gate Charge Sync. (Qg – Qgd) | — | 92 | — | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | 56 | — | ns | $V_{DD}$ = 20V |
| $t_r$ | Rise Time | — | 198 | — | | $I_D$ = 30A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 188 | — | | $R_G$= 2.7Ω |
| $t_f$ | Fall Time | — | 150 | — | | $V_{GS}$ = 4.5V⑤ |
| $C_{iss}$ | Input Capacitance | — | 15140 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 1990 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 1370 | — | | $f$ = 1.0MHz, See Fig.7 |
| $C_{oss\ eff.(ER)}$ | Effective Output Capacitance | — | 2340 | — | | $V_{GS}$ = 0V, VDS = 0V to 32V⑦ |
| $C_{oss\ eff.(TR)}$ | Output Capacitance (Time Related) | — | 2900 | — | | $V_{GS}$ = 0V, VDS = 0V to 32V⑥ |

**Diode Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 414① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ② | — | — | 1707⑩ | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.2 | V | $T_J$ = 25°C,$I_S$ = 100A,$V_{GS}$ = 0V ⑤ |
| dv/dt | Peak Diode Recovery dv/dt④ | — | 2.4 | — | V/ns | $T_J$ = 175°C,$I_S$ = 100A,$V_{DS}$ = 40V |
| $t_{rr}$ | Reverse Recovery Time | — | 41 | — | ns | $T_J$ = 25°C $V_{DD}$ = 34V |
| | | — | 42 | — | | $T_J$ = 125°C $I_F$ = 100A, |
| $Q_{rr}$ | Reverse Recovery Charge | — | 46 | — | nC | $T_J$ = 25°C di/dt = 100A/µs ⑤ |
| | | — | 50 | — | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | — | 2.0 | — | A | $T_J$ = 25°C |

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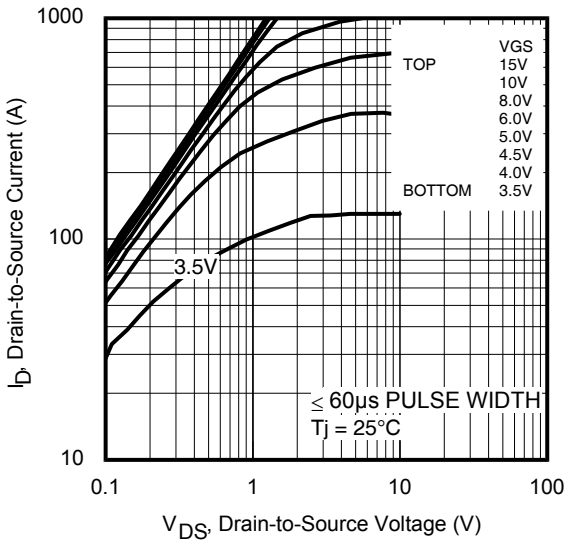



**Fig 3.** Typical Output Characteristics

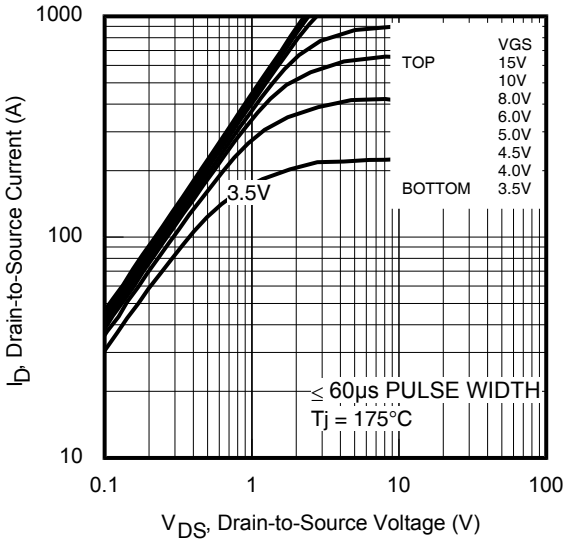



**Fig 4.** Typical Output Characteristics

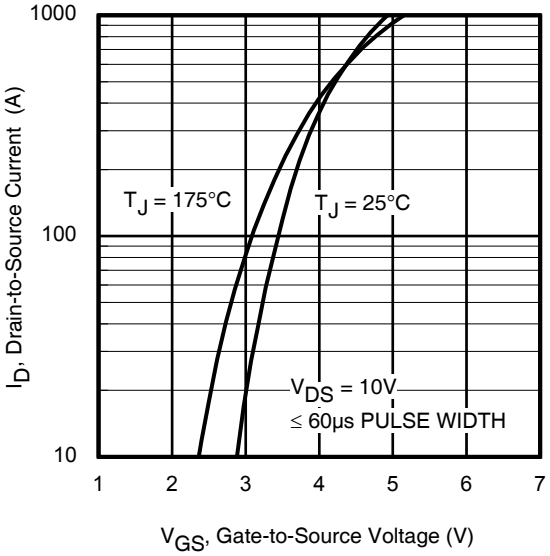



**Fig 5.** Typical Transfer Characteristics

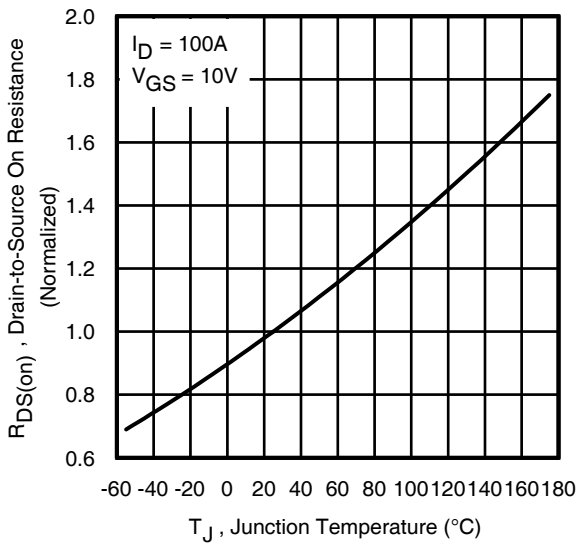



**Fig 6.** Normalized On-Resistance vs. Temperature

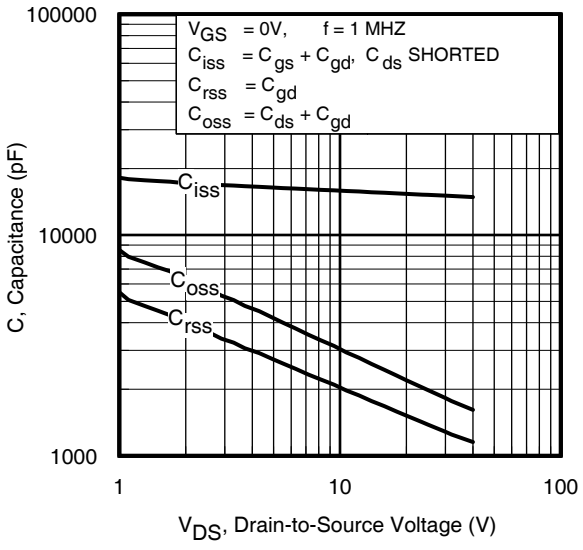



**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

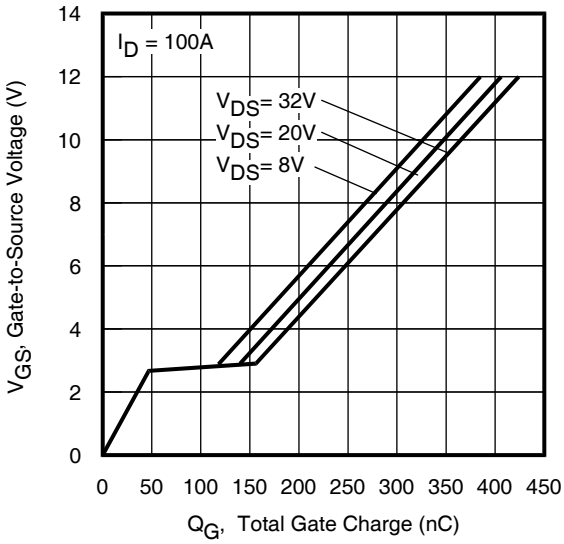



**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage

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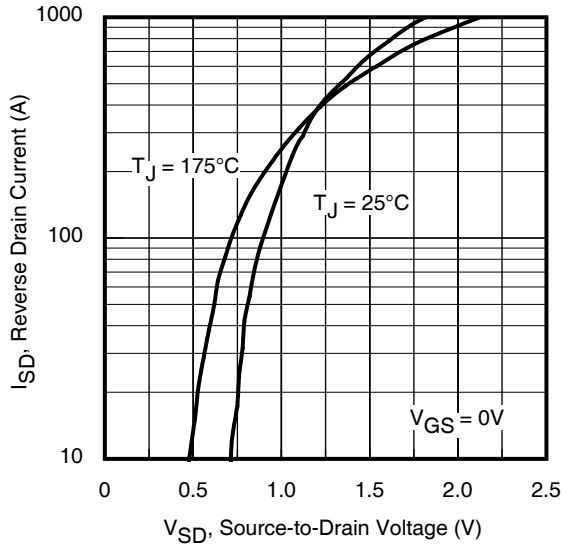



**Fig 9.** Typical Source-Drain Diode Forward Voltage

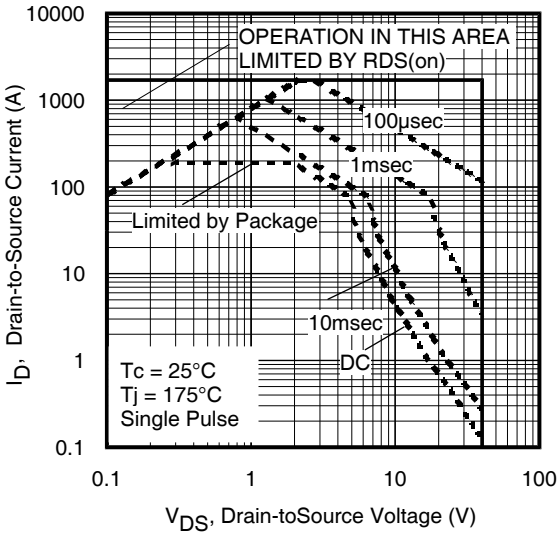



**Fig 10.** Maximum Safe Operating Area

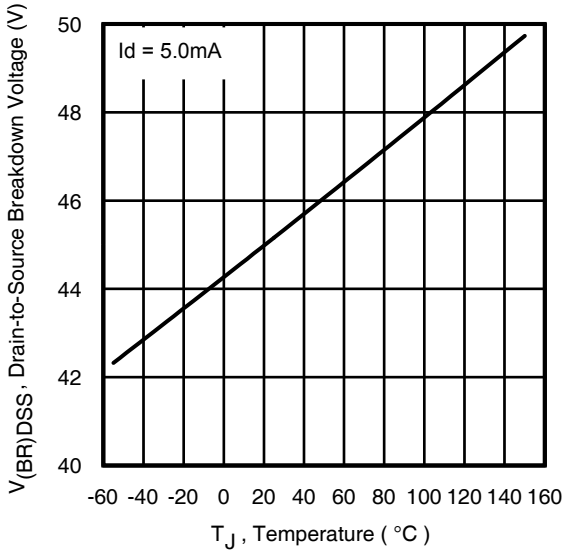



**Fig 11.** Drain-to-Source Breakdown Voltage

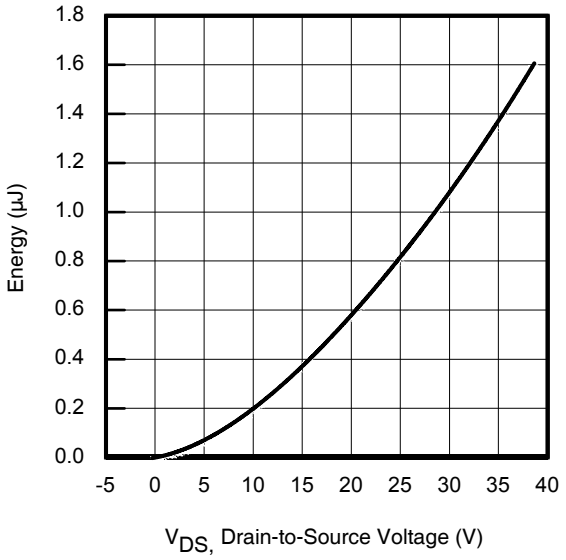



**Fig 12.** Typical $C_{oss}$ Stored Energy

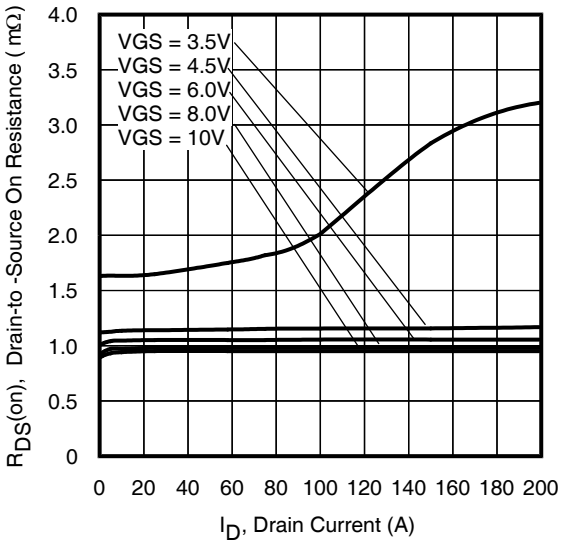



**Fig 13.** Typical On-Resistance vs. Drain Current

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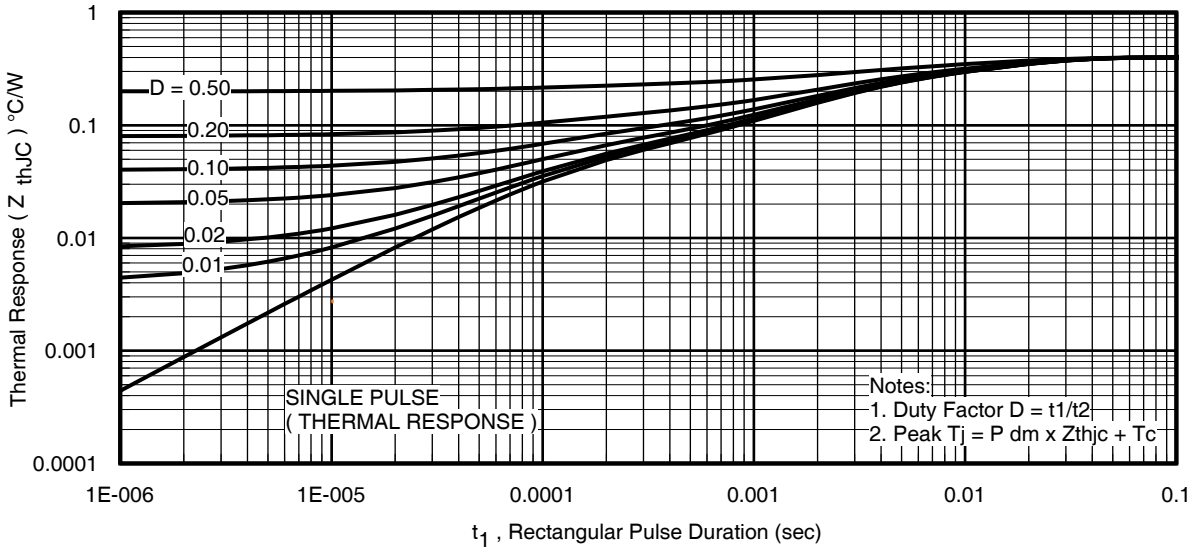



**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

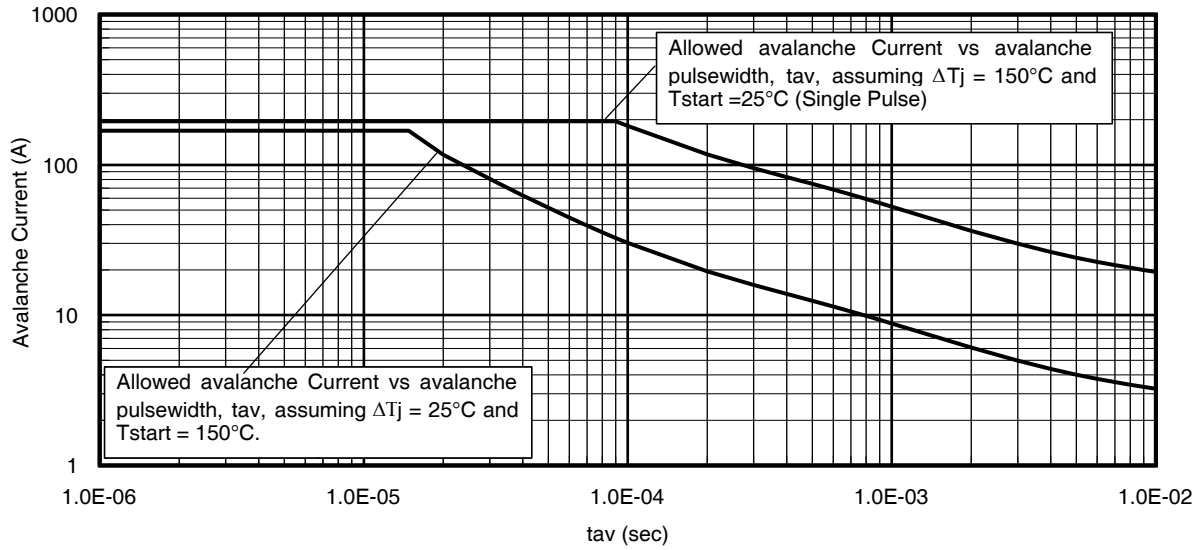



**Fig 15.** Avalanche Current vs. Pulse Width

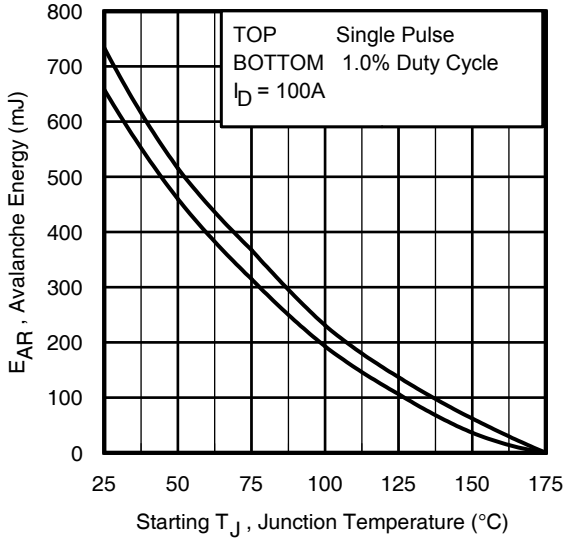



**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at www.irf.com)**

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. $I_{av}$ = Allowable avalanche current.

7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figures14, 15).

$t_{av}$ = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 14)

$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

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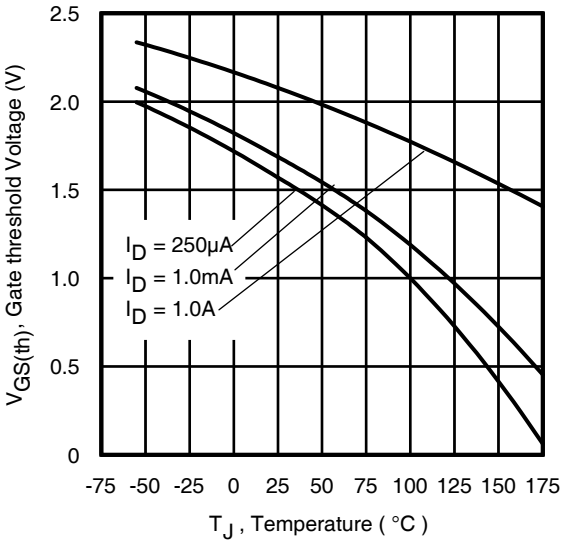



**Fig 17.** Threshold Voltage vs. Temperature

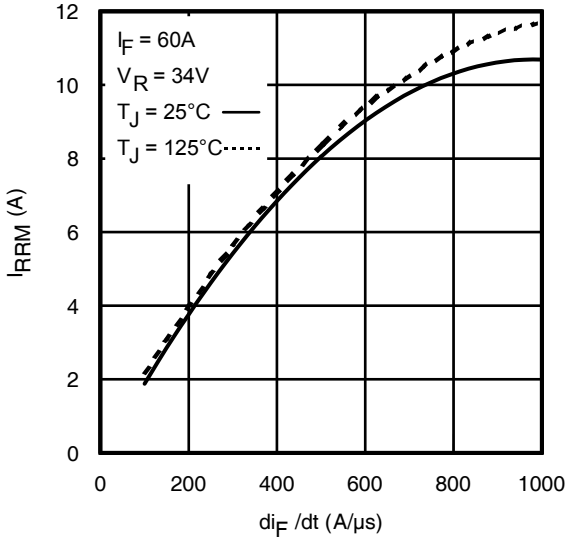



**Fig 18.** Typical Recovery Current vs. dif/dt

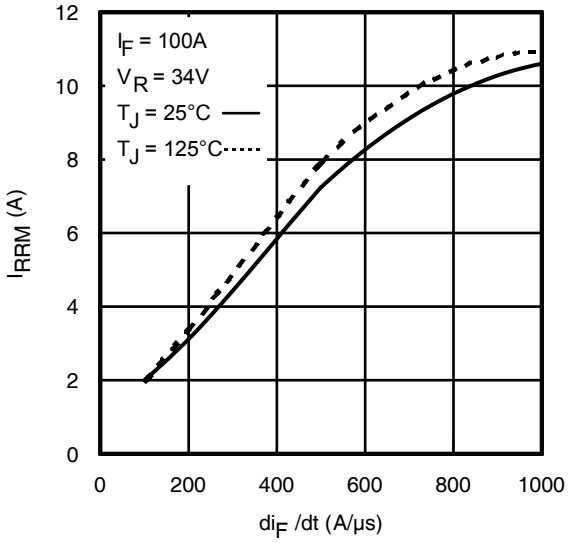



**Fig 19.** Typical Recovery Current vs. dif/dt

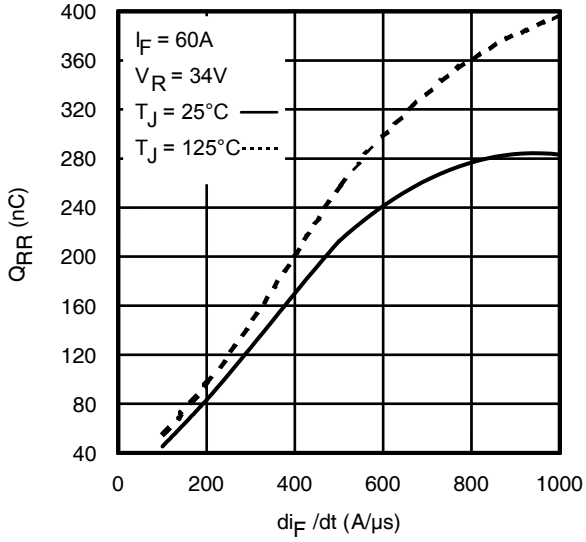



**Fig 20.** Typical Stored Charge vs. dif/dt

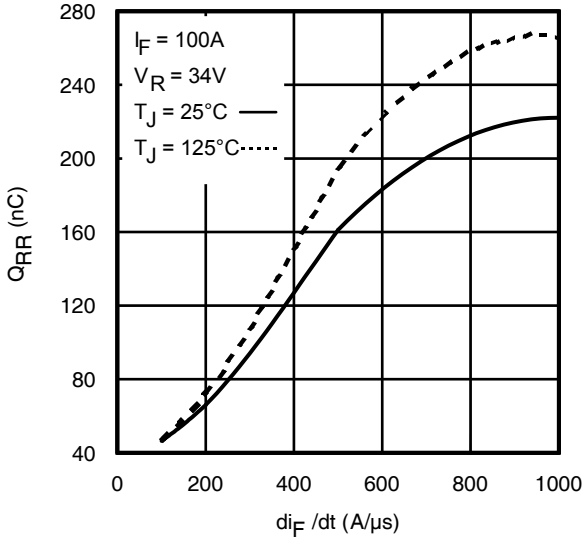



**Fig 21.** Typical Stored Charge vs. dif/dt

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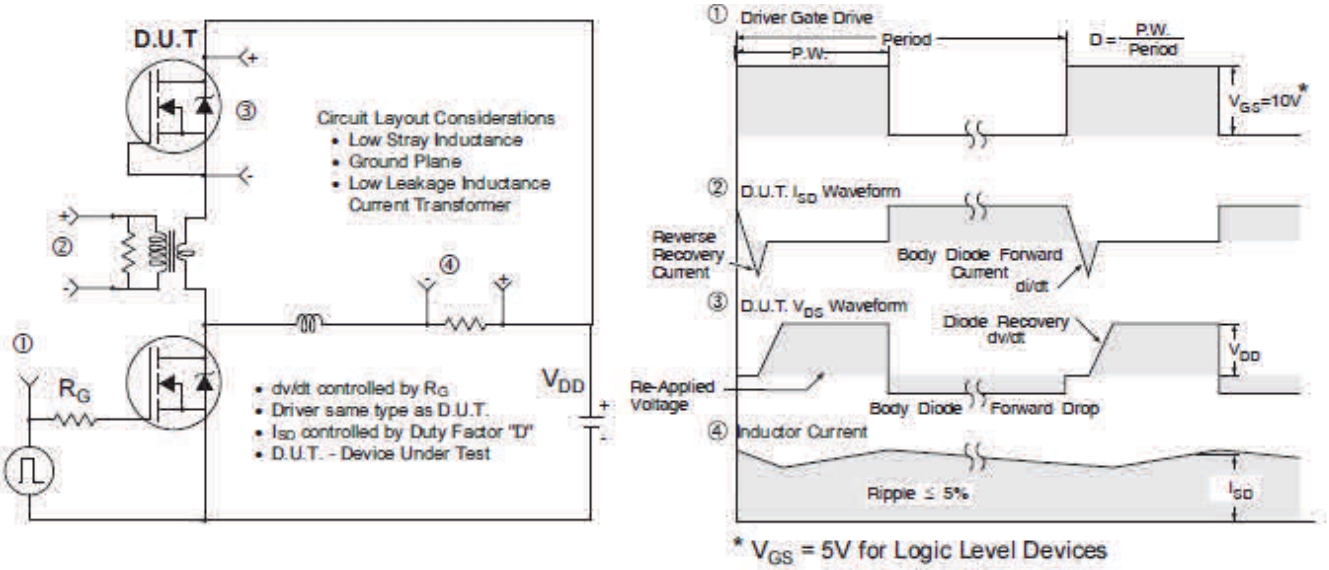



**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

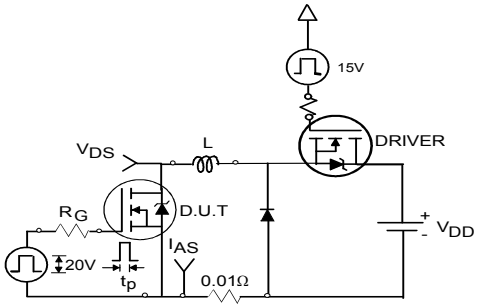



**Fig 23a.** Unclamped Inductive Test Circuit

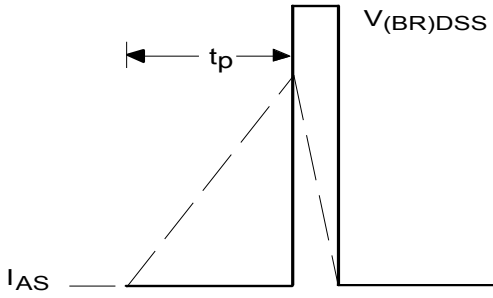



**Fig 23b.** Unclamped Inductive Waveforms

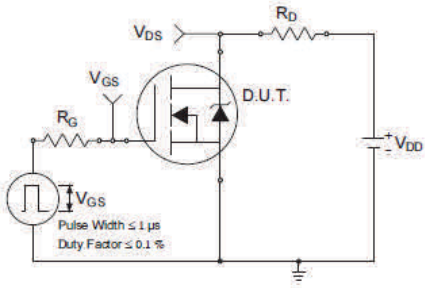



**Fig 24a.** Switching Time Test Circuit

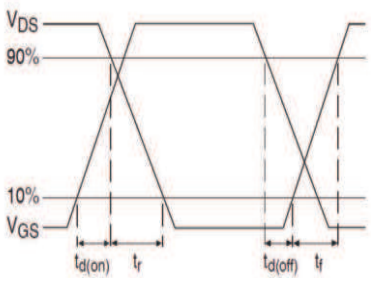



**Fig 24b.** Switching Time Waveforms

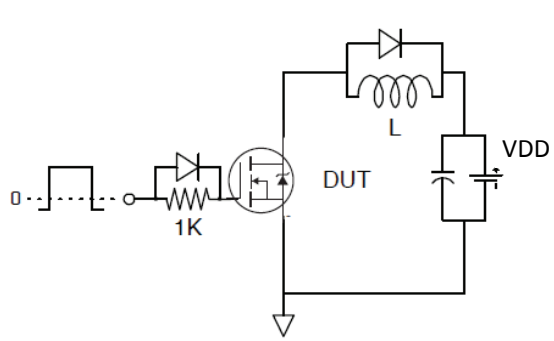



**Fig 25a.** Gate Charge Test Circuit

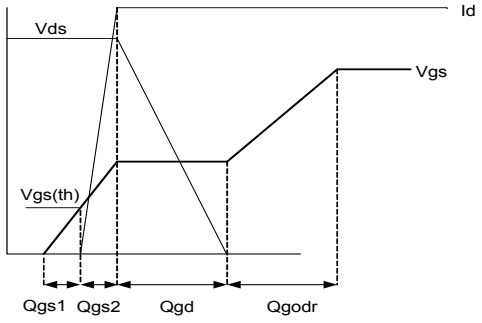
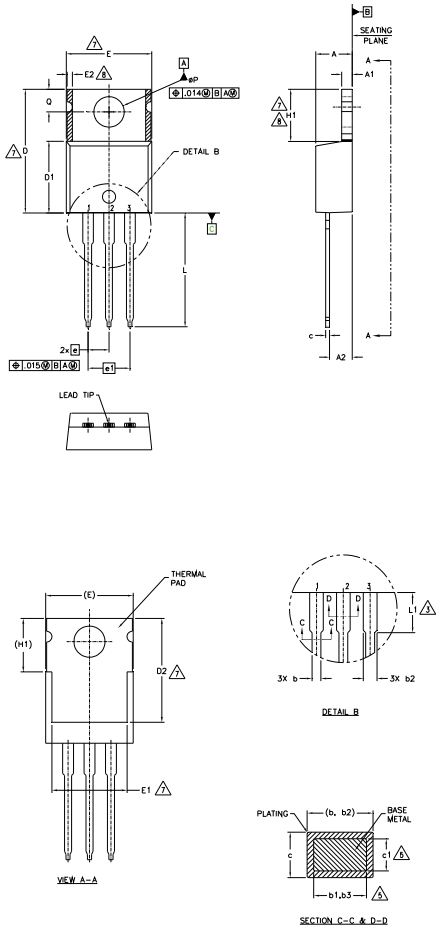



**Fig 25b.** Gate Charge Waveform

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**TO-220AB Package Outline** (Dimensions are shown in millimeters (inches))




NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.– DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.– DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5.– DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
6.– CONTROLLING DIMENSION : INCHES.
7.– THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8.– DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
9.– OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 3.56 | 4.83 | .140 | .190 | |
| A1 | 1.14 | 1.40 | .045 | .055 | |
| A2 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.38 | 1.01 | .015 | .040 | |
| b1 | 0.38 | 0.97 | .015 | .038 | 5 |
| b2 | 1.14 | 1.78 | .045 | .070 | |
| b3 | 1.14 | 1.73 | .045 | .068 | 5 |
| c | 0.36 | 0.61 | .014 | .024 | |
| c1 | 0.36 | 0.56 | .014 | .022 | 5 |
| D | 14.22 | 16.51 | .560 | .650 | 4 |
| D1 | 8.38 | 9.02 | .330 | .355 | |
| D2 | 11.68 | 12.88 | .460 | .507 | 7 |
| E | 9.65 | 10.67 | .380 | .420 | 4,7 |
| E1 | 6.86 | 8.89 | .270 | .350 | 7 |
| E2 | – | 0.76 | – | .030 | 8 |
| e | 2.54 BSC | | .100 BSC | | |
| e1 | 5.08 BSC | | .200 BSC | | |
| H1 | 5.84 | 6.86 | .230 | .270 | 7,8 |
| L | 12.70 | 14.73 | .500 | .580 | |
| L1 | 3.56 | 4.06 | .140 | .160 | 3 |
| øP | 3.54 | 4.08 | .139 | .161 | |
| Q | 2.54 | 3.42 | .100 | .135 | |

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE

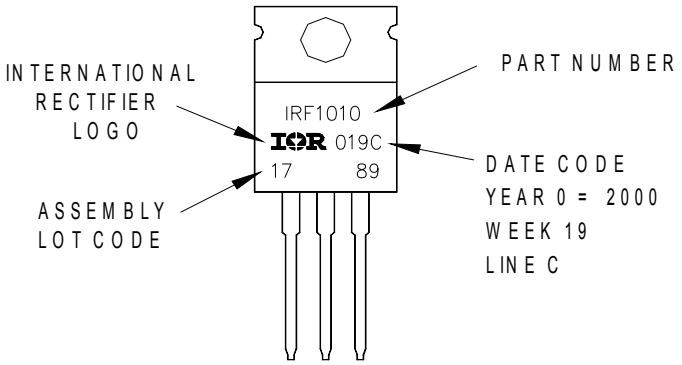
IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES
1.– ANODE
2.– CATHODE
3.– ANODE

**TO-220AB Part Marking Information**

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"




TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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**Qualification Information**†

| | | |
|---|---|---|
| **Qualification Level** | Industrial (per JEDEC JESD47F) †† | |
| **Moisture Sensitivity Level** | TO-220 | N/A |
| **RoHS Compliant** | Yes | |

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

International IOR Rectifier

**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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