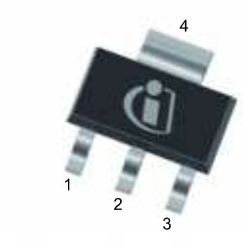
# MOSFET

## OptiMOS™ Power-Transistor, -100 V

PG-SOT223-4

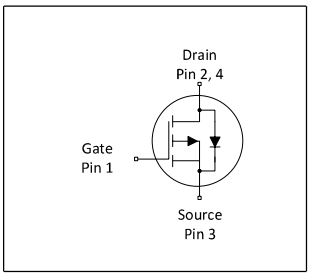



### Features

- P-channel
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}$=4.5 V
- 100% avalanche tested
- Logic level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Fully qualified according to JEDEC for Industrial Applications




### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | -100 | V |
| $R_{DS(on),max}$ | 160 | mΩ |
| $I_D$ | -3.9 | A |
| $Q_{oss}$ | -13 | nC |
| $Q_G$ | -42 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| ISP16DP10LM | PG-SOT223-4 | 16DP10LM | - |

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# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

## Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1] | $I_D$ | -<br>-<br>-<br>- | -<br>-<br>-<br>- | -3.9<br>-2.4<br>-2.2<br>-2.1 | A | $V_{GS}$=-10 V, $T_C$=25 °C<br>$V_{GS}$=-10 V, $T_C$=100 °C<br>$V_{GS}$=-4.5 V, $T_C$=100 °C<br>$V_{GS}$=-4.5 V,$T_A$=25°C,$R_{thJA}$=70 °C/W[2] |
| Pulsed drain current[3] | $I_{D,pulse}$ | - | - | -15.6 | A | $T_A$=25 °C |
| Avalanche energy, single pulse[4] | $E_{AS}$ | - | - | 108 | mJ | $I_D$=-2.2 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | -<br>- | -<br>- | 5<br>1.8 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{thJA}$=70 °C/W[2] |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 150 | °C | IEC climatic category; DIN IEC 68-1: 55/150/56 |

# 2 Thermal characteristics

## Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 25 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm² cooling area | $R_{thJA}$ | - | - | 70 | °C/W | - |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | -100 | - | - | V | $V_{GS}$=0 V, $I_D$=-1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | -1.0 | -1.5 | -2.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=-1037 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | -0.1<br>-10 | -1.0<br>-100 | µA | $V_{DS}$=-100 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=-100 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | -10 | -100 | nA | $V_{GS}$=-20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | -<br>- | 132.8<br>140.5 | 160<br>190 | mΩ | $V_{GS}$=-10 V, $I_D$=-2.2 A<br>$V_{GS}$=-4.5 V, $I_D$=-1.8 A |
| Gate resistance | $R_G$ | - | 5.0 | - | Ω | - |
| Transconductance | $g_{fs}$ | - | 9.4 | - | S | $\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, $I_D$=-2.2 A |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance[1)] | $C_{iss}$ | - | 1600 | 2100 | pF | $V_{GS}$=0 V, $V_{DS}$=-50 V, $f$=1 MHz |
| Output capacitance[1)] | $C_{oss}$ | - | 110 | 140 | pF | $V_{GS}$=0 V, $V_{DS}$=-50 V, $f$=1 MHz |
| Reverse transfer capacitance[1)] | $C_{rss}$ | - | 25 | 44 | pF | $V_{GS}$=0 V, $V_{DS}$=-50 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 18.528 | - | ns | $V_{DD}$=-50 V, $V_{GS}$=-10 V, $I_D$=-2.2 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 13.422 | - | ns | $V_{DD}$=-50 V, $V_{GS}$=-10 V, $I_D$=-2.2 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 74.078 | - | ns | $V_{DD}$=-50 V, $V_{GS}$=-10 V, $I_D$=-2.2 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 16.646 | - | ns | $V_{DD}$=-50 V, $V_{GS}$=-10 V, $I_D$=-2.2 A, $R_{G,ext}$=1.6 Ω |

[1)] Defined by design. Not subject to production test.

## Table 6 Gate charge characteristics[1)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | -4.1 | - | nC | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -4.5 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | -2.4 | - | nC | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -4.5 V |
| Gate to drain charge[2)] | $Q_{gd}$ | - | -9.6 | -14.4 | nC | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -4.5 V |
| Switching charge | $Q_{sw}$ | - | -11.2 | - | nC | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -4.5 V |
| Gate charge total[2)] | $Q_g$ | - | -21 | -26 | nC | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -4.5 V |
| Gate plateau voltage | $V_{plateau}$ | - | -2.5 | - | V | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -4.5 V |
| Gate charge total | $Q_g$ | - | -42 | - | nC | $V_{DD}$=-50 V, $I_D$=-2.2 A, $V_{GS}$=0 to -10 V |
| Output charge[2)] | $Q_{oss}$ | - | -13 | -17 | nC | $V_{DS}$=-50 V, $V_{GS}$=0 V |

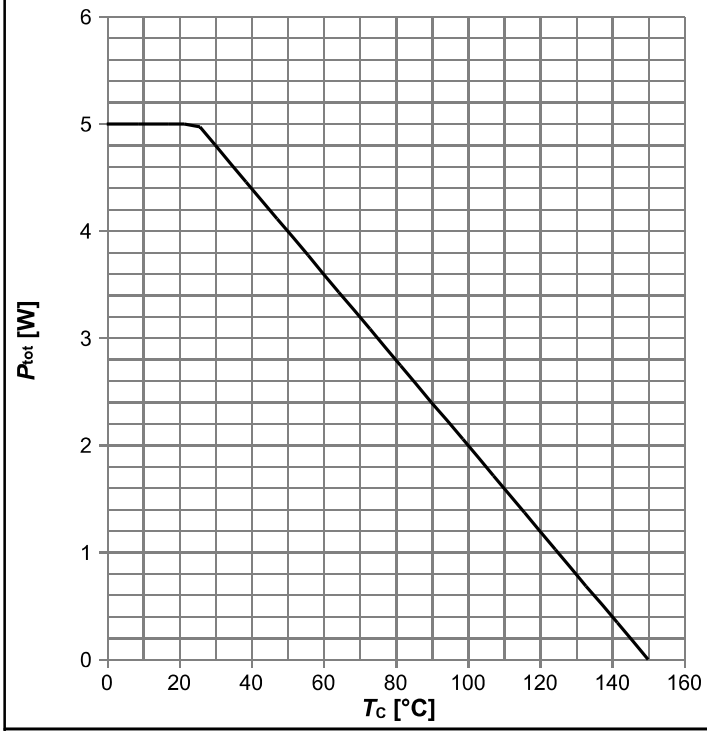
## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | -3.9 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | -15.6 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | -0.78 | -1.2 | V | $V_{GS}$=0 V, $I_F$=-2.2 A, $T_j$=25 °C |
| Reverse recovery time[2)] | $t_{rr}$ | - | 105.02 | 210.04 | ns | $V_R$=-50 V, $I_F$=-2.2 A, $di_F/dt$=-100 A/µs |
| Reverse recovery charge[2)] | $Q_{rr}$ | - | 44.374 | 88.748 | nC | $V_R$=-50 V, $I_F$=-2.2 A, $di_F/dt$=-100 A/µs |

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test.

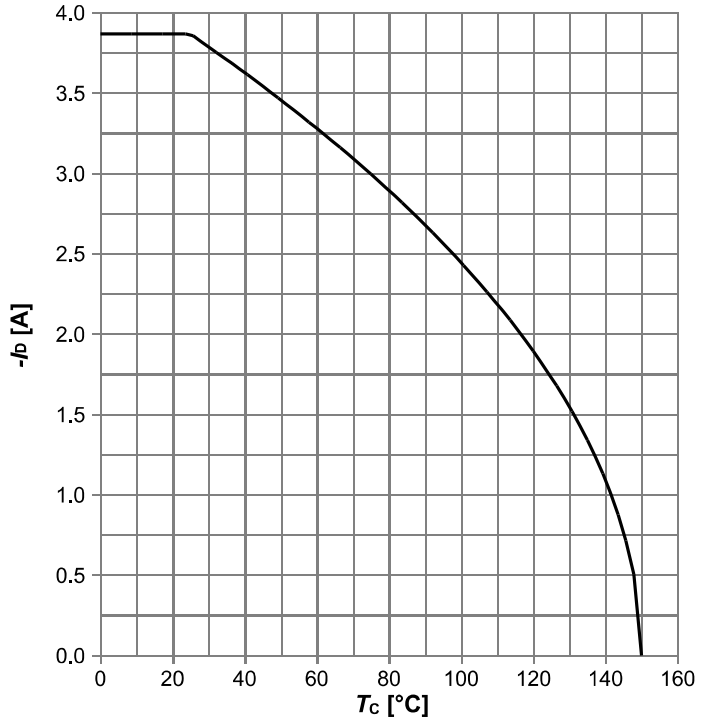
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



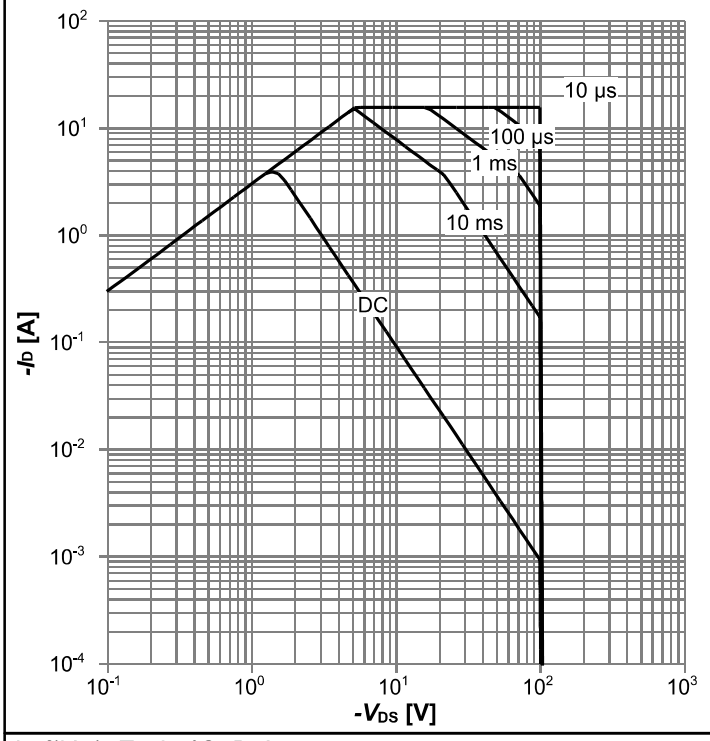

$P_{tot}=f(T_C)$

**Diagram 2: Drain current**



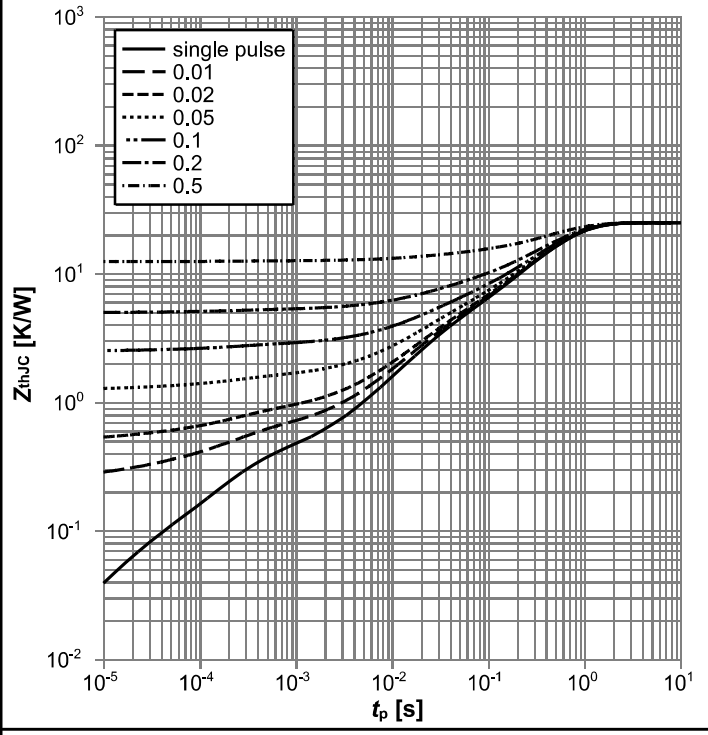

$I_D=f(T_C)$; $|V_{GS}|\geq 10$ V

**Diagram 3: Safe operating area**



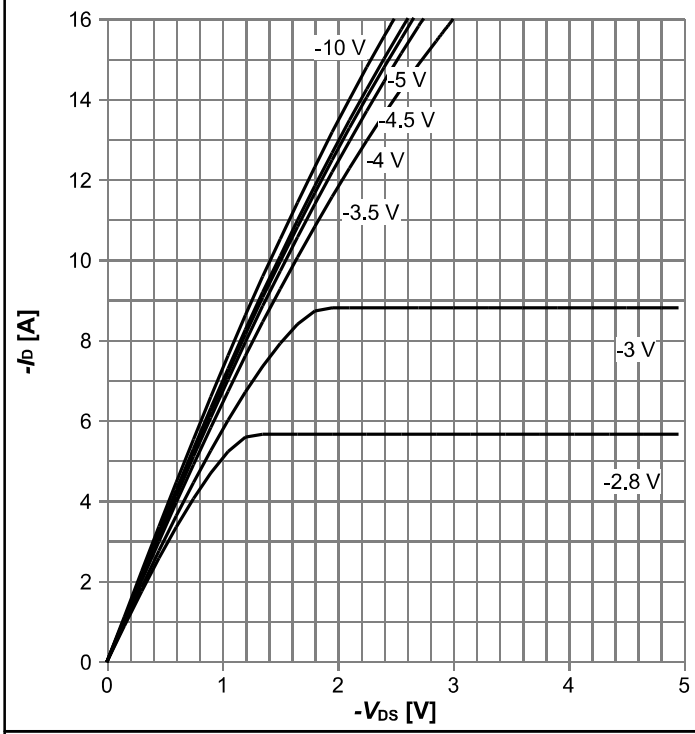

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



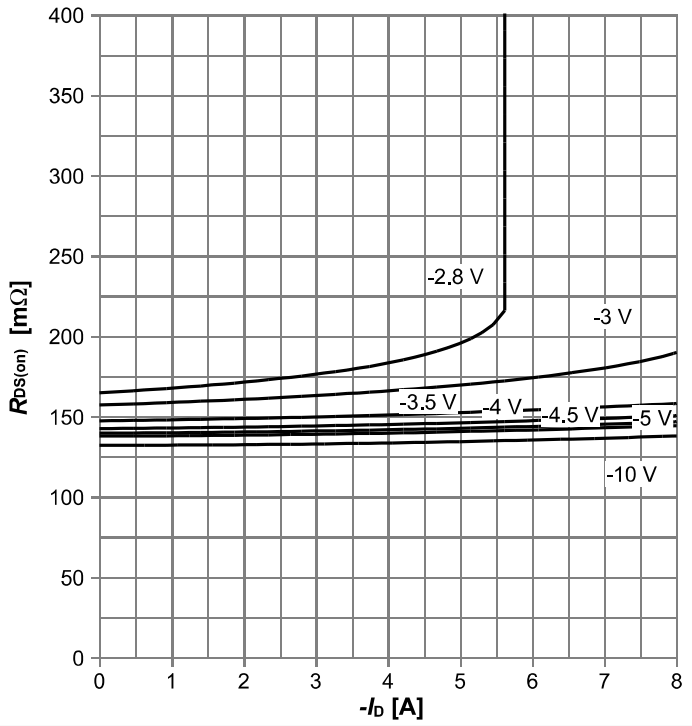

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

**Diagram 5: Typ. output characteristics**



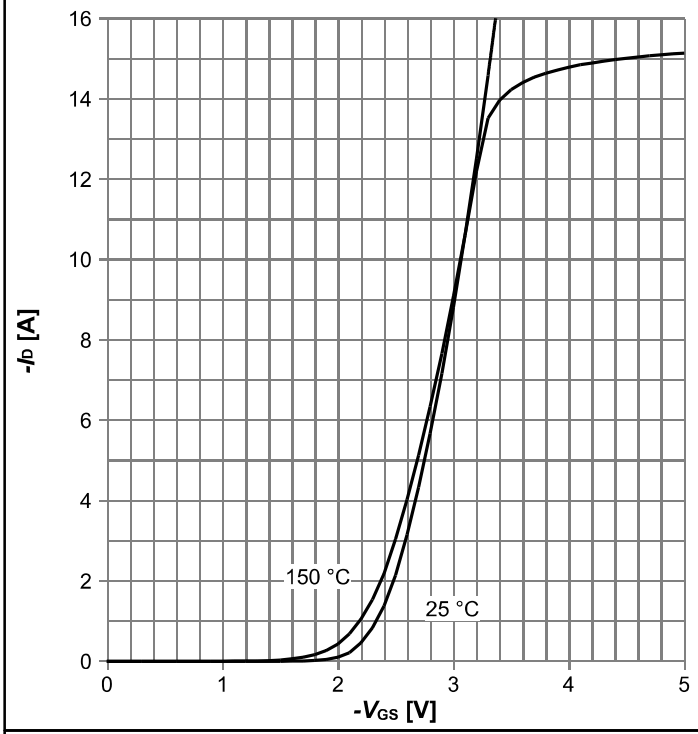

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



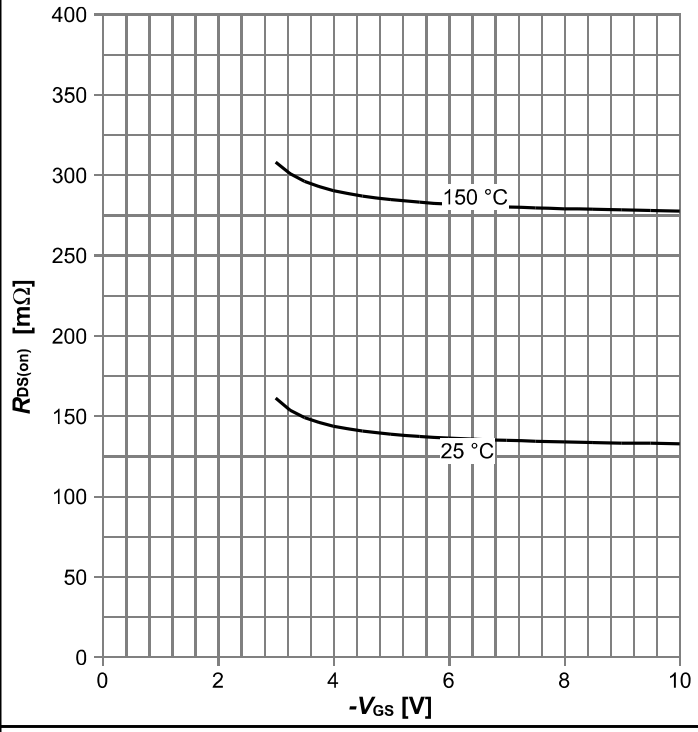

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



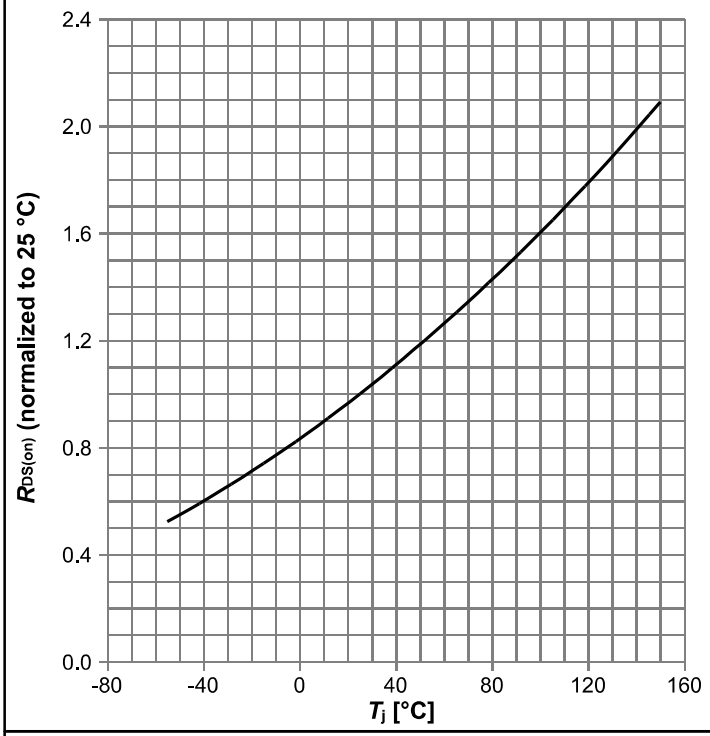

$I_D$=f($V_{GS}$), |$V_{DS}$|>2|$I_D$|$R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**



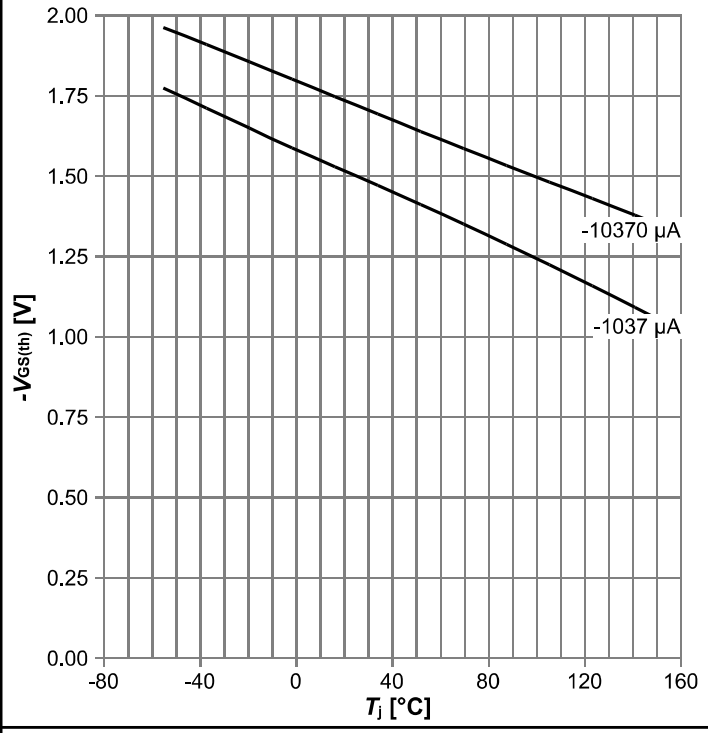

$R_{DS(on)}$=f($V_{GS}$), $I_D$=-2.2 A; parameter: $T_j$

**Diagram 9: Normalized drain-source on resistance**



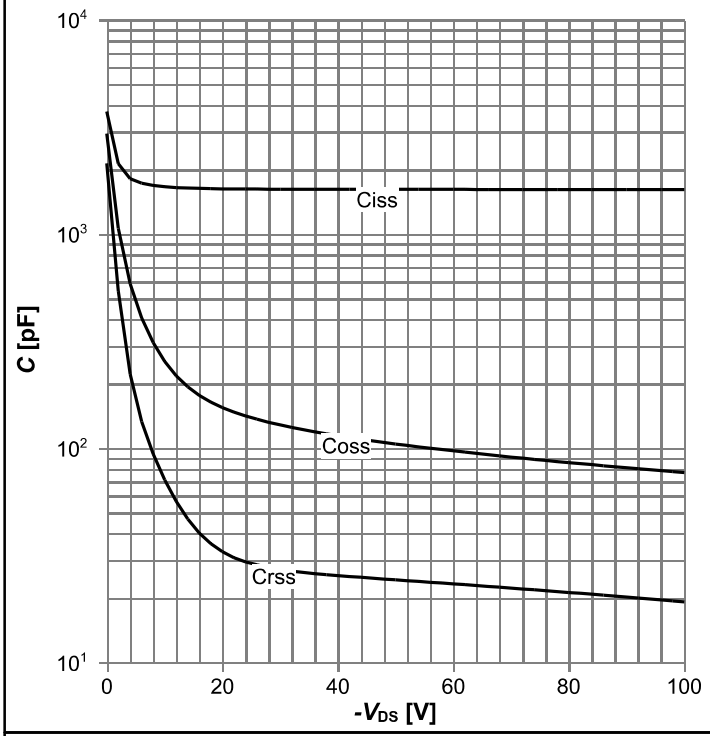

$R_{DS(on)}$=f($T_j$), $I_D$=-2.2 A, $V_{GS}$=-10 V

**Diagram 10: Typ. gate threshold voltage**



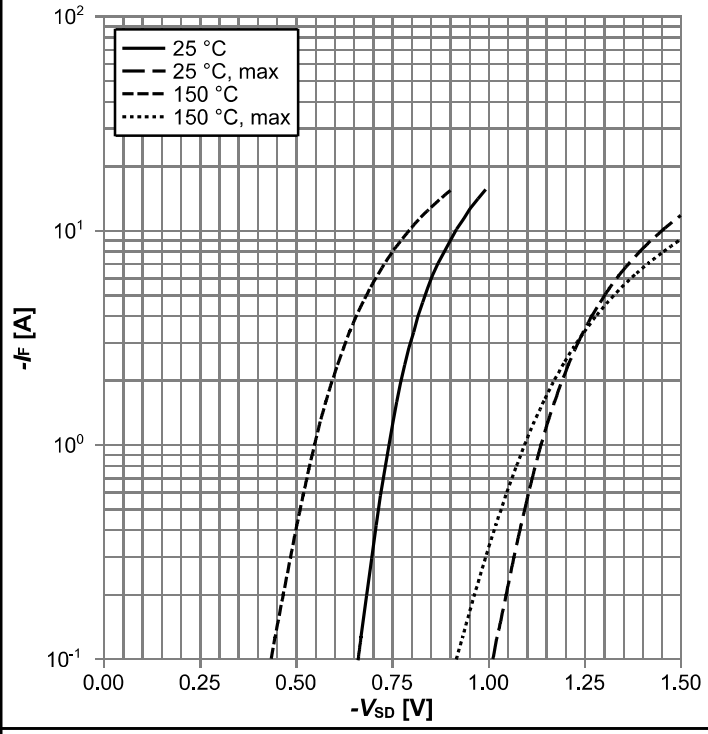

$V_{GS(th)}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**



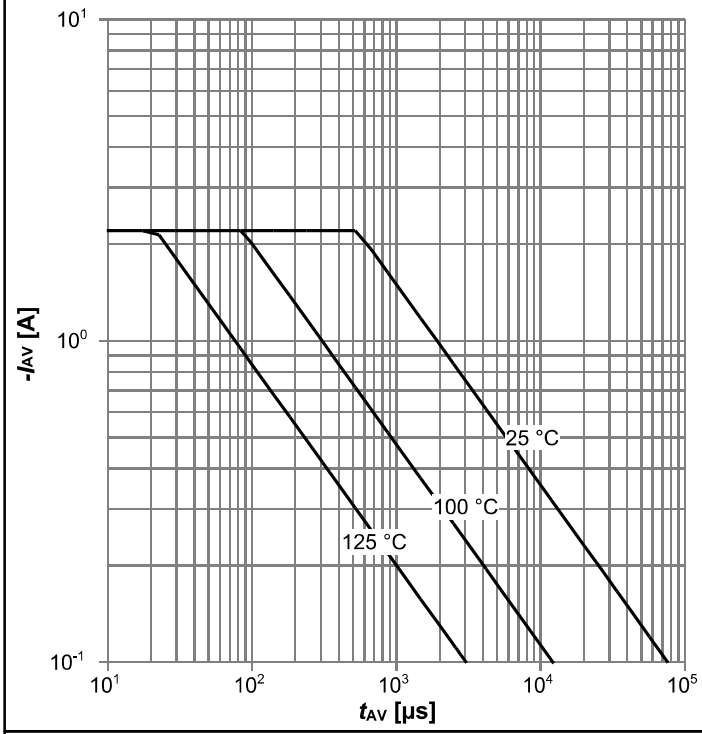

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**



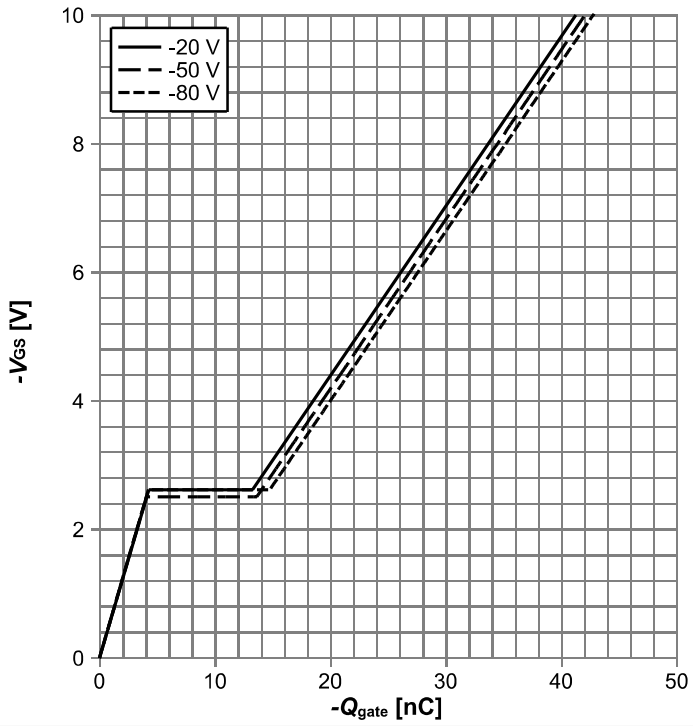

$I_F$=f($V_{SD}$); parameter: $T_j$

**Diagram 13: Avalanche characteristics**



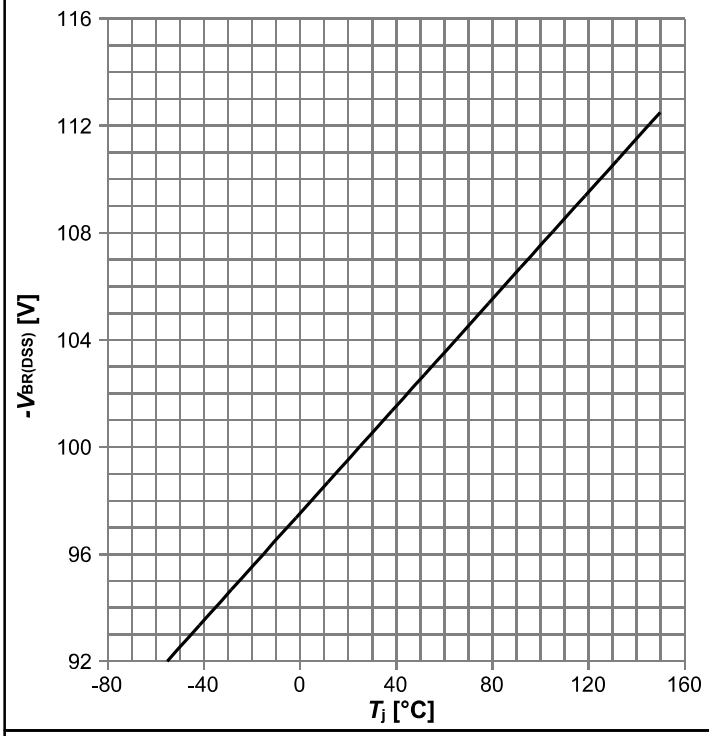

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$

**Diagram 14: Typ. gate charge**



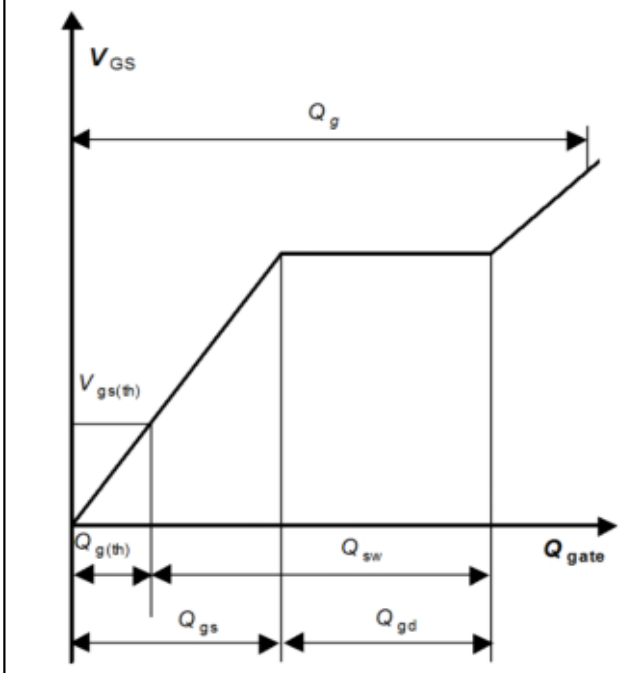

$V_{GS}$=f($Q_{gate}$), $I_D$=-2.2 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

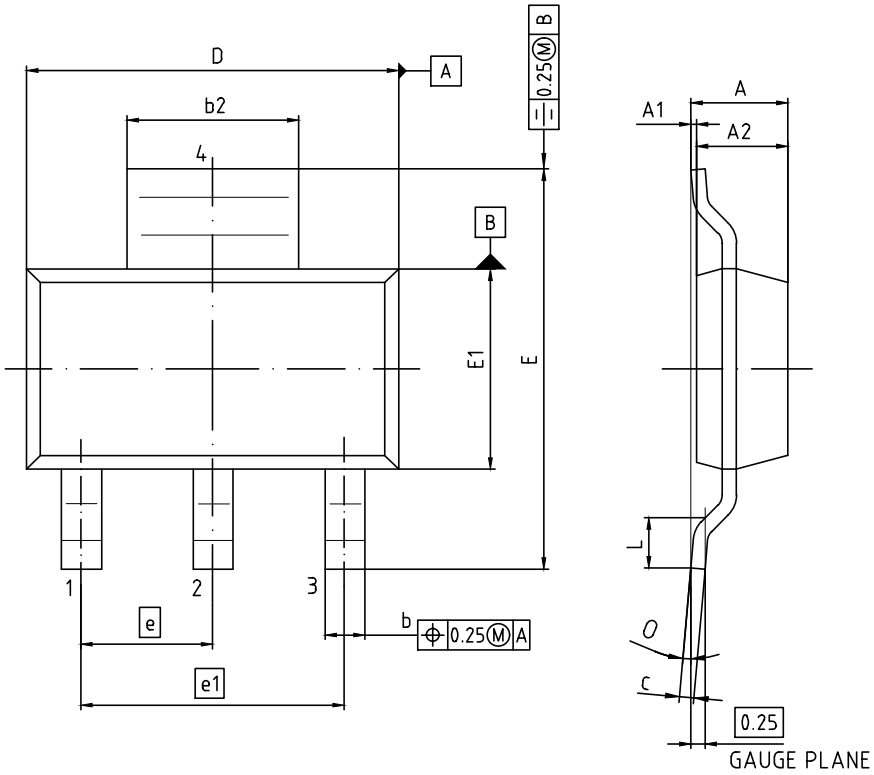



$V_{BR(DSS)}$=f($T_j$); $I_D$=-1 mA

**Diagram Gate charge waveforms**



# 5 Package Outlines




| DIMENSION | MILLIMETERS | |
|---|---|---|
| | MIN. | MAX. |
| A | 1.60 | 1.80 |
| A1 | - | 0.10 |
| A2 | 1.50 | 1.70 |
| b | 0.60 | 0.80 |
| b2 | 2.90 | 3.10 |
| c | 0.24 | 0.32 |
| D | 6.30 | 6.70 |
| E | 6.70 | 7.30 |
| E1 | 3.30 | 3.70 |
| e | 2.30 | |
| e1 | 4.60 | |
| L | 0.75 | - |
| O | 0° | 10° |

| |
|---|
| DOCUMENT NO.<br>Z8B00188348 |
| REVISION<br>01 |
| SCALE 10:1<br>0 1 2mm |
| EUROPEAN PROJECTION |
| ISSUE DATE<br>28.02.2018 |

**Figure 1 Outline PG-SOT223-4, dimensions in mm**

## Revision History

ISP16DP10LM

**Revision: 2021-05-10, Rev. 2.0**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.0 | 2021-05-10 | Release of final version |

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