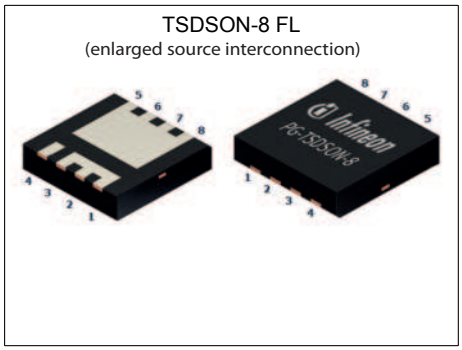
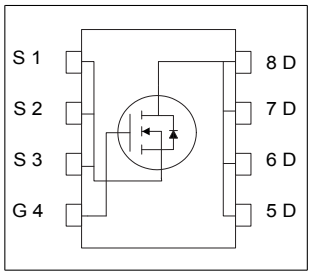
MOSFET

OptiMOS™ Power-MOSFET, 30 V



Features

- Optimized for high performance Buck converter (Server,VGA)
- Very Low FOM_{QOSS} for High Frequency SMPS
- Low FOM_{SW} for High Frequency SMPS
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	1.9	mΩ
I_D	40	A
Q_{OSS}	25	nC
Q_G(0V..10V)	44	nC

Type / Ordering Code	Package	Marking	Related Links
ISZ019N03L5S	PG-TSDSON-8 FL	19N03L5	-

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1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - - - -	- - - - -	40 40 40 40 22	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 K/W
Pulsed drain current[1]	$I_{D,pulse}$	-	-	160	A	T_C=25 °C
Avalanche current, single pulse[2]	I_{AS}	-	-	20	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	150	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.8	K/W	-
Device on PCB, 6 cm^2 cooling area[3]	R_{thJA}	-	-	60	K/W	-

[1] See figure 3 for more detailed information
[2] See figure 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.0 1.6	2.5 1.9	mΩ	V_{GS}=4.5 V, I_D=20 A V_{GS}=10 V, I_D=20 A
Gate resistance	R_G	-	0.8	-	Ω	-
Transconductance	g_{fs}	70	140	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2800	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance	C_{oss}	-	960	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	140	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5.4	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	6.8	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	28	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	4.6	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7.0	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	4.6	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	6.5	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	9.0	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	22	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	44	-	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	18	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	25	-	nC	V_{DD}=15 V, V_{GS}=0 V

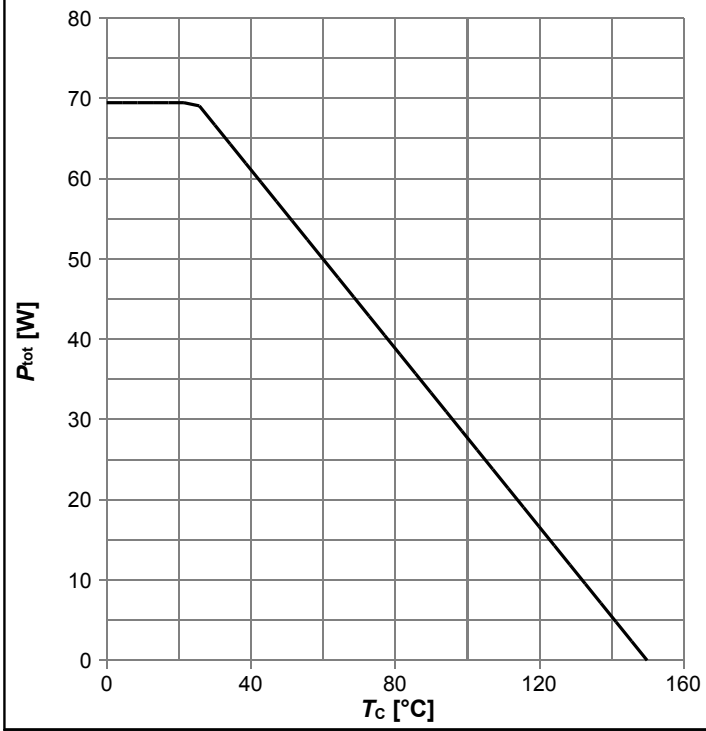
[1)] See ″Gate charge waveforms″ for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	40	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	160	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.8	1	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	20	-	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

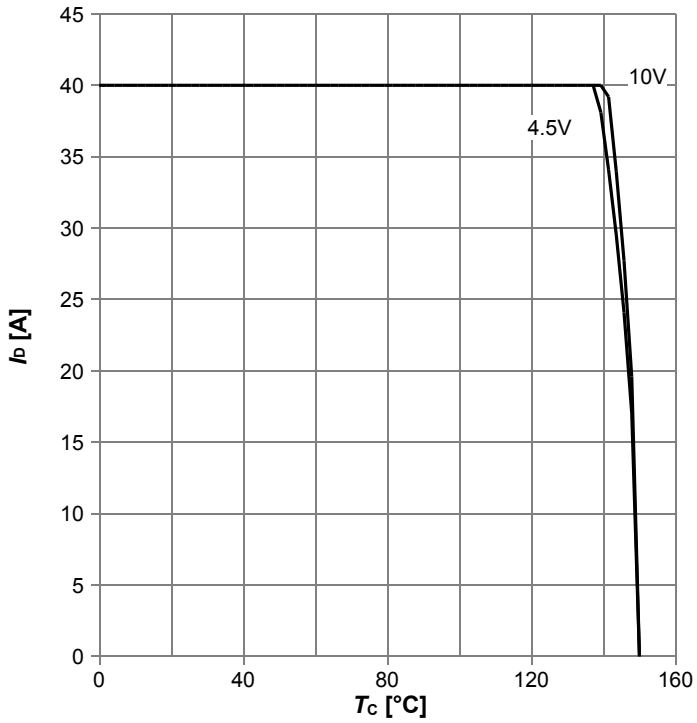
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



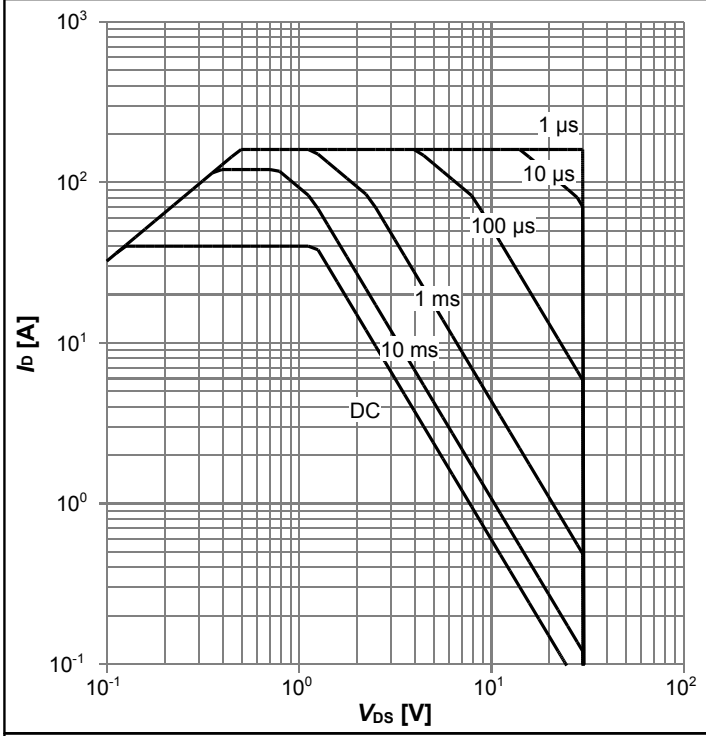
$P_{tot}=f(T_C)$

Diagram 2: Drain current



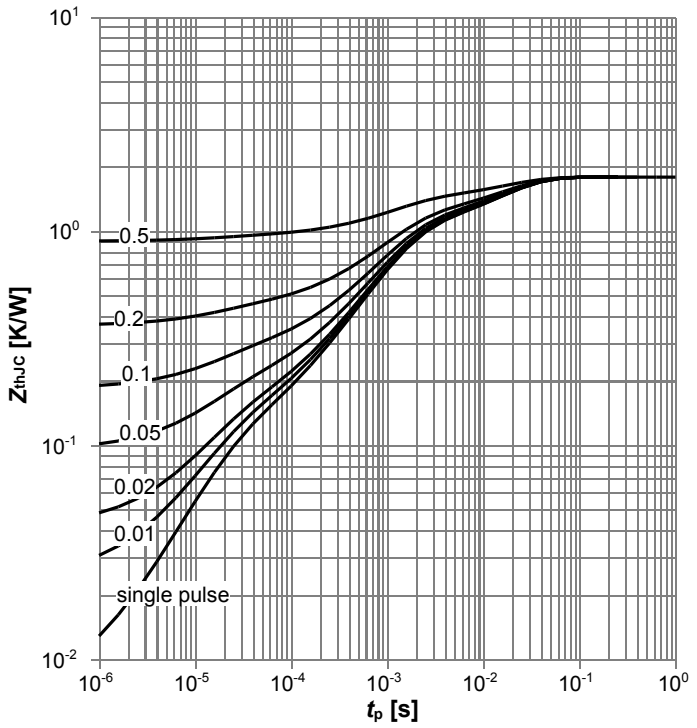
$I_D=f(T_C)$; parameter: V_{GS}

Diagram 3: Safe operating area



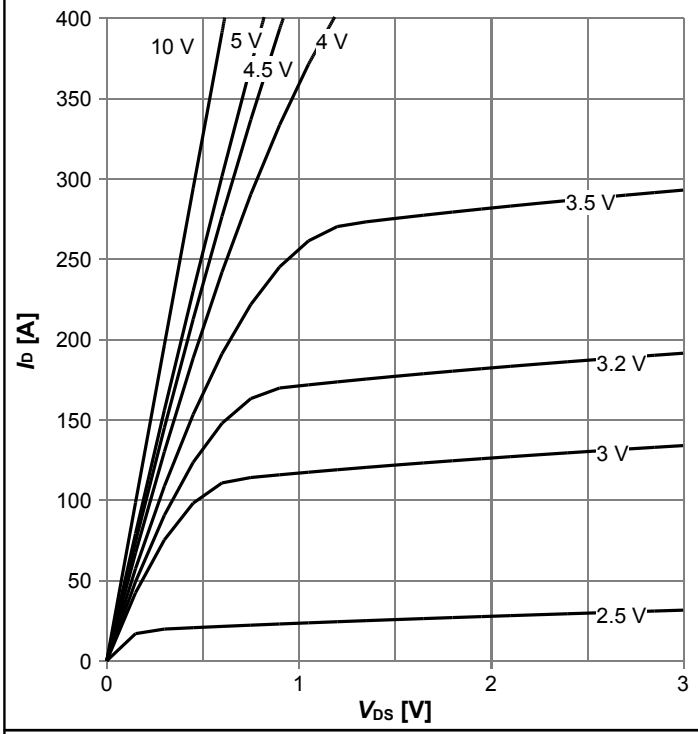
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



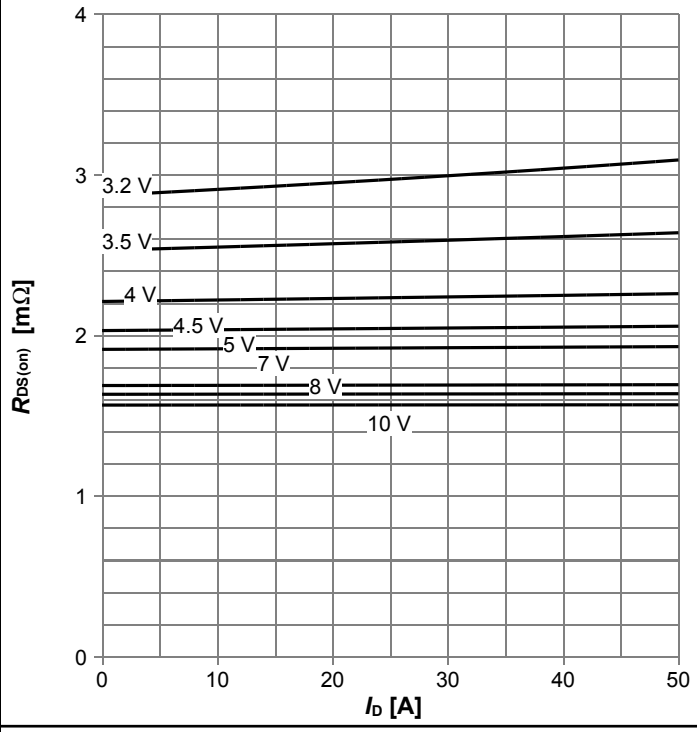
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



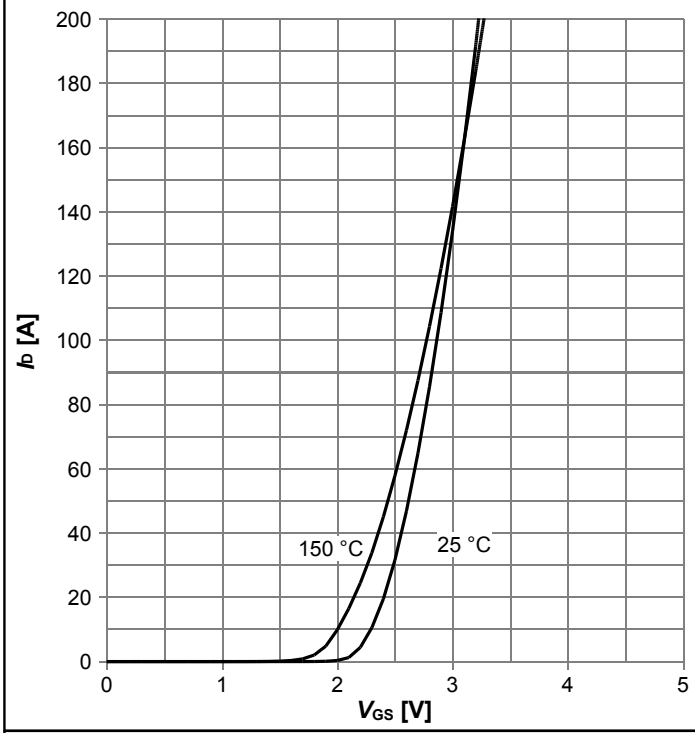
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



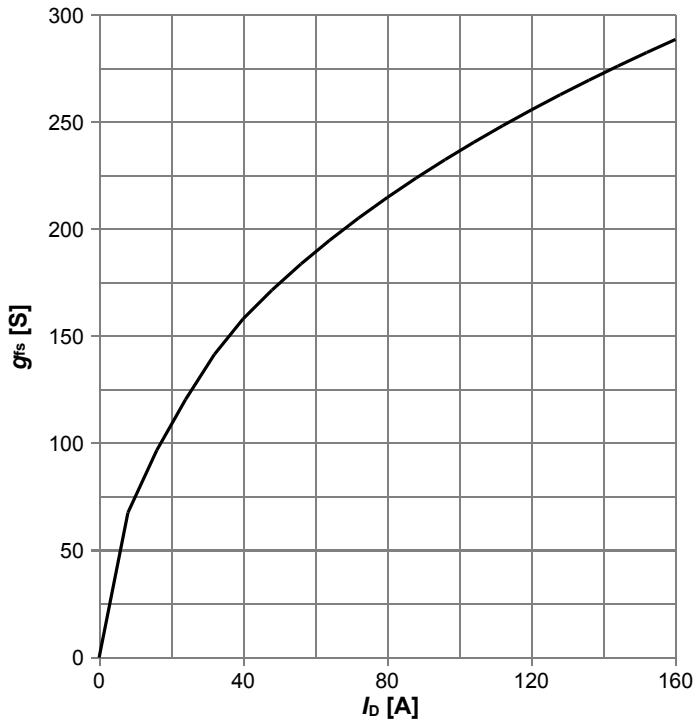
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



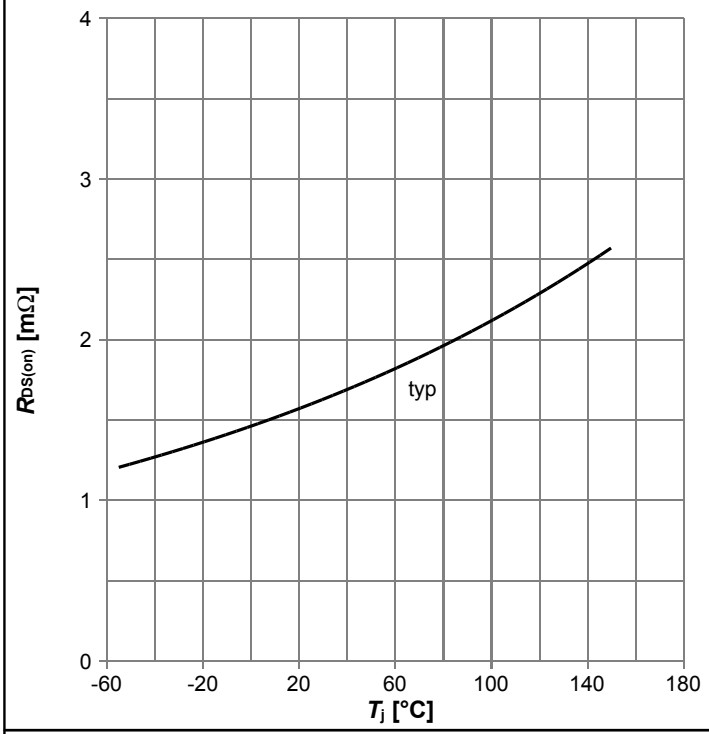
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



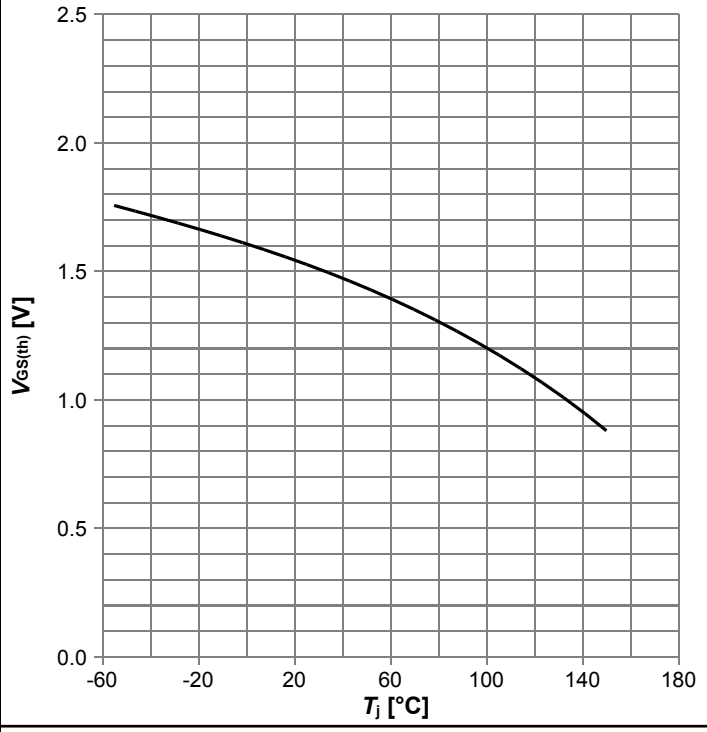
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



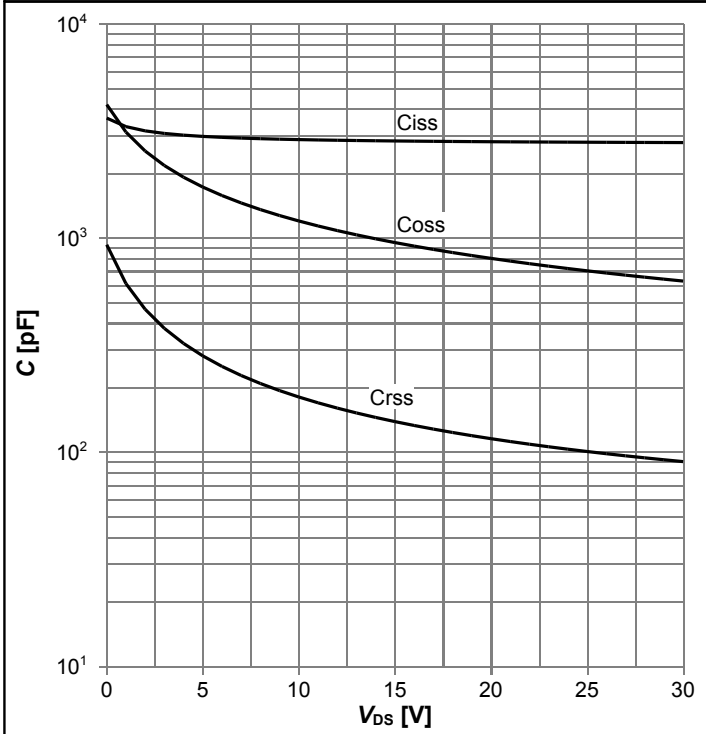
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



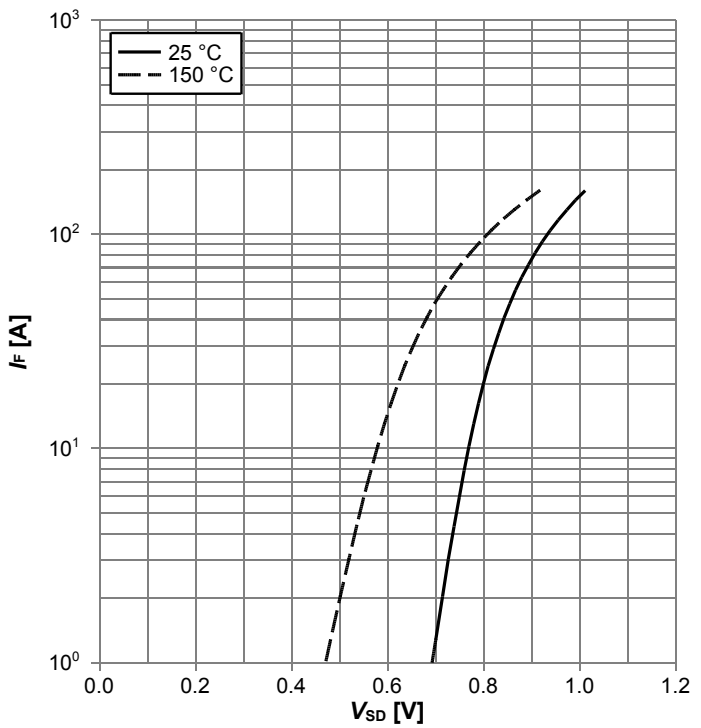
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances



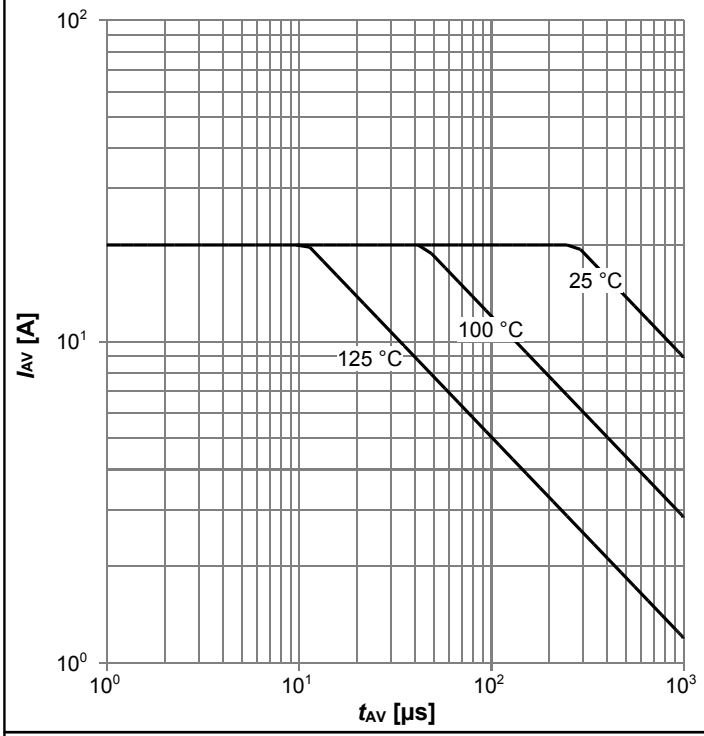
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



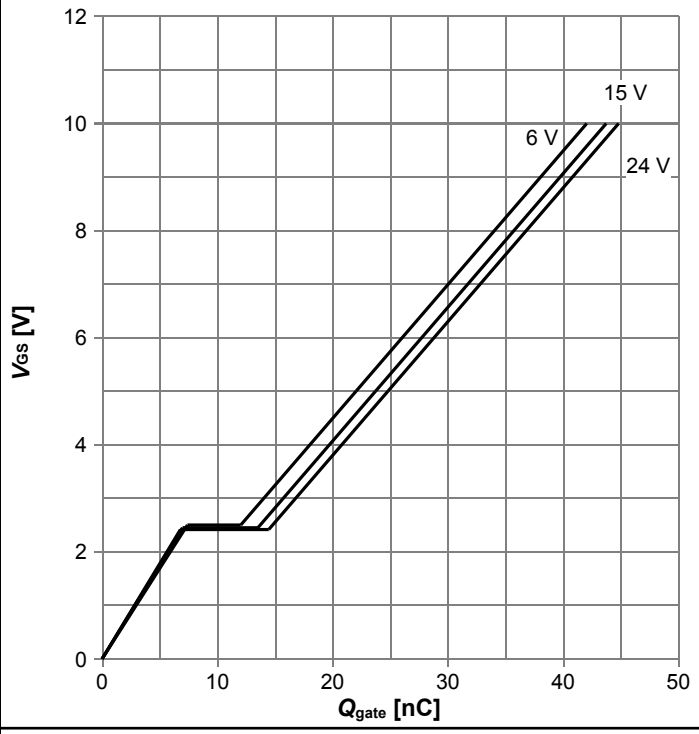
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



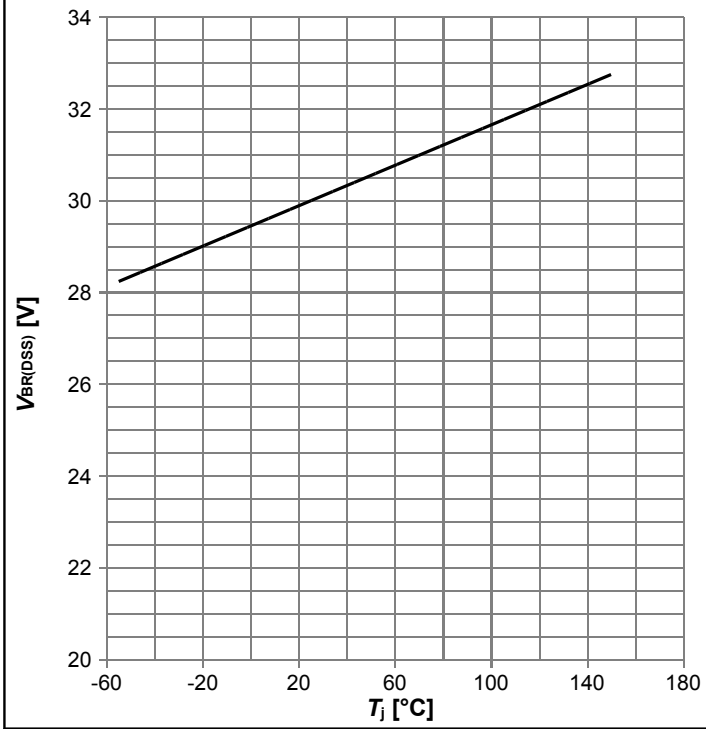
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



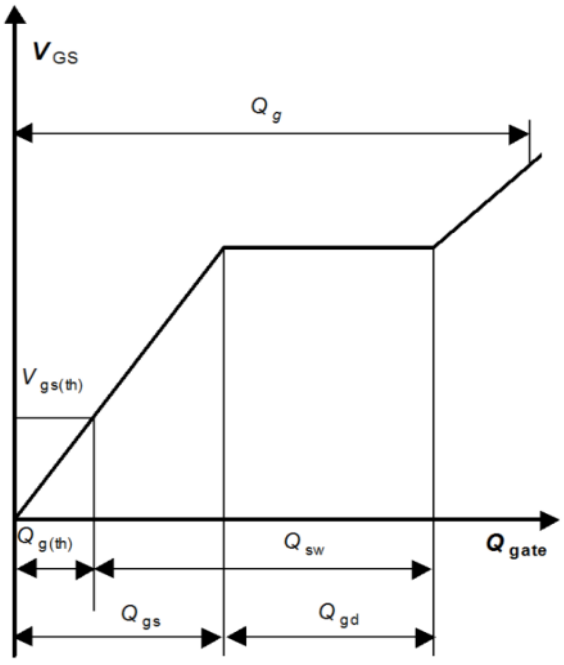
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

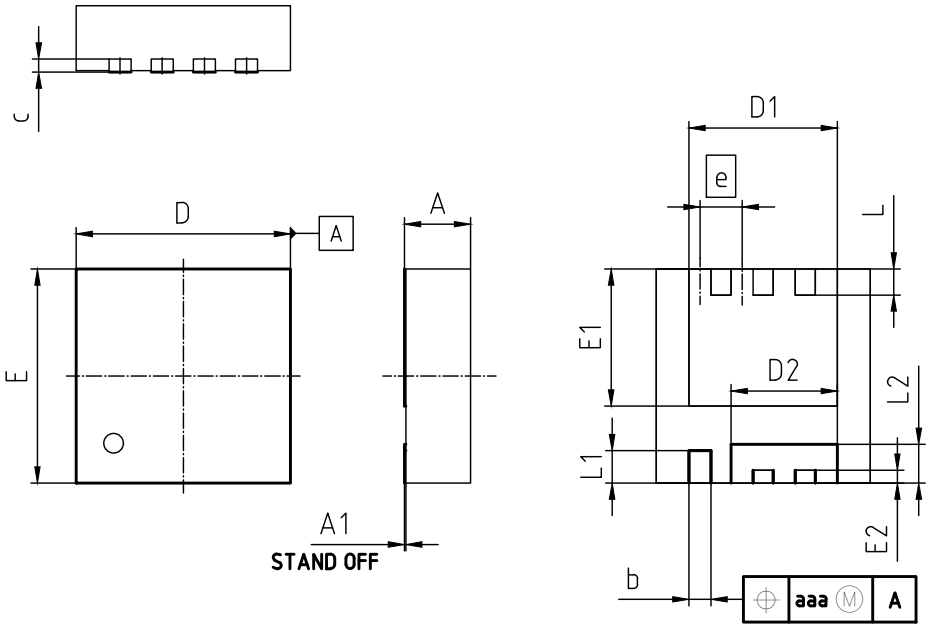


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0	0.05
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.70
L2	0.50	0.70
aaa	0.06	

DOCUMENT NO.	Z8B00158553
REVISION	03
SCALE	10:1 0 1 2 mm
EUROPEAN PROJECTION	
ISSUE DATE	04.03.2020

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm/inches

Revision History

ISZ019N03L5S

Revision: 2020-03-16, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2020-03-16	Release of final version

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