HyperRAM (Self-Refresh DRAM)

3.0 V/1.8 V, 64-Mbit, Automotive-E (Grade 1)

Features

Interface

- HyperBus Interface
- 1.8 V / 3.0 V interface support
  - Single-ended clock (CK) - 11 bus signals
  - Optional differential clock (CK, CK#) - 12 bus signals
- Chip Select (CS#)
- 8-bit data bus (DQ[7:0])
- Hardware reset (RESET#)
- Bidirectional Read-Write Data Strobe (RWDS)
  - Output at the start of all transactions to indicate refresh latency
  - Output during read transactions as Read Data Strobe
  - Input during write transactions as Write Data Mask
- Optional DDR Center-Aligned Read Strobe (DCARS)
  - During read transactions RWDS is offset by a second clock, phase shifted from CK
  - The Phase Shifted Clock is used to move the RWDS transition edge within the read data eye

Performance, Power, and Packages

- 200 MHz maximum clock rate
- DDR - transfers data on both edges of the clock
- Data throughput up to 400 MBps (3,200 Mbps)
- Configurable Burst Characteristics
  - Linear burst
  - Wrapped burst lengths:
    - 16 bytes (eight clocks)
    - 32 bytes (16 clocks)
    - 64 bytes (32 clocks)
    - 128 bytes (64 clocks)
  - Hybrid option - one wrapped burst followed by linear burst
- Configurable output drive strength
- Power Modes
  - Hybrid Sleep Mode
  - Deep Power Down
- Array Refresh
  - Partial Memory Array(1/8, 1/4, 1/2, and so on)
  - Full
- Package
  - 24-ball FBGA

- Operating Temperature Range
  - Automotive, AEC-Q100 Grade 1: –40 °C to +125 °C

Technology

- 38-nm DRAM

Performance Summary

Read Transaction Timings	Unit
Maximum Clock Rate at 1.8 V $V_{CC}/V_{CC}Q$	200 MHz
Maximum Clock Rate at 3.0 V $V_{CC}/V_{CC}Q$	200 MHz
Maximum Access Time (t_{ACC})	35 ns

Maximum Current Consumption	Unit
Burst Read or Write (linear burst at 200 MHz, 1.8 V)	30 mA
Burst Read or Write (linear burst at 200 MHz, 3.0 V)	36 mA

Logic Block Diagram

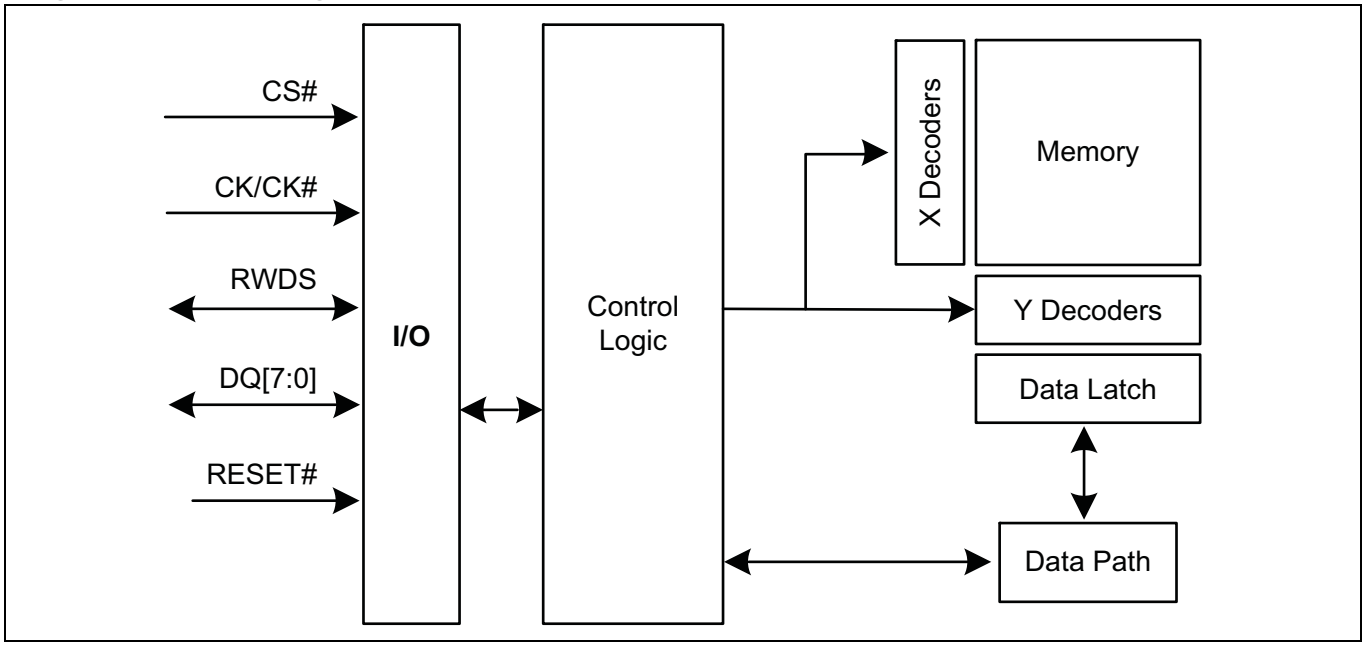


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1 General Description

The Cypress 64-Mb HyperRAM™ device is a high-speed CMOS, self-refresh DRAM, with HyperBus interface. The DRAM array uses dynamic cells that require periodic refresh. Refresh control logic within the device manages the refresh operations on the DRAM array when the memory is not being actively read or written by the HyperBus interface master (host). Since the host is not required to manage any refresh operations, the DRAM array appears to the host as though the memory uses static cells that retain data without refresh. Hence, the memory is more accurately described as Pseudo Static RAM (PSRAM).

Since the DRAM cells cannot be refreshed during a read or write transaction, there is a requirement that the host limit read or write burst transfers lengths to allow internal logic refresh operations when they are needed. The host must confine the duration of transactions and allow additional initial access latency, at the beginning of a new transaction, if the memory indicates a refresh operation is needed.

1.1 HyperBus Interface

HyperBus is a low signal count, DDR interface, that achieves high-speed read and write throughput. The DDR protocol transfers two data bytes per clock cycle on the DQ[7:0] input/output signals. A read or write transaction on HyperBus consists of a series of 16-bit wide, one clock cycle data transfers at the internal HyperRAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible. Device are available as 1.8 V V_{CC}/(V_{CC}Q or 3.0 V V_{CC}/V_{CCQ} (nominal) for array (V_{CC}) and I/O buffer (V_{CCQ}) supplies, through different Ordering Part Numbers (OPN).

Command, address, and data information is transferred over the eight HyperBus DQ[7:0] signals. The clock (CK#, CK) is used for information capture by a HyperBus slave device when receiving command, address, or data on the DQ signals. Command or Address values are center-aligned with clock transitions.

Every transaction begins with the assertion of CS# and Command-Address (CA) signals, followed by the start of clock transitions to transfer six CA bytes, followed by initial access latency and either read or write data transfers, until CS# is deasserted.

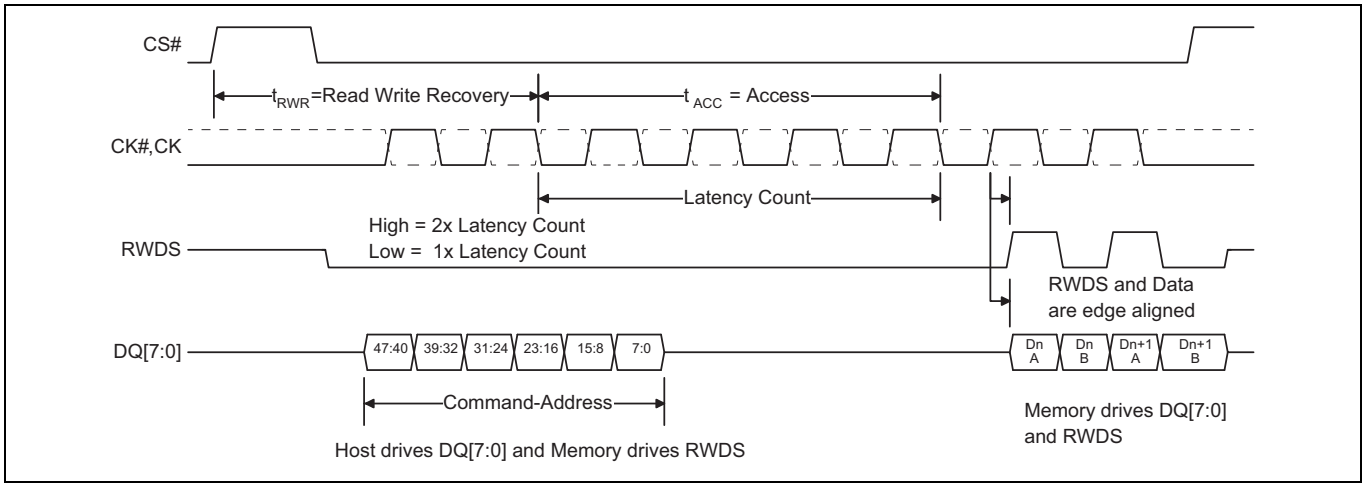


Figure 1-1 Read Transaction, Single Initial Latency Count

The RWDS is a bidirectional signal that indicates:

- when data will start to transfer from a HyperRAM device to the master device in read transactions (initial read latency)
- when data is being transferred from a HyperRAM device to the master device during read transactions (as a source synchronous read data strobe)
- when data may start to transfer from the master device to a HyperRAM device in write transactions (initial write latency)
- data masking during write data transfers

During the CA transfer portion of a read or write transaction, RWDS acts as an output from a HyperRAM device to indicate whether additional initial access latency is needed in the transaction.

During read data transfers, RWDS is a read data strobe with data values edge-aligned with the transitions of RWDS.

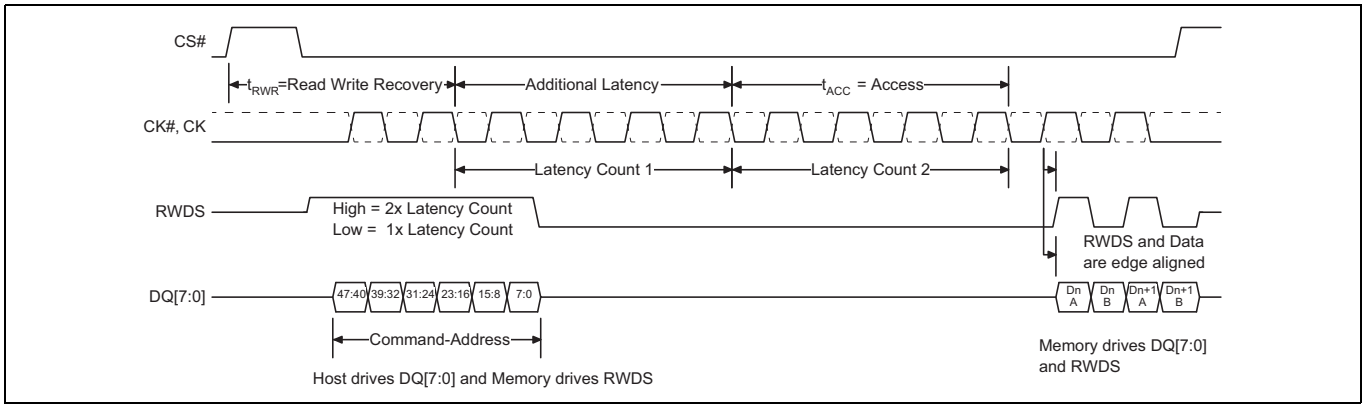


Figure 1-2 Read Transaction, Additional Latency Count

During write data transfers, RWDS indicates whether each data byte transfer is masked with RWDS HIGH (invalid and prevented from changing the byte location in a memory) or not masked with RWDS Low (valid and written to a memory). Data masking may be used by the host to byte align write data within a memory or to enable merging of multiple non-word aligned writes in a single burst write. During write transactions, data is center-aligned with clock transitions.

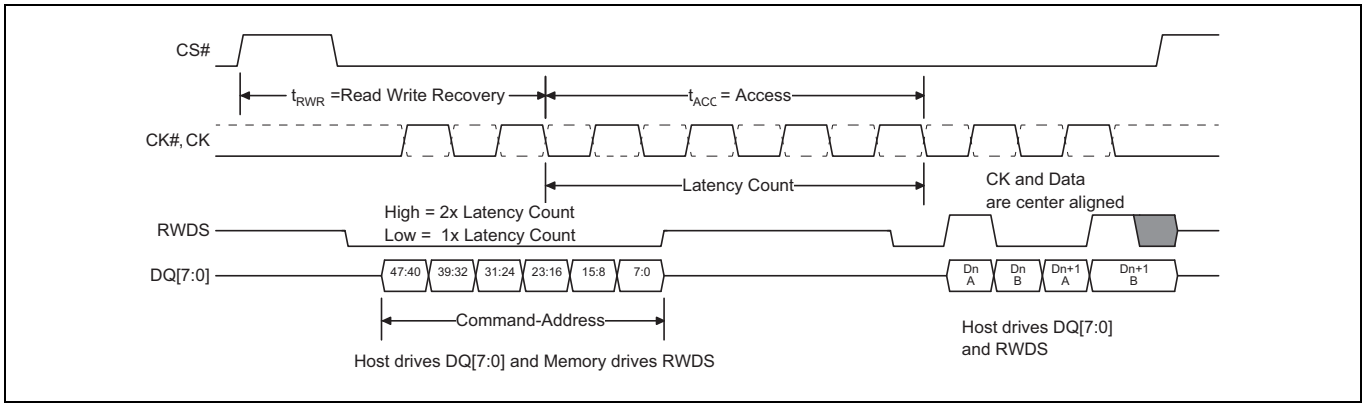


Figure 1-3 Write Transaction, Single Initial Latency Count

Read and write transactions are burst oriented, transferring the next sequential word during each clock cycle. Each individual read or write transaction can use either a wrapped or linear burst sequence.

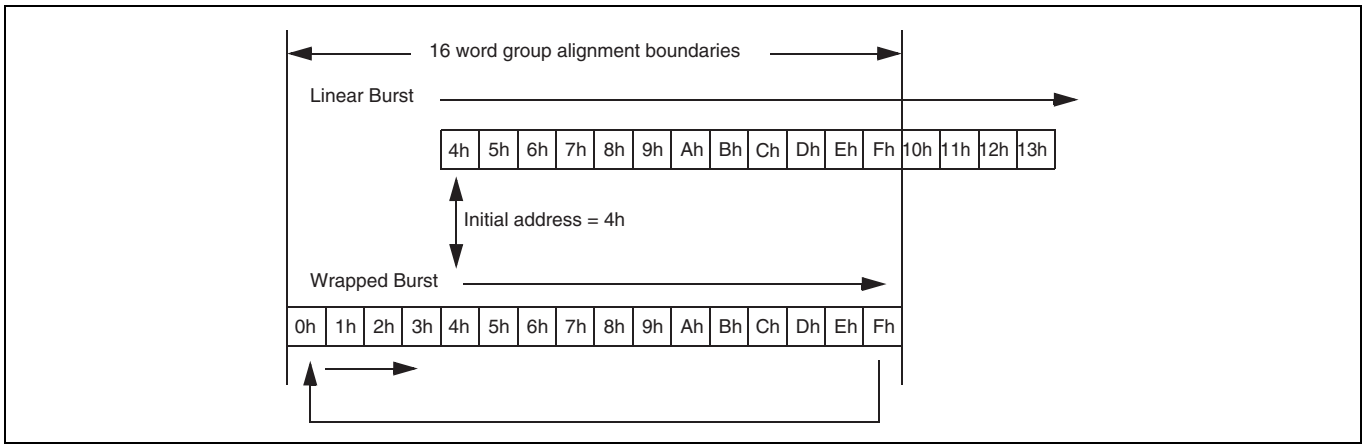


Figure 1-4 Linear Versus Wrapped Burst Sequence

During wrapped transactions, accesses start at a selected location and continue to the end of a configured word group aligned boundary, then wrap to the beginning location in the group, then continue back to the starting location. Wrapped bursts are generally used for critical word first cache line fill read transactions. During linear transactions, accesses start at a selected location and continue in a sequential manner until the transaction is terminated when CS# returns HIGH. Linear transactions are generally used for large contiguous data transfers such as graphic images. Since each transaction command selects the type of burst sequence for that transaction, wrapped and linear bursts transactions can be dynamically intermixed as needed.

2 Product Overview

The 64 Mb HyperRAM device is 1.8 V or 3.0 V array and I/O, synchronous self-refresh DRAM. The HyperRAM device provides a HyperBus slave interface to the host system. The HyperBus interface has an 8-bit (1 byte) wide DDR data bus and use only word-wide (16-bit data) address boundaries. Read transactions provide 16 bits of data during each clock cycle (8 bits on both clock edges). Write transactions take 16 bits of data from each clock cycle (8 bits on each clock edge).

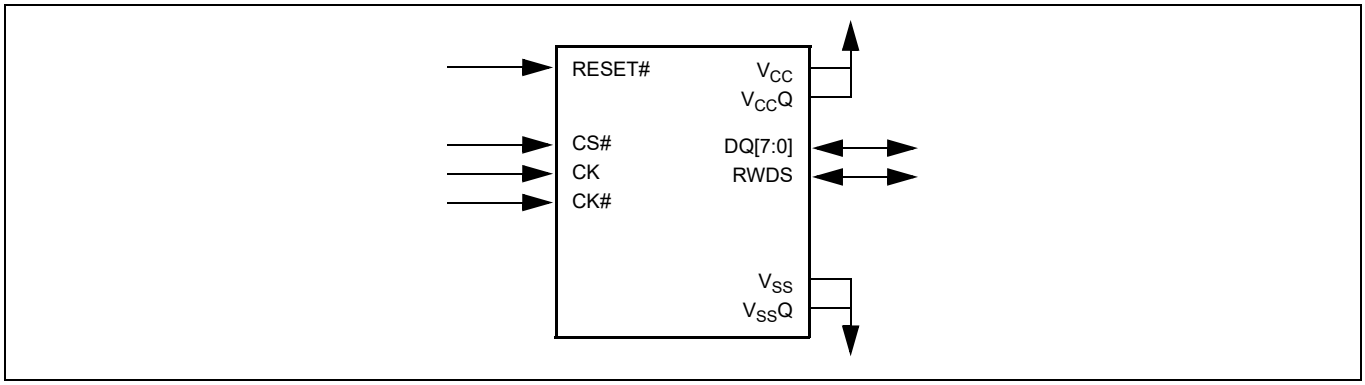


Figure 2-1 HyperRAM Interface[1]

2.1 HyperBus Interface

Read and write transactions require two clock cycles to define the target row address and burst type, then an initial access latency of t_{ACC}. During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time (t_{RFH}) is added to the initial latency; by driving the RWDS signal to the HIGH state. During the CA period, the third clock cycle will specify the target word address within the target row. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequence. When configured in linear burst mode, the device will automatically fetch the next sequential row from the memory array to support a continuous linear burst. Simultaneously accessing the next row in the array while the read or write data transfer is in progress, allows for a linear sequential burst operation that can provide a sustained data rate of 400 MBps [*1 byte (8 bit data bus) * 2 (data clock edges) * 200 MHz = 400 MBps]*.

Note
1. CK# is used in Differential Clock mode, but optional.

3 Signal Description

3.1 Input/Output Summary

HyperRAM signals are shown in **Table 3-1**. Active Low signal names have a hash symbol (#) suffix.

Table 3-1 I/O Summary[3]

Symbol	Type	Description
CS#	Master Output, Slave Input	Chip Select. Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a LOW to HIGH transition. The master device has a separate CS# for each slave.
CK, CK#[2]	Master Output, Slave Input	Differential Clock. Command, address, and data information is output with respect to the crossing of the CK and CK# signals. Use of differential clock is optional. Single Ended Clock. CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
DQ[7:0]	Input/Output	Data Input/Output. Command, Address, and Data information is transferred on these signals during Read and Write transactions.
RWDS	Input/Output	Read-Write Data Strobe. During the Command/Address portion of all bus transactions, RWDS is a slave output and indicates whether additional initial latency is required. Slave output during read data transfer, data is edge-aligned with RWDS. Slave input during data transfer in write transactions to function as a data mask. (HIGH = additional latency, LOW = no additional latency).
RESET#	Master Output, Slave Input, Internal Pull-up	Hardware RESET. When LOW, the slave device will self initialize and return to the STANDBY state. RWDS and DQ[7:0] are placed into the HIGH-Z state when RESET# is LOW. The slave RESET# input includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the HIGH state.
V_{CC}	Power Supply	Array Power.
$V_{CC}Q$	Power Supply	Input/Output Power.
V_{SS}	Power Supply	Array Ground.
$V_{SS}Q$	Power Supply	Input/Output Ground.
RFU	No Connect	Reserved for Future Use. May or may not be connected internally, the signal/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The signal/ball may be used by a signal in the future.

Notes
2. CK# is used in Differential Clock mode, but optional connection. Tie the CK# input pin to either VccQ or VssQ if not connected to the host controller, but do not leave it floating.
3. Optional Center-Aligned Read Strobe (DCARS) pinout and pin description are outlined in section **DDR Center-Aligned Read Strobe (DCARS) Functionality on page 46**.

4 HyperBus Transaction Details

4.1 Command/Address Bit Assignments

All HyperRAM bus transactions can be classified as either read or write. A bus transaction is started with CS# going LOW with clock in idle state (CK = LOW and CK# = HIGH). The first three clock cycles transfer three words of Command/Address (CA0, CA1, CA2) information to define the transaction characteristics. The Command/Address words are presented with DDR timing, using the first six clock edges.

The following characteristics are defined by the Command/Address information:

- Read or Write transaction
- Address Space: memory array space or register space
  - Register space is used to access Device Identification (ID) registers and Configuration Registers (CR) that identify the device characteristics and determine the slave specific behavior of read and write transfers on the HyperBus interface.
- Whether a transaction will use a linear or wrapped burst sequence.
- The target row (and half-page) address (upper order address)
- The target column (word within half-page) address (lower order address)

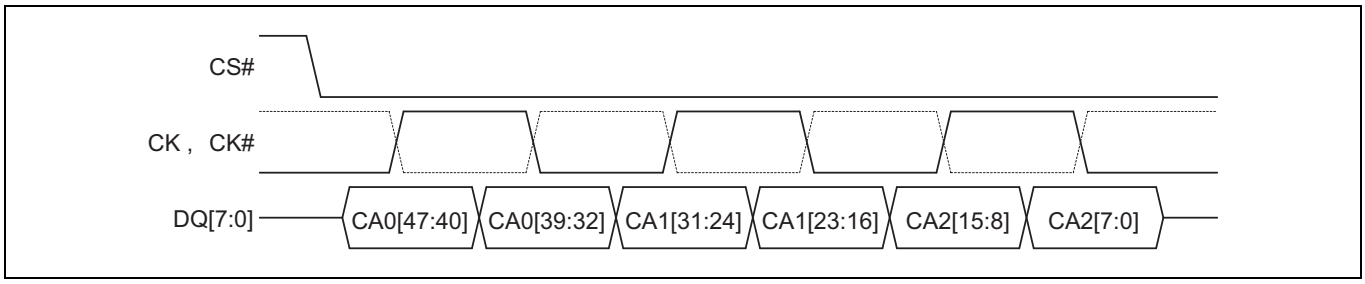


Figure 4-1 Command-Address (CA) Sequence[4, 5, 6, 7]

Table 4-1 CA Bit Assignment to DQ Signals

Signal	CA0[47:40]	CA0[39:32]	CA1[31:24]	CA1[23:16]	CA2[15:8]	CA2[7:0]
DQ[7]	CA[47]	CA[39]	CA[31]	CA[23]	CA[15]	CA[7]
DQ[6]	CA[46]	CA[38]	CA[30]	CA[22]	CA[14]	CA[6]
DQ[5]	CA[45]	CA[37]	CA[29]	CA[21]	CA[13]	CA[5]
DQ[4]	CA[44]	CA[36]	CA[28]	CA[20]	CA[12]	CA[4]
DQ[3]	CA[43]	CA[35]	CA[27]	CA[19]	CA[11]	CA[3]
DQ[2]	CA[42]	CA[34]	CA[26]	CA[18]	CA[10]	CA[2]
DQ[1]	CA[41]	CA[33]	CA[25]	CA[17]	CA[9]	CA[1]
DQ[0]	CA[40]	CA[32]	CA[24]	CA[16]	CA[8]	CA[0]

Notes
4. **Figure 4-1** shows the initial three clock cycles of all transactions on the HyperBus.
5. CK# of differential clock is shown as dashed line waveform.
6. CA information is “center-aligned” with the clock during both Read and Write transactions.
7. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

Table 4-2 Command/Address Bit Assignments[8, 9, 10, 11]

CA Bit#	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W# = 1 indicates a Read transaction R/W# = 0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS = 0 indicates memory space AS = 1 indicates the register space The register space is used to access device ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type = 0 indicates wrapped burst Burst Type = 1 indicates linear burst
44-16	Row & Upper Column Address	Row & Upper Column component of the target address: System word address bits A31-A3 Any upper Row address bits not used by a particular device density should be set to 0 by the host controller master interface. The size of Rows and therefore the address bit boundary between Row and Column address is slave device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are don't care in current HyperBus devices but should be set to 0 by the host controller master interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-A0 selecting the starting word within a half-page.

Notes

8. A Row is a group of words relevant to the internal memory array structure. The number of Rows is also used in the calculation of a distributed refresh interval for HyperRAM memory.
9. The Column address selects the burst transaction starting word location within a Row. The Column address is split into an upper and lower portion. The upper portion selects an 8-word (16-byte) Half-page and the lower portion selects the word within a Half-page where a read or write transaction burst starts.
10. The initial read access time starts when the Row and Upper Column (Half-page) address bits are captured by a slave interface. Continuous linear read burst is enabled by memory devices internally interleaving access to 16 byte half-pages.
11. HyperBus protocol address space limit, assuming:
    29 Row &Upper Column address bits
    3 Lower Column address bits
    Each address selects a word wide (16 bit = 2 byte) data value
    29 + 3 = 32 address bits = 4G addresses supporting 8GB (64Gb) maximum address space
    Future expansion of the column address can allow for 29 Row &Upper Column + 16 Lower Column address bits = 35 Tera-word = 70 Tera-byte address space.

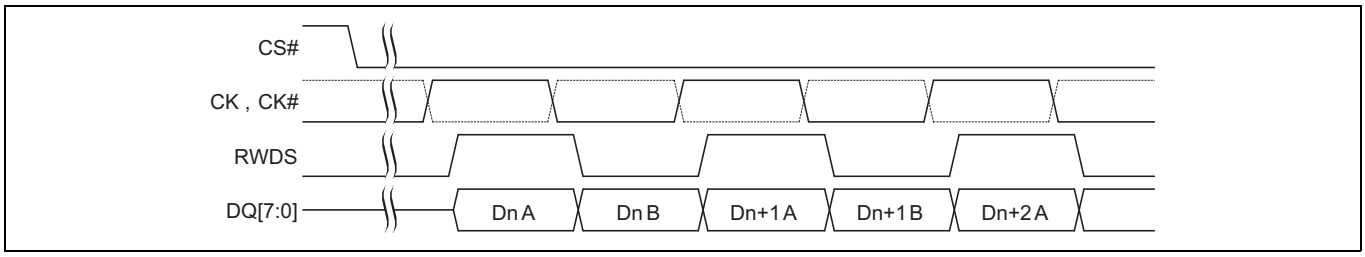


Figure 4-2 Data Placement During a Read Transaction[12, 13, 14, 15, 16]

Data placement during memory Read/Write is dependent upon the host. The device will output data (read) as it was written in (write). Hence both Big Endian and Little Endian are supported for the memory array.

Data placement during register Read/Write is Big Endian.

Notes

12. **Figure 4-2** shows a portion of a Read transaction on the HyperBus. CK# of differential clock is shown as dashed line waveform.
13. Data is “edge-aligned” with the RWDS serving as a read data strobe during read transactions.
14. Data is always transferred in full word increments (word granularity transfers).
15. Word address increments in each clock cycle. Byte A is between RWDS rising and falling edges and is followed by byte B between RWDS falling and rising edges, of each word.
16. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

Table 4-3 Data Bit Placement During Read or Write Transaction

Address Space	Byte Order	Byte Position	Word Data Bit	DQ	Bit Order
Memory	Big-endian	A	15	7	When data is being accessed in memory space: The first byte of each word read or written is the “A” byte and the second is the “B” byte. The bits of the word within the A and B bytes depend on how the data was written. If the word lower address bits 7-0 are written in the A byte position and bits 15-8 are written into the B byte position, or vice versa, they will be read back in the same order. Memory space can be stored and read in either little-endian or big-endian order.
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
		B	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	
	Little-endian	A	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	
	Little-endian	B	15	7	When data is being accessed in memory space: The first byte of each word read or written is the “A” byte and the second is the “B” byte. The bits of the word within the A and B bytes depend on how the data was written. If the word lower address bits 7-0 are written in the A byte position and bits 15-8 are written into the B byte position, or vice versa, they will be read back in the same order. Memory space can be stored and read in either little-endian or big-endian order.

Table 4-3 Data Bit Placement During Read or Write Transaction *(continued)*

Address Space	Byte Order	Byte Position	Word Data Bit	DQ	Bit Order
Memory	Little-endian	B	14	6	When data is being accessed in memory space: The first byte of each word read or written is the “A” byte and the second is the “B” byte. The bits of the word within the A and B bytes depend on how the data was written. If the word lower address bits 7-0 are written in the A byte position and bits 15-8 are written into the B byte position, or vice versa, they will be read back in the same order. Memory space can be stored and read in either little-endian or big-endian order.
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
Register	Big-endian	A	15	7	When data is being accessed in register space: During a Read transaction on the HyperBus two bytes are transferred on each clock cycle. The upper order byte A (Word[15:8]) is transferred between the rising and falling edges of RWDS (edge-aligned). The lower order byte B (Word[7:0]) is transferred between the falling and rising edges of RWDS. During a write, the upper order byte A (Word[15:8]) is transferred on the CK rising edge and the lower order byte B (Word[7:0]) is transferred on the CK falling edge. So, register space is always read and written in Big-endian order because registers have device dependent fixed bit location and meaning definitions.
			14	6	
			13	5	
			12	4	
			11	3	
			10	2	
			9	1	
			8	0	
		B	7	7	
			6	6	
			5	5	
			4	4	
			3	3	
			2	2	
			1	1	
			0	0	

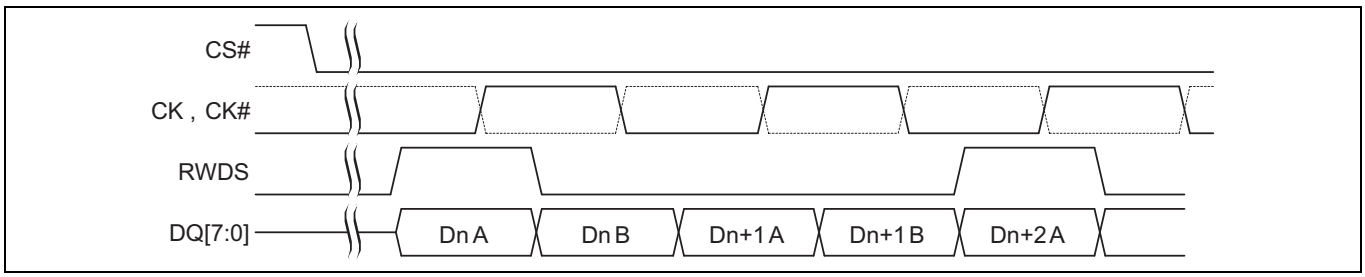


Figure 4-3 Data Placement During a Write Transaction[17, 18, 19, 20]

Notes
17. **Figure 4-3** shows a portion of a Write transaction on the HyperBus.
18. Data is “center-aligned” with the clock during a Write transaction.
19. RWDS functions as a data mask during write data transfers with initial latency. Masking of the first and last byte is shown to illustrate an unaligned 3 byte write of data.
20. RWDS is not driven by the master during write data transfers with zero initial latency. Full data words are always written in this case. RWDS may be driven LOW or left HIGH-Z by the slave in this case.

4.2 Read Transactions

The HyperBus master begins a transaction by driving CS# LOW while clock is idle. The clock then begins toggling while CA words are transferred.

In CA0, CA[47] = 1 indicates that a Read transaction is to be performed. CA[46] = 0 indicates the memory space is being read or CA[46] = 1 indicates the register space is being read. CA[45] indicates the burst type (wrapped or linear). Read transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA(15:0]) identifies the target Word address within the chosen row.

The HyperBus master then continues clocking for a number of cycles defined by the latency count setting in Configuration Register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is LOW during the CA cycles, one latency count is inserted. If RWDS is HIGH during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed the memory starts to simultaneously transition the RWDS and output the target data.

New data is output edge-aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is LOW. Note that burst transactions should not be so long as to prevent the memory from doing distributed refreshes.

Wrapped bursts will continue to wrap within the burst length and linear burst will output data in a sequential manner across row boundaries. When a linear burst read reaches the last address in the array, continuing the burst beyond the last address will provide data from the beginning of the address range. Read transfers can be ended at any time by bringing CS# HIGH when the clock is idle.

The clock is not required to be free-running. The clock may remain idle while CS# is HIGH.

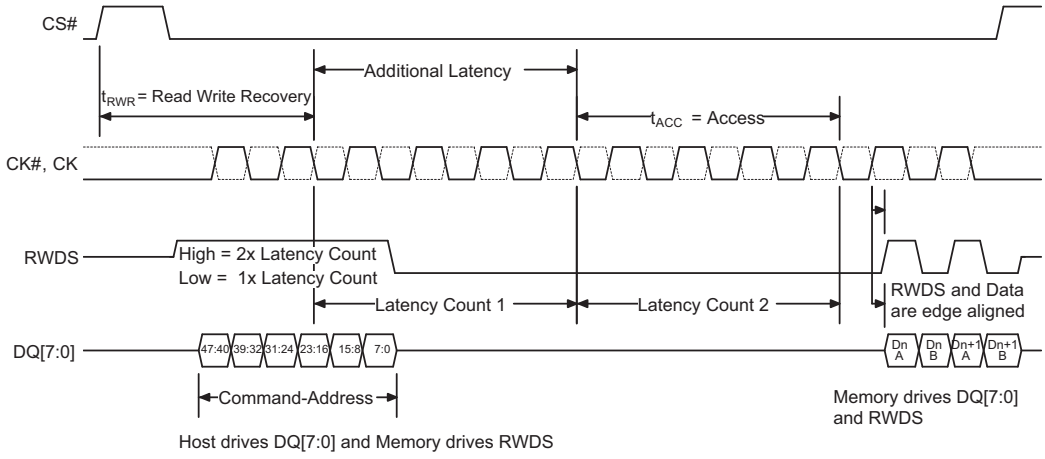


Figure 4-4 Read Transaction with Additional Initial Latency[21-28]

Notes

21. Transactions are initiated with CS# falling while CK = LOW and CK# = HIGH.
22. CS# must return HIGH before a new transaction is initiated.
23. CK# is the complement of the CK signal.CK# of a differential clock is shown as a dashed line waveform.
24. Read access array starts once CA[23:16] is captured.
25. The read latency is defined by the initial latency value in a configuration register.
26. In this read transaction example the initial latency count was set to four clocks.
27. In this read transaction a RWDS HIGH indication during CA delays output of target data by an additional four clocks.
28. The memory device drives RWDS during read transactions.

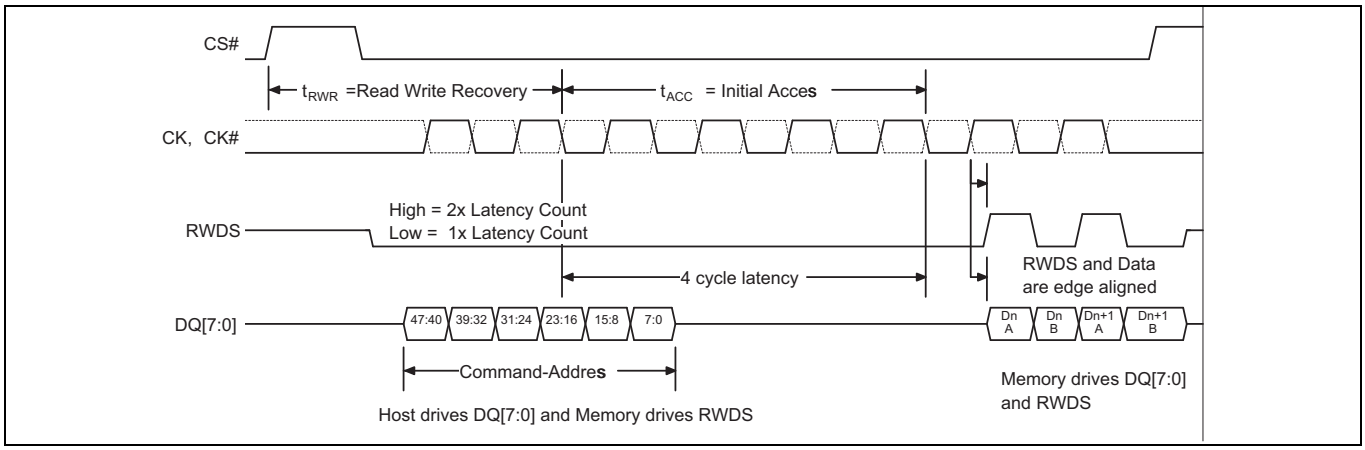


Figure 4-5 Read Transaction Without Additional Initial Latency[29]

4.3 Write Transactions (Memory Array Write)

The HyperBus master begins a transaction by driving CS# LOW while clock is idle. Then the clock begins toggling while CA words are transferred.

In CA0, CA[47] = 0 indicates that a Write transaction is to be performed. CA[46] = 0 indicates the memory space is being written. CA[45] indicates the burst type (wrapped or linear). Write transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA(15:0]) identifies the target word address within the chosen row.

The HyperBus master then continues clocking for a number of cycles defined by the latency count setting in configuration register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is LOW during the CA cycles, one latency count is inserted. If RWDS is HIGH during the CA cycles, an additional latency count is inserted.

Once these latency clocks have been completed, the HyperBus master starts to output the target data. Write data is center-aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of CK and the second byte is captured on the falling edge of CK.

During the CA clock cycles, RWDS is driven by the memory.

During the write data transfers, RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is HIGH, the byte will be masked and the array will not be altered. When data is being written and RWDS is LOW, the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the HyperRAM device are able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Data will continue to be transferred as long as the HyperBus master continues to transition the clock while CS# is LOW. Note that burst transactions should not be so long as to prevent the memory from doing distributed refreshes. Legacy format wrapped bursts will continue to wrap within the burst length. Hybrid wrap will wrap once then switch to linear burst starting at the next wrap boundary. Linear burst accepts data in a sequential manner across page boundaries. Write transfers can be ended at any time by bringing CS# HIGH when the clock is idle.

When a linear burst write reaches the last address in the memory array space, continuing the burst will write to the beginning of the address range.

The clock is not required to be free-running. The clock may remain idle while CS# is HIGH.

Note

29.RWDS is LOW during the CA cycles. In this Read Transaction, there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.

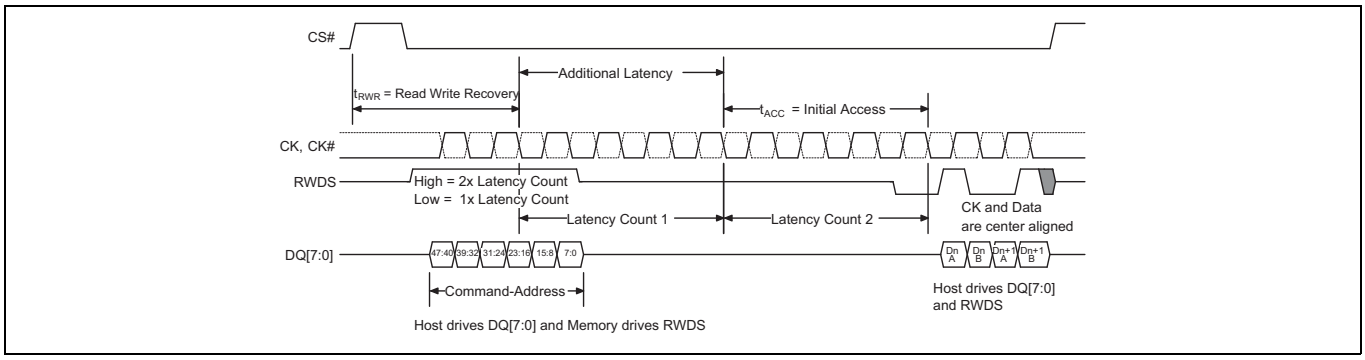


Figure 4-6 Write Transaction with Additional Initial Latency[30-36]

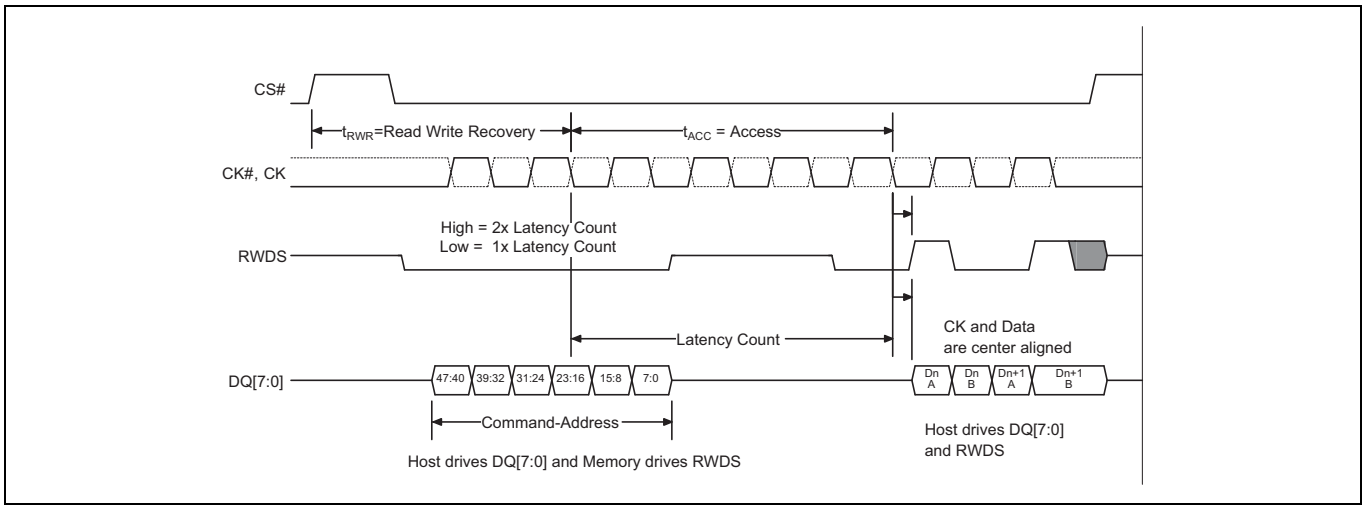


Figure 4-7 Write Transaction Without Additional Initial Latency[32-36]

Notes

30. Transactions must be initiated with CK = LOW and CK# = HIGH.
31. CS# must return HIGH before a new transaction is initiated.
32. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
33. In this example, RWDS indicates that additional initial latency cycles are required.
34. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid LOW before the end of the initial latency to provide a data mask preamble period to the slave.
35. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
36. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

4.4 Write Transactions without Initial Latency (Register Write)

A Write transaction starts with the first three clock cycles providing the Command/Address information indicating the transaction characteristics. CA0 may indicate that a Write transaction is to be performed and also indicates the address space and burst type (wrapped or linear).

Writes without initial latency are used for register space writes. HyperRAM device write transactions with zero latency mean that the CA cycles are followed by write data transfers. Writes with zero initial latency, do not have a turn around period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the HyperRAM device has received the first byte of CA i.e., before the HyperRAM device knows whether the transaction is a read or write to register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the CA period in this case, the HyperRAM device may continue to drive RWDS LOW or may take RWDS to HIGH-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

The first byte of data in each word is presented on the rising edge of CK and the second byte is presented on the falling edge of CK. Write data is center-aligned with the clock inputs. Write transfers can be ended at any time by bringing CS# HIGH when clock is idle. The clock is not required to be free-running.

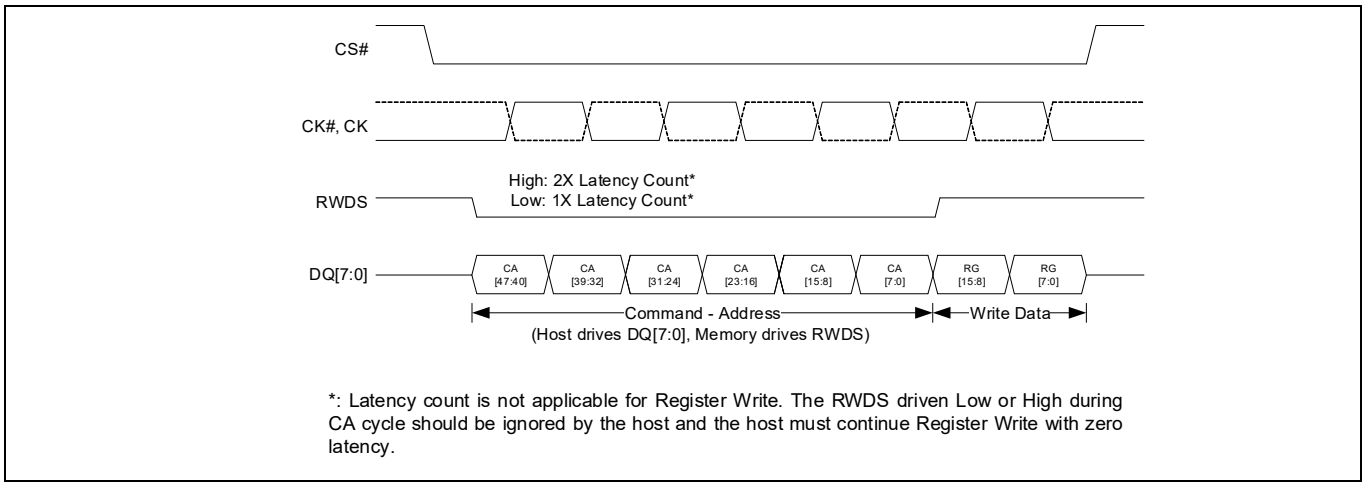


Figure 4-8 Write Operation without Initial Latency

5 Memory Space

5.1 HyperBus Interface

Table 5-1 Memory Space Address Map (word based - 16 bits)

Unit Type	Count	System Word Address Bits	CA Bits	Notes
Row	1 (row)	A8 - A3	21 - 16	512 (word addresses) 1 KB
Half-page	8 (word addresses)	A2 - A0	2 - 0	8 words (16 bytes)

6 Register Space

6.1 HyperBus Interface

When CA[46] is 1, a read or write transaction accesses the Register Space.

Table 6-1 Register Space Address Map

Register	System Address	—	—	—	31-27	26-19	18-11	10-3	—	2-0
	CA Bits	47	46	45[37]	44-40	39-32	31-24	23-16	15-8	7-0
Identification Register 0 Read[38]		C0h or E0h				00h	00h	00h	00h	00h
Identification Register 1 Read[38]		C0h or E0h				00h	00h	00h	00h	01h
Configuration Register 0 Read		C0h or E0h				00h	01h	00h	00h	00h
Configuration Register 0 Write		60h				00h	01h	00h	00h	00h
Configuration Register 1 Read		C0h or E0h				00h	01h	00h	00h	01h
Configuration Register 1 Write		60h				00h	01h	00h	00h	01h
Die Manufacture Information Register (0-17) Read		C0h or E0h				00h	02h	00h	00h	00h - 11h

6.2 Device Identification Registers

There are two read only, nonvolatile word registers, that provide information on the device selected when CS# is LOW.

The device information fields identify:

- Manufacturer
- Type
- Density
  - Row address bit count
  - Column address bit count

Notes

37. CA45 may be either 0 or 1 for either wrapped or linear read. CA45 must be 1 as only linear single word register writes are supported.
38. The Burst type (wrapped/linear) definition is not supported in Register Reads. Hence C0h/E0h have the same effect.

Table 6-2 Identification Register 0 (ID0) Bit Assignments

Bits	Function	Settings (Binary)
[15:14]	MCP Die Address	00 - Default
[13]	Reserved	0 - Default
[12:8]	Row Address Bit Count	00000 - One row address bit ... 11111 - Thirty-two row address bits ... 01100 - 64 Mb - Thirteen row address bits (default)
[7:4]	Column Address Bit Count	0000 - One column address bits ... 1000 - Nine column address bits (default) ... 1111 - Sixteen column address bits
[3:0]	Manufacturer	0001 - Cypress 0000, 0010 to 1111 - Reserved

Table 6-3 Identification Register 1 (ID1) Bit Assignments

Bits	Function	Settings (Binary)
[15:14]	Reserved	0000_0000_0000 (default)
[3:0]	Device Type	0001 - HyperRAM 2.0 0000, 0010 to 1111 - Reserved

6.2.1 Density and Row Boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register. For example: a 64 Mb HyperRAM device has 9 column address bits and 13 row address bits for a total of 22 word address bits = 2^{22} = 4 Mwords = 8 MBs. The 9 column address bits indicate that each row holds 2^{9} = 512 words = 1 KB. The row address bit count indicates there are 8196 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

ID0 value for the 64 Mb HyperRAM is 0x0C81.

6.3 Register Space Access

Register default values are loaded upon power-up or hardware reset. The registers can be altered at any time while the device is in the STANDBY state.

Loading a register is accomplished with write transaction without initial latency using a single 16-bit word write transaction.

Each register is written with a separate single word write transaction. Register write transactions have zero latency, the single word of data immediately follows the CA. RWDS is not driven by the host during the write because RWDS is always driven by the memory during the CA cycles to indicate whether a memory array refresh is in progress. Because a register space write goes directly to a register, rather than the memory array, there is no initial write latency, related to an array refresh that may be in progress. In a register write, RWDS is also not used as a data mask because both bytes of a register are always written and never masked.

Reserved register fields must be written with their default value. Writing reserved fields with other than default values may produce undefined results.

Notes

- The host must not drive RWDS during a write to register space.
- The RWDS signal is driven by the memory during the CA period based on whether the memory array is being refreshed. This refresh indication does not affect the writing of register data.
- The RWDS signal returns to high impedance after the CA period. Register data is never masked. Both data bytes of the register data are loaded into the selected register.

Reading of a register is accomplished with read transaction with single or double initial latency using a single 16 bit read transaction. If more than one word is read, the output becomes indeterminate. The contents of the register is returned in the same manner as reading the memory array, as shown in **Figure 4-4**, with one or two latency counts, based on the state of RWDS during the CA period. The latency count is defined in the Configuration Register 0 Read Latency field (CR0[7:4]).

6.3.1 Configuration Register 0

Configuration Register 0 (CR0) is used to define the power state and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, or 128 byte aligned and length data group)
- Wrapped Burst Type
  - Legacy wrap (Sequential access with wrap around within a selected length and aligned group)
  - Hybrid wrap (Legacy wrap once then linear burst at start of the next sequential group)
- Initial Latency
- Variable Latency
  - Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down (DPD) Mode

Table 6-4 Configuration Register 0 (CR0) Bit Assignments

CR0 Bit	Function	Settings (Binary)
[15]	Deep Power Down Enable	1 - Normal operation (default). HyperRAM will automatically set this value to “1” after DPD exit 0 - Writing 0 causes the device to enter Deep Power Down
[14:12]	Drive Strength	000 - 34 ohms (default) 001 - 115 ohms 010 - 67 ohms 011 - 46 ohms 100 - 34 ohms 101 - 27 ohms 110 - 22 ohms 111 - 19 ohms
[11:8]	Reserved	1 - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.
[7:4]	Initial Latency	0000 - 5 Clock Latency @ 133 MHz Max Frequency 0001 - 6 Clock Latency @ 166 MHz Max Frequency 0010 - 7 Clock Latency @ 200 MHz/166 MHz Max Frequency (default) 0011 - Reserved 0100 - Reserved ... 1101 - Reserved 1110 - 3 Clock Latency @ 85 MHz Max Frequency 1111 - 4 Clock Latency @ 104 MHz Max Frequency
[3]	Fixed Latency Enable	0 - Variable Latency - 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1 - Fixed 2 times Initial Latency (default)
[2]	Hybrid Burst Enable	0: Wrapped burst sequence to follow hybrid burst sequencing 1: Wrapped burst sequence in legacy wrapped burst manner (default) This bit setting is effective only when the "Burst Type" bit in the Command/Address register is set to '0', i.e. CA[45] = '0'; otherwise, it is ignored.
[1:0]	Burst Length	00 - 128 bytes 01 - 64 bytes 10- 16 bytes 11 - 32 bytes (default)

Wrapped Burst

A wrapped burst transaction accesses memory within a group of words aligned on a word boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 bytes alignment and length. During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured word group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

Hybrid Burst

The beginning of a hybrid burst will wrap within the target address wrapped burst group length before continuing to the next half-page of data beyond the end of the wrap group. Continued access is in linear burst order until the transfer is ended by returning CS# HIGH. This hybrid of a wrapped burst followed by a linear burst starting at the beginning of the next burst group, allows multiple sequential address cache lines to be filled in a single access. The first cache line is filled starting at the critical word. Then the next sequential line in memory can be read in to the cache while the first line is being processed.

Table 6-5 CR0[2] Control of Wrapped Burst Sequence

Bit	Default Value	Name
2	1	Hybrid Burst Enable CR0[2] = 0: Wrapped burst sequence to follow hybrid burst sequencing CR0[2] = 1: Wrapped burst sequence in legacy wrapped burst manner

Table 6-6 Example Wrapped Burst Sequences (HyperBus Addressing)

Burst Type	Wrap Boundary (bytes)	Start Address (Hex)	Sequence of Word Addresses (Hex) of Data Words
Hybrid 128	128 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02 (Wrap complete, now linear beyond the end of the initial 128 byte wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02 (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01 (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
Hybrid 32	32 Wrap once then Linear	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09 (wrap complete, now linear beyond the end of the initial 32 byte wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
Wrap 64	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, ...
Wrap 64	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...
Wrap 16	16	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, ...
Wrap 16	16	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, ...
Wrap 32	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...
Linear	Linear Burst	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...

Initial Latency

Memory Space read and write transactions or Register Space read transactions require some initial latency to open the row selected by the CA. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the HyperBus frequency can vary from 3 to 7 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 7 clocks, allowing for operation up to a maximum frequency of 200 MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a Memory Space read or write transaction or Register Space read transaction begins, the RWDS signal goes HIGH during the CA to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register Space write transactions always have zero initial latency. RWDS may be HIGH or LOW during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS HIGH during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh, it simply provides a fixed (deterministic) initial latency for all of these transaction types. The fixed latency option may simplify the design of some HyperBus memory controllers or ensure deterministic transaction performance. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven HIGH only when additional latency for a refresh is required.

Drive Strength

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] and RWDS signal output impedance to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the mid point of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage (1.8 V or 3.0 V) and 50°C. The impedance values may vary from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming state called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within t_{DPDIN} time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# LOW then HIGH, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. For additional details, see **Deep Power Down on page 29**.

6.3.2 Configuration Register 1

Configuration Register 1 (CR1) is used to define the refresh array size, refresh rate and hybrid sleep for the HyperRAM device. Configurable characteristics include:

- Partial Array Refresh
- Hybrid Sleep State
- Refresh rate

Table 6-7 Configuration Register 1 (CR1) Bit Assignments

CR1 Bit	Function	Setting (Binary)
[15:8]	Reserved	FFh - Reserved (default) These bits should always be set to FFh
[7]	Reserved	1 - Reserved (default)
[6]	Master Clock Type	1 - Single-Ended - CK (default) 0 - Differential - CK#, CK
[5]	Hybrid Sleep	1 - Causes the device to enter Hybrid Sleep State 0 - Normal operation (default)
[4:2]	Partial Array Refresh	000 - Full Array (default) 001 - Bottom 1/2 Array 010 - Bottom 1/4 Array 011 - Bottom 1/8 Array 100 - none 101 - Top 1/2 Array 110 - Top 1/4 Array 111 - Top 1/8 Array
[1:0]	Distributed Refresh Interval (Read Only)	10 - 1 µs t_{CSM} (at 125 °C) 11 - Reserved 00 - Reserved 01 - 4 µs t_{CSM} (at 85 °C)

Master Clock Type

Two clock types, namely single ended and differential, are supported. CR1[6] selects which type to use.

Partial Array Refresh

The partial array refresh configuration restricts the refresh operation in HyperRAM to a portion of the memory array specified by CR1[5:3]. This reduces the standby current. The default configuration refreshes the whole array.

Hybrid Sleep (HS)

When the HyperRAM is not needed for system operation but data in the device needs to be retained, it may be placed in Hybrid Sleep state to save more power. Enter Hybrid Sleep state by writing 0 to CR1[5]. Bringing CS# LOW will cause the device to exit HS state and set CR1[5] to 1. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost.

Distributed Refresh Interval

The DRAM array requires periodic refresh of all bits in the array. This can be done by the host system by reading or writing a location in each row within a specified time limit. The read or write access copies a row of bits to an internal buffer. At the end of the access the bits in the buffer are written back to the row in memory, thereby recharging (refreshing) the bits in the row of DRAM memory cells.

HyperRAM devices include self-refresh logic that will refresh rows automatically. The automatic refresh of a row can only be done when the memory is not being actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS HIGH during the CA period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The required refresh interval for the entire memory array varies with temperature as shown in **Table 6-8**. This is the time within which all rows must be refreshed. Refresh of all rows could be done as a single batch of accesses at the beginning of each interval, in groups (burst refresh) of several rows at a time, spread throughout each interval, or as single row refreshes evenly distributed throughout the interval. The self-refresh logic distributes single row refresh operations throughout the interval so that the memory is not busy doing a burst of refresh operations for a long period, such that the burst refresh would delay host access for a long period.

Table 6-8 Array Refresh Interval per Temperature

Device Temperature (°C)	Array Refresh Interval (ms)	Array Rows	Recommended t_{CSM} (µs)
85	64	8192	4

The distributed refresh method requires that the host does not do burst transactions that are so long as to prevent the memory from doing the distributed refreshes when they are needed. This sets an upper limit on the length of read and write transactions so that the refresh logic can insert a refresh between transactions. This limit is called the CS# LOW maximum time (t_{CSM}). The t_{CSM} value is determined by the array refresh interval divided by the number of rows in the array, then reducing this calculation by half to ensure that a distributed refresh interval cannot be entirely missed by a maximum length host access starting immediately before a distributed refresh is needed. Because t_{CSM} is set to half the required distributed refresh interval, any series of maximum length host accesses that delay refresh operations will catch up on refresh operations at twice the rate required by the refresh interval divided by the number of rows.

The host system is required to respect the t_{CSM} value by ending each transaction before violating t_{CSM}. This can be done by host memory controller logic splitting long transactions when reaching the t_{CSM} limit, or by host system hardware or software not performing a single read or write transaction that would be longer than t_{CSM}.

As noted in **Table 6-8**, the array refresh interval is longer at lower temperatures such that t_{CSM} could be increased to allow longer transactions. The host system can either use the t_{CSM} value from the table for the maximum operating temperature or, may determine it dynamically by reading the read only CR1[1:0] bits in order to set the distributed refresh interval prior to every access.

7 Interface States

Table 7-1 describes the required value of each signal for each interface state.

Table 7-1 Interface States

Interface State	V_{CC} / $V_{CC}Q$	CS#	CK, CK#	DQ7-DQ0	RWDS	RESET#
Power-Off	< V_{LKO}	X	X	HIGH-Z	HIGH-Z	X
Power-On (Cold) Reset	≥ V_{CC} / $V_{CC}Q$ min	X	X	HIGH-Z	HIGH-Z	X
Hardware (Warm) Reset	≥ V_{CC} / $V_{CC}Q$ min	X	X	HIGH-Z	HIGH-Z	L
Interface Standby	≥ V_{CC} / $V_{CC}Q$ min	H	X	HIGH-Z	HIGH-Z	H
CA	≥ V_{CC} / $V_{CC}Q$ min	L	T	Master Output Valid	Y	H
Read Initial Access Latency (data bus turn around period)	≥ V_{CC} / $V_{CC}Q$ min	L	T	HIGH-Z	L	H
Write Initial Access Latency (RWDS turn around period)	≥ V_{CC} / $V_{CC}Q$ min	L	T	HIGH-Z	HIGH-Z	H
Read data transfer	≥ V_{CC} / $V_{CC}Q$ min	L	T	Slave Output Valid	Slave Output Valid Z or T	H
Write data transfer with Initial Latency	≥ V_{CC} / $V_{CC}Q$ min	L	T	Master Output Valid	Master Output Valid X or T	H
Write data transfer without Initial Latency[39]	≥ V_{CC} / $V_{CC}Q$ min	L	T	Master Output Valid	Slave Output L or HIGH-Z	H
Active Clock Stop[40]	≥ V_{CC} / $V_{CC}Q$ min	L	Idle	Master or Slave Output Valid or HIGH-Z	Y	H
Deep Power Down	≥ V_{CC} / $V_{CC}Q$ min	H	X or T	HIGH-Z	HIGH-Z	H
Hybrid Sleep	≥ V_{CC} / $V_{CC}Q$ min	H	X or T	HIGH-Z	HIGH-Z	H

Legend

L = V_{IL}
H = V_{IH}
X = either V_{IL} or V_{IH}
Y= either V_{IL} or V_{IH} or V_{OL} or V_{OH}
Z = either V_{OL} or V_{OH}
L/H = rising edge
H/L = falling edge
T = Toggling during information transfer
Idle = CK is LOW and CK# is HIGH.
Valid = all bus signals have stable L or H level

Notes

39. Writes without initial latency (with zero initial latency), do not have a turn around period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required. Since master write data immediately follows the CA period the HyperRAM device may continue to drive RWDS LOW or may take RWDS to HIGH-Z. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).
40. Active Clock Stop is described in **Active Clock Stop on page 28**. DPD is described in **Hybrid Sleep on page 28**.

8 Power Conservation Modes

8.1 Interface Standby

STANDBY is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS# = HIGH). All inputs, and outputs other than CS# and RESET# are ignored in this state.

8.2 Active Clock Stop

The Active Clock Stop state reduces device interface energy consumption to the I_{CC6} level during the data transfer portion of a read or write operation. The device automatically enables this state when clock remains stable for t_{ACC} + 30 ns. While in Active Clock Stop state, read data is latched and always driven onto the data bus. I_{CC6} shown in **DC Characteristics on page 32**.

Active Clock Stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be LOW throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 ns. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The Active Clock Stop state must not be used in violation of the t_{CSM} limit. CS# must go HIGH before t_{CSM} is violated. Clock can be stopped during any portion of the active transaction as long as it is in the LOW state. Note that it is recommended to avoid stopping the clock during register access.

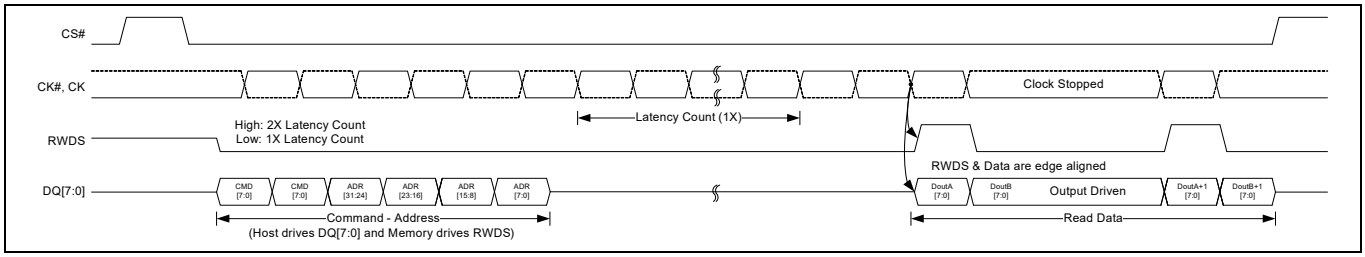


Figure 8-1 Active Clock Stop During Read Transaction (DDR)[41]

8.3 Hybrid Sleep

In the Hybrid Sleep (HS) state, the current consumption is reduced (i_{HS}). HS state is entered by writing a 0 to CR1[5]. The device reduces power within t_{HSIN} time. The data in Memory Space and Register Space is retained during HS state. Bringing CS# LOW will cause the device to exit HS state and set CR1[5] to 1. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost. Returning to STANDBY state requires t_{EXITHS} time. Following the exit from HS due to any of these events, the device is in the same state as entering Hybrid Sleep.

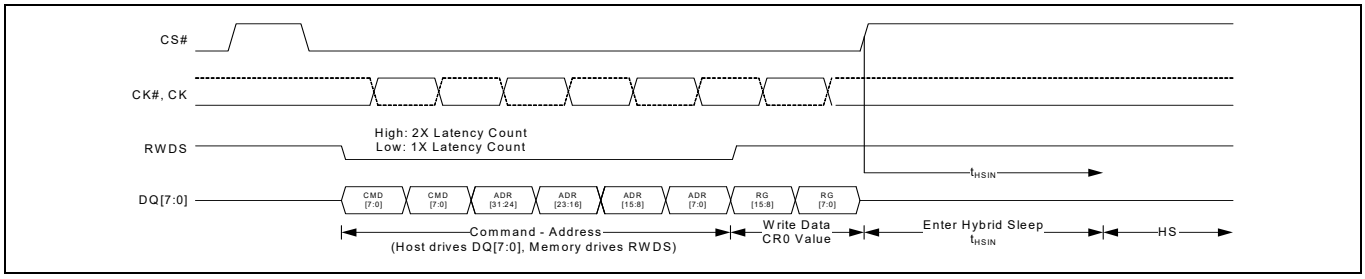


Figure 8-2 Enter HS Transaction

Note

41. RWDS is LOW during the CA cycles. In this Read Transaction, there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.

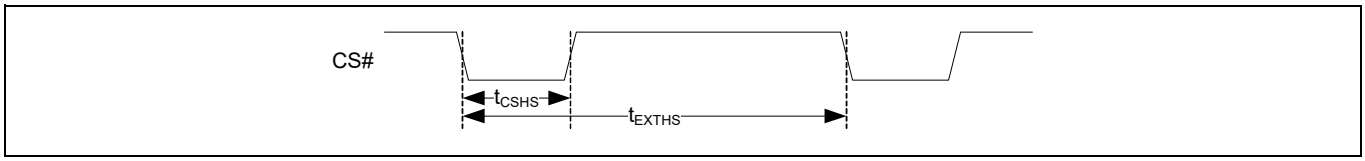


Figure 8-3 Exit HS Transaction

Table 8-1 Hybrid Sleep Timing Parameters

Parameter	Description	Min	Max	Unit
t_{HSIN}	Hybrid Sleep CR1[5] = 0 register write to DPD power level	-	3	µs
t_{CSHS}	CS# Pulse Width to Exit HS	60	3000	ns
t_{EXTHS}	CS# Exit Hybrid Sleep to Standby wakeup time	-	100	µs

8.4 Deep Power Down

In the Deep Power Down (DPD) state, current consumption is driven to the lowest possible level (I_{DPD}). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in Memory Space is lost, (becomes invalid without refresh) during DPD state. Driving CS# LOW then HIGH will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. Returning to STANDBY state requires t_{EXTDPD} time. Returning to STANDBY state following a POR requires t_{VCS} time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

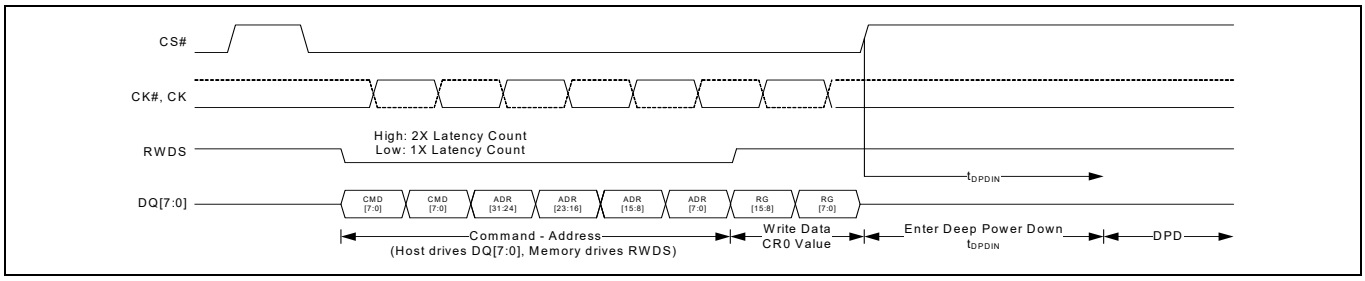


Figure 8-4 Enter DPD Transaction

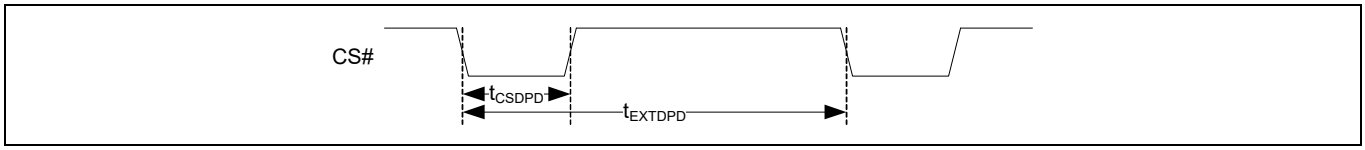


Figure 8-5 Exit DPD Transaction

Table 8-2 Deep Power Down Timing Parameters

Parameter	Description	Min	Max	Unit
t_{DPDIN}	Deep Power Down CR0[15] = 0 register write to DPD power level	-	3	µs
t_{CSDPD}	CS# Pulse Width to Exit DPD	200	3000	ns
t_{EXTDPD}	CS# Exit Deep Power Down to Standby wakeup time	-	150	µs

9 Electrical Specifications

9.1 Absolute Maximum Ratings[44]

Storage Temperature Plastic Packages –65 °C to +150 °C

Ambient Temperature with Power Applied–65 °C to +135 °C

Voltage with Respect to Ground

All signals[42] .....–0.5V to +(V_{CC} + 0.5 V)

Output Short Circuit Current[43]..... 100 mA

V_{CC}, $V_{CC}Q$ ..... –0.5 V to +4.0 V

Electrostatic Discharge Voltage:

Human Body Model (JEDEC Std JESD22-A114-B) 2000 V

Charged Device Model (JEDEC Std JESD22-C101-A) 500 V

9.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may negative overshoot V_{SS} to –1.0 V or positive overshoot to V_{CC} +1.0 V, for periods up to 20 ns.

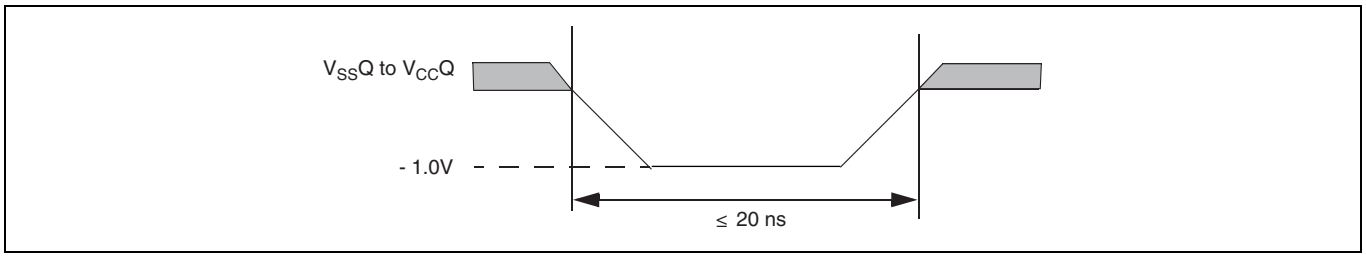


Figure 9-1 Maximum Negative Overshoot Waveform

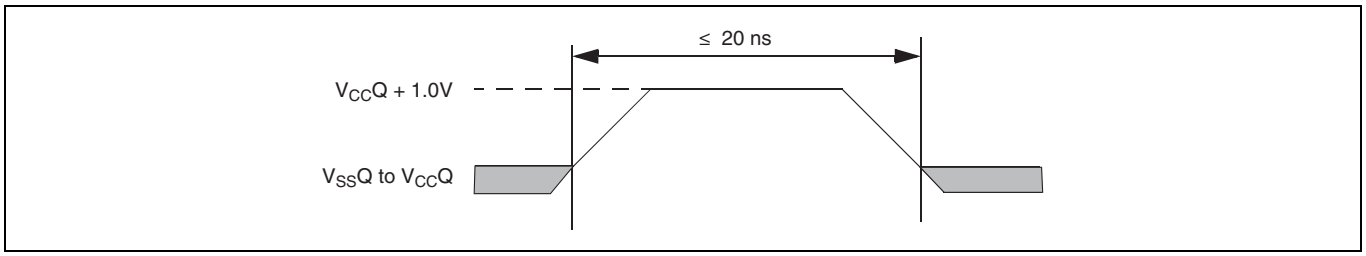


Figure 9-2 Maximum Positive Overshoot Waveform

Notes

42. Minimum DC voltage on input or I/O signal is -1.0 V. During voltage transitions, input or I/O signals may undershoot V_{SS} to -1.0 V for periods of up to 20 ns. See Figure 9-1. Maximum DC voltage on input or I/O signals is V_{CC} +1.0 V. During voltage transitions, input or I/O signals may overshoot to V_{CC} +1.0 V for periods up to 20 ns. See Figure 9-2.
43. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
44. Stresses above those listed under **Absolute Maximum Ratings[44] on page 30** may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Latch-up Characteristics

Table 9-1 Latch-up Specification[45]

Description	Min	Max	Unit
Input voltage with respect to $V_{SS}Q$ on all input only connections	–1.0	$V_{CC}Q$ + 1.0	V
Input voltage with respect to $V_{SS}Q$ on all I/O connections	–1.0	$V_{CC}Q$ + 1.0	V
$V_{CC}Q$ Current	–100	+100	mA

9.3 Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

9.3.1 Temperature Ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Automotive-E, AEC-Q100 Grade 1	–40	125	°C

9.3.2 Power Supply Voltages

Parameter	Min	Max	Unit
1.8 V V_{CC} Power Supply	1.7	2.0	V
3.0 V V_{CC} Power Supply	2.7	3.6	V

Note
45. Excludes power supplies $V_{CC}/V_{CC}Q$. Test conditions: $V_{CC} = V_{CC}Q$, one connection at a time tested, connections not being tested are at V_{SS}.

9.4 DC Characteristics

Table 9-2 DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions	64 Mb			Unit
			Min	Typ[46]	Max	
I_{LI1}	Input Leakage Current 3.0 V Device Reset Signal High Only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	-	-	–0.1	µA
I_{LI2}	Input Leakage Current 1.8 V Device Reset Signal High Only	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	-	-	–0.1	µA
I_{LI3}	Input Leakage Current 3.0 V Device Reset Signal Low Only[47]	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	-	-	+15.0	µA
I_{LI4}	Input Leakage Current 1.8 V Device Reset Signal Low Only[47]	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	-	-	+15.0	µA
I_{CC1}	V_{CC} Active Read Current	CS# = V_{SS}, @200 MHz, V_{CC} = 2.0V	-	15	30	mA
		CS# = V_{SS}, @166 MHz, V_{CC} = 3.6V	-	15	34	mA
		CS# = VSS, @200 MHz, V_{CC} = 3.6V	-	15	36	mA
I_{CC2}	V_{CC} Active Write Current	CS# = V_{SS}, @200 MHz, V_{CC} = 2.0V	-	15	30	mA
		CS# = V_{SS}, @166 MHz, V_{CC} = 3.6V	-	15	34	mA
		CS# = V_{SS}, @200 MHz, V_{CC} = 3.6V	-	15	36	mA
I_{CC4P}	V_{CC} Standby Current (–40 °C to +125 °C)	CS# = V_{CC}, V_{CC} = 2.0 V; Full Array	-	80	495	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Bottom 1/2 Array	-	-	450	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Bottom 1/4 Array	-	-	405	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Bottom 1/8 Array	-	-	375	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Top 1/2 Array	-	-	450	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Top 1/4 Array	-	-	405	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Top 1/8 Array	-	-	375	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; Full Array	-	90	540	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; Bottom 1/2 Array	-	-	495	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; Bottom 1/4 Array	-	-	435	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; Bottom 1/8 Array	-	-	405	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; T op 1/2 Array	-	-	495	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; Top 1/4 Array	-	-	435	µA
		CS# = V_{CC}, V_{CC} = 3.6 V; Top 1/8 Array	-	-	405	µA
I_{CC5}	Reset Current	CS# = V_{CC}, RESET# = V_{SS}, V_{CC} = V_{CC} max	-	-	1.5	mA

Table 9-2 DC Characteristics (CMOS Compatible) *(continued)*

Parameter	Description	Test Conditions	64 Mb			Unit
			Min	Typ[46]	Max	
I_{CC6IP}	Active Clock Stop Current (–40 °C to +125 °C)	CS# = V_{SS}, RESET# = V_{CC}, V_{CC} = V_{CC} max	-	8	15	mA
I_{CC7}	V_{CC} Current during power-up[46]	CS# = V_{CC}, V_{CC} = V_{CC} max, V_{CC} = V_{CCQ} = 2.0V or 3.6 V	-	-	42	mA
I_{DPD}[47]	Deep Power Down Current 3.0 V (–40 °C to +125 °C)	CS# = V_{CC}, V_{CC} = 3.6 V	-	-	23	µA
	Deep Power Down Current 1.8 V (–40 °C to +125 °C)	CS# = V_{CC}, V_{CC} = 2.0 V	-	-	18	µA
I_{HS}[47]	Hybrid Sleep Current 3.0 V (–40 °C to +125 °C)	CS# = V_{CC}, V_{CC} = 2.0 V; Full Array	-	25	450	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Bottom 1/2 Array	-	-	405	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Bottom 1/4 Array	-	-	360	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Bottom 1/8 Array	-	-	315	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Top 1/2 Array	-	-	405	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Top 1/4 Array	-	-	360	µA
		CS# = V_{CC}, V_{CC} = 2.0 V; Top 1/8 Array	-	-	315	µA
	Hybrid Sleep Current 3.0 V (–40 °C to +125 °C)	CS# = VCC, VCC = 3.6 V; Full Array	-	35	495	µA
		CS# = VCC, VCC = 3.6 V; Bottom 1/2 Array	-	-	450	µA
		CS# = VCC, VCC = 3.6 V; Bottom 1/4 Array	-	-	390	µA
		CS# = VCC, VCC = 3.6 V; Bottom 1/8 Array	-	-	375	µA
		CS# = VCC, VCC = 3.6 V; Top 1/2 Array	-	-	450	µA
		CS# = VCC, VCC = 3.6 V; Top 1/4 Array	-	-	390	µA
		CS# = VCC, VCC = 3.6 V; Top 1/8 Array	-	-	375	µA
V_{IL}	Input Low Voltage	-	–0.15 x V_{CCQ}	-	0.30 x V_{CCQ}	V
V_{IH}	Input High Voltage	-	0.70 x V_{CCQ}	-	1.15 x V_{CCQ}	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA for DQ[7:0]	-	-	0.20	V
V_{OH}	Output High Voltage	I_{OH} = 100 µA for DQ[7:0]	V_{CCQ}-0.20	-	-	V

Notes

46.Not 100% tested.

47.RESET# LOW initiates exits from DPD state and initiates the draw of I_{CC5} reset current, making I_{LI} during RESET# LOW insignificant.

9.4.1 Capacitance Characteristics

Table 9-3 3.0 V Capacitive Characteristics[48, 49, 50]

Description	Parameter	64 Mb	Unit
		Max	
Input Capacitance (CK, CK#, CS#)	CI	3.0	pF
Delta Input Capacitance (CK, CK#)	CID	0.25	pF
Output Capacitance (RWDS)	CO	3.0	pF
IO Capacitance (DQx)	CIO	3.0	pF
IO Capacitance Delta (DQx)	CIOD	0.25	pF

Table 9-4 Thermal Resistance

Parameter[51]	Description	Test Conditions	24-ball FBGA Package	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	66.7	°C/W
θ_{JC}	Thermal resistance (junction to case)		37	°C/W

Notes

48. These values are guaranteed by design and are tested on a sample basis only.
49. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, $V_{CC}Q$ are applied and all other signals (except the signal under test) floating. DQ's should be in the high impedance state.
50. Note that the capacitance values for the CK, CK#, RWDS and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (LOW) and data being presented on the DQs bus.
51. This parameter is guaranteed by characterization; not tested in production.

9.5 Power-Up Initialization

HyperRAM products include an on-chip voltage sensor used to launch the power-up initialization process. V_{CC} and $V_{CC}Q$ must be applied simultaneously. When the power supply reaches a stable level at or above V_{CC}(min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied on $V_{CC}Q$ until V_{CC} (min) is reached during power-up, and then CS# must remain HIGH for a further delay of t_{VCS}. A simple pull-up resistor from $V_{CC}Q$ to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is LOW during power up, the device delays start of the t_{VCS} period until RESET# is HIGH. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

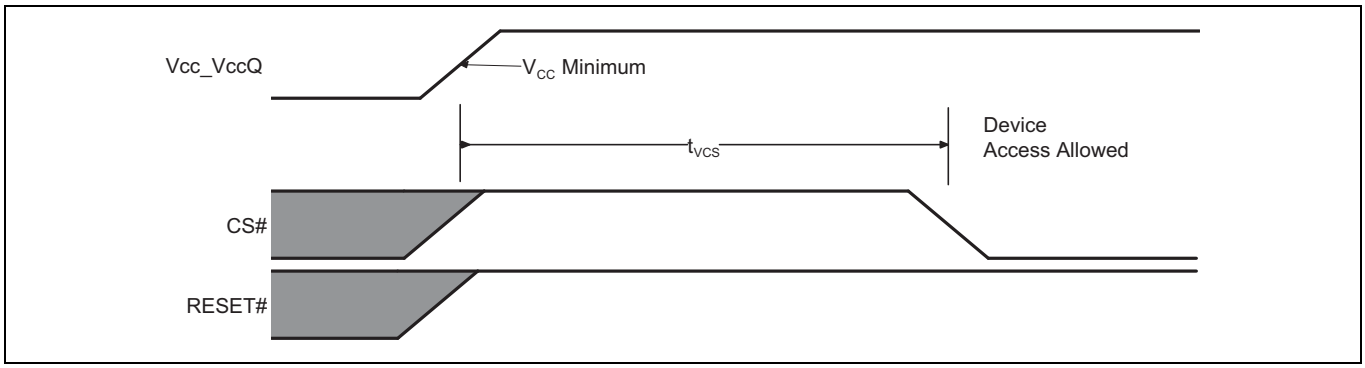


Figure 9-3 Power-up with RESET# HIGH

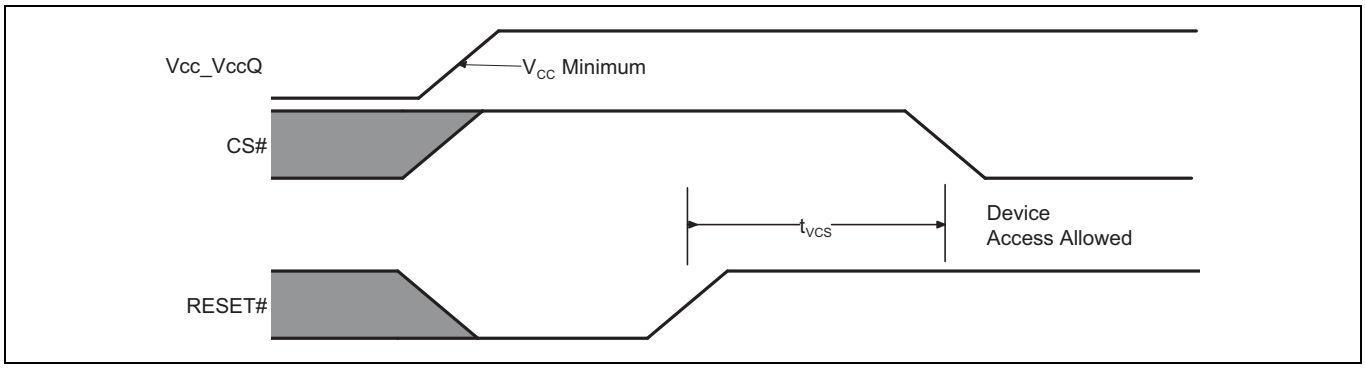


Figure 9-4 Power-up with RESET# LOW

Table 9-5 Power-up and Reset Parameters[52, 53, 54]

Parameter	Description	Min	Max	Unit
t_{VCS}	V_{CC} and $V_{CC}Q \geq$ minimum and RESET# HIGH to first access	-	150	µs

Notes
52. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).
53. $V_{CC}Q$ must be the same voltage as V_{CC}.
54. V_{CC} ramp rate may be non-linear.

9.6 Power Down

HyperRAM devices are considered to be powered-off when the array power supply (V_{CC}) drops below the V_{CC} Lock-Out voltage (V_{LKO}). During a power supply transition down to the V_{SS} level, $V_{CC}Q$ should remain less than or equal to V_{CC}. At the V_{LKO} level, the HyperRAM device will have lost configuration or array data.

V_{CC} must always be greater than or equal to $V_{CC}Q$ ($V_{CC} \geq V_{CC}Q$).

During Power-Down or voltage drops below V_{LKO}, the array power supply voltages must also drop below V_{CC} Reset (V_{RST}) for a Power Down period (t_{PD}) for the part to initialize correctly when the power supply again rises to V_{CC} minimum. See Figure 9-5.

If during a voltage drop the V_{CC} stays above V_{LKO} the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If V_{CC} does not go below and remain below V_{RST} for greater than t_{PD}, then there is no assurance that the POR process will be performed. In this case, a hardware reset will be required ensure the HyperBus device is properly initialized.

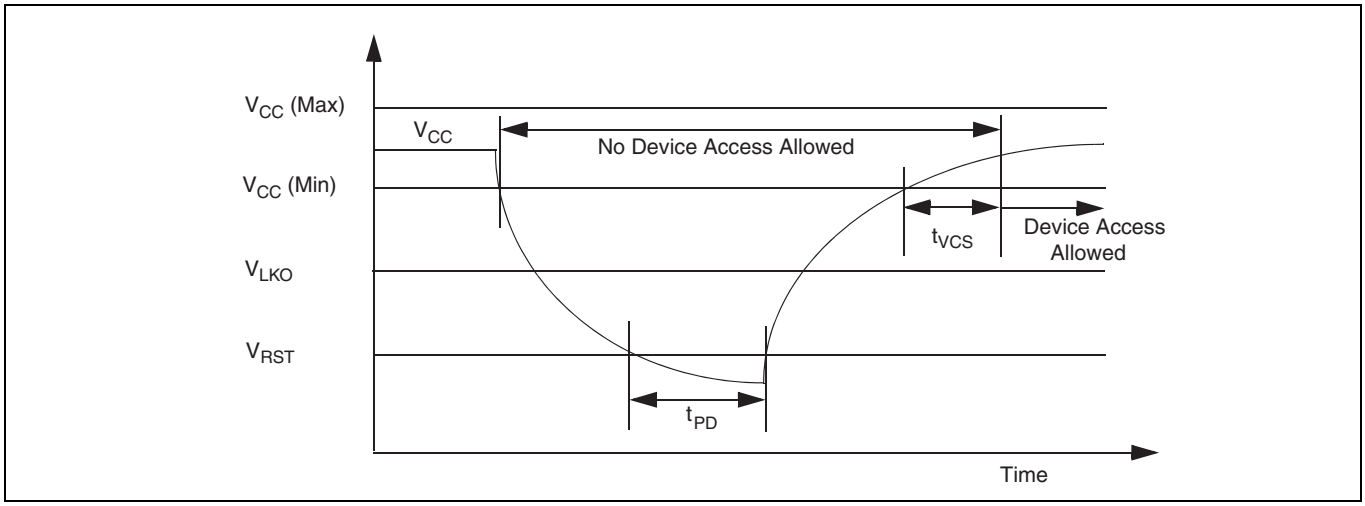


Figure 9-5 Power Down or Voltage Drop

The following section describes the HyperRAM device-dependent aspects of power down specifications.

Table 9-6 1.8 V Power-Down Voltage and Timing[55]

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	1.7	2.0	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	1.5	-	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.7	-	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	50	-	µs

Table 9-7 3.0 V Power-Down Voltage and Timing[55]

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	2.7	3.6	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	2.4	-	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.7	-	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	50	-	µs

Note
55.V_{CC} ramp rate can be non-linear.

9.7 Hardware Reset

The RESET# input provides a hardware method of returning the device to the STANDBY state.

During t_{RPH} the device will draw I_{CC5} current. If RESET# continues to be held LOW beyond t_{RPH}, the device draws CMOS standby current (I_{CC4}). While RESET# is LOW (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A hardware reset will do the following:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is LOW - memory array data is considered as invalid
- Force the device to exit the Hybrid Sleep state
- Force the device to exit the Deep Power Down state

After RESET# returns HIGH, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# LOW, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per **Table 6-8**. This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume DRAM array data is lost after a hardware reset and reload any required data.

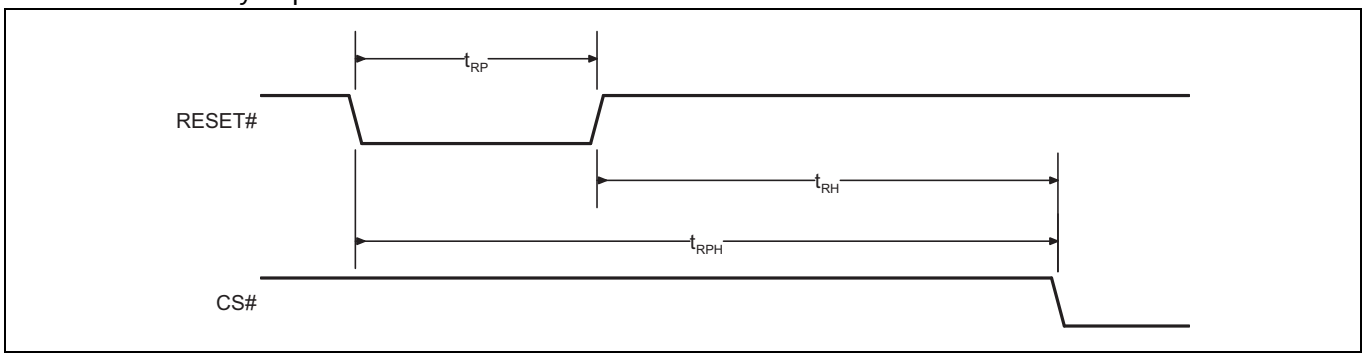


Figure 9-6 Hardware Reset Timing Diagram

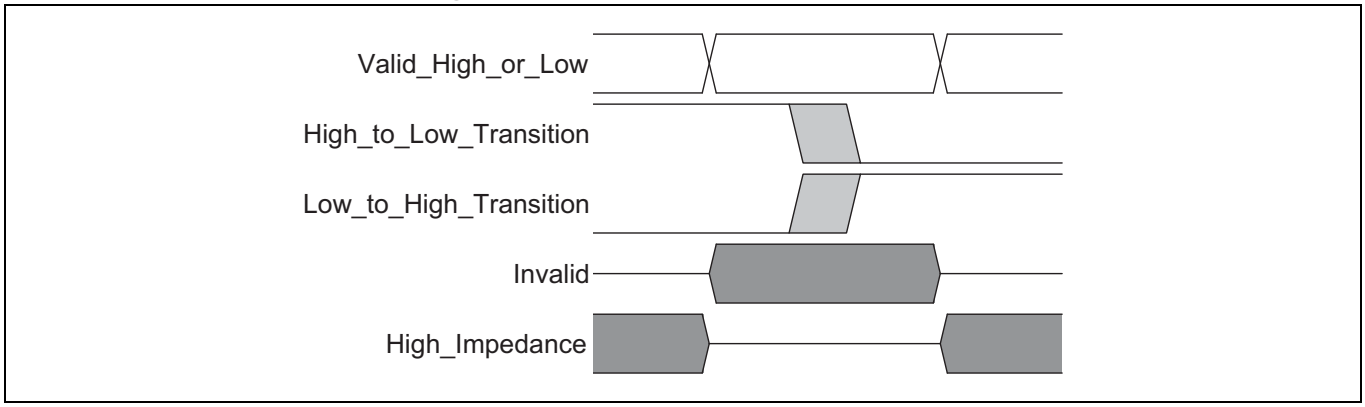
Table 9-8 Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	-	ns
t_{RH}	Time between RESET# (HIGH) and CS# (LOW)	200	-	ns
t_{RPH}	RESET# LOW to CS# LOW	400	-	ns

10 Timing Specifications

The following section describes HyperRAM device dependent aspects of timing specifications.

10.1 Key to Switching Waveforms



10.2 AC Test Conditions

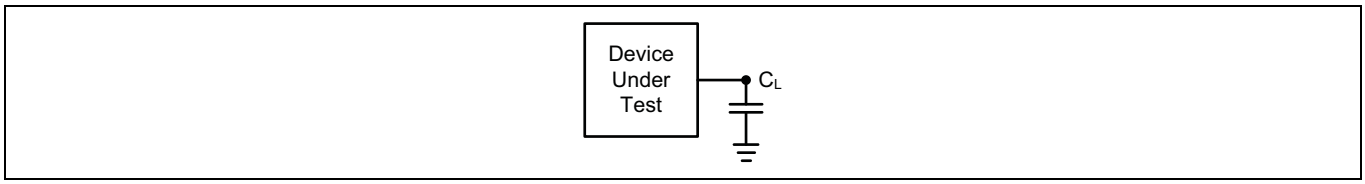


Figure 10-1 Test Setup

Table 10-1 Test Specification[56]

Parameter	All Speeds	Unit
Output Load Capacitance, C_L	15	pF
Minimum Input Rise and Fall Slew Rates (1.8 V) [58]	1.13	V/ns
Minimum Input Rise and Fall Slew Rates (3.0 V) [58]	2.06	V/ns
Input Pulse Levels	0.0-$V_{CC}Q$	V
Input timing measurement reference levels	$V_{CC}Q/2$	V
Output timing measurement reference levels	$V_{CC}Q/2$	V

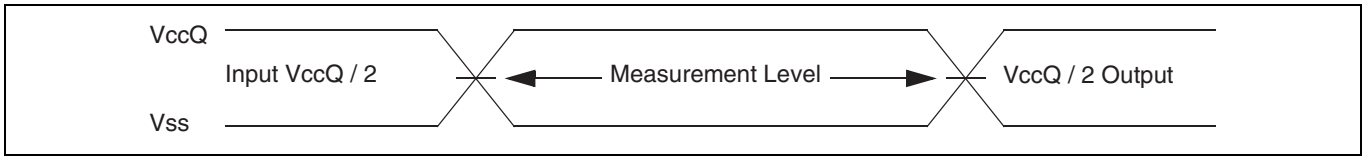


Figure 10-2 Input Waveforms and Measurement Levels[58]

Notes
56.Input and output timing is referenced to $V_{CC}Q/2$ or to the crossing of CK/CK#.
57.All AC timings assume this input slew rate.
58.Input timings for the differential CK/CK# pair are measured from clock crossings.

10.3 CLK Characteristics

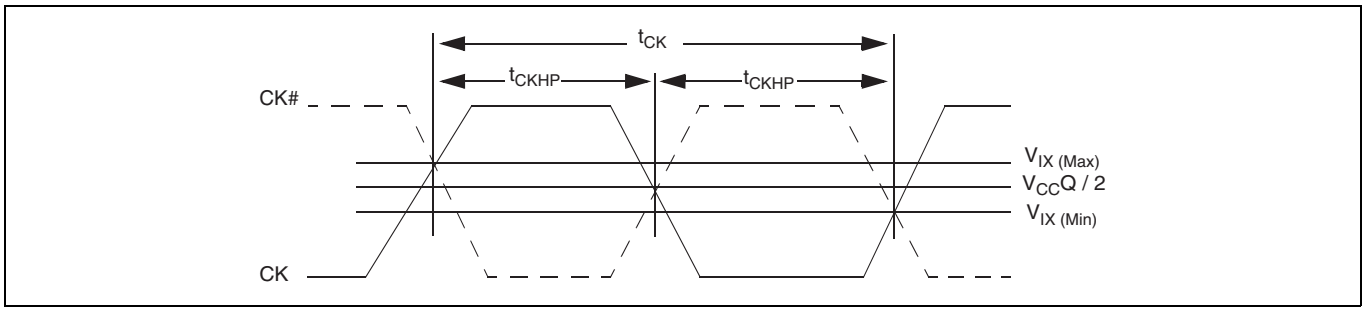


Figure 10-3 Clock Characteristics

Table 10-2 Clock Timings[59, 60, 61]

Parameter	Symbols	200 MHZ		166 MHZ		Unit
		Min	Max	Min	Max	
CK Period	t_{CK}	5	–	6	–	ns
CK Half Period - Duty Cycle	t_{CKHP}	0.45	0.55	0.45	0.55	t_{CK}
CK Half Period at Frequency Min = 0.45 t_{CK} Min Max = 0.55 t_{CK} Min	t_{CKHP}	2.25	2.75	2.7	3.3	ns

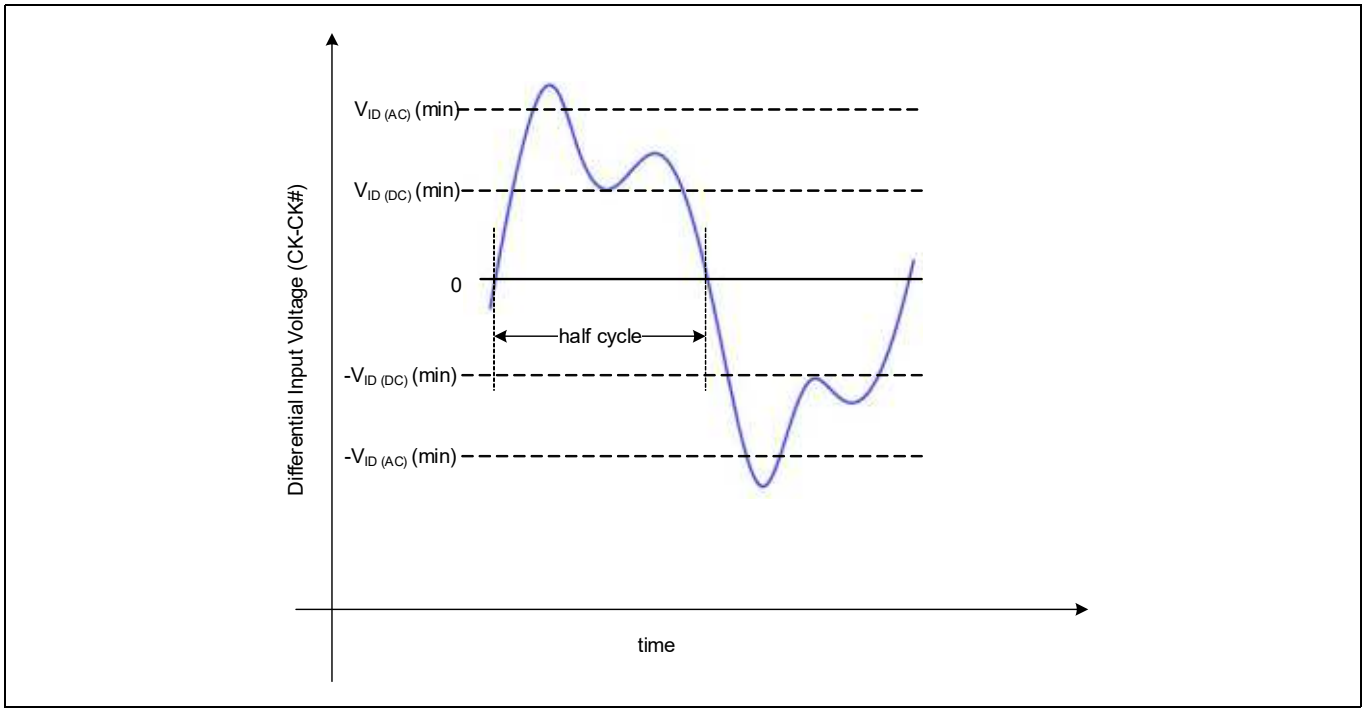


Figure 10-4 Differential Clock (CK/CK#) Input Swing

Notes
59. Clock jitter of ±5% is permitted.
60. Minimum Frequency (Maximum t_{CK}) is dependent upon maximum CS# LOW time (t_{CSM}), Initial Latency and Burst Length.
61. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).

Table 10-3 Clock AC/DC Electrical Characteristics[62, 63]

Parameter	Symbol	Min	Max	Unit
DC Input Voltage	V_{IN}	–0.3	$V_{CC}Q$+ 0.3	V
DC Input Differential Voltage	$V_{ID(DC)}$	$V_{CC}Q \times 0.4$	$V_{CC}Q$+ 0.6	V
AC Input Differential Voltage	$V_{ID(AC)}$	$V_{CC}Q \times 0.6$	$V_{CC}Q$ + 0.6	V
AC Differential Crossing Voltage	V_{IX}	$V_{CC}Q \times 0.4$	$V_{CC}Q$ x 0.6	V

10.4 AC Characteristics

10.4.1 Read Transactions

Table 10-4 HyperRAM Specific Read Timing Parameters

Parameter	Symbol	200 MHz		166 MHz		Unit
		Min	Max	Min	Max	
Chip Select High Between Transactions - 1.8V	t_{CSHI}	6	–	6	–	ns
Chip Select High Between Transactions - 3.0V		6	–	6	–	
HyperRAM Read-Write Recovery Time - 1.8V	t_{RWR}	35	–	36	–	ns
HyperRAM Read-Write Recovery Time - 3.0V		35	–	36	–	
Chip Select Setup to next CK Rising Edge	t_{CSS}	4.0	–	3	–	ns
Data Strobe Valid - 1.8V	t_{DSV}	–	5.0	–	12	ns
Data Strobe Valid - 3.0V		–	6.5	–	12	
Input Setup - 1.8V	t_{IS}	0.5	–	0.6	–	ns
Input Setup - 3.0V		0.5	–	0.6	–	
Input Hold - 1.8V	t_{IH}	0.5	–	0.6	–	ns
Input Hold - 3.0V		0.5	–	0.6	–	
HyperRAM Read Initial Access Time - 1.8V	t_{ACC}	35	–	36	–	ns
HyperRAM Read Initial Access Time- 3.0V		35	–	36	–	
Clock to DQs Low Z	t_{DQLZ}	0	–	0	–	ns
CK transition to DQ Valid - 1.8V	t_{CKD}	1	5.0	1	5.5	ns
CK transition to DQ Valid - 3.0V		1	6.5	1	7	
CK transition to DQ Invalid - 1.8V	t_{CKDI}	0	4.2	0	4.6	ns
CK transition to DQ Invalid - 3.0V		0.5	5.7	0.5	5.6	
Data Valid (t_{DV} min = the lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min) - 1.8V	t_{DV}[64]	1.45	–	1.8	–	ns
Data Valid (t_{DV} min = the lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or t_{CKHP} min - t_{CKD} min + t_{CKDI} min) - 3.0V		1.45	–	1.3	–	
CK transition to RWDS Valid - 1.8V	t_{CKDS}	–	5.0	1	5.5	ns
CK transition to RWDS Valid - 3.0V		–	6.5	1	7	
RWDS transition to DQ Valid - 1.8V	t_{DSS}	–0.4	+0.4	–0.45	+0.45	ns
RWDS transition to DQ Valid - 3.0V		–0.4	+0.4	–0.8	+0.8	

Notes
62. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
63. The value of V_{IX} is expected to equal $V_{CC}Q/2$ of the transmitting device and must track variations in the DC level of $V_{CC}Q$.
64. Refer to **Figure 12-4** for data valid timing.

Table 10-4 HyperRAM Specific Read Timing Parameters *(continued)*

Parameter	Symbol	200 MHz		166 MHz		Unit
		Min	Max	Min	Max	
RWDS transition to DQ Invalid - 1.8V	t_{DSH}	–0.4	+0.4	–0.45	+0.45	ns
RWDS transition to DQ Invalid - 3.0V		–0.4	+0.4	–0.8	+0.8	
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	0	–	ns
Chip Select Inactive to RWDS High-Z - 1.8V	t_{DSZ}	–	5.0	–	6	ns
Chip Select Inactive to RWDS High-Z - 3.0V		–	6.5	–	7	
Chip Select Inactive to DQ High-Z - 1.8V	t_{OZ}	–	5	–	6	ns
Chip Select Inactive to DQ High-Z - 3.0V		–	6.5	–	7	
Refresh Time - 1.8V	t_{RFH}	35	–	36	–	ns
Refresh Time - 3.0V		35	–	36	–	
CK transition to RWDS Low @CA phase @Read - 1.8V	t_{CKDSR}	1	5.5	1	5.5	ns
CK transition to RWDS Low @CA phase @Read - 3.0V		1	7	1	7	

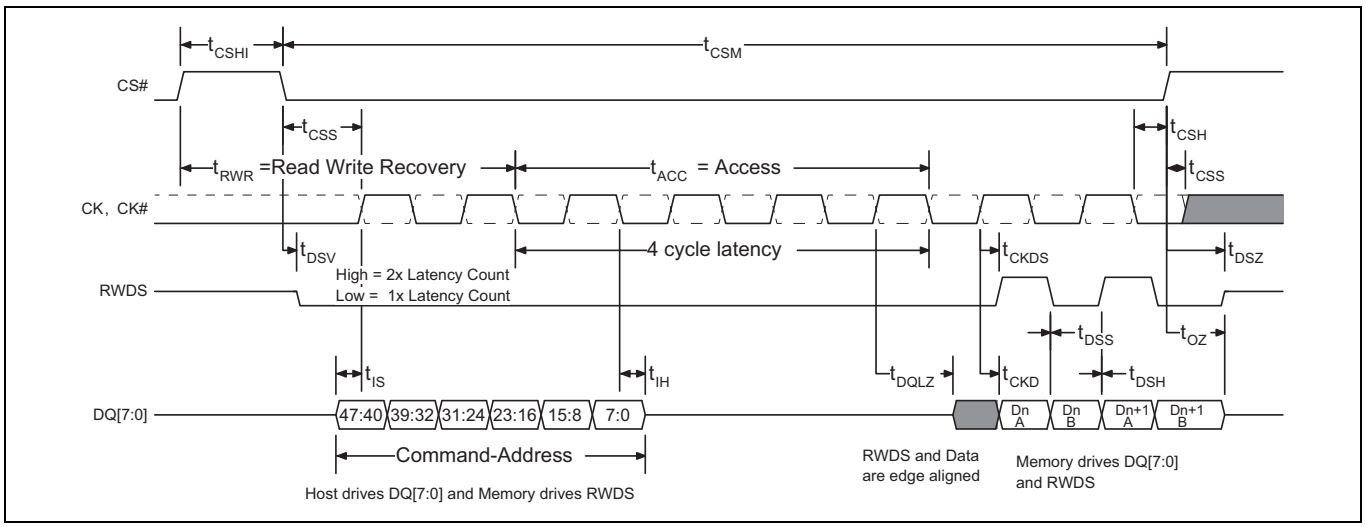


Figure 10-5 Read Timing Diagram — No Additional Latency Required

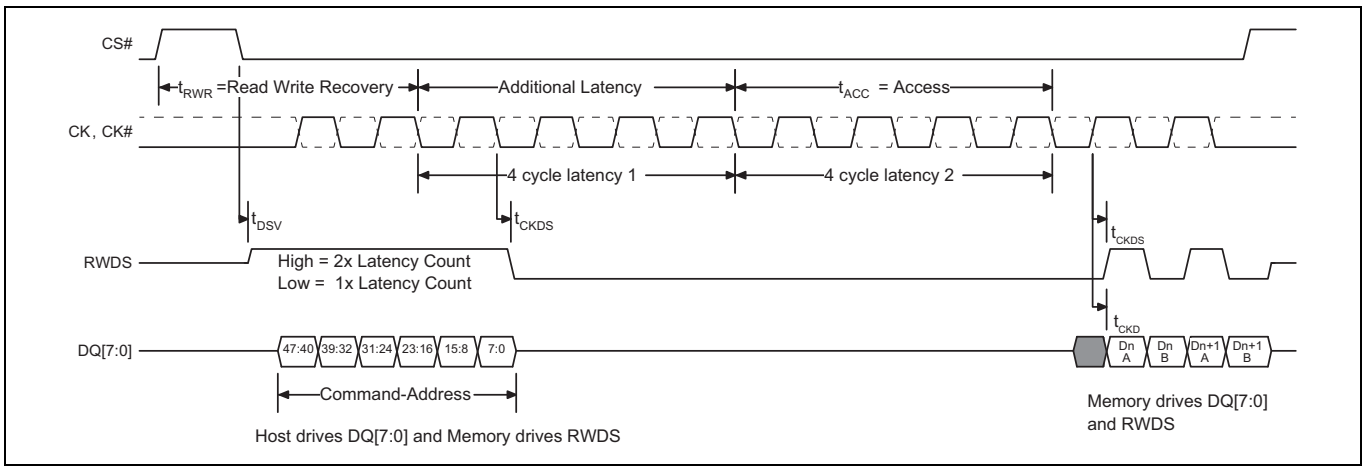


Figure 10-6 Read Timing Diagram — With Additional Latency Required

10.4.2 Write Transactions

Table 10-5 Write Timing Parameters

Parameter	Symbol	200 MHz		166 MHz		Unit
		Min	Max	Min	Max	
Read-Write Recovery Time	t_{RWR}	35	-	36	-	ns
Access Time	t_{ACC}	35	-	36	-	ns
Refresh Time	t_{RFH}	35	-	36	-	ns
Chip Select Maximum Low Time (85 °C)	t_{CSM}	-	4	-	4	µs
Chip Select Maximum Low Time (125 °C)	t_{CSM}	-	1	-	1	µs
RWDS Data Mask Valid	t_{DMV}	0	-	0	-	µs

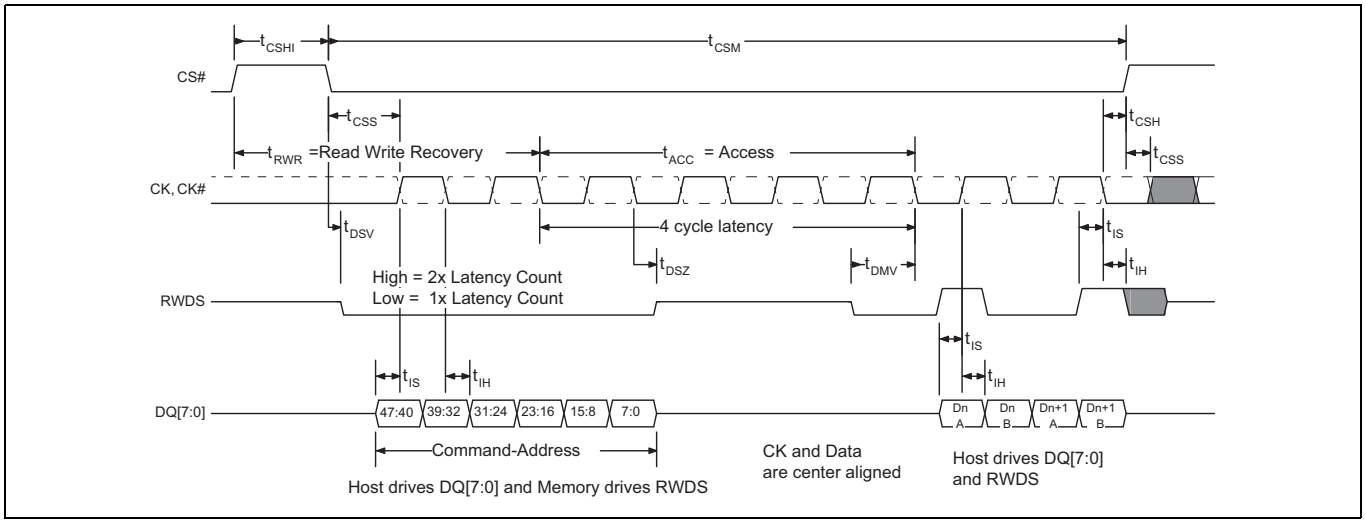


Figure 10-7 Write Timing Diagram — No Additional Latency

10.5 Timing Reference Levels

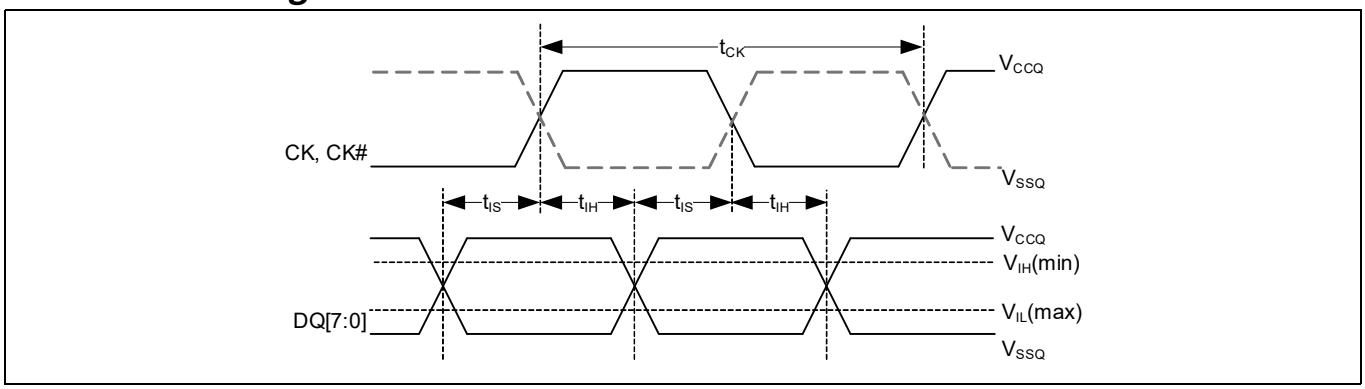


Figure 10-8 DDR Input Timing Reference Levels

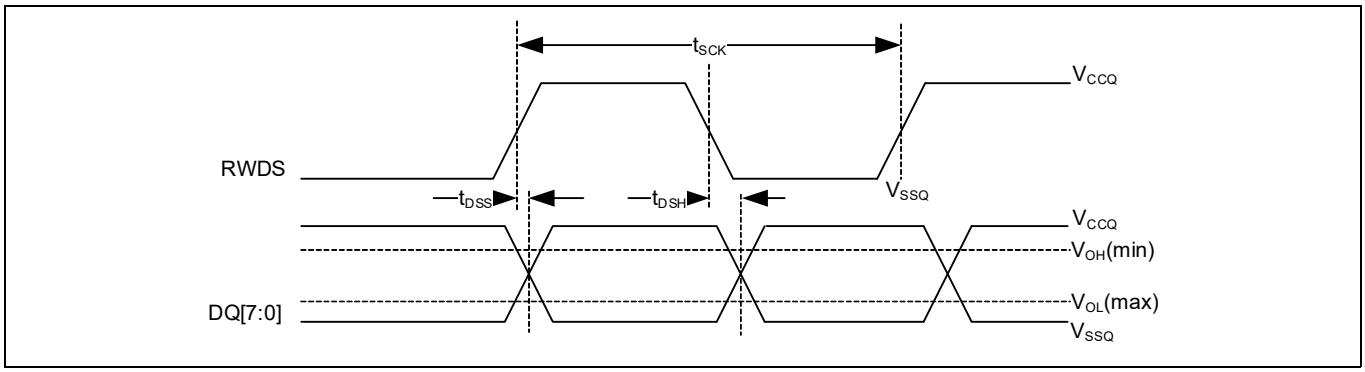


Figure 10-9 DDR Output Timing Reference Levels

11 Physical Interface

11.1 FBGA 24-Ball 5 x 5 Array Footprint

HyperRAM devices are provided in Fortified Ball Grid Array (FBGA), 1 mm pitch, 24-ball, 5 × 5 ball array footprint, with 6mm x 8mm body.

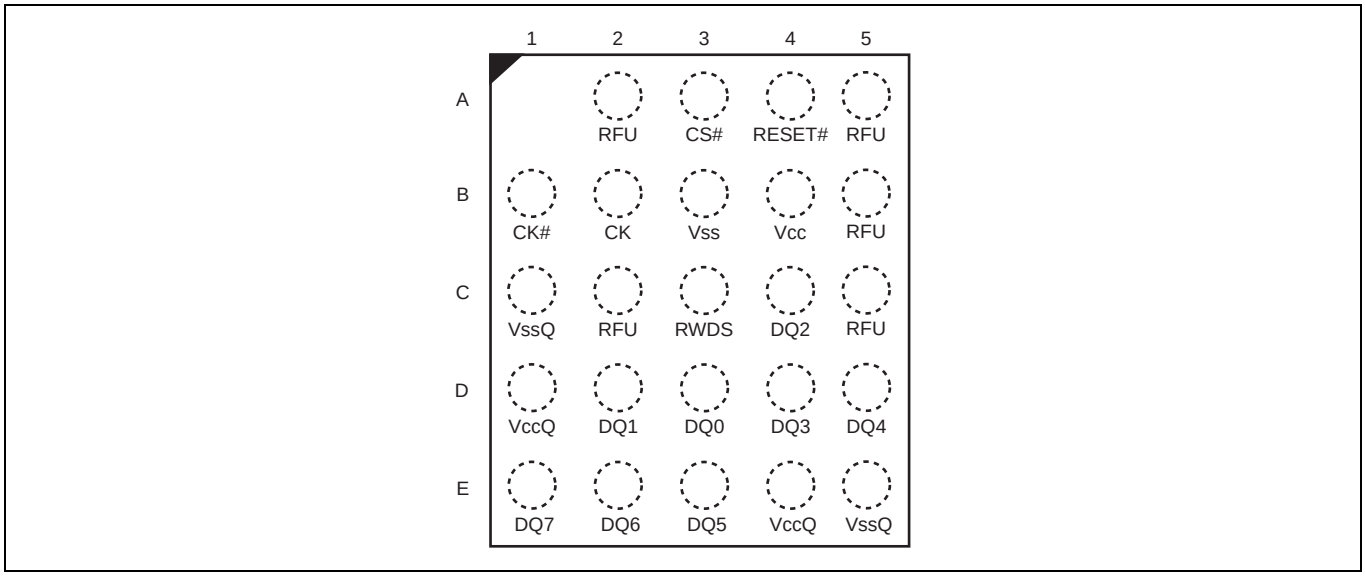
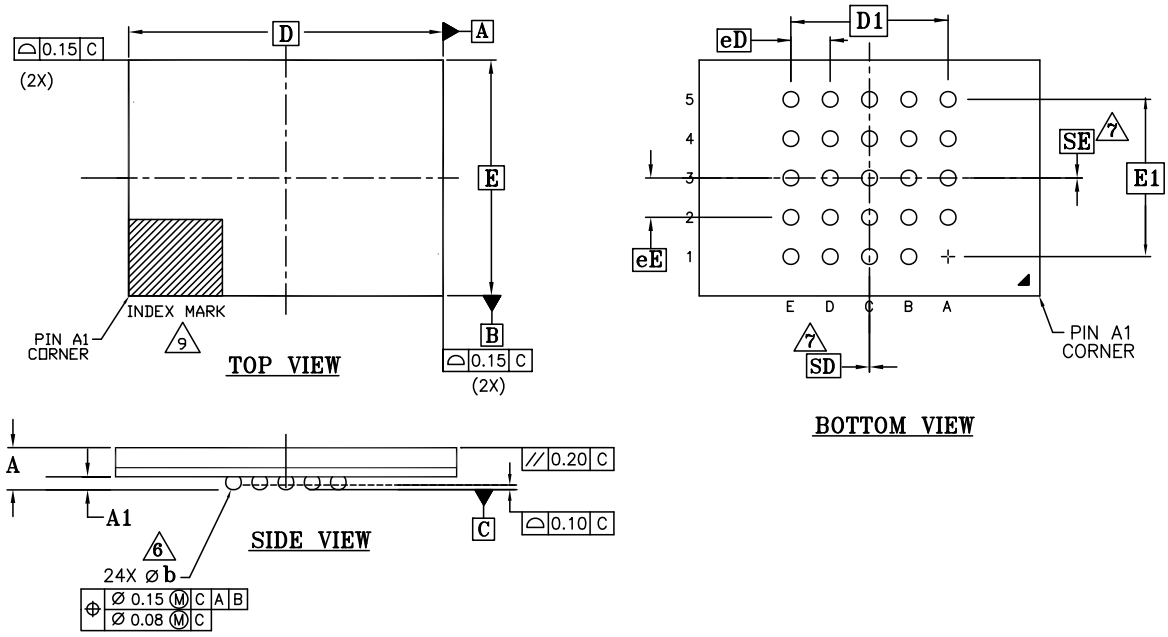


Figure 11-1 24-Ball FBGA, 6 × 8 mm, 5 × 5 Ball Footprint, Top View

11.2 Package Diagrams



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
∅ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

002-15550 *A

Figure 11-2 Fortified Ball Grid Array 24-ball 6 × 8 × 1.0 mm (VAA024)

12 DDR Center-Aligned Read Strobe (DCARS) Functionality

The HyperRAM device offers an optional feature that enables independent skewing (phase shifting) of the RWDS signal with respect to the read data outputs. This feature is provided in certain devices, based on the Ordering Part Number (OPN).

When the DCARS feature is provided, a second differential Phase Shifted Clock input PSC/PSC# is used as the reference for RWDS edges instead of CK/CK#. The second clock is generally a copy of CK/CK# that is phase shifted 90 degrees to place the RWDS edges centered within the DQ signals valid data window. However, other degrees of phase shift between CK/CK# and PSC/PSC# may be used to optimize the position of RWDS edges within the DQ signals valid data window so that RWDS provides the desired amount of data setup and hold time in relation to RWDS edges.

PSC/PSC# is not used during a write transaction. PSC and PSC# may be driven LOW and HIGH respectively or, both may be driven LOW during write transactions.

The PSC/PSC# is used in HyperBus devices. If single-ended mode is selected, then PSC# must be driven LOW but must not be left floating (leakage concerns).

12.1 HyperRAM Products with DCARS Signal Descriptions

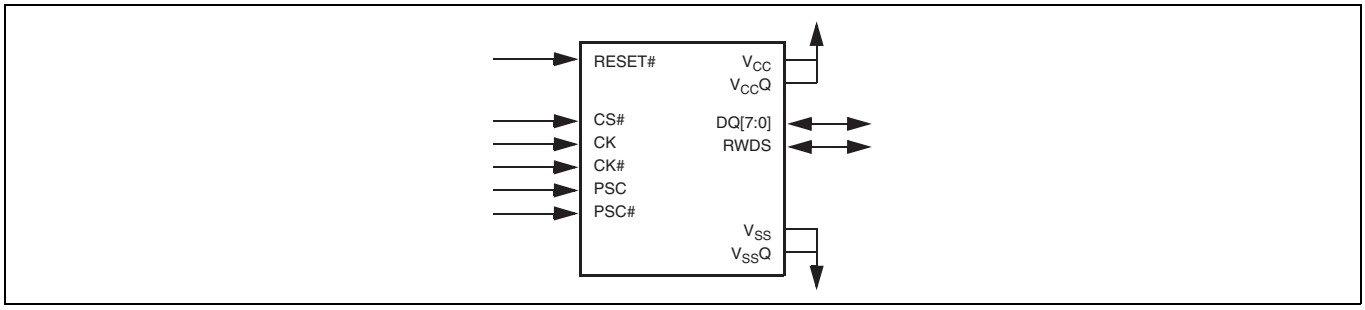


Figure 12-1 HyperBus Product with DCARS Signal Diagram

Table 12-1 Signal Descriptions

Symbol	Type	Description
CS#	Input	**Chip Select.** HyperBus transactions are initiated with a HIGH to LOW transition. HyperBus transactions are terminated with a LOW to HIGH transition.
CK, CK#	Input	**Differential Clock**. Command, address, and data information is output with respect to the crossing of the CK and CK# signals. Use of differential clock is optional. **Single Ended Clock.** CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
PSC, PSC#	Input	**Phase Shifted Clock.** PSC/PSC# allows independent skewing of the RWDS signal with respect to the CK/CK# inputs. If the CK/CK# (differential mode) is configured, then PSC/PSC# are used. Otherwise, only PSC is used (Single Ended). PSC (and PSC#) may be driven HIGH and LOW respectively or both may be driven LOW during write transactions.
RWDS	Output	**Read-Write Data Strobe.** Data bytes output during read transactions are aligned with RWDS based on the phase shift from CK, CK# to PSC, PSC#. PSC, PSC# cause the transitions of RWDS, thus the phase shift from CK, CK# to PSC, PSC# is used to place RWDS edges within the data valid window. RWDS is an input during write transactions to function as a data mask. At the beginning of all bus transactions RWDS is an output and indicates whether additional initial latency count is required (1 = additional latency count, 0 = no additional latency count).
DQ[7:0]	Input/Output	**Data Input/Output.** CA/Data information is transferred on these DQs during Read and Write transactions.

Table 12-1 Signal Descriptions *(continued)*

Symbol	Type	Description
RESET#	Input	**Hardware RESET**. When LOW, the device will self initialize and return to the idle state. RWDS and DQ[7:0] are placed into the HIGH-Z state when RESET# is LOW. RESET# includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the HIGH state.
V_{CC}	Power Supply	Array Power.
$V_{CC}Q$	Power Supply	Input/Output Power.
V_{SS}	Power Supply	Array Ground.
$V_{SS}Q$	Power Supply	Input/Output Ground.

12.2 HyperRAM Products with DCARS — FBGA 24-ball, 5 x 5 Array Footprint

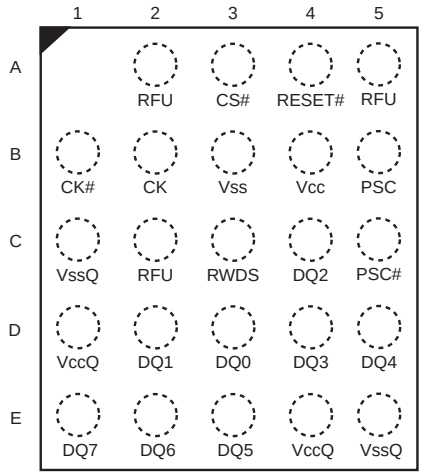


Figure 12-2 24-ball FBGA, 5 × 5 Ball Footprint, Top View

12.3 HyperRAM Memory with DCARS Timing

The illustrations and parameters shown here are only those needed to define the DCARS feature and show the relationship between the Phase Shifted Clock, RWDS, and data.

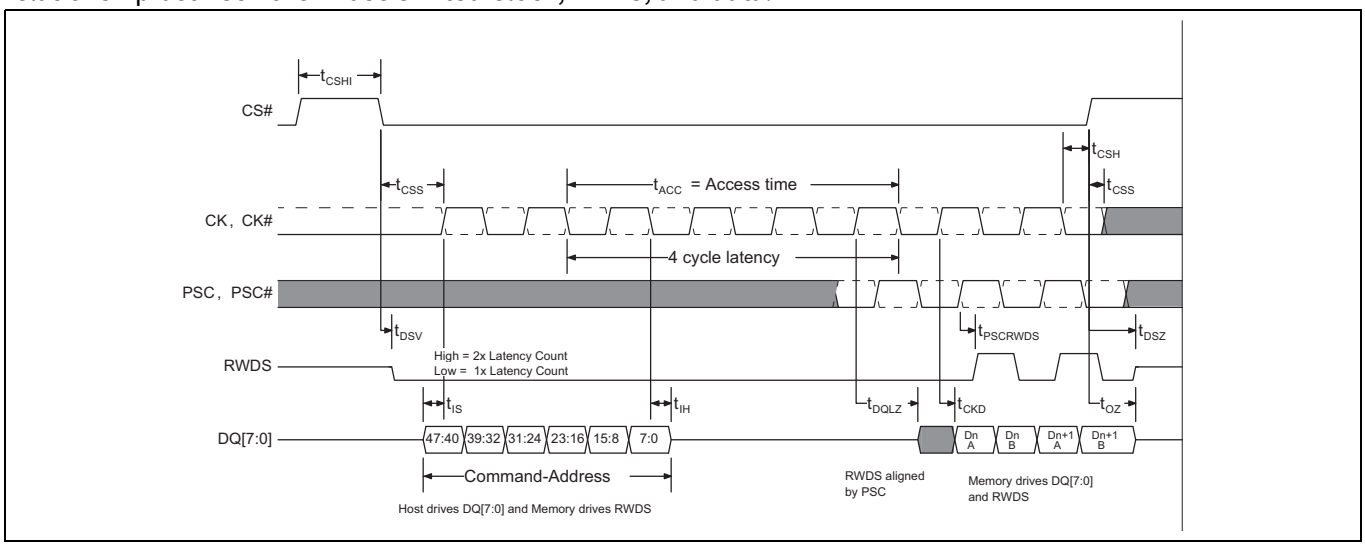


Figure 12-3 HyperRAM Memory DCARS Timing Diagram[65, 66, 67]

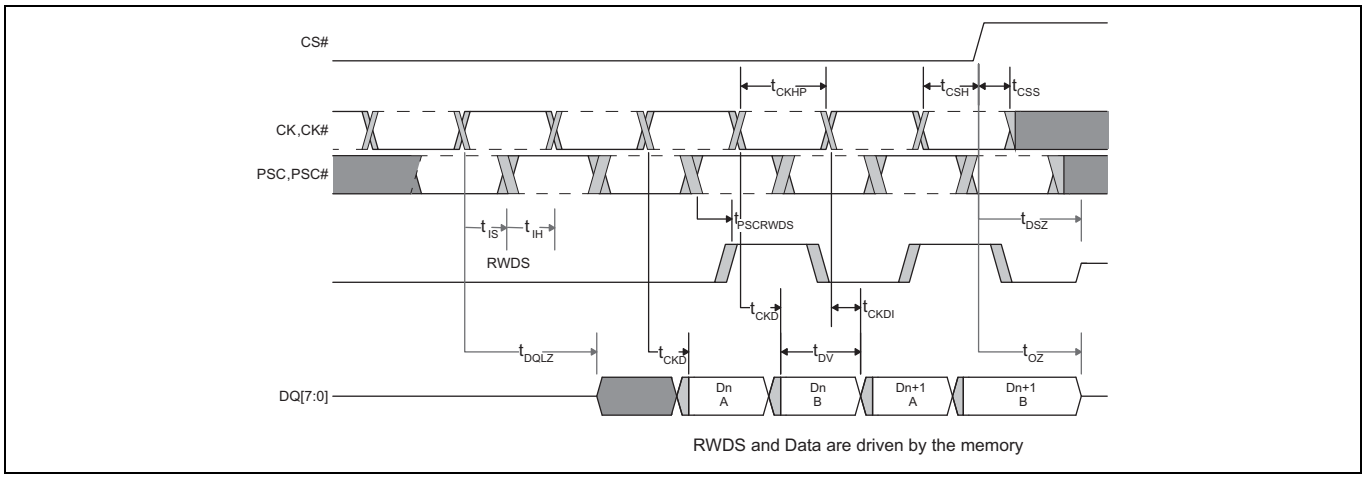


Figure 12-4 DCARS Data Valid Timing[72, 70, 70]

Notes

65. Transactions must be initiated with CK = LOW and CK# = HIGH. CS# must return HIGH before a new transaction is initiated.
66. The memory drives RWDS during read transactions.
67. This example demonstrates a latency code setting of four clocks and no additional initial latency required.
68. Sampled, not 100% tested.
69. This figure shows a closer view of the data transfer portion of **Figure 12-1 on page 46** in order to more clearly show the Data Valid period as affected by clock jitter and clock to output delay uncertainty.
70. The delay (phase shift) from CK to PSC is controlled by the HyperBus master interface (Host) and is generally between 40 and 140 degrees in order to place the RWDS edge within the data valid window with sufficient set-up and hold time of data to RWDS. The requirements for data set-up and hold time to RWDS are determined by the HyperBus master interface design and are not addressed by the HyperBus slave timing parameters.
71. The HyperBus timing parameters of t_{CKD}, and t_{CKDI} define the beginning and end position of the data valid period. The t_{CKD} and t_{CKDI} values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.

DDR Center-Aligned Read Strobe (DCARS) Functionality

Table 12-2 DCARS Read Timing

Parameter	Symbol	200 MHZ		166 MHZ		Unit
		Min	Max	Min	Max	
Input Setup - CK/CK# setup w.r.t PSC/PSC# (edge to edge)	t_{IS}	0.5	–	0.6	–	ns
CK Half Period - Duty Cycle (edge to edge)	t_{IH}	0.5	–	0.6	–	ns
HyperRAM PSC transition to RWDS transition	$t_{PSCRWDS}$	–	5	–	6.5	ns
Time delta between CK to DQ valid and PSC to RWDS[72]	$t_{PSCRWDS} - t_{CKD}$	–1.0	+0.5	–1.0	+0.5	ns

Note
72.Sampled, not 100% tested.

13 Ordering Information

13.1 Ordering Part Number

The ordering part number is formed by a valid combination of the following:

S27KS 064 2 DP B H M 02 0

Packing Type
0 = Tray
3 = 13” Tape and Reel

Model Number (Additional Ordering Options)
02 = Standard 6 x 8 x 1.0 mm package (VAA024)
03 = DDR center-aligned Read Strobe (DCARS) 6 x 8 x 1.0 mm package (VAA024)

Temperature Range / Grade
M = Automotive, AEC-Q100 Grade 1 (–40 °C to + 125 °C)

Package Materials
H = Low-Halogen, Pb-free

Package Type
B = 24-ball FBGA, 1.00 mm pitch (5x5 ball footprint)

Speed
GA = 200 MHz
DP = 166 MHz

Device Technology
2 = 38-nm DRAM Process Technology - HyperBus
3 = 38-nm DRAM Process Technology - Octal

Density
64 = 64 Mb

Device Family
S27KS
Cypress Memory 1.8 V-only, HyperRAM Self-refresh DRAM
S27KL
Cypress Memory 3.0 V-only, HyperRAM Self-refresh DRAM

13.2 Valid Combinations — Automotive Grade / AEC-Q100

Table 13-1 list configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 13-1 Valid Combinations — Automotive Grade / AEC-Q100

Device Family	Density	Technology	Speed	Package, Material, and Temperature	Model Number	Packing Type	Ordering Part Number	Package Marking
S27KL	064	2	GA	BHM	02	0	S27KL0642GABHM020	7KL0642GAHM02
S27KL	064	2	GA	BHM	02	3	S27KL0642GABHM023	7KL0642GAHM02
S27KS	064	2	GA	BHM	02	0	S27KS0642GABHM020	7KS0642GAHM02
S27KS	064	2	GA	BHM	02	3	S27KS0642GABHM023	7KS0642GAHM02

Revision History

Document version	Date of release	Description of changes
**	2021-03-22	Initial release.

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