OPTIREG™ linear TLE4254

High accuracy low dropout voltage tracking regulator

AEC Qualified

RoHS

Features

- 70 mA output current capability
- Very tight output tracking tolerance to reference
- Output voltage adjustable down to 2.0 V
- Stable operation with 1 µF ceramic output capacitor
- Flexibility of output voltage adjust higher or lower than reference, proportional to the reference voltage (version GA / EJ A)
- Status output to indicate short circuits at the output (version GS / EJ S)
- Very low dropout voltage of typ. 0.2 V @ maximum output current
- Combined reference / enable input
- Very low current consumption in OFF mode
- Wide input voltage range -20 V ≤ V_I ≤ +45 V
- Wide temperature range: -40 °C ≤ T_j ≤ 150 °C
- Output protected against short circuit to GND and battery
- Input protected against reverse polarity
- Overtemperature protection
- Green product (RoHS compliant)



PG-DSO-8



PG-DSO-8
exposed pad

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ linear TLE4254 is a monolithic integrated low-dropout voltage tracking regulator with high accuracy in small PG-DSO-8 packages. The IC is designed to supply off-board systems, e. g. sensors in powertrain management systems under the severe conditions of automotive applications. Therefore, the IC is equipped with additional protection functions against reverse polarity and short circuit to GND and battery.

With supply voltages up to 40 V, the output voltage follows a reference voltage applied at the adjust input with very high accuracy. The reference voltage applied directly to the adjust input or by an e. g. external resistor divider can be 2.0 V at minimum.

The output is able to drive loads up to 70 mA while the device follows with high accuracy the e. g. 5 V output of a main voltage regulator acting as reference.

The TLE4254 can be set into shutdown mode in order to reduce the current consumption to a minimum. This suits the IC for low power battery applications.

Versions “GS” and “EJ S” offer an open collector status output indicating an overvoltage and undervoltage error condition of the output voltage.

Versions “GA” and “EJ A” allow setting the output voltage to higher value than the reference voltage by connecting a voltage divider to the feedback pin “FB”.

Type	Package	Marking
TLE4254GA	PG-DSO-8	4254GA
TLE4254GS	PG-DSO-8	4254GS
TLE4254EJA	PG-DSO-8 exposed pad	4254EJA
TLE4254EJS	PG-DSO-8 exposed pad	4254EJS

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1 Block diagram

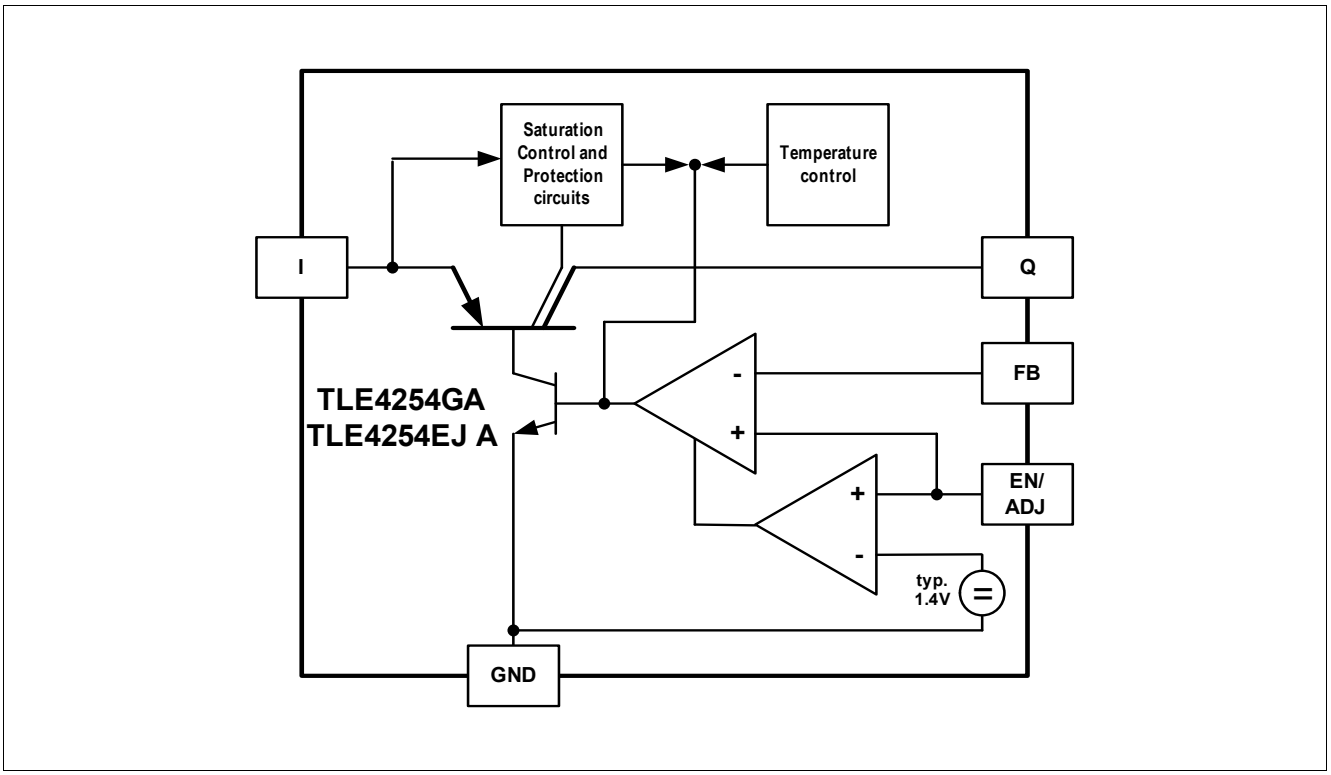


Figure 1 Block diagram TLE4254GA and TLE4254EJA

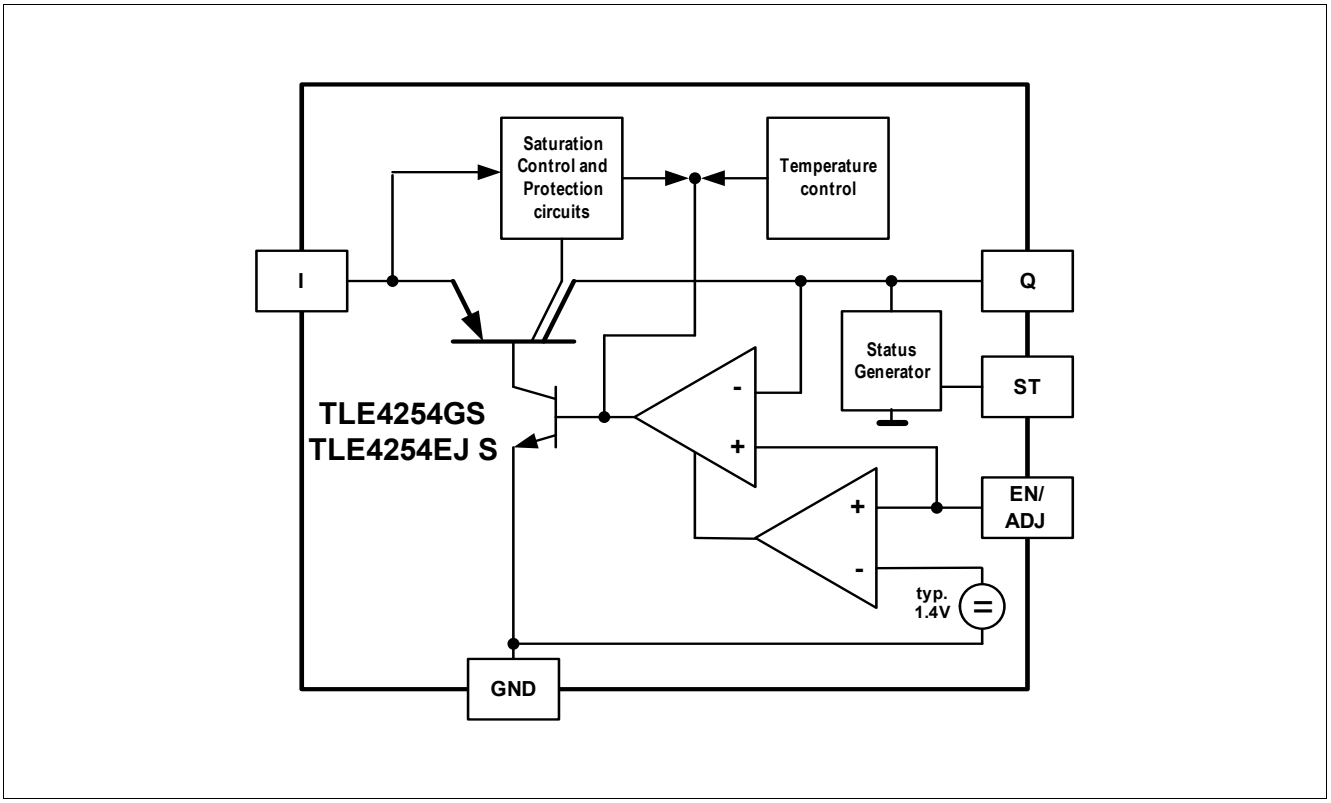


Figure 2 Block diagram TLE4254GS and TLE4254EJS

2 Pin configuration

2.1 Pin assignment TLE4254GA and TLE4254EJA

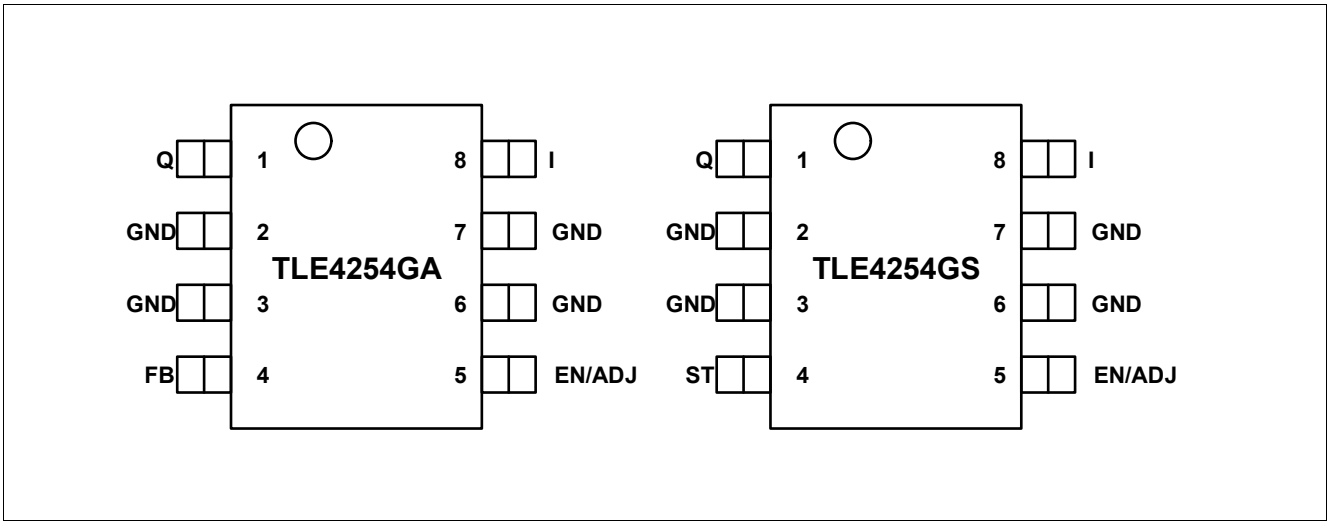


Figure 3 Pin configurations TLE4254GA and TLE4254GS

2.2 Pin definitions and functions TLE4254GA and TLE4254GS

Table 1 Pin functions TLE4254GA and TLE4254GS

Pin	Symbol	Function
1	Q	**Tracker output** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table “Functional Range”.
2, 3, 6, 7	GND	**Ground reference** Interconnect the pins on PCB. Connect to heatsink area.
4	FB (version GA)	**Feedback input (version GA only)** Inverting input of the internal error amplifier to control the output voltage. Connect this pin directly to the output pin in order to obtain lower or equal output voltages with respect to the reference voltage. Connect a voltage divider for higher output voltages than the reference. (See also **Chapter 5**.)
4	ST (version GS)	**Tracking regulator status output (version GS only)** Open collector output. Connect via a pull-up resistor to a positive voltage rail. A low signal indicates fault conditions at the regulator’s output.
5	EN/ADJ	**Adjust/enable** Connect the reference to this pin. The active high signal of the reference turns on the device; a low signal disables the IC. The reference voltage can be connected directly or by a voltage divider for lower output voltages (see **Chapter 5**).
8	I	**Input** IC supply. For compensating line influences, a capacitor close to the IC terminals is recommended.

2.3 Pin assignment TLE4254EJA and TLE4254EJS

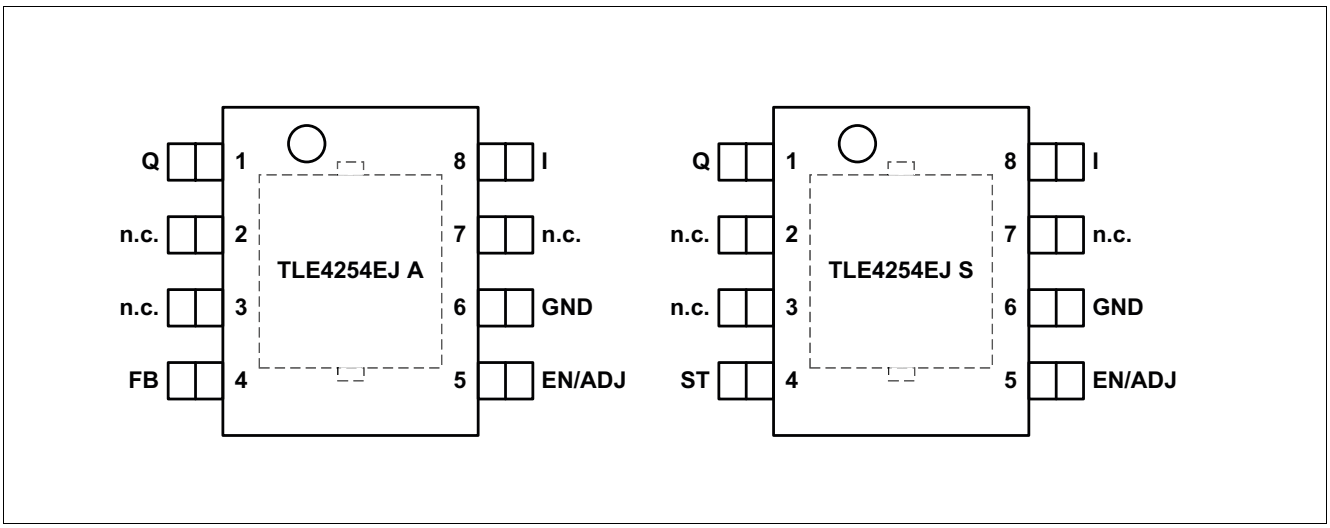


Figure 4 Pin configurations TLE4254EJA and TLE4254EJS

2.4 Pin definitions and functions TLE4254EJA and TLE4254EJS

Table 2 Pin functions TLE4254EJA and TLE4254EJS

Pin	Symbol	Function
1	Q	**Tracker output** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table “Functional Range”.
2, 3, 7	n.c.	**Not connected** Connect to GND.
4	FB (version EJA)	**Feedback input (version EJA only)** Inverting input of the internal error amplifier to control the output voltage. Connect this pin directly to the output pin in order to obtain lower or equal output voltages with respect to the reference voltage. Connect a voltage divider for higher output voltages than the reference. (See also **Chapter 5**.)
4	ST (version EJS)	**Tracking regulator status output (version EJS only)** Open collector output. Connect via a pull-up resistor to a positive voltage rail. A low signal indicates fault conditions at the regulator’s output.
5	EN/ADJ	**Adjust/enable** Connect the reference to this pin. The active high signal of the reference turns on the device; a low signal disables the IC. The reference voltage can be connected directly or by a voltage divider for lower output voltages (see **Chapter 5**).
6	GND	**Ground reference** Interconnect the pins on PCB. Connect to heatsink area.
8	I	**Input** IC supply. For compensating line influences, a capacitor close to the IC terminals is recommended.
Pad	–	**Exposed pad** Connect to GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 3 Absolute maximum ratings [1)]

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Input voltage	V_I	-20	–	45	V		P_4.1.1
Adjust/enable input voltage	$V_{ADJ/EN}$	-20	–	45	V		P_4.1.2
Output voltage	V_Q	-5	–	45	V		P_4.1.3
Feedback input voltage (version GA/EJA)	V_{FB}	-20	–	45	V		P_4.1.4
Status output voltage (version GS/EJS)	V_{ST}	-0.3	–	7	V		P_4.1.5
Temperatures							
Junction temperature	T_j	-40	–	150	°C		P_4.1.6
Storage temperature	T_{stg}	-50	–	150	°C		P_4.1.7
ESD Rating							
ESD susceptibility	$\|V_{ESD,HBM}\|$	4	–	–	kV	HBM [2)]	P_4.1.8
	$\|V_{ESD,CDM}\|$	1	–	–	kV	CDM [3)]	P_4.1.9

1) Not subject to production test, specified by design

2) ESD susceptibility Human Body Model “HBM” according to AEC-Q100-002 - JESD22-A114.

3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	4	–	45	V	$V_I \geq V_Q + V_{Dr}$	P_4.2.1
Adjust/enable input voltage (voltage tracking range)	$V_{ADJ/EN}$	2.0	–	–	V	–	P_4.2.5
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.2
Output capacitor	C_Q	1	–	–	µF	1)	P_4.2.3
	ESR_{CQ}	–	–	5	Ω	1)	P_4.2.4

1) Not subject to production test; specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PG-DSO-8							
Junction to ambient	R_{thJA}	–	155	–	K/W	Footprint only 1)2)	P_4.3.1
		–	96	–	K/W	300 mm² PCB heatsink area 1)2)	P_4.3.2
		–	86	–	K/W	600 mm² PCB heatsink area 1)2)	P_4.3.3
PG-DSO-8 exposed pad							
Junction to case	R_{thJC}	–	15	–	K/W	Measured to exposed pad	P_4.3.4
Junction to ambient	R_{thJA}	–	47	–	K/W	3)	P_4.3.5
		–	159	–	K/W	Footprint only 1)2)	P_4.3.6
		–	71	–	K/W	300 mm² PCB heatsink area 1)2)	P_4.3.7
		–	60	–	K/W	600 mm² PCB heatsink area 1)2)	P_4.3.8

1) Not subject to production test; specified by design.

2) Package mounted on PCB FR4; 80 × 80 × 1.5 mm³; 35 µm Cu, 5 µm Sn; horizontal position; zero airflow.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4 Functional description

4.1 Tracking regulator

The output voltage V_Q is controlled by comparing it to the voltage applied at pin ADJ/EN and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit and the load. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "Functional Range" have to be maintained. For details see also the typical performance graph **Output capacitor series resistor ESRCQ vs. output current IQ**. Also, the output capacitor shall be sized to buffer load transients.

An input capacitor C_I is strongly recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at high input voltages.

The overtemperature protection circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by reducing the output current. A thermal balance below 200°C junction temperature is established. Please note that a junction temperature above 150°C is outside the maximum ratings and reduces the IC lifetime.

The TLE4254 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

4.1.1 Electrical characteristics tracking regulator

Table 6 Electrical characteristics tracking regulator

V_I = 13.5 V; $V_{ADJ/EN} \geq$ 2.0 V; $V_{FB} = V_Q$ (version GA/EJA); T_j = -40°C to 150°C; C_Q = 1 µF;
all voltages with respect to ground (unless otherwise specified)

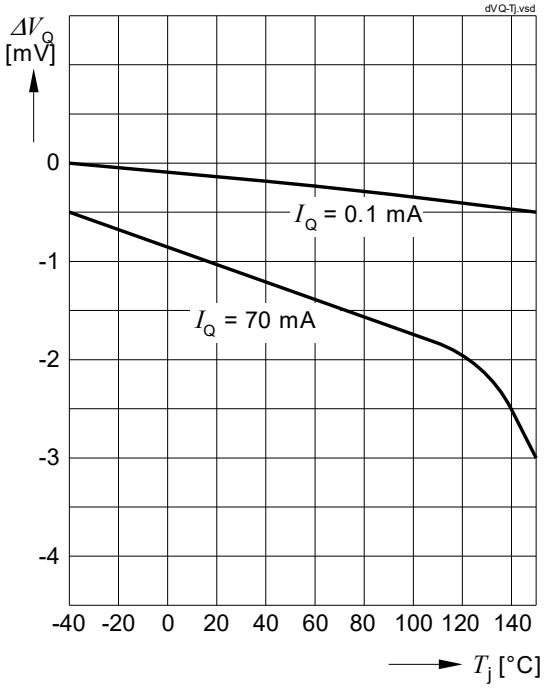
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage tracking accuracy $\Delta V_Q = V_{EN/ADJ} - V_Q$	ΔV_Q	-5	–	5	mV	8 V ≤ V_I ≤ 18 V; 0.1 mA ≤ I_Q ≤ 60 mA; $V_{ADJ/EN}$ = 5 V	P_5.1.1
		-10	–	10	mV	5.5 V ≤ V_I ≤ 26 V; 0.1 mA ≤ I_Q ≤ 60 mA; $V_{ADJ/EN}$ = 5 V	P_5.1.2
		-10	–	10	mV	5.5 V ≤ V_I ≤ 32 V; 0.1 mA ≤ I_Q ≤ 30 mA; $V_{ADJ/EN}$ = 5 V	P_5.1.3
Load regulation steady-state	$\lvert\Delta V_{Q,load}\rvert$	–	1	10	mV	I_Q = 0.1 mA to 70 mA; $V_{ADJ/EN}$ = 5 V	P_5.1.4
Line regulation steady-state	$\lvert\Delta V_{Q,line}\rvert$	–	1	10	mV	V_I = 5.5 V to 32 V; I_Q = 5 mA; $V_{ADJ/EN}$ = 5 V	P_5.1.5
Power supply ripple rejection	*PSRR*	60	–	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp; I_Q = 5 mA; C_Q = 10 µF, ceramic type [1]	P_5.1.6
Dropout voltage $V_{Dr} = V_I - V_Q$	V_{Dr}	–	200	400	mV	I_Q = 70 mA [2]	P_5.1.7
Output current limitation	$I_{Q,max}$	71	100	150	mA	$V_Q = (V_{ADJ/EN} - 0.1\ V)$; $V_{ADJ/EN}$ = 5 V	P_5.1.8
Reverse current	I_Q	-4	-2	–	mA	V_I = 0 V; V_Q = 32 V; $V_{ADJ/EN}$ = 5 V	P_5.1.9
Reverse current at negative input voltage	I_I	-5	-3	–	mA	V_I = -16 V; V_Q = 0 V; $V_{ADJ/EN}$ = 5 V	P_5.1.10
Feedback input FB (version GA/EJA only)							
Feedback input biasing current	I_{FB}	–	0.1	0.5	µA	V_{FB} = 5 V	P_5.1.11
Overtemperature protection							
Junction temperature equilibrium	$T_{j,eq}$	151	–	200	°C	T_j increasing due to power dissipation generated by the IC [1]	P_5.1.12

1) Parameter not subject to production test; specified by design.

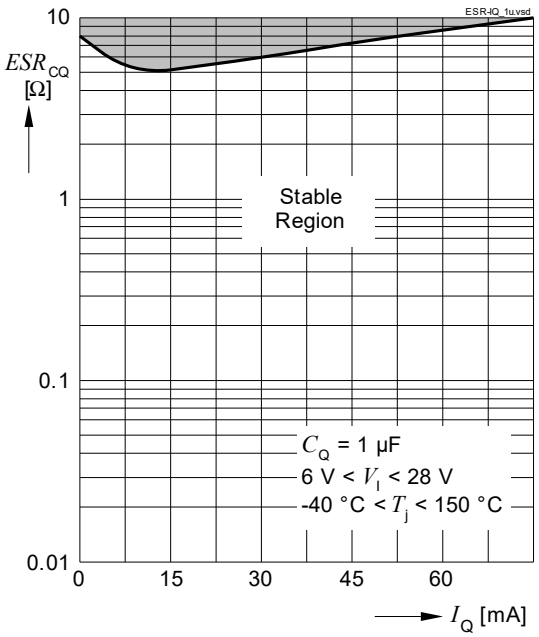
2) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

4.1.2 Typical performance characteristics tracking regulator

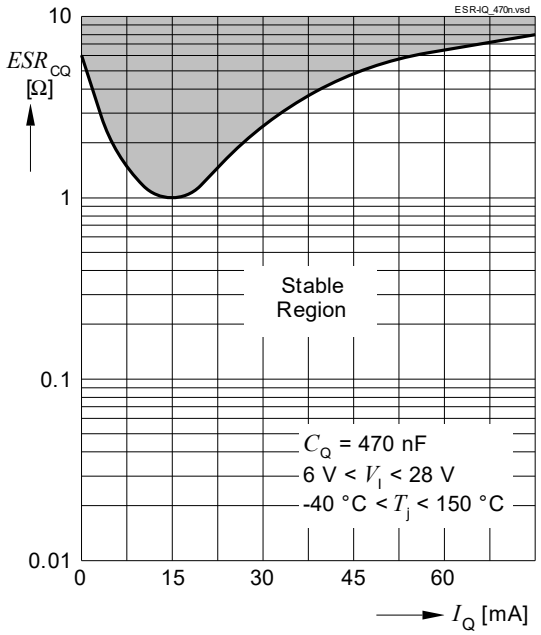
Tracking accuracy ΔV_Q vs. junction temperature T_j



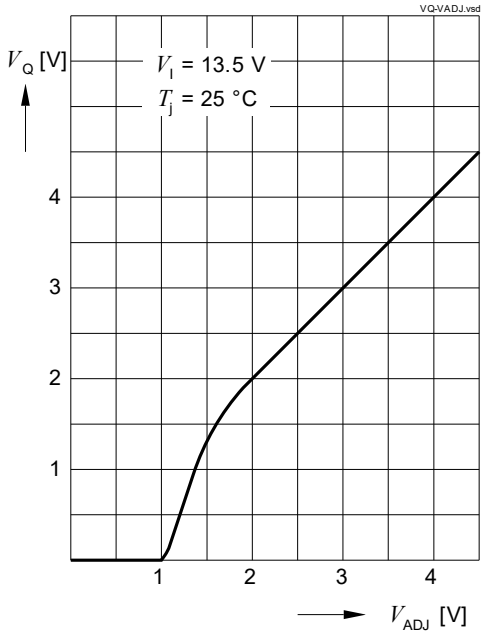
Output capacitor series resistor ESR_{CQ} vs. output current I_Q



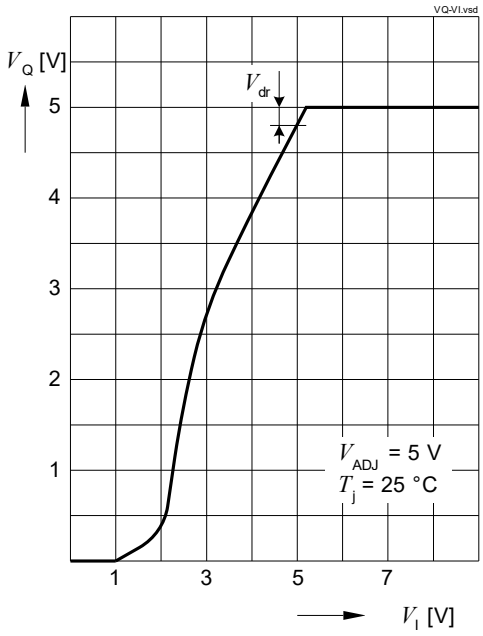
Output capacitor series resistor ESR_{CQ} vs. output current I_Q



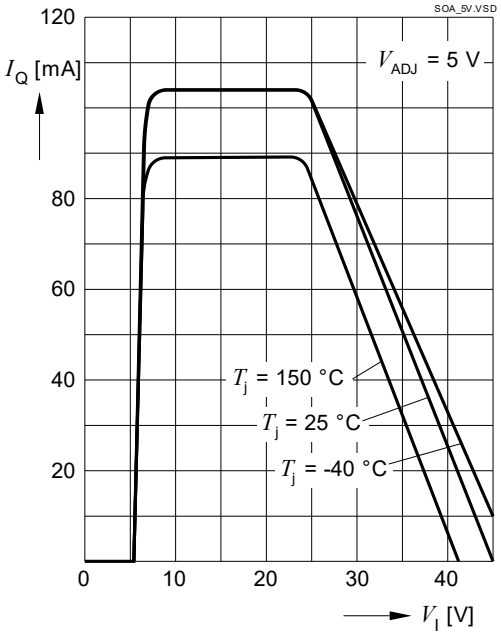
Output voltage V_Q vs. adjust voltage $V_{ADJ,EN}$



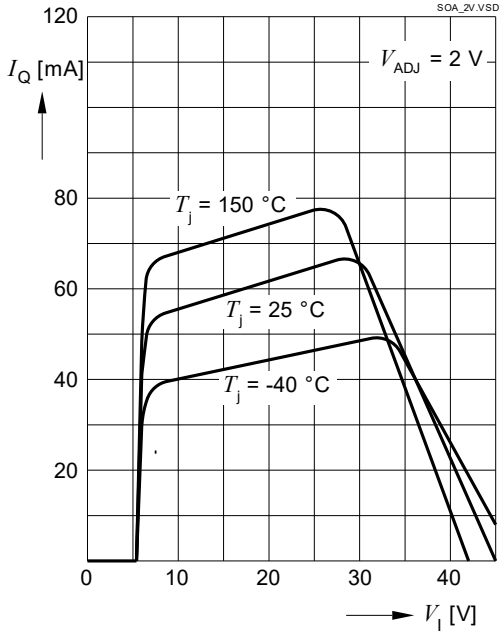
Output voltage V_Q vs. input voltage V_I



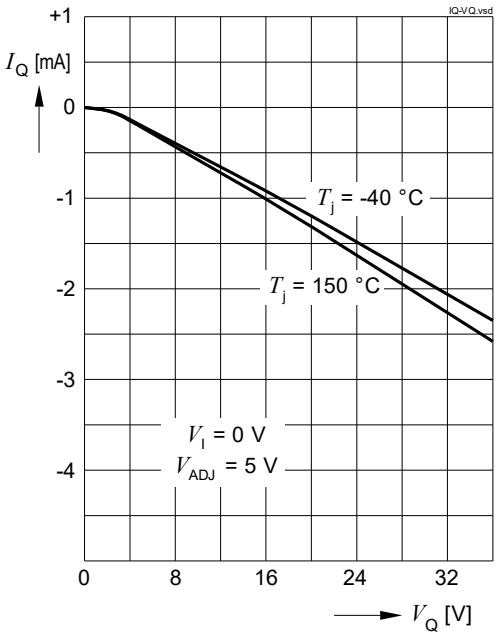
Output current limitation $I_{Q,max}$ vs. input voltage V_I, $V_{ADJ,EN}$ = 5 V



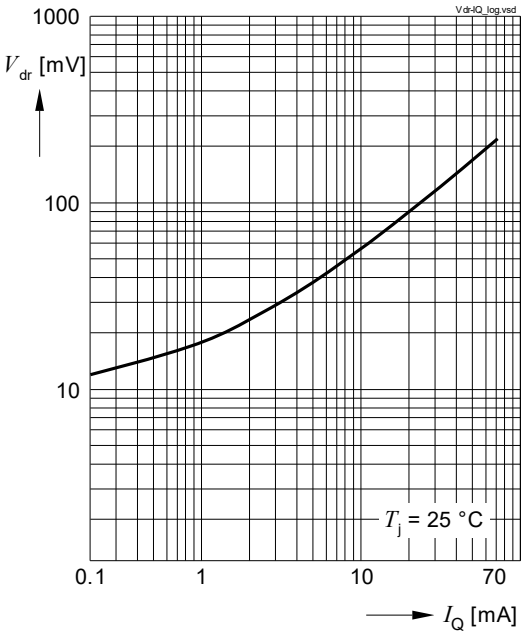
Output current limitation $I_{Q,max}$ vs. input voltage V_I, $V_{ADJ,EN}$ = 2V



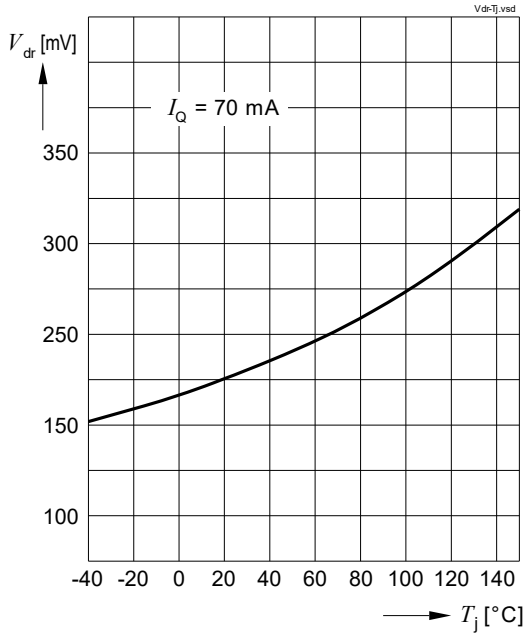
Reverse output current I_Q vs. output voltage V_Q



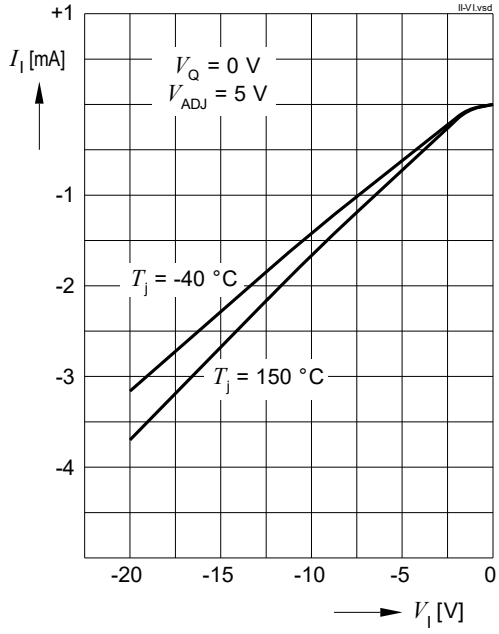
Dropout voltage V_{Dr} vs. output current I_Q



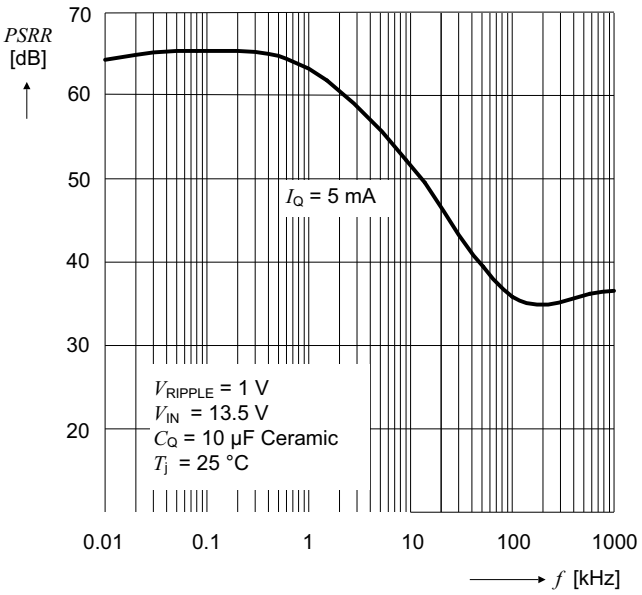
Dropout voltage V_{Dr} vs. junction temperature T_j



Reverse current I_I vs. input voltage V_I



Power supply ripple rejection *PSRR* vs. ripple frequency *f*



4.2 Current consumption

4.2.1 Electrical characteristics current consumption

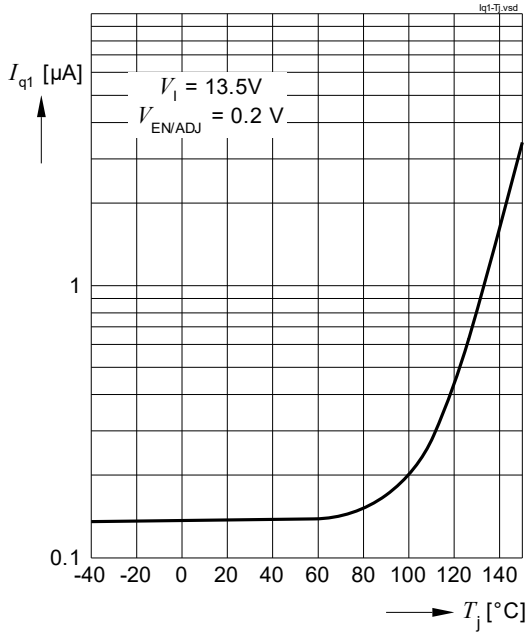
Table 7 Electrical characteristics current consumption

V_I = 13.5 V; $V_{ADJ/EN}$ ≥ 2.0 V; V_{FB} = V_Q (version GA/EJA); T_j = -40°C to 150°C; C_Q = 1 µF;
all voltages with respect to ground (unless otherwise specified)

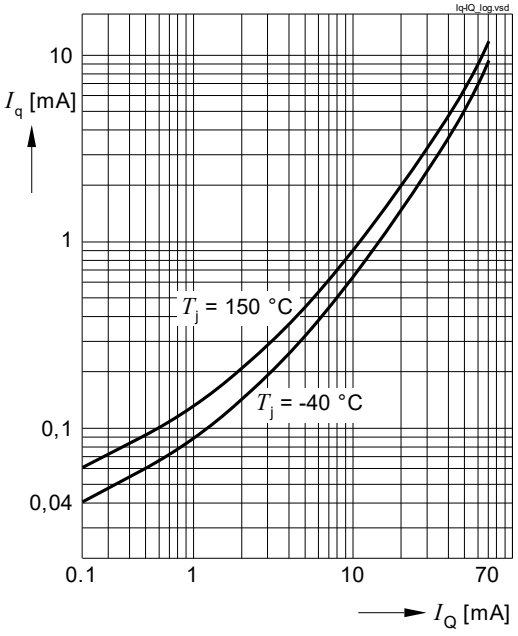
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Quiescent current stand-by mode	I_{q1}	–	1	5	µA	$V_{ADJ/EN}$ ≤ 0.4 V; T_j ≤ 125 °C	P_5.2.13
Current consumption $I_q = I_I - I_Q$	I_{q2}	–	50	80	µA	I_Q ≤ 100 µA; $V_{ADJ/EN}$ = 5 V	P_5.2.14
		–	9	15	mA	I_Q ≤ 70 mA; $V_{ADJ/EN}$ = 5 V	P_5.2.15

4.2.2 Typical performance characteristics current consumption

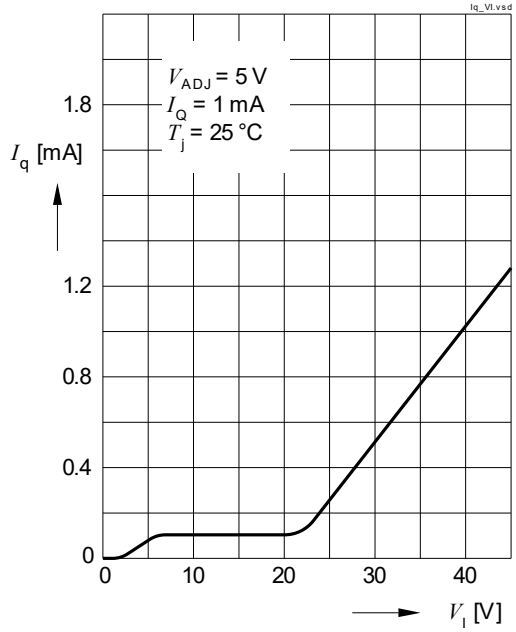
Quiescent current I_{q1} vs. junction temperature T_j



Current consumption I_{q2} vs. output current I_Q



Current consumption I_q vs. input voltage V_I



4.3 Adjust/enable input

In order to reduce the quiescent current to a minimum, the TLE4254 can be switched to stand-by mode by setting the adjust/enable input “ADJ/EN” to “low”.

In case the pin “ADJ/EN is left open, an internal pull-down resistors keeps the voltage at the pin low and therefore ensures that the regulator is switched off.

4.3.1 Electrical characteristics adjust/enable

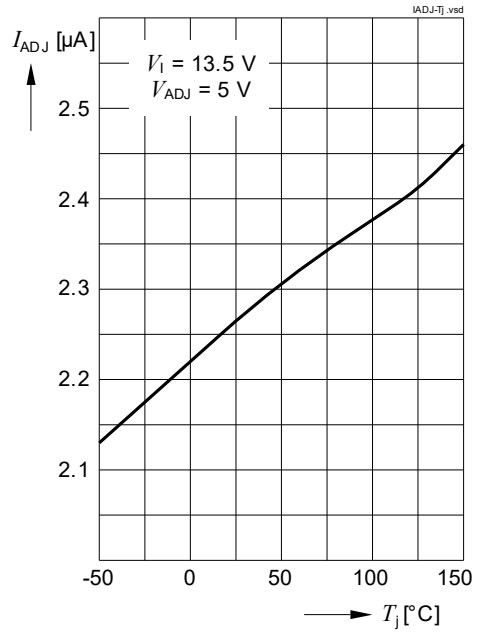
Table 8 Electrical characteristics adjust/enable

V_I = 13.5 V; $V_{ADJ/EN} \geq$ 2.0 V; $V_{FB} = V_Q$ (version GA/EJA); T_j = -40°C to 150°C; C_Q = 1 µF
all voltages with respect to ground (unless otherwise specified).

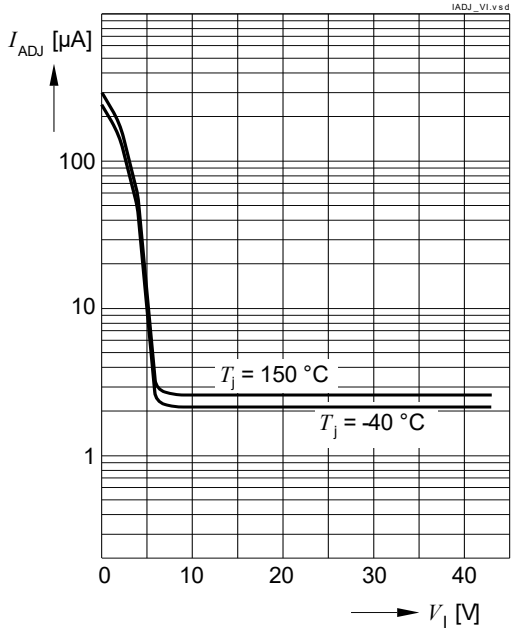
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Adjust/enable low signal valid	$V_{ADJ/EN,low}$	–	–	0.4	V	V_Q = 0 V; $I_Q \leq$ 5 µA @ $T_j \leq$ 125°C	P_5.3.16
Adjust/enable high signal valid (tracking region)	$V_{ADJ/EN,high}$	2	–	–	V	V_Q settled	P_5.3.17
Adjust/enable input current	$I_{ADJ/EN}$	–	2	3	µA	$V_{ADJ/EN}$ = 5 V	P_5.3.18
Adjust/enable input current if Input tied to GND	$I_{ADJ/EN}$	–	0.3	0.6	mA	$V_{ADJ/EN}$ = 5 V; V_I = 0 V	P_5.3.19
Adjust/enable internal pull-down resistor	$R_{ADJ/EN}$	1.7	2.5	3.3	MΩ	–	P_5.3.20

4.3.2 Typical performance characteristics adjust/enable input

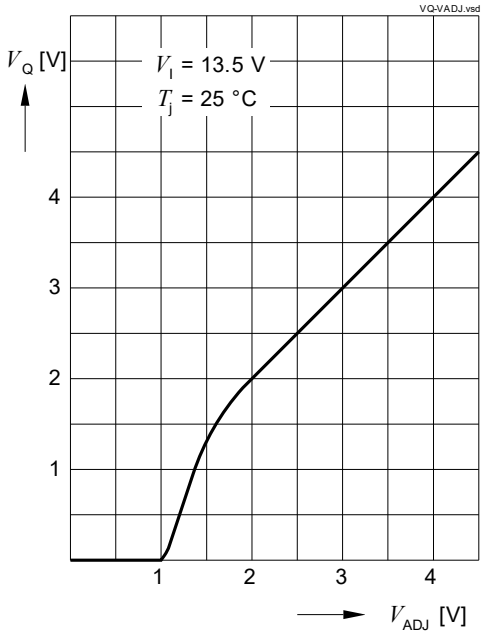
Adjust/enable input current $I_{ADJ/EN}$ vs. junction temperature T_j



Adjust/enable input current $I_{ADJ/EN}$ vs. input voltage V_I



Startup sequence V_Q vs. adjust/enable input current $V_{ADJ/EN}$



4.4 Status output (version GS/EJS only)

The status output ST indicates an overvoltage or undervoltage situation at the regulator's output Q. Therefore, the output voltage V_Q is compared to the reference voltage $V_{ADJ/EN}$. Variations of the output voltage are indicated by a low signal at the status output ST. Transients shorter than the status reaction time $t_{ST,r}$ will not trigger the status output.

The status output ST is an open collector output, requiring a pull-up resistor to a positive voltage rail.

4.4.1 Electrical characteristics status output

Table 9 Electrical characteristics status output ST (version GS/EJS only)

V_I = 13.5 V; $V_{ADJ/EN} \geq$ 2.0 V; T_j = -40°C to 150°C; C_Q = 1 µF
all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Status switching threshold, undervoltage	$V_{Q,UV}$	$V_{ADJ/EN}$ - 120	$V_{ADJ/EN}$ - 70	$V_{ADJ/EN}$ - 50	mV	V_Q decreasing	P_5.4.21
Status switching threshold, overvoltage	$V_{Q,OV}$	$V_{ADJ/EN}$ + 50	$V_{ADJ/EN}$ + 70	$V_{ADJ/EN}$ + 120	mV	V_Q increasing	P_5.4.22
Status reaction time	$t_{ST,r}$	10	15	30	µs	–	P_5.4.23
Status output low voltage	$V_{ST,low}$	–	–	0.4	V	I_{ST} = 1 mA; $V_I \geq$ 4 V	P_5.4.24
Status output sink current limitation	$I_{ST,max}$	1	–	–	mA	I_{ST} = 1 mA; V_{ST} = 0.8 V	P_5.4.25
Status output leakage current	$I_{ST,leak}$	–	0	2	µA	$V_Q = V_{ADJ/EN}$ V_{ST} = 5 V	P_5.4.26

5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The application circuits shown are simplified examples. The function must be verified in the real application.

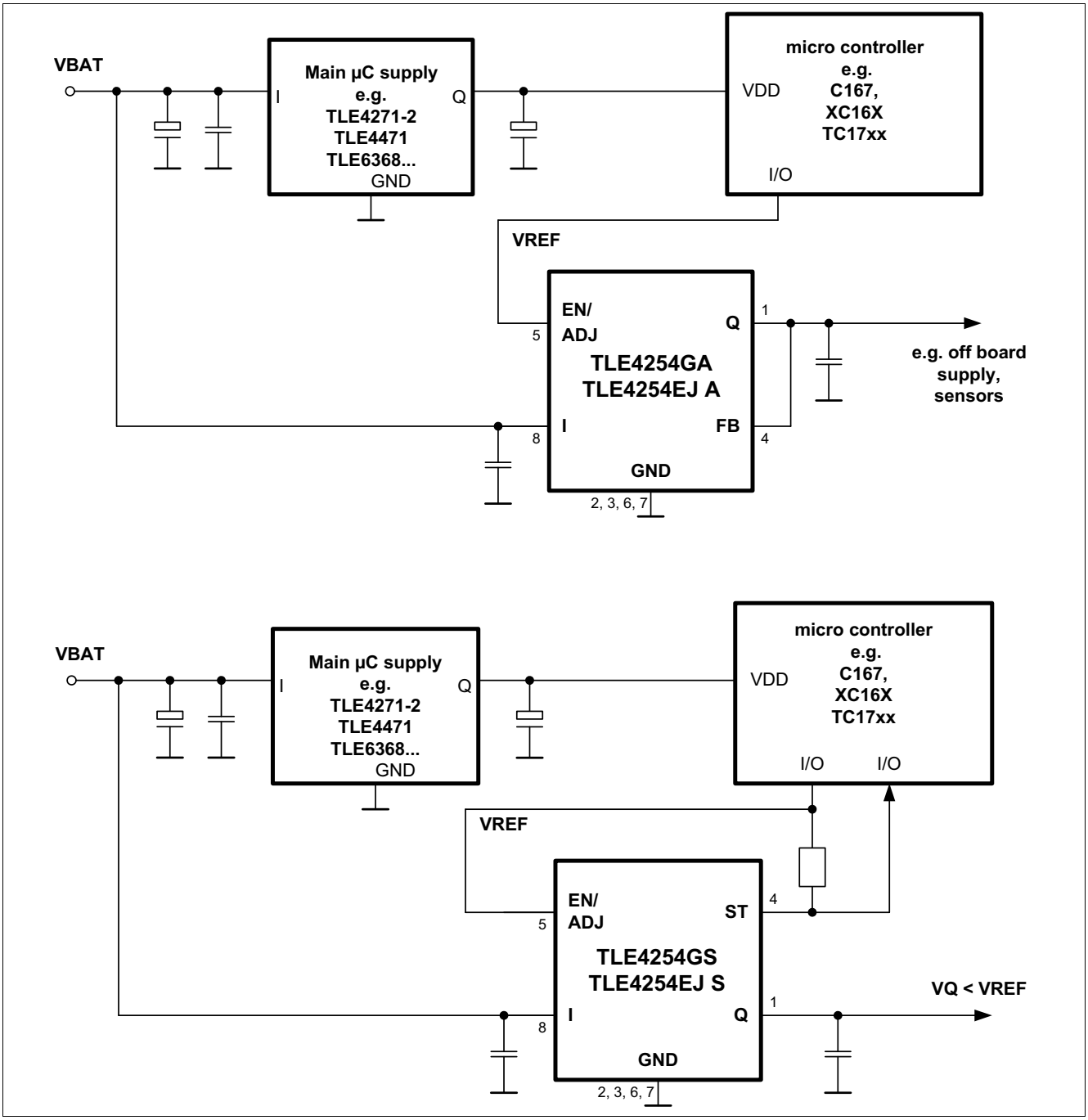


Figure 5 Application circuit: output voltage V_Q equal to reference voltage $V_{ADJ/EN}$

Figure 5 shows a typical schematic for applications where the tracker output voltage V_Q equals the reference voltage V_{REF} applied to the pin “EN/ADJ”. At version GA/EJA, the pin FB is directly connected to the output “Q”. The reference voltage is directly applied to “EN/ADJ”.

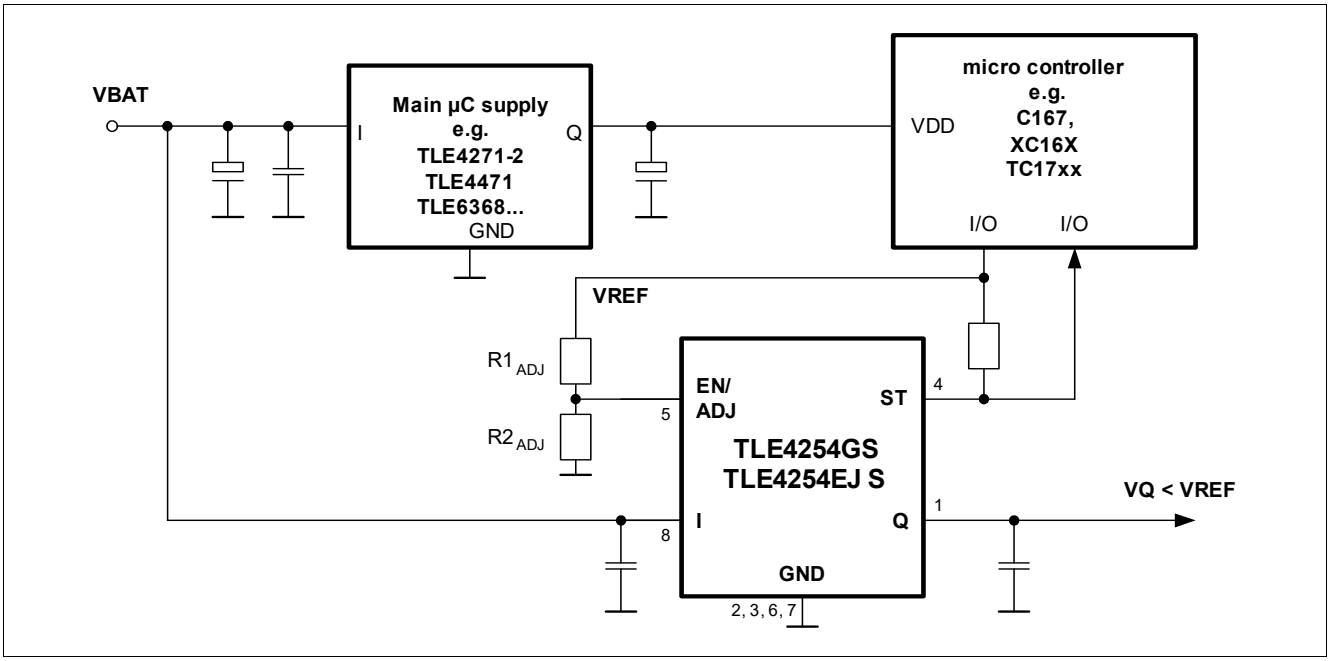


Figure 6 Application circuit: output voltage V_Q lower than reference voltage V_{REF} status output feedback to microcontroller (version GS/EJS)

In order to obtain a lower output voltage V_Q at the tracker output than the reference voltage V_{REF}, a voltage divider according to **Figure 6** has to be used. The output voltage V_Q then calculates:

(5.1)

$$V_Q = V_{REF} \cdot \left(\frac{R2_{ADJ}}{R1_{ADJ} + R2_{ADJ}} \right)$$

With a given reference voltage V_{REF}, the desired output voltage V_Q and the resistor value $R1_{ADJ}$, the resistor value for $R2_{ADJ}$ is given by:

(5.2)

$$R2_{ADJ} = R1_{ADJ} \cdot \left(\frac{V_Q}{V_{REF} - V_Q} \right)$$

Taking into consideration also the effect of the internal EN/ADJ pull-down resistor, the external resistor divider's $R2_{ADJ}$ has to be selected to:

(5.3)

$$R2_{ADJ,select} = \left(\frac{R2_{ADJ} \cdot R_{PullDown,min}}{R_{PullDown,min} - R2_{ADJ}} \right)$$

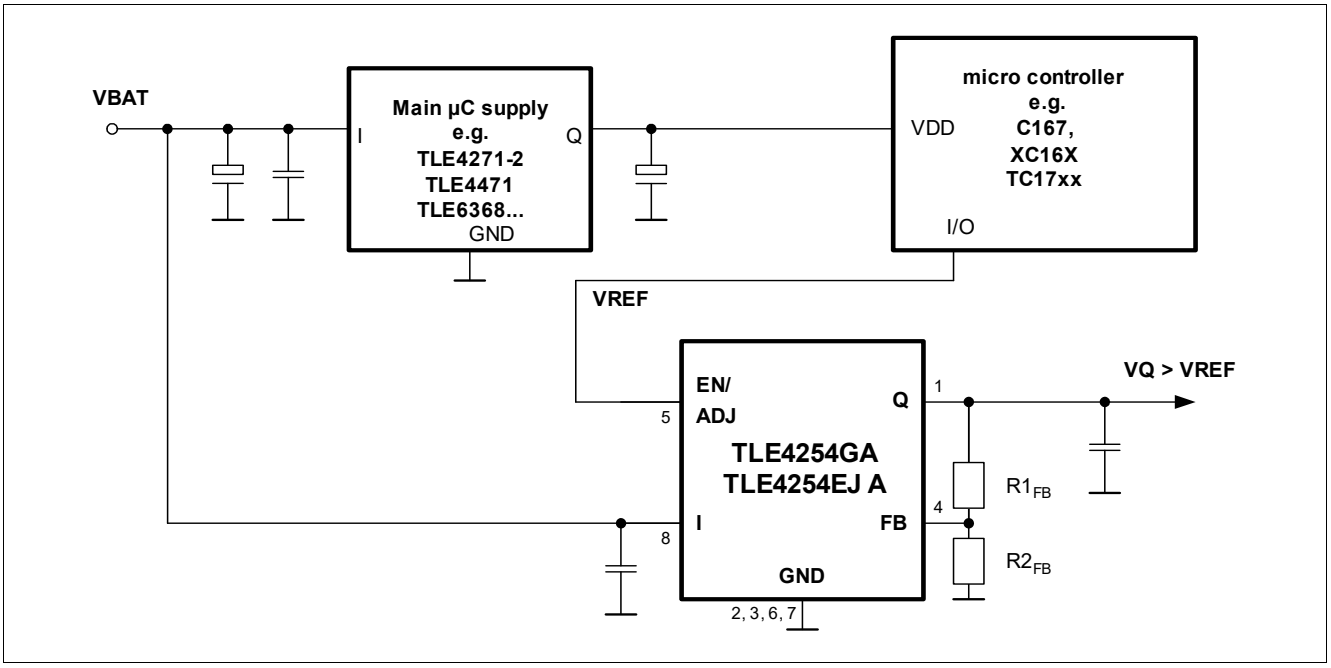


Figure 7 Application circuit: output voltage V_Q higher than reference voltage V_{REF} (version GA/EJA only)

For output voltages higher than the reference voltage, the voltage divider has to be applied between the feedback and the output according to **Figure 7**. The equation for the output voltage with respect to the reference voltage is given by:

(5.4)

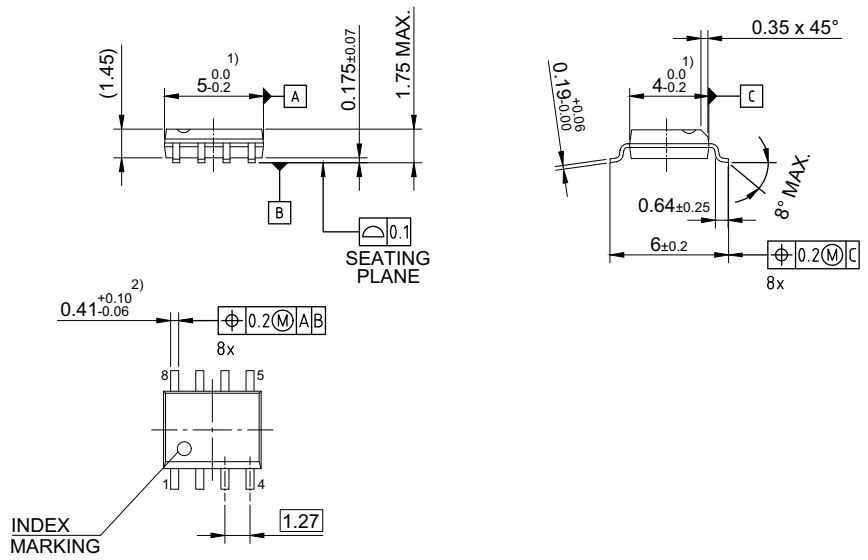
$$V_Q = V_{REF} \cdot \left(\frac{R1_{FB} + R2_{FB}}{R2_{FB}} \right)$$

Keep in mind that the input voltage has to be at minimum equal to the output voltage plus the dropout voltage of the regulator.
With a given reference voltage V_{REF}, the desired output voltage V_Q and the resistor value $R1_{FB}$, the resistor value for $R2_{FB}$ is given by:

(5.5)

$$R2_{FB} = R1_{FB} \cdot \left(\frac{V_{REF}}{V_Q - V_{REF}} \right)$$

6 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 8 Outline PG-DSO-8

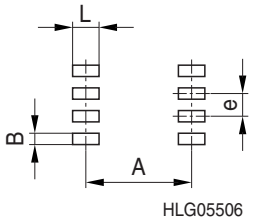


Figure 9 Footprint PG-DSO-8

Reflowing soldering dimensions:

e = 1.27

A = 5.69

L = 1.31

B = 0.65

Package information

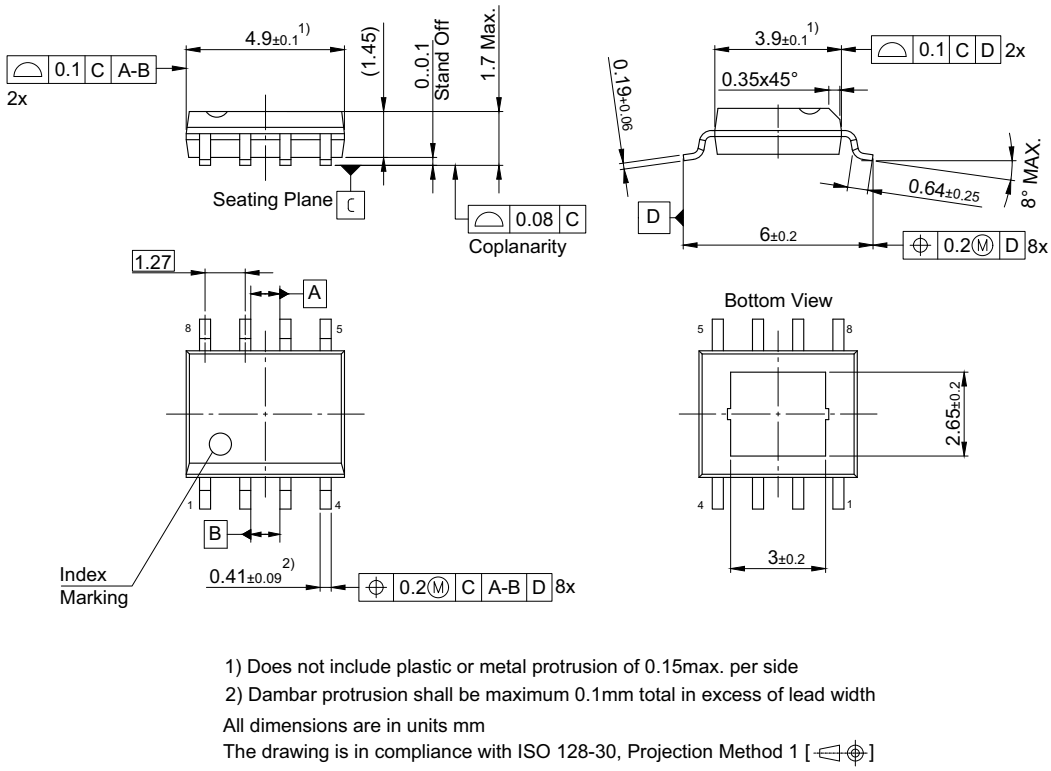


Figure 10 Outline PG-DSO-8 exposed pad

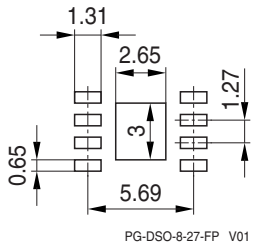


Figure 11 Footprint PG-DSO-8 exposed pad

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

7 Revision history

Revision	Date	Changes
1.3	2021-06-15	Updated layout and structure. Page 13: added PSRR graph. Editorial changes.
1.2	2009-11-18	Updated Version, product versions TLE4254EJA and TLE4254EJS in PG-DSO-8 exposed pad and all related description added.
1.1	2008-07-16	Typing errors corrected.
1.0	2006-11-22	Package outlines drawing updated.

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