TLE7181EM

H-Bridge and Dual Half Bridge Driver IC

AEC Qualified

RoHS



Features

- PWM/DIR-interface drives 4 N-Channel Power MOSFETs
- Unlimited D.C. switch on time of low and high-side MOSFETs
- 0 … 95% at 20 kHz & 100% duty cycle of high-side MOSFETs
- 0 … 100% duty cycle of low-side MOSFETs
- Additional output to drive a reverse polarity protection N-MOSFET
- Current sense OPAMP
- Low quiescent current mode
- Internal shoot through protection
- Adjustable dead time
- 1-bit diagnosis / $\overline{\text{ERR}}$
- Overcurrent warning based on current sense OPAMP with fixed warning level
- Analog adjustable short circuit protection levels via SCDL pin with open pin detection
- Overtemperature warning
- Overvoltage warning
- Undervoltage warning and shutdown
- Green Product (RoHS compliant)
- AEC Qualified

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

Typical applications are fans, pumps and electric power steering. The TLE7181EM is designed for a 12 V power net.

Table 1 Product summary

Parameter	Symbol	Values
Specified operating voltage	V_{SOP}	7.0 V … 34 V
Junction temperature	T_j	-40°C … 150°C
Maximum output source resistance	R_{Sou}	13.5 Ω
Maximum output sink resistance	R_{Sink}	9 Ω
Maximum quiescent current[1)]	I_{QVS}	8 µA

1) Typical value at T_j = 25°C

Type	Package	Marking
TLE7181EM	PG-SSOP-24	TLE7181EM

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1 Block diagram

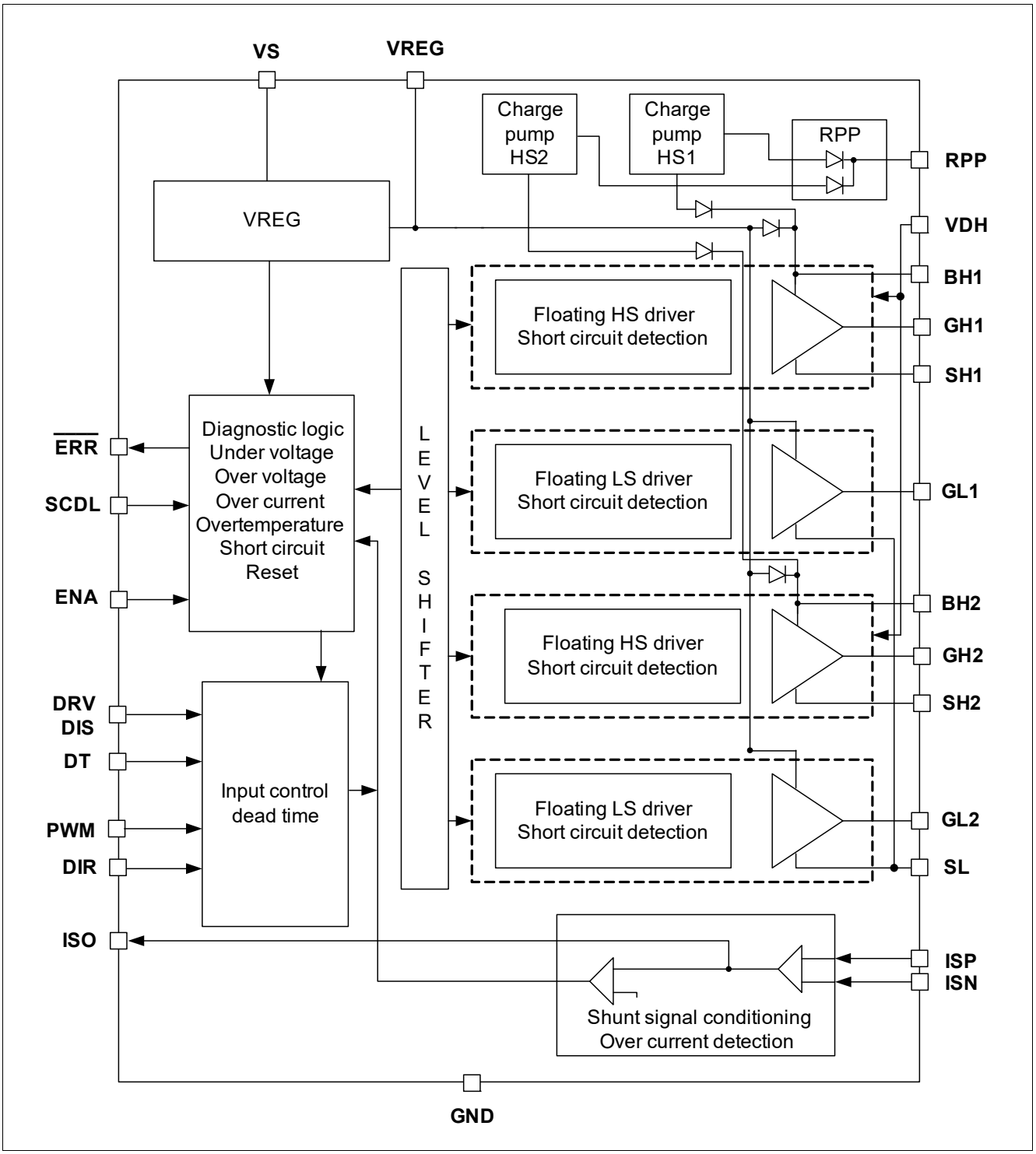


Figure 1 Block diagram TLE7181EM

2 Pin configuration

2.1 Pin assignment

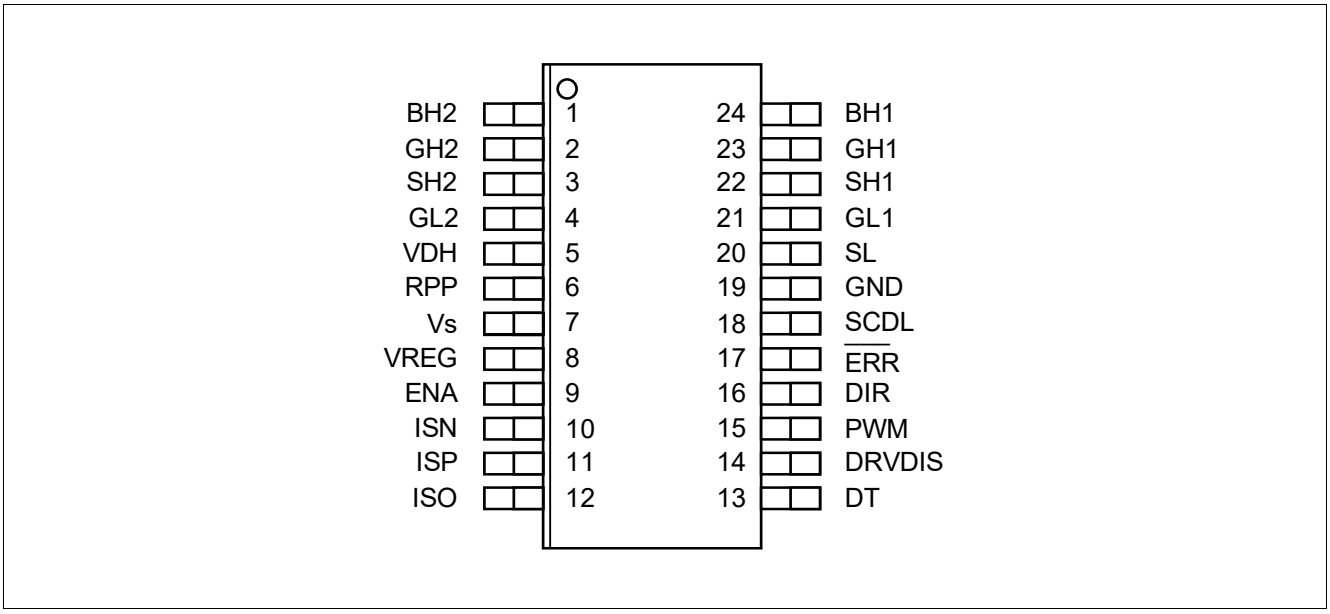


Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 2 Pin definitions and functions

Pin No.	Symbol	Function
1	BH2	Pin for + terminal of the bootstrap capacitor of phase 2
2	GH2	Output pin for gate of high-side MOSFET 2
3	SH2	Pin for source connection of high-side MOSFET 2
4	GL2	Output pin for gate of low-side MOSFET 2
5	VDH	Voltage input common drain high side for short circuit detection
6	RPP	Charge pump output for reverse polarity protection of the motor bridge
7	VS	Pin for supply voltage
8	VREG	Output of supply for driver output stage - connect to a capacitor
9	ENA	Input pin for reset of $\overline{\text{ERR}}$ registers, active switch off of external MOSFETs and low quiescent current mode, set HIGH to enable operation
10	ISN	Input for OPAMP - terminal
11	ISP	Input for OPAMP + terminal
12	ISO	Output of OPAMP
13	DT	Input for adjustable dead time function, connect to GND via resistor
14	DRVDIS	Disable DIR/PWM interface & all output stages switched off
15	PWM	Control input for PWM frequency and duty cycle

Pin configuration

Table 2 Pin definitions and functions (cont'd)

Pin No.	Symbol	Function
16	DIR	Control input for spinning direction of the motor
17	$\overline{\text{ERR}}$	Push pull output stage
18	SCDL	Input pin for adjustable short circuit detection function
19	GND	Ground pin
20	SL	Pin for common source of low-side MOSFETs
21	GL1	Output pin for gate of low-side MOSFET 1
22	SH1	Pin for source connection of high-side MOSFET 1
23	GH1	Output pin for gate of high-side MOSFET 1
24	BH1	Pin for + terminal of the bootstrap capacitor of phase 1
Tab	Tab	Should be connected to GND

3 General product characteristics

3.1 Absolute maximum ratings

Table 3 Absolute maximum ratings [1)]

40°C ≤ T_j ≤ 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage at VS	V_{VS}	-0.3	–	45	V	–	P_4.1.1
Supply voltage at VS	V_{VSRP}	-4.0	–	45	V	R_{VS} ≥ 10 Ω	P_4.1.2
Voltage range at VDH	V_{VDH}	-0.3	–	55	V	–	P_4.1.3
Voltage range at RPP	V_{RPP}	-0.3	–	55	V	–	P_4.1.4
maximum current at RPP	I_{RPP}	-2.5	–	2.5	mA	–	P_4.1.5
Voltage range at ENA	V_{ENA}	-0.3	–	45	V	–	P_4.1.6
Voltage range at SCDL	V_{SCDL}	-0.3	–	6	V	–	P_4.1.7
Voltage range at PWM, DIR, DT, DRVDIS	V_{DPI}	-0.3		6	V	–	P_4.1.8
Voltage range at $\overline{ERR}$, ISO	V_{DPO}	-0.3	–	6	V	–	P_4.1.9
Voltage range at ISP, ISN	V_{OPI}	-5.0	–	5.0	V	–	P_4.1.10
Voltage range at VREG	V_{VREG}	-0.3	–	15	V	–	P_4.1.11
Voltage range at BHx	V_{BH}	-0.3	–	55	V	–	P_4.1.12
Voltage range at GHx	V_{GH}	-0.3	–	55	V	–	P_4.1.13
Voltage range at GHx	V_{GHP}	-7.0	–	55	V	t_P < 1 µs; f = 50 kHz	P_4.1.14
Voltage range at SHx	V_{SH}	-2.0	–	45	V	–	P_4.1.15
Voltage range at SHx	V_{SHP}	-7.0	–	45	V	t_P < 1 µs; f = 50 kHz	P_4.1.16
Voltage range at GLx	V_{GL}	-0.3	–	18	V	–	P_4.1.17
Voltage range at GLx	V_{GLP}	-7.0	–	18	V	t_P < 0.5 µs; f = 50 kHz	P_4.1.18
Voltage range at SL	V_{SL}	-1.0	–	5.0	V	–	P_4.1.19
Voltage range at SL	V_{SLP}	-7.0	–	5.0	V	t_P < 0.5 µs; f = 50 kHz; C_{BS} ≥ 330 nF	P_4.1.20
Voltage difference Gxx-Sxx	V_{GS}	-0.3	–	15	V	–	P_4.1.21
Voltage difference BHx-SHx	V_{BS}	-0.3	–	15	V	–	P_4.1.22
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.23

Table 3 Absolute maximum ratings (cont'd)[1)]

40°C ≤ T_j ≤ 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.24
Lead soldering temperature (1/16'' from body)	T_{sol}	–	–	260	°C	–	P_4.1.25
Peak reflow soldering temperature[2)]	T_{ref}	–	–	260	°C	–	P_4.1.26
Power dissipation							
Power dissipation (DC)	P_{tot}	–	–	2	W	–	P_4.1.27
ESD susceptibility							
ESD resistivity[3)]	V_{ESD}	–	–	2	kV	–	P_4.1.28
CDM	V_{CDM}	–	–	1	kV	–	P_4.1.29

1) Not subject to production test, specified by design.
2) Reflow profile IPC/JEDEC J-STD-020C.
3) ESD susceptibility HBM according to EIA/JESD 22-A 114B.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Specified supply voltage range	V_{VS1}	7.0	–	34	V	–	P_4.2.1
Supply voltage range[1)]	V_{VS2}	5.5	–	45	V	V_{VS} < 7 V reduced functionality	P_4.2.2
Quiescent current at VS	I_{QVS1}	–	–	8	µA	V_{VS}, V_{VDH} = 12 V; ENA = Low; T_j = 25°C	P_4.2.3
Quiescent current at VS	I_{QVS2}	–	–	10	µA	V_{VS}, V_{VDH} < 15 V; ENA = Low; T_j ≤ 85°C	P_4.2.4
Quiescent current at VDH	I_{QVDH1}	–	–	8	µA	V_{VS}, V_{VDH} = 12 V; ENA = Low; T_j = 25°C	P_4.2.5
Quiescent current at VDH	I_{QVDH2}	–	–	10	µA	V_{VS}, V_{VDH} < 15 V; ENA = Low; T_j ≤ 85°C	P_4.2.6
Supply current at Vs (device enabled)[2)]	$I_{Vs(1)}$	–	–	22	mA	No switching	P_4.2.7

Table 4 Functional range (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply current at Vs (device enabled)	$I_{Vs(2)}$	–	–	45	mA	$4 \times Q_{GS} \times f_{PWM} \leq 20mA$; $V_{VS} = 7.0 \ldots 34$ V	P_4.2.8
D.C. switch on time of output stages	D_{DC}	–	–	∞	s	–	P_4.2.9
Duty cycle high-side output stage[3)]	D_{HS}	0	–	95	%	f_{PWM} = 20 kHz; continuous operation; $C_{BS} \geq 330$ nF	P_4.2.10
Duty cycle low-side output stage	D_{LS}	0	–	100	%	–	P_4.2.11

1) Operation above 34 V limited by max. allowed power dissipation and max. ratings.
2) Current can be higher, if driver output stages are unsupplied.
3) Max. limit of D.C. will increase, if f_{PWM} or external gate charge of the MOSFETs is reduced.

The PWM frequency is limited by thermal constraints and the maximum duty cycle (minimum charging time of bootstrap capacitor).

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case[1)]	R_{thJC}	–	–	5	K/W	–	P_4.3.1
Junction to ambient[1)]	R_{thJA}	–	35	–	K/W	2)	P_4.3.2

1) Not subject to production test, specified by design.
2) **Exposed Heatslug Package use this sentence**: Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3.3.1 Default state of inputs

Table 6 Default state of inputs (if left open)

Characteristic	State	Remark
Default state of PWM and DIR	Low	Low-side MOSFETs off and high-side MOSFETs on
Default state of DT	OPEN	Maximum deadtime
Default state of ENA	Low	Output stages disabled device in sleep mode
Default state of SCDL	OPEN	Short circuit detection deactivation & warning
Default state of DRVDIS	High	All output stages off & no error will be reported

4 Description and electrical characteristics

4.1 MOSFET driver

4.1.1 Driving MOSFET output stages

The TLE7181EM incorporates 2 high-side and low-side output stages for 4 external MOSFETs.

The 4 MOSFET output stages will be driven by the PWM/DIR interface. With the PWM/DIR interface only 2 inputs pins are necessary to drive a typical H-bridge topology for a DC-brush motor. The rotation direction of the motor can be chosen with the input pin DIR. The speed of the motor can is controlled by applying a PWM-signal at pin PWM.

The DRVDIS pin allows to switch off all 4 MOSFETs. **Table 7** provides an overview of the different states with this interface.

Table 7 PWM/DIR interface normal operation

DIR	DRVDIS	PWM	High-side switch1	Low-side switch1	High-side switch2	Low-side switch2
0	0	0	ON	OFF	ON	OFF
0	0	1	ON	OFF	OFF	ON
0	1	0	ON	OFF	ON	OFF
0	1	1	OFF	ON	ON	OFF
1	x	x	OFF	OFF	OFF	OFF

4.1.2 MOSFET output stages

The four push-pull MOSFET driver stages of the TLE7181EM are implemented as separate floating blocks. This means that the output stage is follows the individual MOSFET source voltages and so ensuring stable MOSFET driving even in harsh electrical environment.

All 4 output stages have the same output power and thanks to the used bootstrap principle they can be switched all up to high frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see **Chapter 4.3.2**.

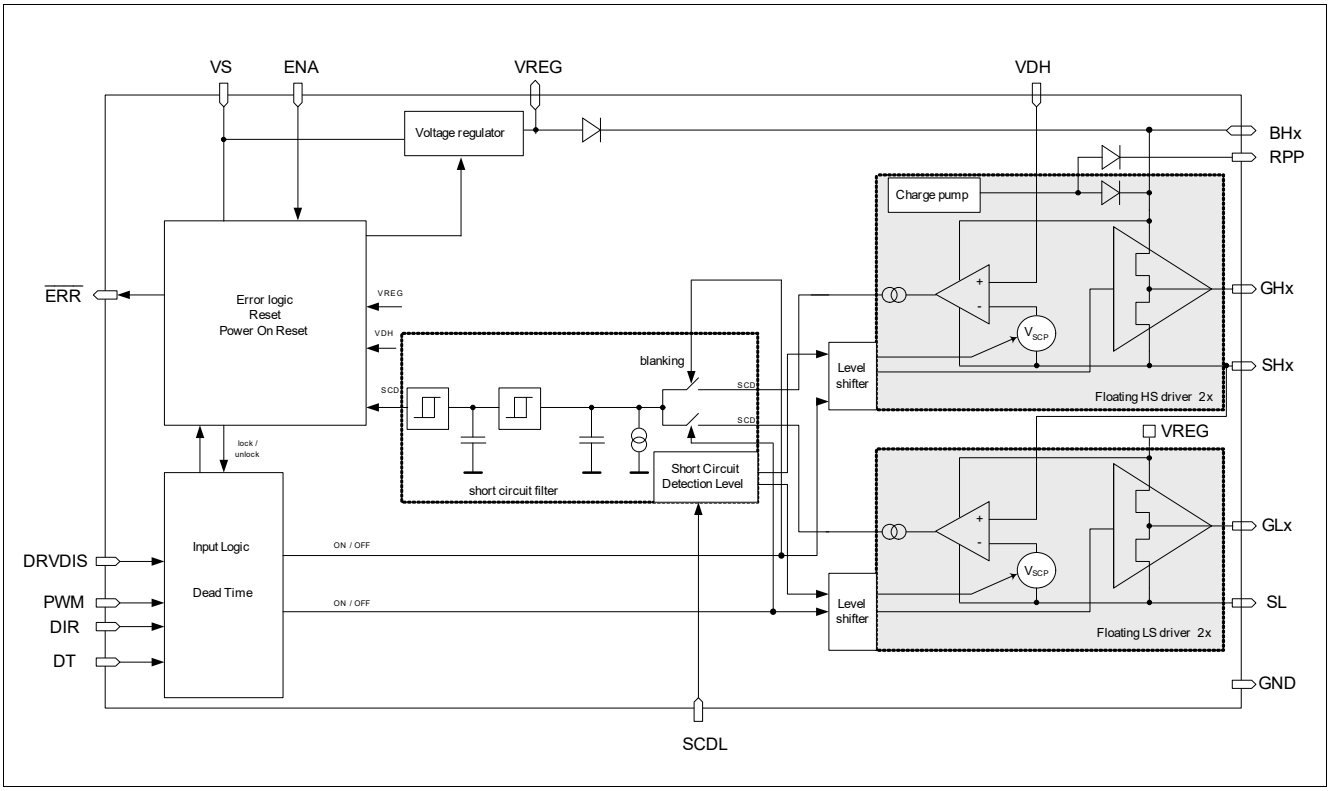


Figure 3 Block diagram of driver stages including short circuit detection

4.1.3 Dead time

In bridge applications it has to be assured that the external high-side and low-side MOSFETs are not “on” at the same time, connecting directly the battery voltage to GND. The dead time generated in the TLE7181EM can be programmed by applying an resistor between the DT pin and GND. Higher external resistor values lead to higher dead time.

A minimum dead time applied, if the DT pin is connected to GND.

The typical dead time can be calculated with the following formula:

(4.1)

$$t_{deadtime}[\mu s] = \frac{0.081}{0.02 + {}^{2.4}\!/\!_{4+Rdt[k\Omega]}}$$

If an exact dead time of the bridge is needed, the use of the µC PWM generation unit is recommended.

4.1.4 Bootstrap principle

The TLE7181EM provides a bootstrap based supply for its high-side output stages.

The bootstrap capacitors are charged by switching on the external low-side MOSFETs, connecting the bootstrap capacitor to GND. Under this condition the bootstrap capacitor will be charged from the VREG capacitor via the integrated bootstrap diode. If the low-side MOSFET is switched off and the high-side MOSFET is switched on, the bootstrap capacitor will float together with the SHx voltage to the supply voltage of the bridge. Under this condition the supply current of the high-side output stage will discharge the bootstrap capacitor. This current is specified. The size of the capacitor together with this current will determine how long the high-side MOSFET can be kept on without recharging the bootstrap capacitor.

4.1.5 100% D.C. charge pumps

100% D.C. charge pumps are implemented for each high-side output stage. Therefore the high-side output stages can be switch on for an unlimited time. These integrated charge pumps can handle leakage currents which will be caused by external MOSFETs and the TLE7181EM itself. They are not strong enough to drive a 99% duty cycle for a longer time. The charge pumps are running when the driver is not in sleep mode and assure that the bootstrap capacitors are charged as long as the user does not apply critical duty cycle for a longer time.

4.1.6 Reverse polarity protection of motor bridge

The TLE7181EM provides an additional RPP pin to protect motor bridge for reverse polarity. This RPP pin can drive an additional external N-channel power MOSFET designed in between battery and the motor bridge. The RPP pin is internally supplied by the two integrated 100% D.C. charge pumps. They are especially designed to handle additional current which is needed to drive a the gate charge of the reverse polarity MOSFET. The guaranteed output current of the charge pumps is specified.

4.1.7 Sleep mode

If ENA pin is set to low, the ERR flag will be set to low and the output stages will be switched off.

After ENA pin is kept low for t_{LQM} the sleep mode of the Driver IC will be activated.

In sleep mode the entire chip is deactivated. This means the internal supply structure of the TLE7181EM will be switched off. This mode is designed for lowest current consumption from the power net of the car. The passive clamping is active. For details see the description of passive clamping in **Chapter 4.3.8**.

The TLE7181EM will wake up if ENA is set to high.The ENA pin is 45 V compatible, so ENA can be directly be connected to the ignition key signal KL15.

4.1.8 Wake up

A special start up procedure is implemented into the TLE7181EM to guarantee charged bootstrap capacitors.

This start up procedure is performed before the normal H-bridge motor control with PWM/DIR is possible.

If the ENA pin is set to high, the VREG voltage starts to increase. As soon as the under voltage threshold VREG_UV is reached, both low-side output stages will be switched on for a short period of time for fast charging of the bootstrap capacitors. When the bootstrap capacitor voltage is high enough the start up procedure is completed and the low-side MOSFETs will be driven according the input pattern.

During wake up procedure the ERR signal is set to low. It will be set to high if no error occurs at the TLE7181EM and start up procedure is completed.

If the TLE7181EM wakes up with a chip temperature between $T_{j(PW)}$ - $dT_{j(OW)}$ and $T_{j(PW)}$, it may happen that the overtemperature warning is set. Toggling the enable pin will not remove the warning.

To assure that the driver is finally in normal mode, V_S has to be greater than V_{S_Start} and it is necessary to perform a dedicated wake-up procedure:

1. Keep DRVDIS and ENA low in sleep mode.
2. Set ENA high to trigger start up.
3. Wait t_{toggle}.
4. Set DRVDIS pin to high.
5. Wait t_{toggle}.
6. Set DRVDIS pin to low.
7. Wait 100 µs.

8. Check if $\overline{\text{ERR}}$ pin is set to high (start up procedure completed).
9. If $\overline{\text{ERR}}$ pin is still low, repeat once step 3 to 8.

After that procedure the output stages can be driven by PWM/DIR interface.

4.2 Electrical characteristics

Table 8 Electrical characteristics MOSFET drivers

V_S = 7.0 to 34 V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Control inputs							
Low level input voltage of PWM; DIR	V_{I_LL}	–	–	1.0	V	–	P_5.1.1
High level input voltage of PWM; DIR	V_{I_HL}	2.0	–	–	V	–	P_5.1.2
Input hysteresis of PWM; DIR	d_{VI}	100	200	–	mV	–	P_5.1.3
PWM; DIR pull-down resistors to GND	R_{IL}	20	–	50	kΩ	–	P_5.1.4
Low level input voltage of ENA	V_{E_LL}	–	–	0.75	V	–	P_5.1.5
High level input voltage of ENA	V_{E_HL}	2.1	–	–	V	–	P_5.1.6
Input hysteresis of ENA	d_{VE}	50	200	–	mV	–	P_5.1.7
ENA pull-down resistor to GND	R_{IL}	70	125	200	kΩ	–	P_5.1.8
Low level input voltage of DRVDIS	V_{D_LL}	–	–	1.0	V	–	P_5.1.9
High level input voltage of DRVDIS	V_{D_HL}	2.0	–	–	V	–	P_5.1.10
Input hysteresis of DRVDIS	d_{VD}	100	200	–	mV	–	P_5.1.11
DRVDIS pull-up resistor to internal supply	R_{DH}	30	50	80	kΩ	–	P_5.1.12
MOSFET driver output							
Output source resistance	R_{Sou}	2	–	13.5	Ω	I_{Load} = -20 mA	P_5.1.13
Output sink resistance	R_{Sink}	2	–	9.0	Ω	I_{Load} = 20 mA	P_5.1.14
High level output voltage Gxx vs. Sxx	V_{Gxx1}	–	11	15	V	13.5 V ≤ V_{VS} ≤ 34 V; I_{Load} = 0 mA	P_5.1.15
High level output voltage Gxx vs. Sxx	V_{Gxx2}	–	11	13.5	V	13.5 V ≤ V_{VS} ≤ 34 V; C_{Load} = 20 nF; D.C. = 50%; f_{PWM} = 20 kHz	P_5.1.16
High level output voltage GHx vs. SHx[1)]	V_{GHx3}	–	V_{VS} - 1.5	–	V	7.0 V < V_{VS} < 13.5 V; C_{Load} = 20 nF; D.C. = 50%; f_{PWM} = 20 kHz	P_5.1.17

Table 8 Electrical characteristics MOSFET drivers

V_S = 7.0 to 34 V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High level output voltage GLx vs. GND[1)]	V_{GLx3}	–	V_{VS} - 0.5	–	V	7.0 V < V_{VS} < 13.5 V; C_{Load} = 20 nF; f_{PWM}=20 kHz & D.C. = 50%; or D.C = 100%	P_5.1.18
High level output voltage GHx vs. SHx[1)2)]	V_{GHx4}	5.0 +V_{diode}	–	–	V	V_{VS} = 7.0 V; C_{Load} = 20 nF; D.C. = 95%; f_{PWM} = 20 kHz; passive freewheeling	P_5.1.19
High level output voltage GHx vs. SHx[1)]	V_{GHx5}	5.0	–	–	V	V_{VS} = 7.0 V; C_{Load} = 20 nF; D.C. = 95%; f_{PWM} = 20 kHz	P_5.1.20
High level output voltage GLx vs. SLx[1)]	V_{GLx5}	6.0	–	–	V	V_{VS} = 7.0 V; C_{Load} = 20 nF; D.C. = 95%; f_{PWM} = 20kHz	P_5.1.21
High level output voltage GHx vs. SHx[1)]	V_{GHx5}	10	–	–	V	7.0 V ≤ V_{VS} ≤ 13.5 V; C_{Load} = 20 nF; D.C. = 100%	P_5.1.22
High level output voltage GLx vs. SLx[1)]	V_{GLx5}	6.5	–	–	V	V_{VS} = 7.0 V; C_{Load} = 20 nF; D.C. = 100%	P_5.1.23
Rise time	t_{rise}	–	250	–	ns	C_{Load} = 11 nF; R_{Load} = 1 Ω; V_{VS} = 7 V; 20-80%	P_5.1.24
Fall time	t_{fall}	–	200	–	ns	C_{Load} = 11 nF; R_{Load} = 1 Ω; V_{VS} = 7 V; 20-80%	P_5.1.25
High level output voltage (in passive clamping)[1)]	V_{GxxUV}	–	–	1.2	V	Sleep mode or VS_UVLO	P_5.1.26
Pull-down resistor at BHx to GND	R_{BHUVx}	–	–	85	kΩ	Sleep mode or VS_UVLO	P_5.1.27
Pull-down resistor at VREG to GND	R_{VRUV}	–	–	30	kΩ	Sleep mode or VS_UVLO	P_5.1.28
Bias current into BHx	I_{BHx}	–	–	150	µA	V_{CBS} > 5 V; no switching	P_5.1.29

Table 8 Electrical characteristics MOSFET drivers

V_S = 7.0 to 34 V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bias current out of SHx	I_{SHx}	–	40	–	µA	$V_{SHx} = V_{SL}$ = GND; ENA=HIGH; affected high-side output stage static on; 5 V < V_{CBS} < 13 V	P_5.1.30
Bias current out of SL	I_{SL}	–	–	1.4	mA	0 ≤ V_{SHx} ≤ V_{VS} + 1 V; ENA = HIGH; no switching; V_{CBS} > 5 V	P_5.1.31
Dead time & input propagation delay times							
Programmable internal dead time	t_{DT}	0.08 0.25 0.82 1.0 2.0	0.13 0.42 1,21 1.88 3.62	0.20 0.57 1.65 2.7 5.6	µs	R_{DT} = 0 kΩ R_{DT} = 10 kΩ R_{DT} = 47 kΩ R_{DT} = 100 kΩ R_{DT} = 1000 kΩ	P_5.1.32
Max. internal dead time	t_{DT_MAX}	2.3	4.0	6.4	µs	DT pin open	P_5.1.33
Dead time deviation between channels	d_{tDT1}	-20	–	20	%	–	P_5.1.34
		-15	–	15	%	R_{DT} ≤ 47 kΩ	
Dead time deviation between channels LSoff -> HS on	d_{tDTH1}	-14	–	14	%	–	P_5.1.35
		-12	–	12	%	R_{DT} ≤ 47 kΩ	
Dead time deviation between channels HSoff -> LS on	d_{tDTL1}	-14	–	14	%	–	P_5.1.36
		-12	–	12	%	R_{DT} ≤ 47 kΩ	
Input propagation time (low on)	$t_{P(ILN)}$	0	100	200	ns	C_{Load} = 10 nF; R_{Load} = 1 Ω	P_5.1.37
Input propagation time (low off)	$t_{P(ILF)}$	0	100	200	ns	C_{Load} = 10 nF; R_{Load} = 1 Ω	P_5.1.38
Input propagation time (high on)	$t_{P(IHN)}$	0	100	200	ns	C_{Load} = 10 nF; R_{Load} = 1 Ω	P_5.1.39
Input propagation time (high off)	$t_{P(IHF)}$	0	100	200	ns	C_{Load} = 10 nF; R_{Load} = 1 Ω	P_5.1.40
Absolute input propagation time difference between above propagation times	$t_{P(diff)}$	–	50	100	ns	C_{Load} = 10 nF; R_{Load} = 1 Ω	P_5.1.41

Table 8 Electrical characteristics MOSFET drivers

V_S = 7.0 to 34 V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VREG							
VREG output voltage	V_{VREG}	11	12.5	14	V	$V_{VS} \geq 13.5$ V; I_{Load} = -35 mA	P_5.1.42
VREG overcurrent limitation	$I_{VREGOCL}$	100	–	500	mA	–[3]	P_5.1.43
Voltage drop between Vs and VREG	V_{VsVREG}	–	–	0.5	V	$V_{VS} \geq 7$ V; I_{Load} = -35 mA; Ron operation	P_5.1.44
100% D.C. charge pump							
Charge pump frequency[1]	f_{CP}	–	21	–	MHz	–	P_5.1.45
Motor bridge reverse polarity protection output							
High level output voltage RPP vs. VS	V_{RPP1}	–	11	15	V	I_{Load} = 0 µA	P_5.1.46
High level output voltage RPP vs. VS	V_{RPP2}	–	11	12.5	V	$I_{Load} \geq$ -30 µA	P_5.1.47
D.C. output current at RPP	I_{RPP1}	–	-110	-150	µA	$V_{RPP} \geq 10$ V; Low side on	P_5.1.48
Rise time[1]	$t_{RPPrise}$	–	1	2	ms	C_{LOAD} = 10 nF	P_5.1.49
Rise time[1]	$t_{RPPrise}$	–	10	20	µs	C_{LOAD} = 100 pF	P_5.1.50
ENA and low quiescent current mode							
ENA propagation time to output stages switched off	t_{PENA_H-L}	–	2.0	3.0	µs	–	P_5.1.51
Low time of ENA signal without clearing error register	t_{RST0}	–	–	1.2	µs	–	P_5.1.52
High time of ENA signal after ENA rising edge for error logic active	t_{RST1}	4	5.75	7	µs	–	P_5.1.53
Go to sleep time	t_{sleep}	310	415	540	µs	–	P_5.1.54
Start up conditions							
Time until GLx is set to high automatically during start up	$t_{GL_H_Start}$	–	50	100	µs	C_{REG} = 2.2 µF; C_{BS} = 330 nF	P_5.1.55
Minimum VS voltage for start up	V_{S_Start}	8	–	–	V	–	P_5.1.56
DRVDIS toggling time	t_{toggle}	1	–	–	ms	C_{REG} = 2.2 µF; C_{BS} = 330 nF	P_5.1.57

1) Not subject to production test, specified by design.

2) V_{diode} is the bulk diode of the external low-side MOSFET.

3) Normally no error flag; error flag might by triggered by undervoltage VREG caused by very high load current.

4.3 Protection and diagnostic functions

4.3.1 State diagram of different operation modes

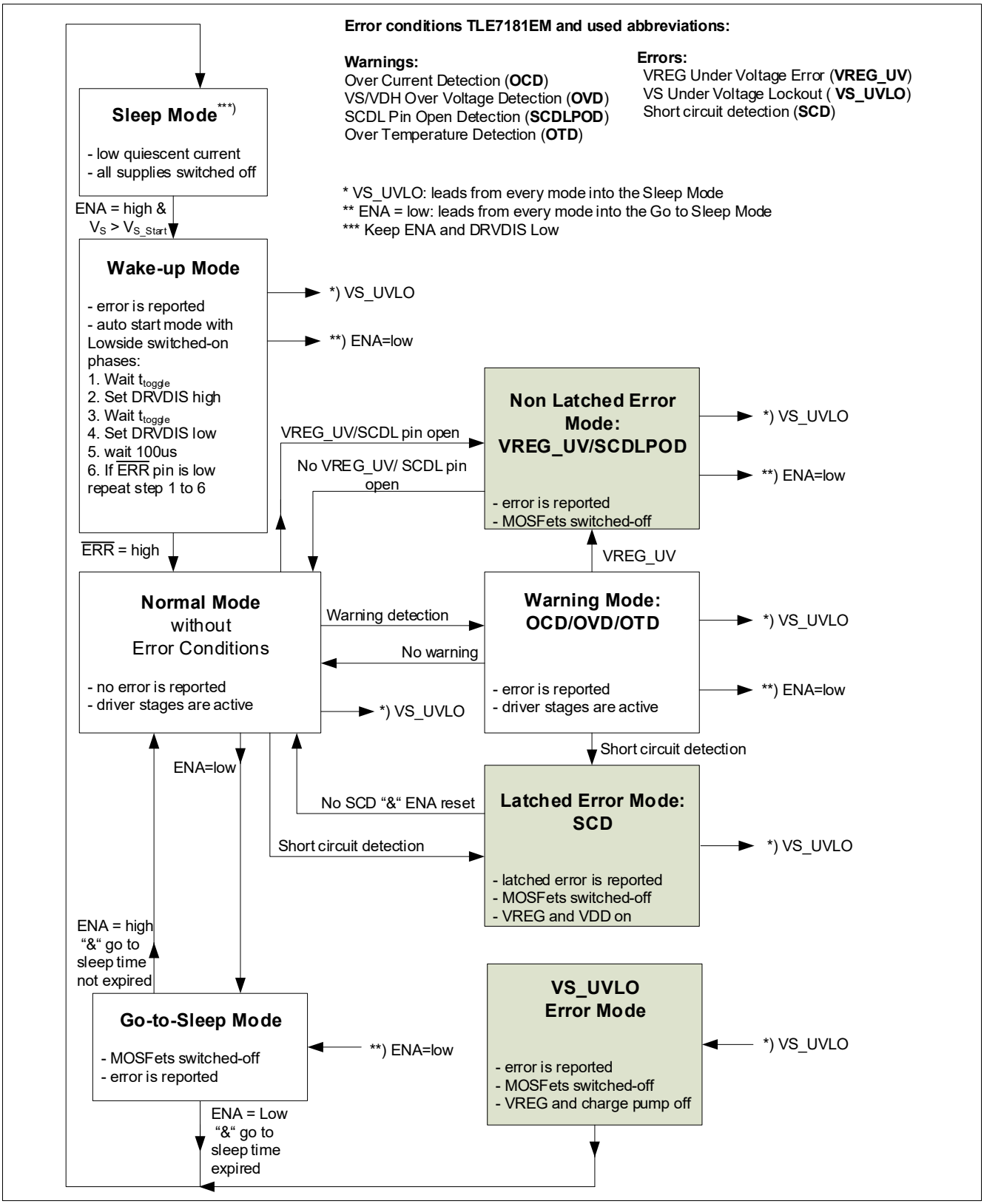


Figure 4 State diagramTLE7181EM

4.3.2 Short circuit protection

The TLE7181EM provides a short circuit protection for the external MOSFETs by monitoring the drain-source voltage of the external MOSFETs.

This monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding driver output stage is set to “on” and the dead time and the blanking time are expired.

The blanking time starts when the dead time has expired and assures that the switch on process of the MOSFET is not taken into account. It is recommended to keep the switching times of the MOSFETs below the blanking time.

The short circuit detection level is adjustable in an analog way by the voltage setting at the SCDL pin. There is a 1:1 translation between the voltage applied to the SCDL pin and the drain-source voltage limit. E.g. to trigger the SCD circuit at 1 V drain-source voltage, the SCDL pin must be set to 1 V. The drain-source voltage limit can be chosen between 0.2 … 2 V.

If after the expiration of the blanking time the drain source voltage of the observed MOSFET is still higher then the SCDL level, the SCD filter time t_{SCP} starts to run. A capacitor is charged with a current. If the capacitor voltage reaches a specific level (filter time t_{SCP}), the error signal is set and the IC goes into SCDL Error Mode. If the SCD condition is removed before the SC is detected, the capacitor is discharged with the same current. The discharging of the capacitor happens as well when the MOSFET is switched off. It has to be considered that the high-side and the low-side output of one phase are working with the same capacitor.

4.3.3 SCDL pin open detection

An integrated structure at the SCDL pin assures that in case of an open pin the SCDL voltage is pulled to a medium voltage level. The external MOSFETs are actively switched off and an ERR flag is set. This error is self-clearing.

4.3.4 Vs and VDH overvoltage warning

The TLE7181EM has an integrated overvoltage warning to minimize risk of destruction of the IC at high supply voltages caused by violation of the maximum ratings. For the overvoltage warning the voltage is observed at the pin VS and VDH. If the voltage level has reached, the fixed overvoltage threshold V_{OVW} for the filter time $t_{OV,}$ a warning at ERR pin is set and TLE7181EM will go in normal operation with warning.

The overvoltage warning is self clearing. If the voltage at pin VS and VDH returns into the specified voltage range, the Error register will be cleared and TLE7181EM returns to normal operation mode.

It is the decision of the user if and how to react on the overvoltage warning.

4.3.5 VS undervoltage shutdown

The TLE7181EM has an integrated VS undervoltage shutdown to assure that the behavior of the complete IC is predictable in all supply voltage ranges. As soon as the undervoltage threshold V_{UVVR} is reached for a specified filter time the TLE7181EM is in VS_UVLO error mode. The error signal will be set and output stages, voltage regulator and charge pump will be switched off so the IC will go into sleep mode. An enable is necessary to restart the TLE7181EM.

4.3.6 VREG undervoltage warning

The TLE7181EM has an integrated undervoltage warning detection at VREG. If the supply voltage at VREG reaches the VREG undervoltage threshold V_{UVVR}, a warning at ERR pin is set and the TLE7181EM will go into VREG error mode. In case of VREG error mode all output stages will actively switched off to prevent low gate source voltages at the power MOSFETs causing high RDSon. If supply voltage at the VREG pin recovers; the error flag will be cleared and the TLE7181EM will return in normal operation mode.

4.3.7 Overtemperature warning

The TLE7181EM provides an integrated digital overtemperature warning to minimize risk of destruction of the IC at high temperature. The temperature will be detected by a embedded sensor. During overtemperature warning the ERR signal is set and the TLE7181EM is in normal operation mode with warning.

The overtemperature warning is self clearing. If the temperature is below $T_{j(PW)} - dT_{j(OW)}$, the warning will be cleared and TLE7181EM returns to normal operation mode.

It is the decision of the user to react on the overtemperature warning.

4.3.8 Overcurrent warning

The TLE7181EM offers an integrated overcurrent detection. The output signal of the current sense OpAmp will be monitored. If the output signal reaches the specified voltage threshold V_{OCTH} for a certain time, overcurrent will be detected. After the comparator the filter time t_{OC} is implemented to avoid false triggering caused by overswing of the current sense signal. The ERR pin will be set to low and the TLE7181EM will go into normal operation mode with warning.

The error signal disappears as soon as the current decreases below the overcurrent threshold V_{OCTH}. The error signal disappears as well when the current commutates from the low-side MOSFET to the associated high-side MOSFET and is no longer flowing over the shunt resistor.

It is the decision of the user to react on the overcurrent signal by modifying input patterns.

4.3.9 Passive Gxx clamping

If VS undervoltage shutdown is detected or the device is in Sleep Mode, a passive clamping is active as long as the voltage at VS or VDH is higher than 3 V. Even below 3 V it is assured that the MOSFET driver stage will not switch on the MOSFET actively.

The passive clamping means that the BHx and the VREG pin are pulled to GND with specified pull down resistors. Together with the intrinsic diode of the push stage of the output stages which connect the gate output to BHx respectively VREG, this assures that the gate of the external MOSFETs are not floating undefined.

4.3.10 $\overline{\text{ERR}}$ pin

The TLE7181EM has a status pin to provide diagnostic feedback to the µC. The output of this pin is a push pull output stage with an integrated pull-down resistor to GND (see **Figure 5**).

Reset of error registers and Disable

The TLE7181EM can be reset by the enable pin $\overline{\text{ENA}}$. If the $\overline{\text{ENA}}$ pin is pulled to low for a specified minimum time, the error registers are cleared. ERR output is still set to low. After the next rising edge at ENA pin ERR pin will be set to high and no error condition is applied.

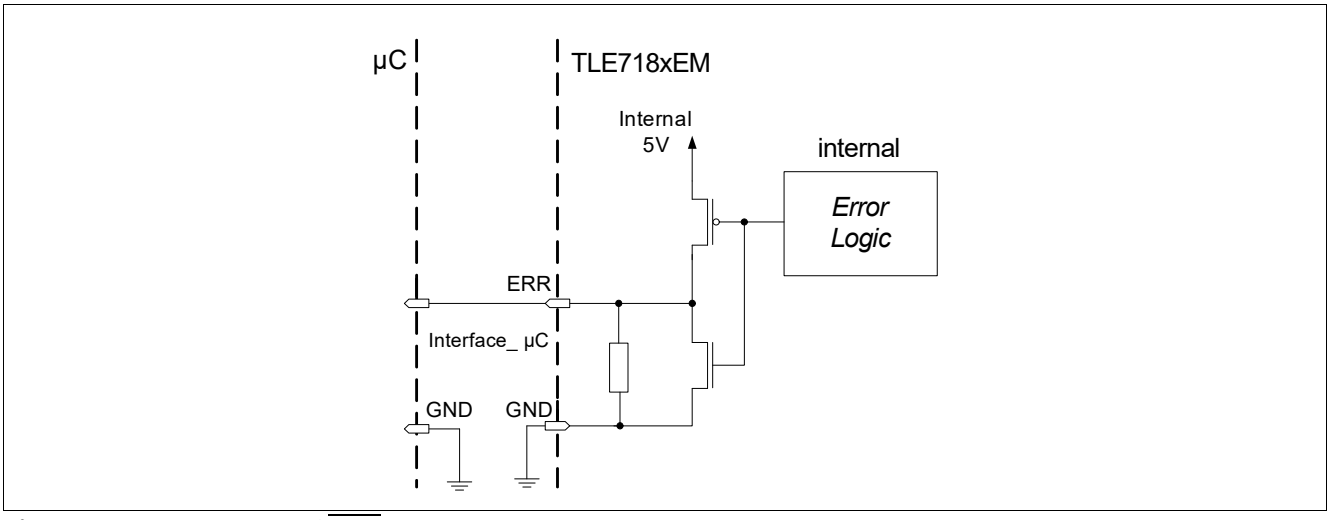


Figure 5 Structure of $\overline{\text{ERR}}$ output

Table 9 Overview of error condition

$\overline{\text{ERR}}$	Driver conditions	Driver action	Restart
High	No errors	Fully functional	–
Low	Overtemperature	Warning only	Self clearing
Low	Overvoltage VS/VDH	Warning only	Self clearing
Low	Overcurrent OPAMP	Warning only	Self clearing
Low	Undervoltage error VREG	All MOSFETs actively switched off	Self clearing
Low	Undervoltage shutdown based on VS	MOSFET, charge pump, Vreg switched off	Self clearing restart when enable high[1)]
Low	SCDL open pin	All MOSFETs actively switched off	Self clearing
Low	Short circuit detection	All MOSFETs actively switched off	Reset at ENA needed
Low	Go to sleep mode	All MOSFETs actively switched off	Immediate restart when ENA goes high
Low	Wake-up mode	Start up	–

1) If SC detected, reset with ENA necessary.

Table 10 Prioritization of errors

Priority	Errors and Warnings
0	Undervoltage lockout at Vs (VS_UVLO)
1	Short circuit detection error (SCD) SCDL pin open warning (SCDLPOD)
2	Undervoltage detection VREG (UV_VREG) Overvoltage detection warning (OVD) Overtemperature warning (OTD) Overcurrent warning (OCD)

4.3.11 Electrical characteristics

Table 11 Electrical characteristics - protection and diagnostic functions

V_S = 7.0 to 34 V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Short circuit protection							
Short circuit protection detection level input range	V_{SCDL}	0.2	–	2.0	V	Programmed by SCDL pin	P_5.2.1
Short circuit protection detection accuracy	A_{SCP1}	-50	–	+50	%	0.2 V ≤ V_{SCDL} ≤ 0.3 V	P_5.2.2
Short circuit protection detection accuracy	A_{SCP2}	-30	–	+30	%	0.3 V ≤ V_{SCDL} ≤ 1.2 V	P_5.2.3
Short circuit protection detection accuracy	A_{SCP3}	-10	–	+10	%	1.2 V ≤ V_{SCDL} ≤ 2.0 V	P_5.2.4
Filter time of short circuit protection	$t_{SCP(off)}$	2.5	3.5	4.5	µs	–	P_5.2.5
Filter time and blanking time of short circuit protection	t_{SCPBT}	4	6	8	µs	–	P_5.2.6
Internal pull-up resistor SCDL to 3 V	R_{SCDL}	180	300	475	kΩ	–	P_5.2.7
SCDL open pin detection level	V_{SCPOP}	2.1	–	3.2	V	–	P_5.2.8
Filter time of SCDL open pin detection	t_{SCPOP}	1.5	2.5	3.5	µs	–	P_5.2.9
SCDL open pin detection level hysteresis[1)]	V_{SCOPH}	–	0.3	–	V	–	P_5.2.10
Over- and undervoltage monitoring							
Overvoltage warning at Vs and/or VDH	V_{OVW}	34.5	36.5	38.5	V	V_{VS} and/or V_{VDH} increasing	P_5.2.11
Overvoltage warning hysteresis for Vs and/or VDH	V_{OVWhys}	2.1	3.1	4.1	V	–	P_5.2.12
Overvoltage warning filter time for Vs and/or VDH	t_{OV}	13	19	25	µs	–	P_5.2.13
Undervoltage shutdown at Vs	V_{UVVR}	4.5	5.0	5.5	V	V_{VS} decreasing	P_5.2.14
Undervoltage shutdown filter time for VS[1)]	t_{UVLO}	–	20	–	µs	–	P_5.2.15
Undervoltage warning at VREG	V_{UVVR}	5.5	6.0	6.5	V	V_{VS} decreasing	P_5.2.16
Undervoltage diagnosis filter time for VREG	t_{UVVR}	10	–	30	µs	–	P_5.2.17
Undervoltage hysteresis at VREG	V_{UWRhys}	–	0.5	–	V	–	P_5.2.18
Temperature monitoring							
Overtemperature warning	$T_{j(PW)}$	160	170	180	°C	–	P_5.2.19

Table 11 Electrical characteristics - protection and diagnostic functions (cont'd)

V_S = 7.0 to 34 V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Hysteresis for overtemperature warning	$dT_{j(OW)}$	10	–	20	°C	–	P_5.2.20
Overcurrent detection							
Overcurrent detection level	V_{OCTH}	4.5	–	4.99	V	–	P_5.2.21
Filter time for overcurrent detection	t_{OC}	2.3	–	4.3	µs	–	P_5.2.22
$\overline{\text{ERR}}$ pin[2)]							
$\overline{\text{ERR}}$ output voltage	V_{ERR}	4.6	–	–	V	V_{VS} = 7 V	P_5.2.23
Rise time $\overline{\text{ERR}}$ (20 - 80% of internal 5 V)	$t_{f(ERR)}$	–	–	3	µs	C_{LOAD} = 1 nF	P_5.2.24
Internal pull-down resistor $\overline{\text{ERR}}$ to GND	$R_{f(ERR)}$	60	100	170	kΩ	–	P_5.2.25

1) Not subject to production test, specified by design.

2) $\overline{\text{ERR}}$ pin and reset & enable functional between V_{VS} = 6 …7 V, but characteristics might be out of specified range.

4.4 Shunt signal conditioning

The TLE7181EM incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. The gain of the OpAmp is adjustable by external resistors within a range higher than 5. The usage of higher gains in the application might be limited by required settling time and band width.

It is recommended to apply a small offset to the OpAmp, to avoid operation in the lower rail at low currents.

The output of the OpAmp ISO is not short-circuit proof.

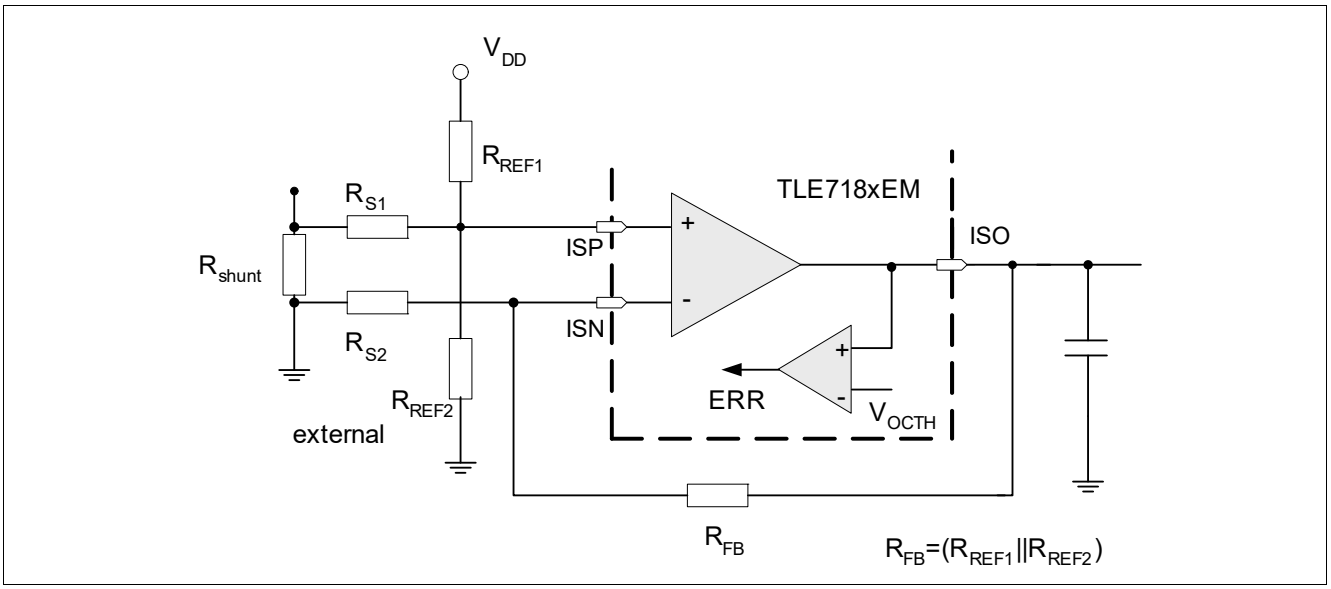


Figure 6 Shunt signal conditioning block diagram and overcurrent limitation

For a description of the overcurrent warning, please see **Chapter 4.3.7**.

4.4.1 Electrical characteristics

Table 12 Electrical characteristics - current sense signal conditioning

V_S = 7.0 to 36 V, T_j = -40 to + 150°C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Series resistors	R_S	100	500	1000	Ω	–	P_5.3.1
Feedback resistor Limited by the output voltage dynamic range	R_{fb}	2000	7500	–	Ω	–	P_5.3.2
Resistor ratio (gain ratio)	$R_{fb/RS}$	5	–	–	–	–	P_5.3.3
Steady state differential input voltage range across VIN	$V_{IN(ss)}$	-400	–	400	mV	–	P_5.3.4
Input differential voltage (ISP - ISN)	V_{IDR}	-800	–	800	mV	–	P_5.3.5
Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	2000	mV	–	P_5.3.6
Input offset voltage of the I-DC link OpAmp, including temperature drift	V_{IO}	–	–	±2	mV	R_S = 500 Ω; V_{CM} = 0 V; V_{ISO} = 1.65 V;	P_5.3.7
Input bias current (ISN,ISP to GND)	I_{IB}	-300	–	–	µA	V_{CM} = 0 V; V_{ISO} = open	P_5.3.8
Low level output voltage of ISO	V_{OL}	-0.1	–	0.2	V	I_{OH} = 3 mA	P_5.3.9
High level output voltage of ISO	V_{OH}	4.75	–	5.2	V	I_{OH} = -3 mA	P_5.3.10
Output short circuit current	I_{SCOP}	5	–	–	mA	–	P_5.3.11
Differential input resistance[1)]	R_I	100	–	–	kΩ	–	P_5.3.12
Common mode input capacitance[1)]	C_{CM}	–	–	10	pF	10 kHz	P_5.3.13
Common mode rejection ratio at DC CMRR = 20*Log((Vout_diff/Vin_diff) * (Vin_CM/Vout_CM))	C_{MRR}	80	100	–	dB	–	P_5.3.14
Common mode suppression[2)] with CMS = 20*Log(Vout_CM/Vin_CM) Freq = 100 kHz Freq = 1 MHz Freq = 10 MHz	C_{MS}	–	 62 43 23	–	dB	V_{IN} = 360 mV* sin(2*π*freq*t); R_s = 500 Ω; R_{fb} = 7500 Ω	P_5.3.15
Slew rate	$d_{V/dt}$	–	10	–	V/µs	Gain ≥ 5; R_L = 1.0 kΩ; C_L = 500 pF	P_5.3.16

Table 12 Electrical characteristics - current sense signal conditioning (cont'd)

V_S = 7.0 to 36 V, T_j = -40 to + 150°C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Large signal open loop voltage gain (DC)	A_{OL}	80	100	–	dB	–	P_5.3.17
Unity gain bandwidth[1)]	G_{BW}	10	20	–	MHz	R_L = 1 kΩ; C_L = 100 pF	P_5.3.18
Phase margin [1)]	F_M	–	50	–	°	Gain ≥ 5; R_L = 1 kΩ; C_L = 100 pF	P_5.3.19
Gain margin [1)]	A_M	–	12	–	dB	R_L = 1 kΩ; C_L = 100 pF	P_5.3.20
Bandwidth	B_{WG}	0.7	1.3	–	MHz	Gain = 15; R_L = 1 kΩ; C_L = 500 pF; R_S= 500 Ω	P_5.3.21
Output settle time to 98%	t_{set1}	–	1	1.8	µs	Gain = 15; R_L = 1 kΩ; C_L = 500 pF; 0.3 < V_{ISO} < 4.8 V; R_S = 500 Ω	P_5.3.22
Output settle time to 98%[1)]	t_{set2}	–	4.6	–	µs	Gain = 75; R_L = 1 kΩ; C_L = 500 pF; 0.3 < V_{ISO} < 4.8 V; R_S = 500 Ω	P_5.3.23

1) Not subjected to production test; specified by design.

2) Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This is the description how the IC is used in its environment.

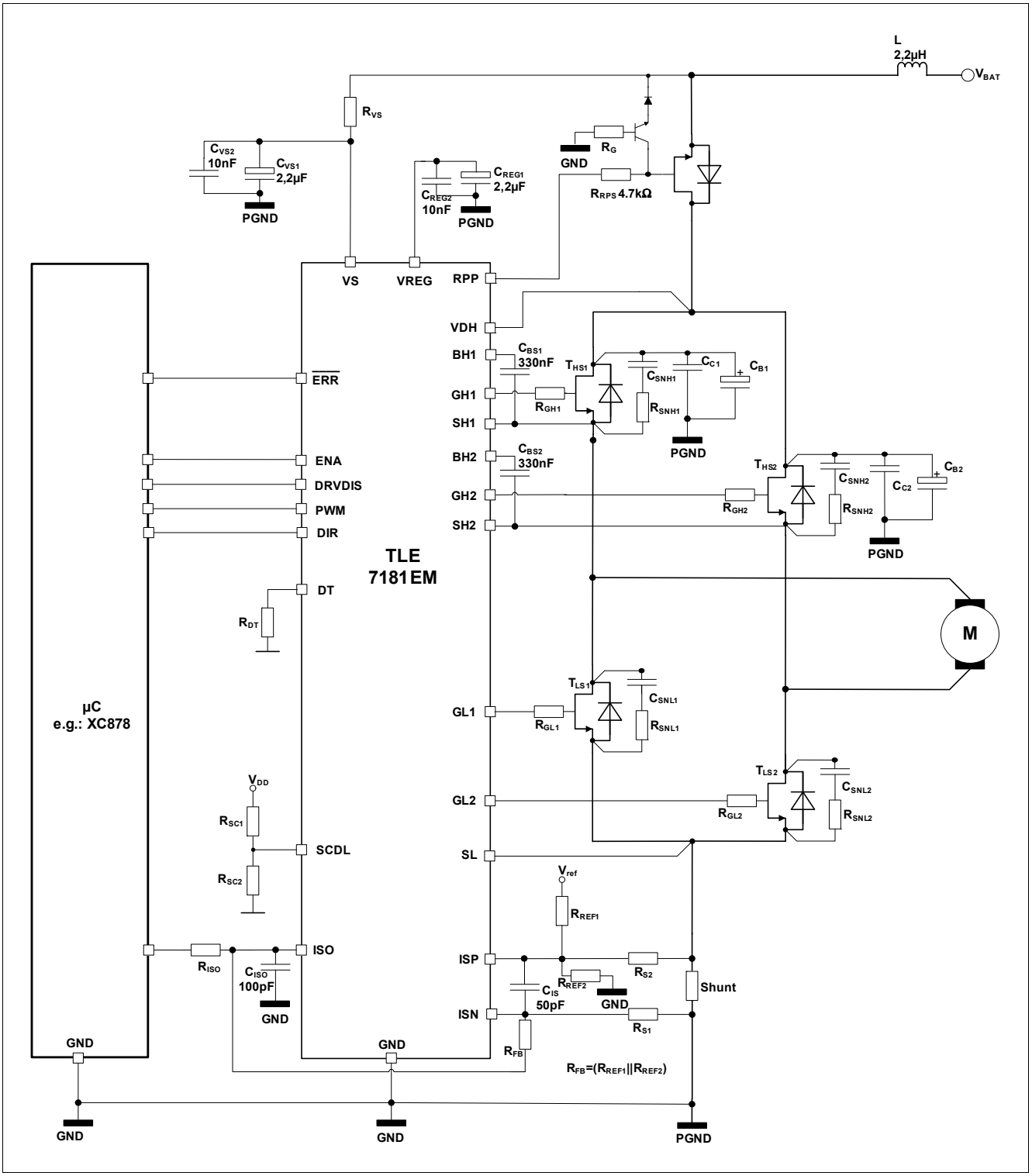


Figure 7 Application diagram 1: DC-Brush motor controlled by TLE7181EM

Note: This are very simplified examples of an application circuit. The function must be verified in the real application.

5.1 Layout guidelines

Please refer also to the simplified application example.

- Two separated bulk capacitors CB should be used - one per half bridge.
- Two separated ceramic capacitors CC should be used - one per half bridge.
- Each of the two bulk capacitors CB and each of the two ceramic capacitors CC should be assigned to one of the half bridges and should be placed very close to it.
- The components within one half bridge should be placed close to each other: high-side MOSFET, low-side MOSFET, bulk capacitor CB and ceramic capacitor CC (CB and CC are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide.
- The connection between the source of the high-side MOSFET and the drain of the low-side MOSFET should be as low inductive and as low resistive as possible.
- VDH is the sense pin used for short circuit detection; VDH should be routed (via Rvdh) to the common point of the drains of the high-side MOSFETs to sense the voltage present on drain high side.
- SL is the sense pin used for short circuit detection; SL should be routed o the common point of the source of the low-side MOSFETs to sense the voltage present on source low side.
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ω) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors).
- If available, the exposed pad on the backside of the package should be connected to GND.

5.2 Further application information

- For further information please contact **http://www.infineon.com/**

6 Package information

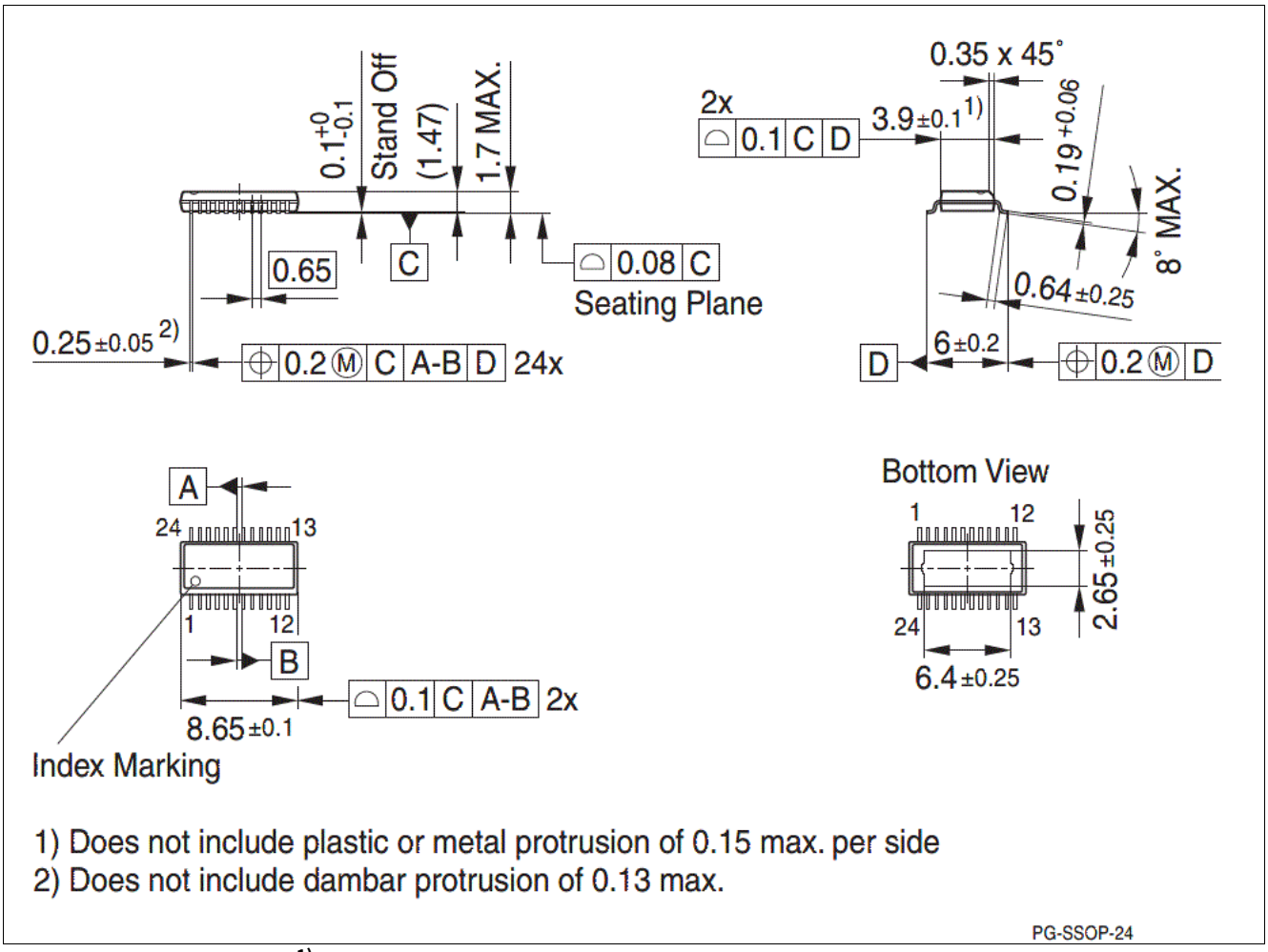


Figure 8 PG-SSOP-24[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
1.2	2019-03-14	Datasheet Updated layout and structure Improved description for wake-up mode in state diagram (see **Chapter 4.3.1**) Improved description for wake-up mode (see **Chapter 4.1.8**) Updated parameter description and symbol for **P_5.1.55** Specification of minimum VS voltage for start-up (see **P_5.1.56**) Specification of DRVDIS toggling time t_{toggle} (see **P_5.1.57**) Updated condition for bias current out of SHx I_{SHx} (see **P_5.1.30**) Corrected maximum current for I_{RPP} (see **P_4.1.5**) Typos corrected in pin list and text (see **Chapter 2.2**) Editorial changes
1.1	2010-09-30	Datasheet Max rating of current at RPP pin increased
1.0	2010-09-29	Datasheet Thermal resistance of package adjusted Output rise time adjusted Pull up and pull down resistor values adapted Dead time values centered Go to sleep time modified Filter time of short circuit detection adjusted SCDL pin open detection description improved Overview of error condition table improved Filter time and blanking time of short circuit detection adjusted SCDL open pin detection level added Filter time of SCDL open pin detection adjusted Overvoltage warning at Vs and/or VDH centered Overvoltage warning hysteresis for Vs and/or VDH centered Overvoltage warning filter time for Vs and/or VDH centered ERR output voltage added OpAmp bandwidth adjusted

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Edition 2019-03-14
Published by
Infineon Technologies AG
81726 Munich, Germany

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