TLE7184F-3V

System IC for B6 motor drives

Datasheet

Rev.1.2, 2016-01-27

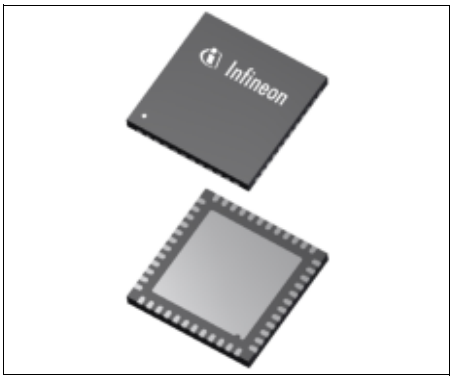
Automotive Power

Table of Contents

	Table of Contents	2
1	**Overview**	4
2	**Block Diagram**	5
3	**Pin Configuration**	6
3.1	Pin Assignment TLE7184F-3V	6
3.2	Pin Definitions and Functions	7
4	**General Product Characteristics**	9
4.1	Absolute Maximum Ratings	9
4.2	Functional Range	10
4.3	Thermal Resistance	11
4.4	Default State of Inputs	11
5	**MOSFET Driver**	12
5.1	Inputs and Dead Time	12
5.2	Output Stages	12
5.3	Bootstrap Principle	13
5.4	Currents at SH pins	13
5.5	Electrical Characteristics	13
6	**Shunt Signal Conditioning**	16
6.1	Electrical Characteristics	16
7	**3.3 V Low Drop Voltage Regulator**	18
7.1	Electrical Characteristics	18
8	**Interface, VDH Switch and $\overline{\text{INH}}$ Digital Output**	20
8.1	PWM Interface (IFMA)	20
8.2	VDHS Switch	21
8.3	Digital Output $\overline{\text{INHD}}$	21
8.4	Electrical Characteristics	21
9	**Description of Modes, Protection and Diagnostic Functions**	23
9.1	Description of modes	23
9.2	Protection and Diagnosis Functions	25
9.2.1	Over Temperature Shut Down (OTSD)	25
9.2.2	Analog Temperature Monitoring	26
9.2.3	VS Under Voltage Lockout (VS_UVLO)	26
9.2.4	VDD Under Voltage Diagnosis (VDD_UVD)	26
9.2.5	VDD Under Voltage Shut Down (VDD_UVSD)	26
9.2.6	VREG Under Voltage Diagnosis (VREG_UVD)	27
9.2.7	VREG Under Voltage Shut Down (VREG_UVSD)	27
9.2.8	IOV and VDH Over Voltage Shut Down (IOV_OVSD, VDH_OVSD)	27
9.2.9	Dead Time and Shoot Through Protection	27
9.2.10	Short Circuit Protection (SCP)	28
9.2.11	SCDL Pin Open Detection (SCDL_open)	28
9.2.12	Over Current Shut Down (OCSD)	28
9.2.13	VDD Current Limitation	28
9.2.14	Passive Gxx Clamping	28
9.3	$\overline{\text{ERR}}$ Pin	28
9.4	Electrical Characteristics	30

10 Application Description 33
11 Package Outlines 34
12 Revision History 35

1 Overview



PG-VQFN-48

Features

- Drives 6 N-Channel Power MOSFETs
- Integrated 3.3V Vreg-Controller to power µC
- Integrated switch for VDH voltage
- Separate control input for each MOSFET
- Adjustable dead time
- Shoot through protection
- Analog adjustable Short Circuit Protection levels
- Low quiescent current mode
- 1 bit diagnosis $\overline{\text{ERR}}$
- Over Temperature shut down and analog temperature output
- Under Voltage shut down
- Adjustable Over Voltage shut down
- Current sense OpAmp
- Over current shut down based on Current sense OpAmp, fixed shut down level
- 0 …94% duty cycle at 25 kHz PWM frequency
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7184F-3V is a system IC for Brushless Motor Control. It incorporates a voltage supply for a µC, a bridge driver for a B6 configuration, an application typical PWM interface and some other smaller features. Target is to reduce the number of discrete components in typical BLDC automotive applications and give enough flexibility for custom specific adaptations.

It works with 3-phase motors and brush DC motors. Its exposed pad package allows the usage even at high ambient temperatures.

Type	Package	Marking
TLE7184F-3V	PG-VQFN-48	TLE7184F-3V

2 Block Diagram

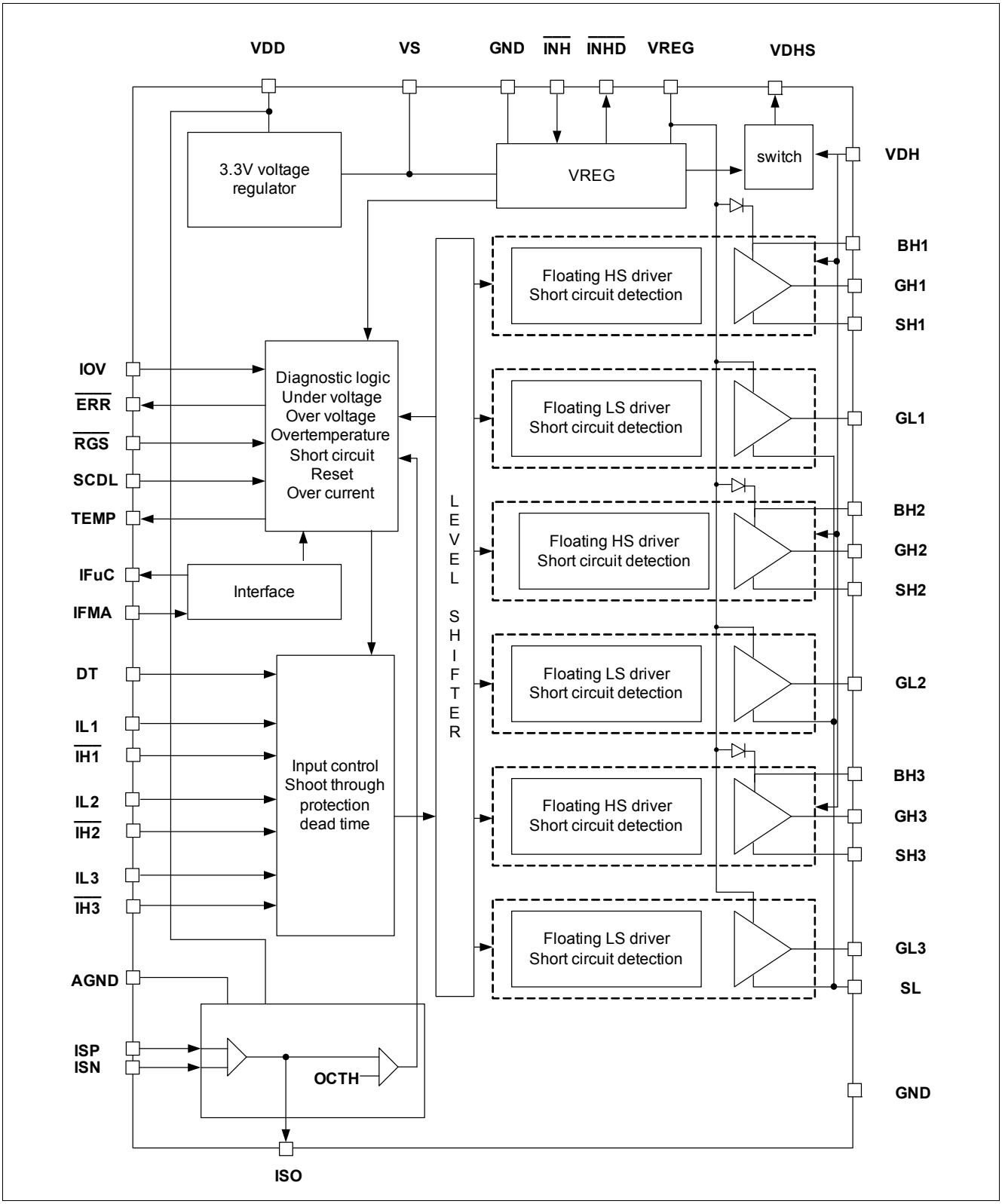


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment TLE7184F-3V

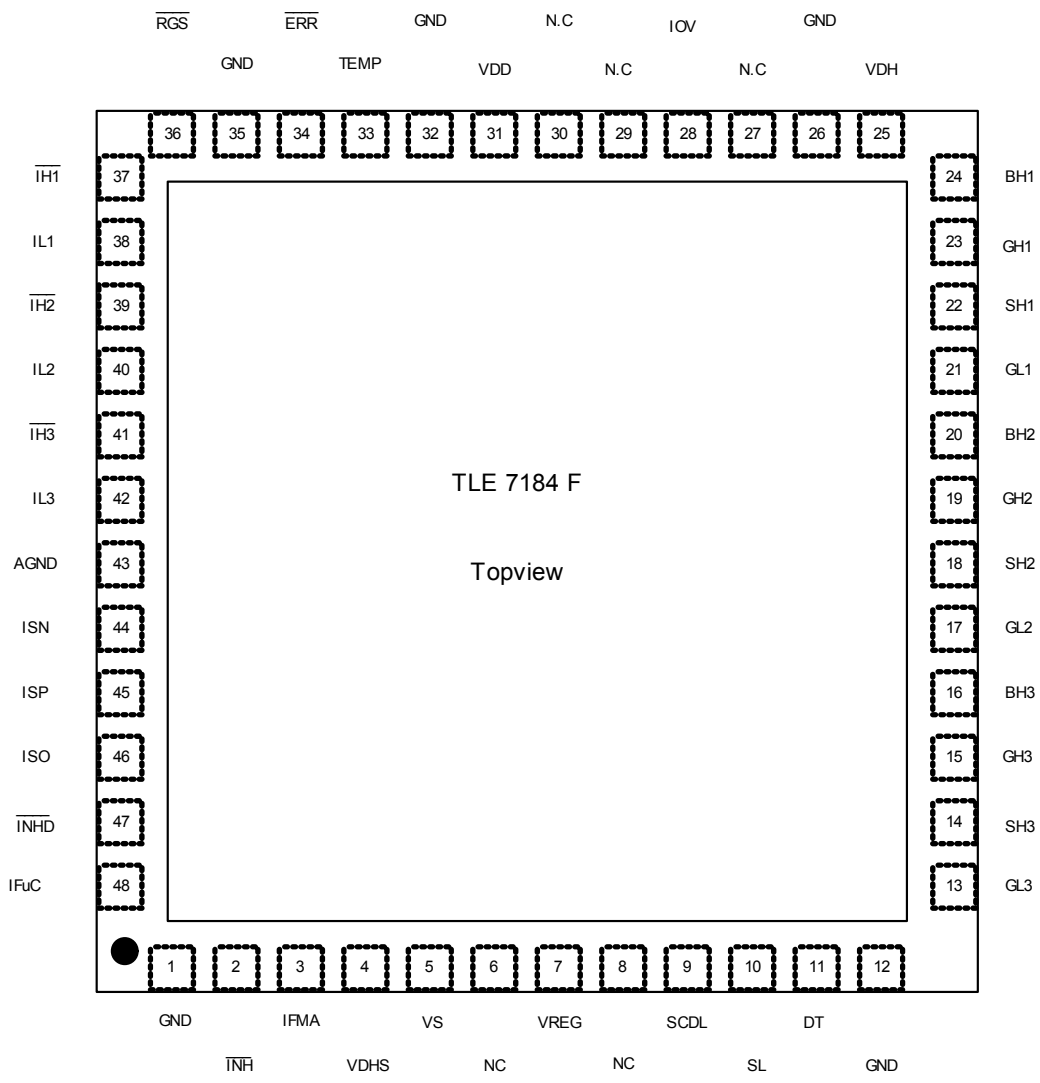


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
5	VS	Supply Pin
7	VREG	Output of supply for driver output stages - connect to capacitor
31	VDD	Output of 3.3V supply for µC - connect to capacitor
2	$\overline{\text{INH}}$	Input pin wake up the complete system IC
47	$\overline{\text{INHD}}$	Digital output 3.3V for $\overline{\text{INH}}$ state (high when $\overline{\text{INH}}$ is high)
4	VDHS	Switched output of VDH voltage; switch open in sleep mode
33	TEMP	Output pin for analog temperature signal
36	$\overline{\text{RGS}}$	Reset and Go-to-Sleep input pin for reset of error registers, set HIGH to avoid to go-to-sleep
38	IL1	Input for low side switch 1 (active high)
37	$\overline{\text{IH1}}$	Input for high side switch 1 (active low)
40	IL2	Input for low side switch 2 (active high)
39	$\overline{\text{IH2}}$	Input for high side switch 2 (active low)
42	IL3	Input for low side switch 3(active high)
41	$\overline{\text{IH3}}$	Input for high side switch 3(active low)
11	DT	Input pin for adjustable dead time function, connect to GND via resistor
9	SCDL	Analog input pin for adjustable Short Circuit Detection function, connect to voltage divider
28	IOV	Input pin for Over Voltage detection.
34	$\overline{\text{ERR}}$	Open drain error output
25	VDH	Voltage input common drain high side for short circuit detection
24	BH1	Pin for + terminal of the bootstrap capacitor of phase 1
23	GH1	Output pin for gate of high side MOSFET 1
22	SH1	Pin for source connection of high side MOSFET 1
21	GL1	Output pin for gate of low side MOSFET 1
20	BH2	Pin for + terminal of the bootstrap capacitor of phase 2
19	GH2	Output pin for gate of high side MOSFET 2
18	SH2	Pin for source connection of high side MOSFET 2
17	GL2	Output pin for gate of low side MOSFET 2
16	BH3	Pin for + terminal of the bootstrap capacitor of phase 3
15	GH3	Output pin for gate of high side MOSFET 3
14	SH3	Pin for source connection of high side MOSFET 3
13	GL3	Output pin for gate of low side MOSFET 3
10	SL	Pin for common source connection of low side MOSFETs
44	ISN	Input for OpAmp - terminal
45	ISP	Input for OpAmp + terminal
46	ISO	Output of OpAmp
43	AGND	Analog GND for Opamp and analog temperature output
3	IFMA	Interface to master ECU (used for wake up)
48	IFuC	Interface to µC

Pin	Symbol	Function
1	GND	Ground pin
12	GND	Ground pin
26	GND	Ground pin
32	GND	Ground pin
35	GND	Ground pin
6	NC	connect to GND
8	NC	connect to GND
27	NC	connect to GND
29	NC	connect to GND
30	NC	connect to GND

Exposed pad to be connected to GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Voltage range at VS, IFMA, $\overline{\text{INH}}$, IOV	V_{VS1}	-0.3	45	V	–
4.1.2	Voltage range at IFMA, $\overline{\text{INH}}$	V_{IFMA}	-6.0	45	V	R >= 10kΩ
4.1.3	Voltage range at VS	V_{VS2}	-3.0	45	V	R_{VS} >= 4.7Ω; 60s, 5x;
4.1.4	Voltage range at VS	V_{VS3}	-3.0	45	V	R_{VS} >= 2.0Ω;; 200ms, 5x;
4.1.5	Voltage range at VREG output	V_{VREG}	-0.3	15	V	
4.1.6	Voltage range at VDH, VDHS	V_{VDHx}	-0.3	55	V	–
4.1.7	Voltage range at VDH	V_{VDH1}	-3.0	55	V	With R_{VDH} >=10Ω; 60s, 5x; T_j<=150°C
4.1.8	Voltage range at $\overline{\text{IHx}}$, ILx, $\overline{\text{RGS}}$, $\overline{\text{ERR}}$, IFuC, $\overline{\text{INHD}}$, SCDL	V_{DP}	-0.3	3.7	V	–
4.1.9	Voltage range at TEMP, DT, VDD, ISO	V_{DP}	-0.3	6.0	V	–
4.1.10	Voltage range at ISP, ISN	V_{OPI}	-5.0	5.0	V	–
4.1.11	Voltage difference between ISP and ISN	V_{OPD}	-5.0	5.0	V	
4.1.12	Voltage range at BHx	V_{BH}	-0.3	55	V	–
4.1.13	Voltage range at GHx	V_{GH}	-0.3	55	V	–
4.1.14	Voltage range at GHx	V_{GHP}	-7.0	55	V	t_P < 1µs; f=50kHz
4.1.15	Voltage range at SHx	V_{SH}	-2.0	45	V	–
4.1.16	Voltage range at SHx	V_{SHP}	-7.0	45	V	t_P < 1µs; f=50kHz
4.1.17	Voltage range at GLx	V_{GL}	-0.3	18	V	–
4.1.18	Voltage range at GLx	V_{GLP}	-7.0	18	V	t_P < 0.5µs; f=50kHz
4.1.19	Voltage range at SL	V_{SL}	-0.3	5.0	V	–
4.1.20	Voltage range at SL	V_{SLP}	-7.0	5.0	V	t_P < 0.5µs; f=50kHz
4.1.21	Voltage difference Gxx-Sxx	V_{GS}	-0.3	15	V	–
4.1.22	Voltage difference BHx-SHx	V_{BS}	-0.3	15	V	–
4.1.23	Minimum bootstrap capacitor C_{BS}	C_{BS}	330	–	nF	-10% tolerance allowed
4.1.24	Minimum buffer capacitor C_{VREG}	C_{VREG}	1	–	µF	
Temperatures						
4.1.25	Junction temperature	T_j	-40	150	°C	–
4.1.26	Storage temperature	T_{stg}	-55	150	°C	–

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.27	Case temperature[2)]	T_{Case}	–	145	°C	–
ESD Susceptibility						
4.1.28	ESD Resistivity[3)]	V_{ESD}	-2	+2	kV	–
4.1.29	CDM	V_{CDM}	–	500	V	–

1) Not subject to production test, specified by design.

2) Calculation based on Tjmax, RthJC and the assumption of 1W power dissipation

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage at VS	V_{VS}	6.0	45	V	below 7V reduced functionality[1) 2)]
4.2.2	Quiescent current (I_{VS} + I_{VDH} + I_{IFMA})	I_Q	–	50	µA	V_S<16V; sleep mode V_{VS}=V_{VDH}=V_{IFMA}
4.2.3	Supply current at VS (device enabled)	$I_{VS(0)}$	–	19	mA	V_s=8...18V; no load[3)]; f_{PWM}=25kHz;
4.2.4	Duty cycle HS	D_{HS}	0	95	%	f_{PWM}=20kHz; continuous operation
4.2.5	Duty cycle LS	D_{LS}	0	100	%	
4.2.6	Junction temperature	T_J	-40	150	°C	–

1) MOS driver output deactivated and ERROR pin set to low if VREG is lower UVVR

2) MOS driver output stage will operate at Vs=6.7V with 5mA load current at VREG

3) no load at VDD, ERR, ISO, IFµC, VDHS, GXX, TEMP, DT

The limitations in the PWM frequency are given by thermal constraints and limitations in the duty cycle (charging time of bootstrap capacitor).

All maximum ratings have to be considered

All basic functions will work between T_J=150°C and Over Temperature shut down. In this temperature range, the parameters might leave the specified range.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	–	5	K/W	–
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	29	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Default State of Inputs

Table 1 Default State of Inputs

Characteristic	State	Remark
Default state of ILx (if ILx left open -pull down)	Low	Low side MOSFETs off
Default state of $\overline{\text{IHx}}$ (if $\overline{\text{IHx}}$ left open - pull up)	High	High side MOSFETs off
Default state of $\overline{\text{RGS}}$ (if $\overline{\text{RGS}}$ left open - pull down)	Low	Error signal is reset and TLE7184F-3V goes to sleep
Default state of $\overline{\text{INH}}$ (if $\overline{\text{INH}}$ left open - pull down)	Low	no wake up by $\overline{\text{INH}}$
Default state of SCDL (if SCDL left open - pull up)	High	Error signal is set; all MOSFETs switched off
Default state of IFMA (if IFMA left open - pull up)[1)]	High	no wake up by IFMA
Default state of IOV (if IOV left open - pull down)	Low	no Over Voltage detection by IOV
Default state of DT (if DT left open)	max. dead time	max. dead time

1) external capacitance < 25pF

5 MOSFET Driver

5.1 Inputs and Dead Time

There are 6 independent control inputs to control the 6 MOSFETs individually. However, the control inputs for the High Side MOSFETs $\overline{IHx}$ are inverted. Hence, the control inputs for High Side $\overline{IHx}$ and Low Side MOSFETs ILx of the same half bridge can be tight together to control one half bridge by one control signal. To avoid shoot through currents within the half bridges, a dead time is provided by the TLE7184F-3V.

For more details about the dead time please see **Chapter 9.2.9**

5.2 Output Stages

The 3 low side and 3 high side powerful push-pull output stages of the TLE7184F-3V are all floating blocks.

All 6 output stages have the same output power and thanks to the bootstrap principle used, all MOSFETs can be switched all up to high frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see **Chapter 9.2.10**.[1)]

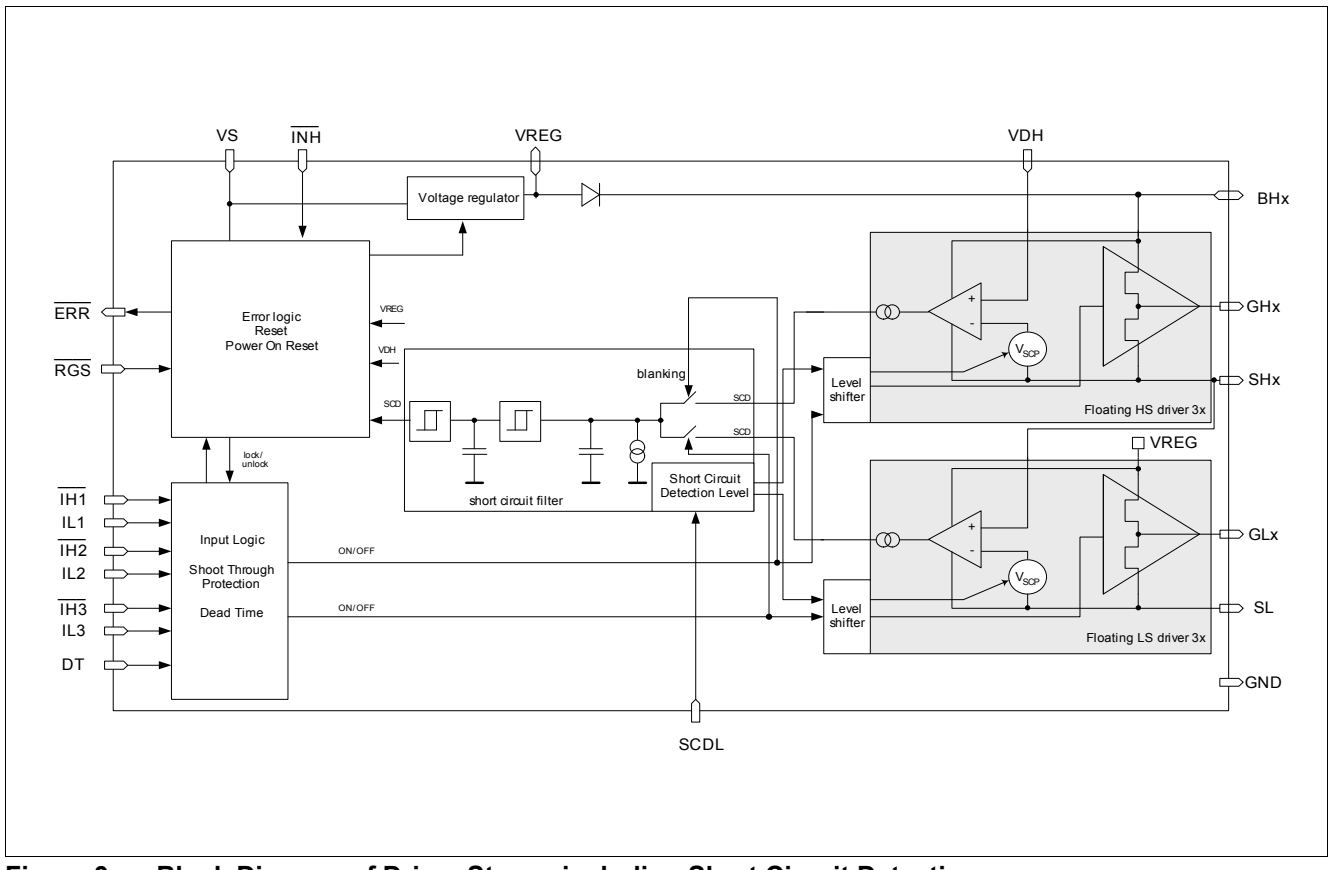


Figure 3 Block Diagram of Driver Stages including Short Circuit Detection

1) The high side outputs are not designed to be used for low side MOSFETs; the low side outputs are not designed to be used for high side MOSFETs

5.3 Bootstrap Principle

The TLE7184F-3V provides a bootstrap based supply for its high side output stages. The benefit of this principle is a fast switching of the high side switches - supporting active freewheeling in high side.

The bootstrap capacitors are charged by switching on the external low side MOSFETs connecting the bootstrap capacitor to GND. Under this condition the bootstrap capacitor will be charged from the VREG capacitor. If the low side MOSFET is switched off and the high side MOSFET is switched on, the bootstrap capacitor will float together with the SHx voltage to the supply voltage of the bridge. Under this condition the supply current of the high side output stage will discharge the bootstrap capacitor. This current is specified. The size of the capacitor together with this current will determine how long the high side MOSFET can be kept on without recharging the bootstrap capacitor.

When all external MOSFETs are switched off, the SHx voltage can be undefined. Under this condition, the bootstrap capacitors can be discharged, dependent on the SHx voltage.

5.4 Currents at SH pins

The currents at the SH pins can be used for diagnostic purposes to check the health state of the power stage.

The simplified structure related to the SH currents the TLE7184F-3V is described by **Figure 4**.

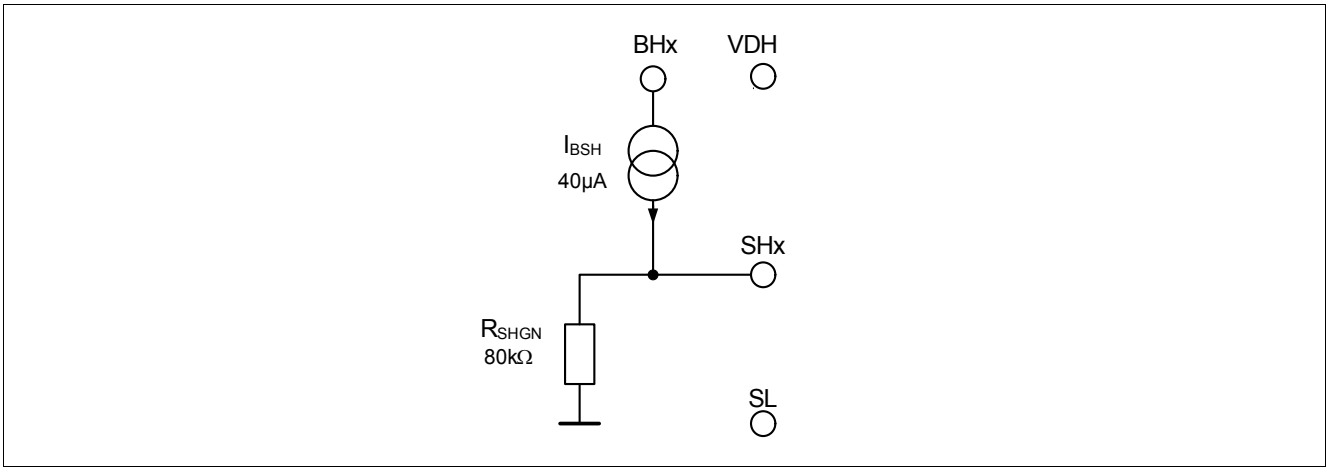


Figure 4 Block Diagram of SHx pin configuration

5.5 Electrical Characteristics

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 33 V, T_j = -40 °C to +150 °C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Inputs							
5.5.1	Low level input voltage of ILx; $\overline{\text{IHx}}$	V_{I_LL}	–	–	1.6	V	–
5.5.2	High level input voltage of ILx; $\overline{\text{IHx}}$	V_{I_HL}	2.8	–	–	V	–
5.5.3	Input hysteresis of $\overline{\text{IHx}}$; ILx[2)]	d_{VI}	100	–	–	mV	–
5.5.4	$\overline{\text{IHx}}$ pull-up resistors to VDD	R_{IH}	28.5	–	76.5	kΩ	–
5.5.5	ILx pull-down resistors to GND	R_{IL}	178.5	–	564	kΩ	–

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 33 V, T_j = -40 °C to +150 °C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
MOSFET driver output							
5.5.6	Output source resistance	R_{Sou}	2	–	13.5	Ω	I_{load}=20mA
5.5.7	Output sink resistance	R_{Sink}	2	–	9	Ω	I_{load}=20mA
5.5.8	High level output voltage Gxx vs. Sxx	V_{Gxx1}	–	11	14	V	13,5V <=V_{VS}<=45V[3)], V_{IOV}<=V_{OVIOV}, V_{VDH}<=V_{OVVDH} I_{load}=37,5mA
5.5.9	High level output voltage GHx vs. SHx[2)]	V_{Gxx2}	6	–	–	V	V_{Vs}=8V, C_{load}=20nF, dc=95%; f_{PWM}=20kHz
5.5.10	High level output voltage GHx vs. SHx[2)4)]	V_{Gxx3}	6 +V_{diode}	–	–	V	V_{Vs}=8V, C_{load}=20nF, dc=95%; f_{PWM}=20kHz; passive freewheeling
5.5.11	High level output voltage GLx vs. GND	V_{Gxx4}	6.7	–	–	V	V_{VS}=8V, C_{load}=20nF, dc=95%; f_{PWM}=20kHz;
5.5.12	Rise time T_j = -40°C T_j = 150°C	t_{rise}	 100 150	 – –	 230 350	ns	C_{Load}=11nF; R_{Load}=1Ω V_{VS}=7V 20-80%
5.5.13	Fall time T_j = -40°C T_j = 150°C	t_{fall}	 80 150	 – –	 210 290	ns	
5.5.14	High level output voltage (in passive clamping)	V_{GUV}	–	–	1.2	V	sleep mode or VS_UVLO[2) 5)]
5.5.15	Pull-down resistor at BHx to GND	R_{BHUV}	–	–	80	kΩ	
5.5.16	Pull-down resistor at VREG to GND	R_{VRUV}	–	–	30	kΩ	
5.5.17	Bias current into BHx	I_{BH}	–	–	150	µA	V_{BHx}-V_{SHx}=5...13V; no switching
5.5.18	Current between BHx and SHx	I_{BSH}	15	40	60	µA	V_{BHx}-V_{SHx}=5...13V; V_{SHX} = GND
5.5.19	Resistor between SHx and GND	R_{SHGN}	48	80	112	kΩ	
5.5.20	Bias current out of SL	I_{SL}	–	–	2	mA	0V<=VSH<=VS+1 V; no switching; V_{CBS}>5V

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 33 V, T_j = -40 °C to +150 °C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.21	Input propagation time (low on)	$t_{P(ILN)}$	50	–	200	ns	C=11nF; R_{Load}=1Ω
5.5.22	Input propagation time (low off)	$t_{P(ILF)}$	50	–	200	ns	
5.5.23	Input propagation time (high on)	$t_{P(IHN)}$	50	–	200	ns	
5.5.24	Input propagation time (high off)	$t_{P(IHF)}$	50	–	200	ns	
5.5.25	Absolute input propagation time difference between above propagation times	$t_{P(diff)}$	–	–	100	ns	
VREG							
5.5.26	VREG output voltage	V_{VREG}	11	12.5	14	V	V_{VS} >= 13,5V; I_{load}=37,5mA
5.5.27	VREG over current limitation	$I_{VREGOCL}$	100	–	500	mA	no activation of error; V_{VREG}>V_{VRSD}
5.5.28	Voltage drop between Vs and VREG	V_{VsVREG}	–	–	0.5	V	V_{VS}>= 7V; I_{load}=37,5mA; Ron operation

1) R_{Load} and C_{Load} in series
2) Not subject to production test; specified by design
3) Values above 33V not subjected to production test; specified by design
4) V_{diode} is the bulk diode of the external low side MOSFET
5) see **Chapter 9.2.14**

6 Shunt Signal Conditioning

The TLE7184F-3V incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. The gain of the OpAmp is adjustable by external resistors within a range higher than 5. The usage of high gains in the application might be limited by required settling time and band width.

It is recommended to apply a small offset to the OpAmp, to avoid operation close to the lower rail at low currents.

The output of the OpAmp ISO is not short-circuit proof.

In addition to the integrated operational amplifier, the TLE7184F-3V incorporates a comparator to detect over current situations. The output voltage V_{ISO} is compared to a reference voltage V_{OCTH} close to the upper rail of the 3.3V OpAmp supply (VDD). If V_{ISO} reaches this level an error is set.

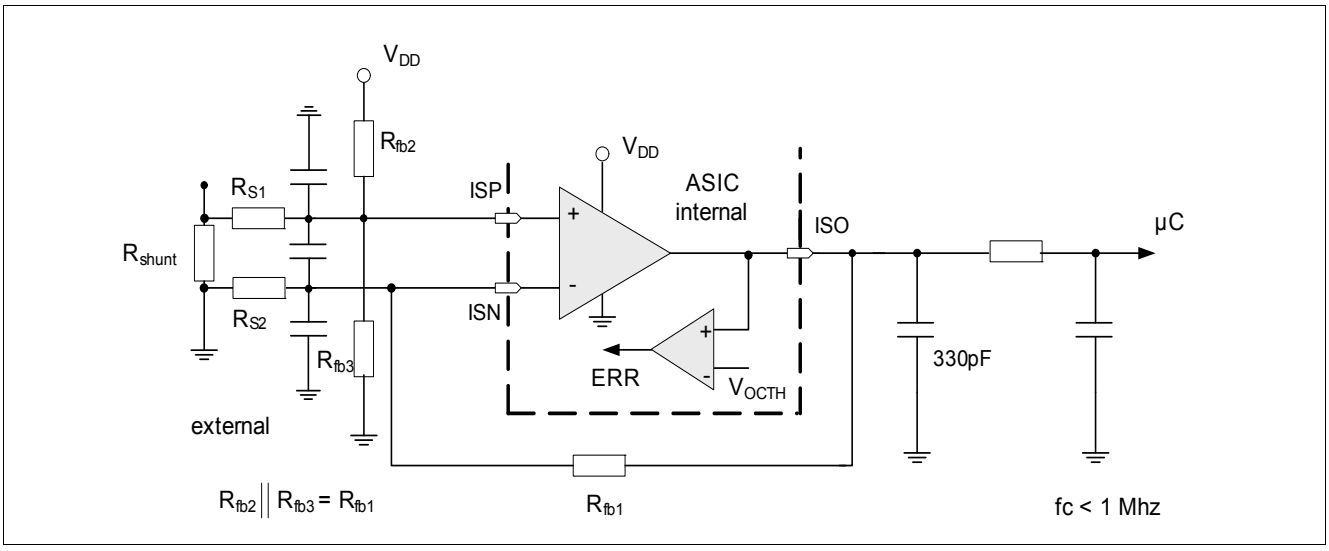


Figure 5 Shunt Signal Conditioning Block Diagram and Over Current Limitation

Over current shut down see **Chapter 9.2.12**.

6.1 Electrical Characteristics

Electrical Characteristics - Current sense signal conditioning

V_S = 6.0 to 33 V, T_j = -40 °C to +150 °C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.1	Series resistors	R_S	100	500	1000	Ω	–
6.1.2	Feedback resistor Limited by the output voltage dynamic range	R_{fb}	2000	7500	–	Ω	–
6.1.3	Resistor ratio (gain ratio), max. gain limited by settling time	$R_{fb/RS}$	5	–	–	–	R_L>3kΩ;
6.1.4	Input differential voltage (ISP - ISN)	V_{IDR}	-800	–	800	mV	–
6.1.5	Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	800	mV	–
6.1.6	Input offset voltage of the I-DC link OpAmp, including temperature drift	V_{IO}	–	–	+/-2	mV	R_S=500Ω; V_{CM}=0V; V_{ISO}=1.65V;

Electrical Characteristics - Current sense signal conditioning (cont'd)

V_S = 6.0 to 33 V, T_j = -40 °C to +150 °C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.7	Input bias current (ISN,ISP to GND)	I_{IB}	-300	–	–	µA	V_{CM}=0V; V_{ISO}=open
6.1.8	High level output voltage of ISO	V_{OH}	V_{VDD}-0.22	–	V_{VDD}	V	I_O=-3mA
6.1.9	Low level output voltage of ISO	V_{OL}	-0.1	–	0.22	V	I_O=3mA
6.1.10	Guaranteed output current capability	I_{GOC}	5	–	–	mA	–
6.1.11	Differential input resistance[2)]	R_I	100	–	–	kΩ	–
6.1.12	Common mode input capacitance[2)]	C_{CM}	–	–	10	pF	10kHz
6.1.13	Common mode rejection ratio at DC CMRR = 20*Log((Vout_diff/Vin_diff) * (Vin_CM/Vout_CM))	C_{MRR}	75	100	–	dB	–
6.1.14	Common mode suppression[3)2)] with CMS = 20*Log(Vout_CM/Vin_CM) Freq =100kHz Freq = 1MHz Freq = 10MHz	C_{MS}	–	 62 43 33	–	dB	V_{IN}=360mV* sin(2*π*freq*t); R_s=500Ω; R_{fb}=7500Ω
6.1.15	Slew rate	$d_{V/dt}$	–	10	–	V/µs	Gain>= 5; R_L=3kΩ; C_L=500pF
6.1.16	Large signal open loop voltage gain (DC)	A_{OL}	75	100	–	dB	–
6.1.17	Unity gain bandwidth	G_{BW}	10	20	–	MHz	R_L=3kΩ; C_L=100pF
6.1.18	Phase margin [2)]	F_M	–	50	–	°	Gain>= 5; R_L=3kΩ; C_L=100pF
6.1.19	Gain margin [2)]	A_M	–	12	–	dB	R_L=3kΩ; C_L=100pF
6.1.20	Bandwidth	B_{WG}	1.3	–	–	MHz	Gain=15; R_L=3kΩ; C_L=500pF; R_s=500Ω
6.1.21	Output settle time to 98% R_{fb}/R_S=15 R_{fb}/R_S=75	t_{set1}	 – –	 1 4.6	 1.8 8	µs	R_L=3kΩ; C_L=500pF; 0.3<V_{ISO}< VDD-0.3V; R_s=500Ω

1) A minimum capacitance of 100pF is needed at the output of the OpAmp (parasitic or real capacitor); R_L is the total load resistance including the feedback network; In the application it is not recommended to apply a resistor from the output ISO to GND directly in addition to the feedback network.

2) Not subject to production test; specified by design

3) Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

7 3.3 V Low Drop Voltage Regulator

The TLE7184F-3V incorporates a 3.3V LDO for µC supply. The voltage regulator is protected against Over Temperature by the central temperature sensor (see **Chapter 9.2.1** and **Chapter 9.2.2**). It has an integrated current limitation and Under Voltage detection.

Parameters for Under Voltage detection see **Chapter 9.2.4**.

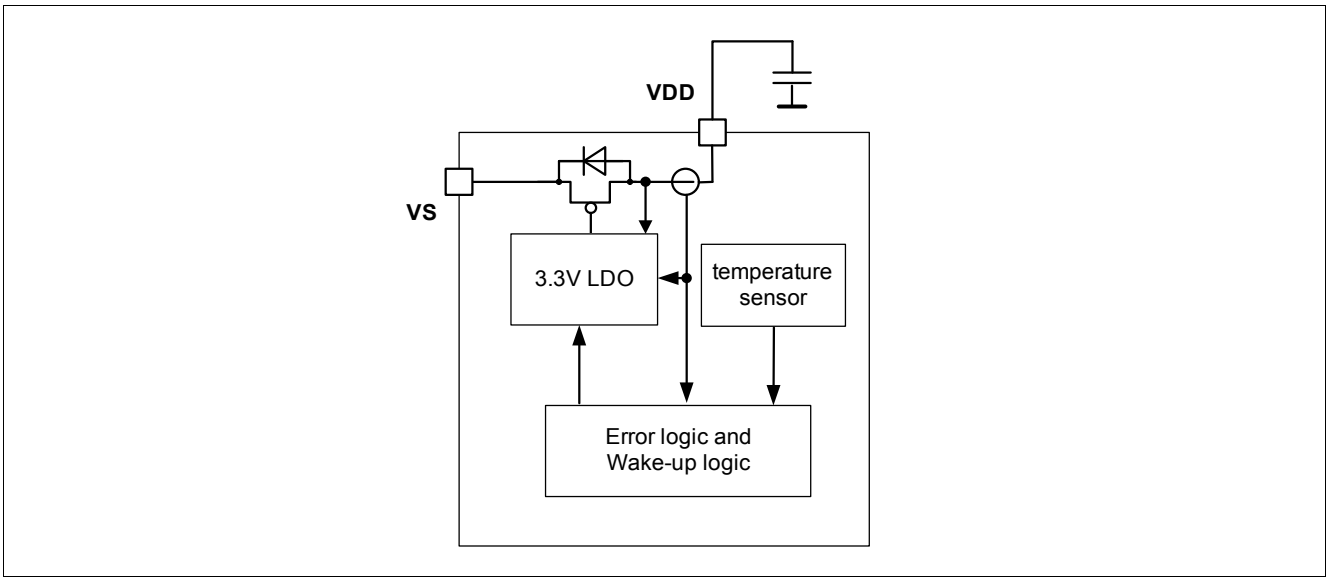


Figure 6 Block diagram of 3.3V LDO

7.1 Electrical Characteristics

Electrical Characteristics - Current sense signal conditioning

V_S = 6.0 to 45 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.1.1	Output voltage	V_{DD1}	3.15	3.35	3.53	V	2mA <=I_{load}<=70mA; C_{load}= 1...22uF[1)]
7.1.2	Output voltage	V_{DD2}	3.2	3.35	3.5	V	5mA <=I_{load}<=25mA; C_{load}= 1...22uF[1)]
7.1.3	LDO over current limitation	I_{OCL}	130	–	270	mA	no activation of error by current limitation
7.1.4	Load regulation	D_{VDD}	–	50	100	mV	I_{oad} step 0...20mA; C_{VDD}=1uF
7.1.5	Power supply ripple rejection[2)]	P_{SRR}	50	–	–	dB	100Hz sine wave; 0.5V_{pp} V_{VS}>=7V
7.1.6	Power supply ripple rejection[2)]	P_{SRR}	–	31	–	dB	100Hz sine wave; 0.5V_{pp} 6V<=V_{VS}<7V

1) ceramic C with 100nF with ESR<0.1Ω in parallel

2) Not subject to production test; specified by design

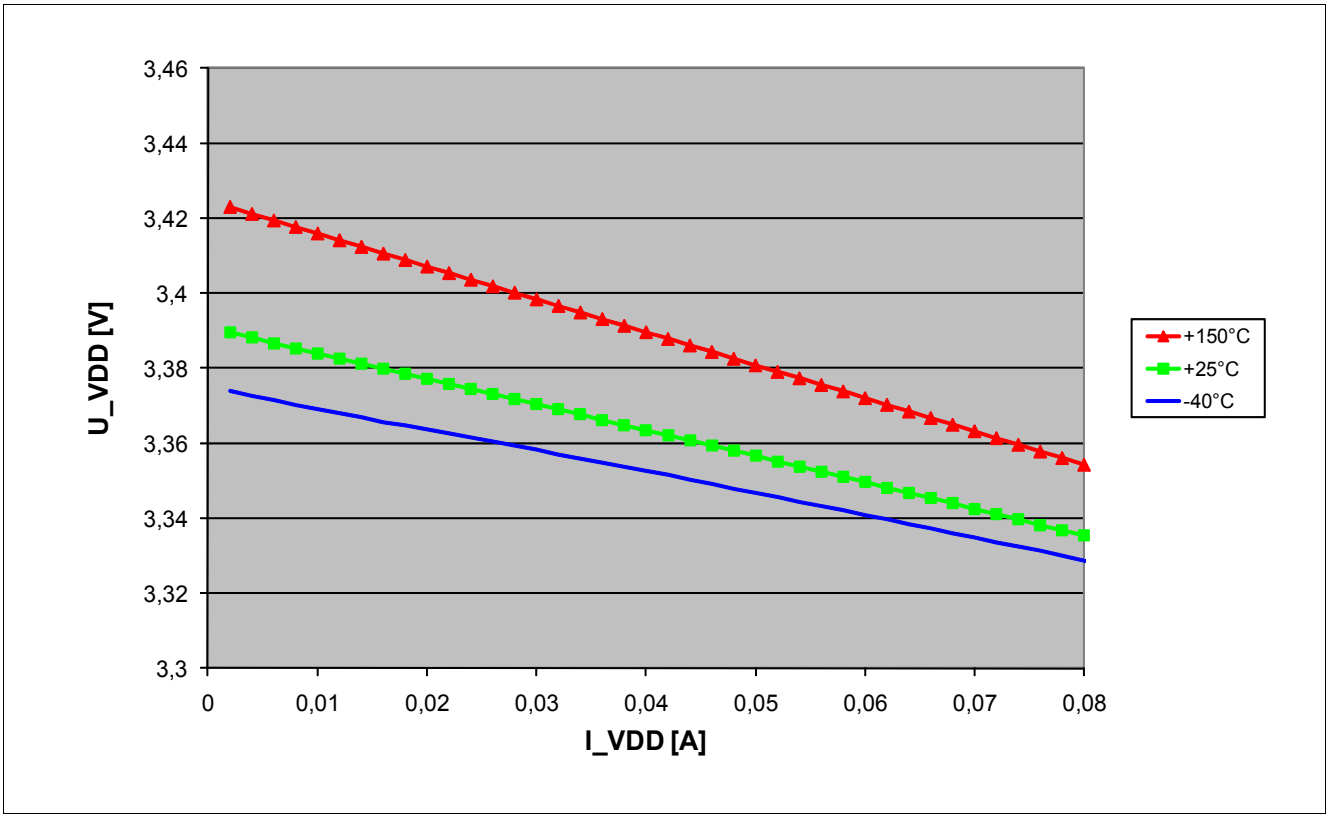


Figure 7 Typ. VDD output voltage vs. load current

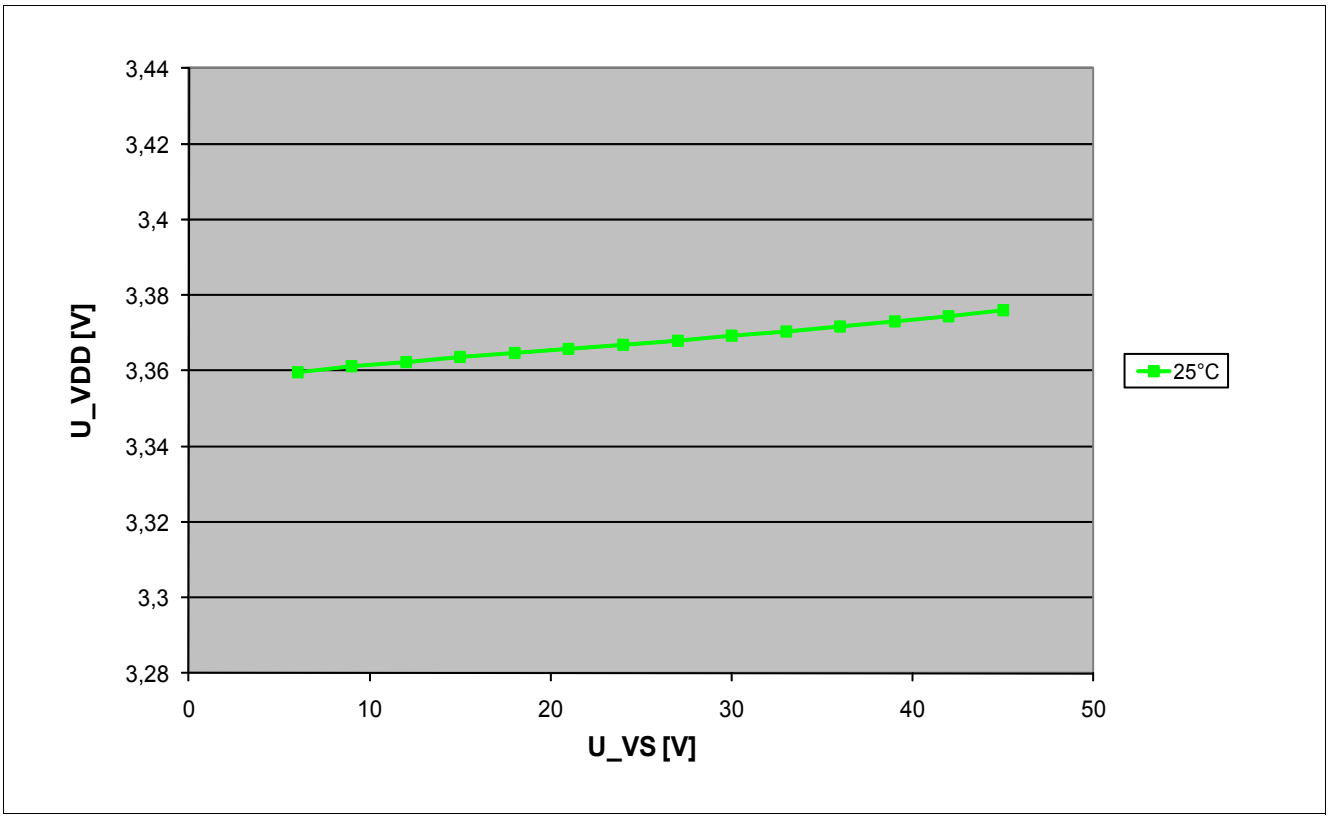


Figure 8 Typ. VDD output voltage vs. supply voltage

8 Interface, VDH Switch and $\overline{\text{INH}}$ Digital Output

8.1 PWM Interface (IFMA)

The TLE7184F-3V has an integrated interface supporting the typical PWM interface between a remote master ECU and the µC. The link to the external master ECU is a single wire communication based on the battery voltage and running typ. with about 10 to 400 Hz. The information is encoded in the duty cycle of the signal.

This communication line requires a signal conditioning to connect to the on board µC.

The integrated circuit supports the incoming data path.

The outgoing data path is formed by external components

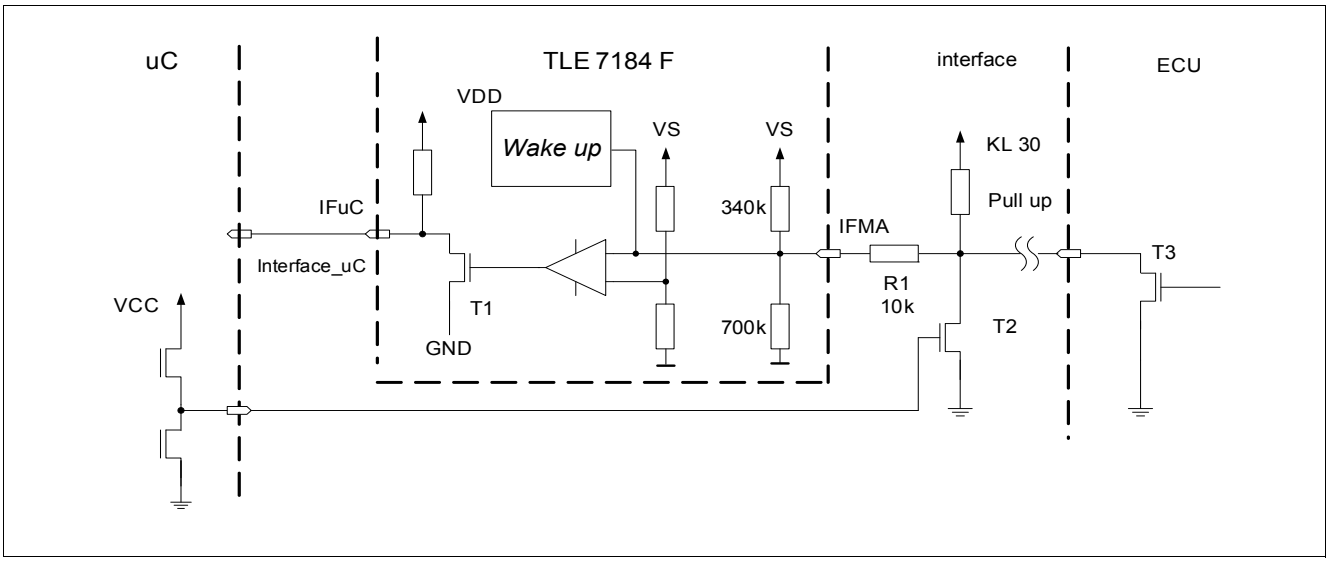


Figure 9 Structure PWM Interface

The integrated circuitry is described in **Figure 9**.

The main task of this interface is level shifting and protection of the µC.

The IFuC signal is following the IFMA signal, passing the duty cycle information from IFMA to the IFuC.

The µC port is used as input and is listening to the IFuC signal. The voltage at IFMA is monitored. If IFMA is low the IFuC open drain output is switched on - forcing the IFuC signal to low.

If IFMA is high, the IFuC open drain output is deactivated and the IFuC signal is pulled to high by the internal pull-up resistor.

The IFMA input is used as well for wake-up. See **Chapter 9.1**

Influence of serial resistor at IFMA pin

As shown in **Figure 9** a 10k resistor R1 is recommended to protect the IFMA pin against negative voltage levels coming from the interface signal. The integrated pull down and pull up resistors at the IFMA pin form an voltage divider together with the resistor R1. This will influence the resulting switching level of the IFMA interface in the application compared to the levels specified directly at the IFMA pin.

In this datasheet an additional parameter is provided to calculate the influence of the 10k resistor. The specified IFMA input current divided by Vs allows to calculate the drop over R1 with the following formula:

$$Voltage_drop_over_R1 = \frac{I_{IFMA}}{V_{VS}} * V_{VS} * R1$$

8.2 VDHS Switch

The System IC has an integrated switch connecting the VDH pin to the VDHS pin. This allows to place an external voltage divider for VDH voltage monitoring at the VDHS pin and to disconnect this voltage divider from VDH during sleep mode to assure low current consumption. The VDHS switch is only deactivated when the VDD regulator is switched off.

8.3 Digital Output $\overline{\text{INHD}}$

The System IC provides a digital output $\overline{\text{INHD}}$ showing the logic state of $\overline{\text{INH}}$ (e.g. KL15) after a complete wake-up of the driver (approx. 1ms). The input levels of $\overline{\text{INH}}$ for the $\overline{\text{INHD}}$ output are defined separately from the levels for wake-up. Voltage levels for $\overline{\text{INH}}$ wake-up function please see **Chapter 9.4** section Wake-up and go-to-sleep. The output stage consists of an integrated low side switch with a pull-up resistor to VDD.

8.4 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

V_S = 6.0 to 20V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Interface - static parameters							
8.4.1	IFMA input voltage high level (for IFµC high)	V_{IMHL}	59	–	–	%	of V_{VS}; IC not in Sleep Mode
8.4.2	IFMA input voltage low level (for IFµC low)	V_{IMLL}	–	–	46	%	of V_{VS}; IC not in Sleep Mode;
8.4.3	IFMA input hysteresis (for IFµC)	V_{IMhy}	0.5	–	9	%	of V_{VS}; IC not in Sleep Mode
8.4.4	IFMA wake up voltage high level = V_S-V_{IFMA}	V_{IMWH}	2	–	4	V	valid in Sleep Mode
8.4.5	IFMA low time to guarantee wake up	t_{IFlow}	100	–	–	µs	V_{VS}=7...20V
8.4.6	IFMA internal pull-up resistor to V_S	R_{IMu}	210	340	495	kΩ	–
8.4.7	IFMA internal pull-down resistor to GND	R_{IMd}	420	700	980	kΩ	not active in Sleep Mode
8.4.8	IFMA input current related to VS V_{IFMA} = 59% of V_{VS} V_{IFMA} = 46% of V_{VS}	I_{IFMA}/V_{VS}	 -2.0 -3.0	 – –	 +2.0 +1.0	µA/V	–
8.4.9	IFµC output low voltage	V_{IuLL}	–	–	0.5	V	no external load
8.4.10	IFµC internal pull-up resistor to V_{DD}	R_{Iu}	8.5	–	23	kΩ	–
Interface - dynamic parameters							
8.4.11	IFµC duty cycle	d_{Iu}	0	–	100	%	–
8.4.12	Propagation time rising edge IFµC	t_{PRE}	–	–	6	µs	Including rise time to 80% of V_{VDD}; C_{load}=100pF
8.4.13	Propagation time falling edge IFµC	t_{PFE}	–	–	5	µs	Including fall time to 20% of V_{VDD}; C_{load}=100pF

Electrical Characteristics - Protection and diagnostic functions (cont'd)

V_S = 6.0 to 20V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.14	Deviation between rising and falling IFµC	t_{PD}	–	–	4	µs	C_{load}=100pF
VDH switch							
8.4.15	Ron VDH switch	R_{VDH}	–	–	150	Ω	Load current = 1mA
$\overline{\text{INHD}}$ digital output							
8.4.16	Low level input voltage $\overline{\text{INH}}$ (for $\overline{\text{INHD}}$=low)	V_{INHDL}	–	–	1.5	V	–
8.4.17	High level input voltage $\overline{\text{INH}}$ (for $\overline{\text{INHD}}$=high)	V_{INHDH}	2.2	–	–	V	–
8.4.18	Input hysteresis of $\overline{\text{INH}}$ for $\overline{\text{INHD}}$[1)]	d_{VINHD}	100	–	–	mV	–
8.4.19	$\overline{\text{INHD}}$ low level output voltage	V_{INHD}	–	–	0.5	V	no external load
8.4.20	$\overline{\text{INHD}}$ Internal pull-up resistor to V_{DD}	R_{INHD}	42.5	–	115	kΩ	–

1) Not subject to production test; specified by design

9 Description of Modes, Protection and Diagnostic Functions

9.1 Description of modes

The operation of TLE7184F-3V can be described by different operation modes

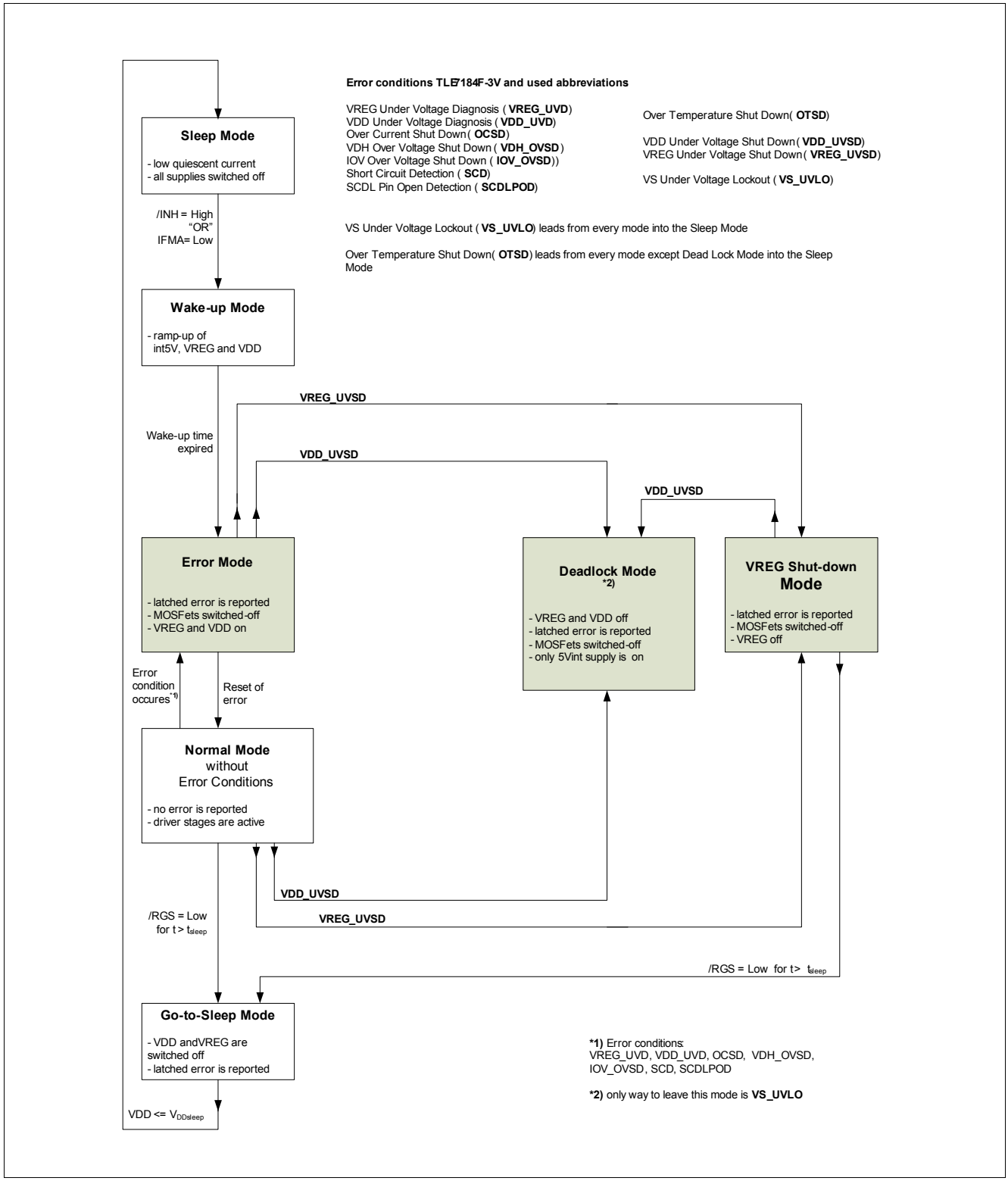


Figure 10 State diagram TLE7184F-3V

Sleep Mode:

The sleep mode is entered if the device is in the Go-to-sleep Mode and the VDD voltage is lower than $V_{DDsleep}$. The complete chip is deactivated beside the wake-up function (see Wake-up Mode). This mode is designed for lowest current consumption from the power net of the car. The passive clamping is active. For details see the description of passive clamping, see **Chapter 9.2.14**.

The only way to leave the Sleep Mode is to go to the Wake-up Mode.

Wake-up Mode:

The TLE7184F-3V wakes up if $\overline{INH}$ (=KL15) is high or if IFMA is low and V_{VS} is higher than V_{VSLO}.

In this mode all supplies are ramping up. As soon as the internal 5V is available, a so called wake-up timer starts to run. If the IC reaches this state, the wake-up will continue even if the wake-up signals at $\overline{INH}$ or IFMA disappear. The PWM interface (IFMA) is active as soon as the VDD voltage is sufficiently high. During this time it is expected that the supplies are powered up and the µC sets the $\overline{RGS}$ to high. All external MOSFETs are switched off actively or passively. When the wake-up timer is expired the IC goes into the Error mode.

In this mode all errors will be ignored beside Over Temperature Shut Down or V_S Under Voltage Lockout.

Error Mode

The Error Mode can be reached in 2 different ways:

1. The device is in Wake-up Mode and the wake-up timer expires
2. The device is in Normal Mode and one or more of the following errors occur: VREG Under Voltage Shut Down, VDD Under Voltage Shut Down, Over Current Shut Down, VDH Over Voltage Shut Down, IOV Over Voltage Shut Down, Short Circuit Detection or SCDL Open Detection.

In this mode an Error is set at the ERROR Pin and all external MOSFETs are actively switched off as long as the bootstrap voltages allows it. The interface is active. VDHS switch is on and the current sense functions are working. VDD and VREG are active. Passive clamping is not active.

The Error mode can be left in the following ways:

1. If no error is present, the IC can be sent to Normal Mode by a reset with the $\overline{RGS}$ pin.
2. If a VREG Under Voltage Shut Down occurs the device will go to VREG Shut-down Mode.
3. If VDD Under Voltage Shut Down occurs the device will go into Deadlock Mode.

Normal Mode

The Normal Mode can be reached by:

1. The device is in Error Mode, no error is present and a reset is performed by the $\overline{RGS}$ pin.

In the Normal Mode all functions are active and available with the regular limitations of the bootstrap principle. The gate drive output stages can be controlled with the input pins.

The Normal Mode can be left in 4 ways:

1. The devices goes to the Go-To-Sleep Mode by setting $\overline{RGS}$ to low for a time longer than t_{sleep}.
2. If a VREG Under Voltage Shut Down occurs the device will go to VREG Shut-down Mode.
3. If VDD Under Voltage Shut Down occurs the device will go into Deadlock Mode.
4. If one or more of the following errors occur, the device goes to the Error Mode: VREG Under Voltage Shut Down, VDD Under Voltage Shut Down, Over Current Shut Down, VDH Over Voltage Shut Down, IOV Over Voltage Shut Down, Short Circuit Detection or SCDL Open Detection.

Go-To-Sleep Mode

The Go-To-Sleep Mode can be reached in 2 different ways:

1. The device is in Normal Mode and $\overline{RGS}$ is set to low for a time longer than t_{sleep}.
2. The device is in VREG Shut-down Mode and $\overline{RGS}$ is set to low for a time longer than t_{sleep}.

In this mode all external MOSFETs are actively or passively switched off. An Error is set and is shown as long as VDD is sufficient high. In this mode VDD and VREG is switched off. As soon as VDD voltage reaches the $V_{VDDsleep}$ level the IC goes into the Sleep Mode.

Deadlock Mode

This mode is intended to prevent the IC for long time toggling in Over Temperature if a short is present at the VDD pin.

There are 3 ways to enter this mode:

1. The IC is in Error Mode and a VDD Under Voltage Shut Down occurs.
2. The IC is in Normal Mode and a VDD Under Voltage Shut Down occurs.
3. The IC is in VREG Shut Down Mode and a VDD Under Voltage Shut Down occurs.

In this mode VDD and VREG regulators are switched off. The gates of the external MOSFETs are passively clamped.

The VDHS switch is deactivated.

The IC will not react to IFMA or $\overline{INH}$ signals. Even a Over Temperature Shut Down detection will have no influence.

The internal logic is supplied and prevents the IC from going into “Go-to-Sleep Mode”.

The only way to leave this state is that VS is lower than V_{VSLO}, means a VS Under Voltage Lockout occurs. In this case the IC goes to Sleep Mode.

VREG Shut Down Mode

This mode is intended to prevent the IC from long time toggling in Over Temperature if a short is present at the VREG pin.

There are 2 ways to enter this mode:

1. The IC is in the Error Mode and a VREG Under Voltage Shut-down occurs.
2. The IC is in the Normal Mode and a VREG Under Voltage Shut-down occurs.

In this mode VREG is switched off, but VDD is still present. The VDHS switch is still active and the PWM interface (IFMA) is working.

The IC will not react to IFMA or $\overline{INH}$ signals.

In this situation the µC is still able to provide diagnostic information by the interface. It can prevent the IC from Go-to-Sleep Mode and can avoid unintended toggling as long there is no Over Temperature Shut Down.

This state can be left by 2 ways:

1. The µC has to set $\overline{RGS}$ to low for a time longer than t_{sleep}. In this case the IC goes to Sleep Mode.
2. If a VDD Under Voltage Shut Down occurs the IC will go into the Deadlock Mode.

9.2 Protection and Diagnosis Functions

9.2.1 Over Temperature Shut Down (OTSD)

If the junction temperature is exceeding the Over Temperature shut down level an error signal is set. The driver IC will pull down the gate-source voltage of all external MOSFETs, deactivate the VDD and VREG supply and go directly into the Sleep Mode.

In the Sleep Mode the regular wake-up conditions will be used. Over Temperature cycling is possible and will lead to accelerated aging of the IC.

In Deadlock Mode an Over Temperature Shut Down is ignored.

9.2.2 Analog Temperature Monitoring

The TEMP output of the TLE7184F-3V provides an analog voltage signal proportional to the chip temperature. This function is not available in Deadlock Mode.

9.2.3 VS Under Voltage Lockout (VS_UVLO)

The TLE7184F-3V has an integrated VS Under Voltage Lockout to assure that the behavior of the complete IC is predictable in all supply voltage ranges.

If the supply voltage at VS reaches the Under Voltage shut down level V_{VSLO} for a minimum specified filter time the IC goes into Go-to-Sleep Mode and finally into Sleep Mode.

9.2.4 VDD Under Voltage Diagnosis (VDD_UVD)

The TLE7184F-3V has an integrated VDD Under Voltage Diagnosis to assure that the behavior of the bridge driver output stages is predictable in all supply voltage ranges.

If the voltage at VDD reaches the Under Voltage diagnosis level V_{UVVDD} for a minimum specified filter time, an error is set and the IC goes into Error Mode.

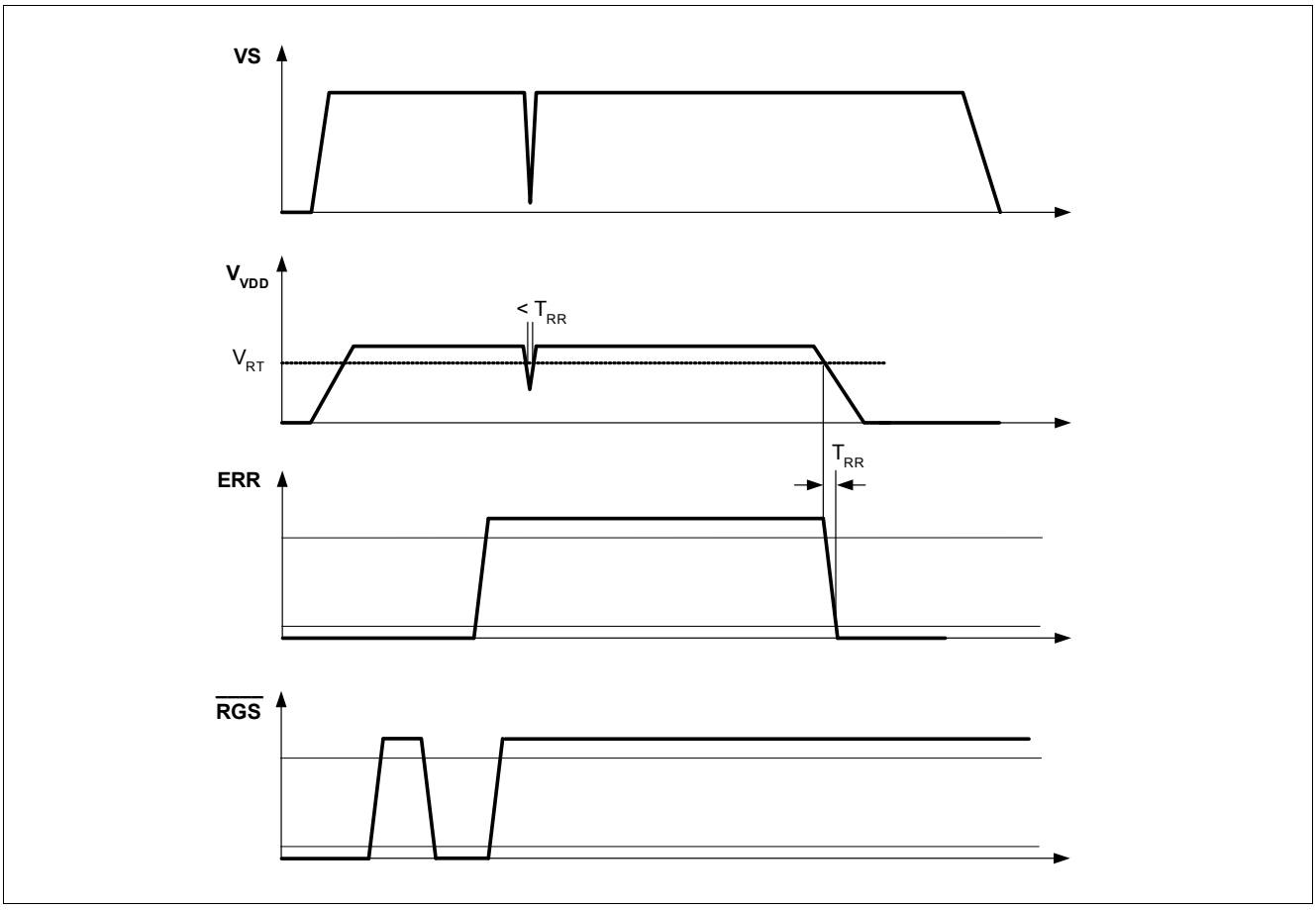


Figure 11 Timing of VDD Under Voltage Diagnosis

9.2.5 VDD Under Voltage Shut Down (VDD_UVSD)

The TLE7184F-3V has an integrated VDD Under Voltage Shut Down to avoid operation with VDD shorted to GND.

If the supply voltage at VDD reaches the Under Voltage shut down level $V_{VDDsleep}$ and the wake-up time is expired, VREG and VDD will be switched off and the IC will go to the Deadlock Mode.

9.2.6 VREG Under Voltage Diagnosis (VREG_UVD)

The TLE7184F-3V has an integrated VREG Under Voltage Diagnosis to assure that the behavior of the bridge driver output stages is predictable in all supply voltage ranges.

If the voltage at VREG reaches the Under Voltage diagnosis level V_{UVVR} for a minimum specified filter time an error is set the IC goes into Error Mode.

As long as the VS Under Voltage Lock Out is not reached, the low side MOSFETs will stay actively switched off. The status of the high side MOSFET drivers is dependent on the bootstrap voltage - which depends on the SHx voltage. It is expected that the SHx nodes will be pulled to VDH level by the high side MOSFETs and this will switch off the high side MOSFETs passively.

In this situation the short circuit detection of this output stage is deactivated to avoid wrong error reporting.

9.2.7 VREG Under Voltage Shut Down (VREG_UVSD)

The TLE7184F-3V has an integrated VREG Under Voltage Shut Down to avoid operation with VREG shorted to GND.

If the supply voltage at VREG reaches the Under Voltage shut down level V_{VRSD} “AND” the wake up time is expired, VREG will be switched off and the IC will go to the VREG Shut Down Mode. In this condition the µC is still supplied and can communicate via the PWM interface (IFMA), the MOSFETs are switched off and an error is set. The only way to leave this mode is to go to “Sleep Mode”.

9.2.8 IOV and VDH Over Voltage Shut Down (IOV_OVSD, VDH_OVSD)

The TLE7184F-3V has an integrated Over Voltage shut down to minimize the risk of destruction of the IC at high supply voltages caused by violation of the maximum ratings.

The voltages are observed at the Over Voltage input pin IOV and at the VDH pin. If the voltage at the IOV pin or at the VDH pin exceeds the Over Voltage shut down level for more than the specified filter time, the IC goes into Error Mode.

The effective Over Voltage level can be adjusted by a voltage divider at the IOV pin. This voltage devider is normally supplied by the VDHS pin. The Over Voltage level at VDH is fix.

9.2.9 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side MOSFETs are not “on” at the same time, connecting the battery voltage directly to GND. The dead time generated in the TLE7184F-3V is set to a minimum value if the DT pin is connected to GND. This function assures a minimum dead time if a common input signal for ILx and $\overline{\text{IHx}}$ is used.

The dead time can be increased by connecting the DT pin via a dead time resistor R_{DT} to GND. Larger dead time resistors result in a longer dead time.

The typical dead time can be calculated with the following formula:

$$t_{deadtime} = \frac{0.081}{0.02 + {}^{2.4}\!/_{4+Rdt}}\,\mu s$$

Please put in the R_{dt} in kΩ.

If an exact dead time of the bridge is needed, the use of the µC PWM generation unit is recommended.

In case of an open DT pin, the dead time is set to the internal maximum value.

In addition to this dead time, the TLE7184F-3V provides a locking mechanism avoiding that both external MOSFETs of one half bridge can be switched on at the same time. This functionality is called shoot through protection.

If the command to switch on both high and low side switches in the same half bridge is given at the input pins, the command will be ignored. The outputs will stay in the state like before the conflicting input.

9.2.10 Short Circuit Protection (SCP)

The TLE7184F-3V provides a short circuit protection for the external MOSFETs. It is monitoring of the drain-source voltage of the external MOSFETs. (see **Figure 3**)

The drain-source voltage monitoring for a certain external MOSFET is active as soon as the corresponding driver output stage is set to “on” and the dead time and the blanking time is expired.

The blanking time starts when the dead time is expired and assures that the switch on process of the MOSFET is not taken into account. It is recommended to keep the switching times of the MOSFETs below the blanking time.

The short circuit detection level is adjustable in an analogue way by the voltage setting at the SCDL pin. There is a 1:1 translation between the voltage applied to the SCDL pin and the drain-source voltage limit. E.g. to trigger the SCD circuit at 1 V drain-source voltage, the SCDL pin must be set to 1 V as well. The drain-source voltage limit can be chosen between 0.3 ... 2 V.

In the case that after the expiration of the blanking time the drain source voltage of the observed MOSFET is still higher then the SCDL level, the SCD filter time t_{SCP} starts to run. A capacitor is charged with a current. If the capacitor voltage reaches a specific level (filter time t_{SCP}), the error signal is set and the IC goes into Error Mode. If the SCD condition is removed before the SC is detected, the capacitor is discharged with the same current. The discharging of the capacitor happens as well when the MOSFET is switched off. It has to be considered that the high side and the low side outputs of one phase are working with the same capacitor.

9.2.11 SCDL Pin Open Detection (SCDL_open)

For safety reasons a pull-up resistor at the SCDL pin assures that in case of an open pin the SCDL voltage is pulled to a high level. In this case an error is set and the IC goes into Error Mode.

9.2.12 Over Current Shut Down (OCSD)

The TLE7184F-3V is monitoring the output signal of the operational amplifier. If the output signal reaches a specified level close to the upper rail (VDD) for a specified time, the System IC detects an over current condition and sets an error signal. The driver output pulls down the gate-source voltage of all external MOSFETs actively and stays in the Error Mode.

9.2.13 VDD Current Limitation

The TLE7184F-3V has an integrated voltage supply for an external µC. The output current of the supply is limited to a specified value. This limitation does not cause any error reporting. In this situation a VDD Under Voltage detection is likely. If the current is limited for a longer time, the Over Temperature protection will react.

9.2.14 Passive Gxx Clamping

If VS Under Voltage Lock Out is detected or the device is in Sleep Mode, a passive clamping is active as long as the voltage at VS or VDH is higher than 3V. Even below 3V it is assured that the MOSFET driver stage will not switch on the MOSFET actively.

The passive clamping means that the BHx and the VREG pin are pulled to GND with specified pull down resistors. Together with the intrinsic diode of the push stage of the output stages which connect the gate output to BHx respectively VREG, this assures that the gate of the external MOSFETs are not floating.

9.3 $\overline{\text{ERR}}$ Pin

The TLE7184F-3V has a status pin to provide diagnostic feedback to the µC. The logical output of this pin is an open drain output with integrated pull-down resistor to GND (see **Figure 12**).

Reset of error registers and Disable

The TLE7184F-3V can be reset by the enable pin $\overline{RGS}$. If the $\overline{RGS}$ pin is pulled to low for a specified minimum time, the error registers are cleared. If the error is still existing when the $\overline{RGS}$ pin is pulled to low, no reset will be performed and the $\overline{ERR}$ pin stays low.

Figure 13 describes the timing behavior during error reset:

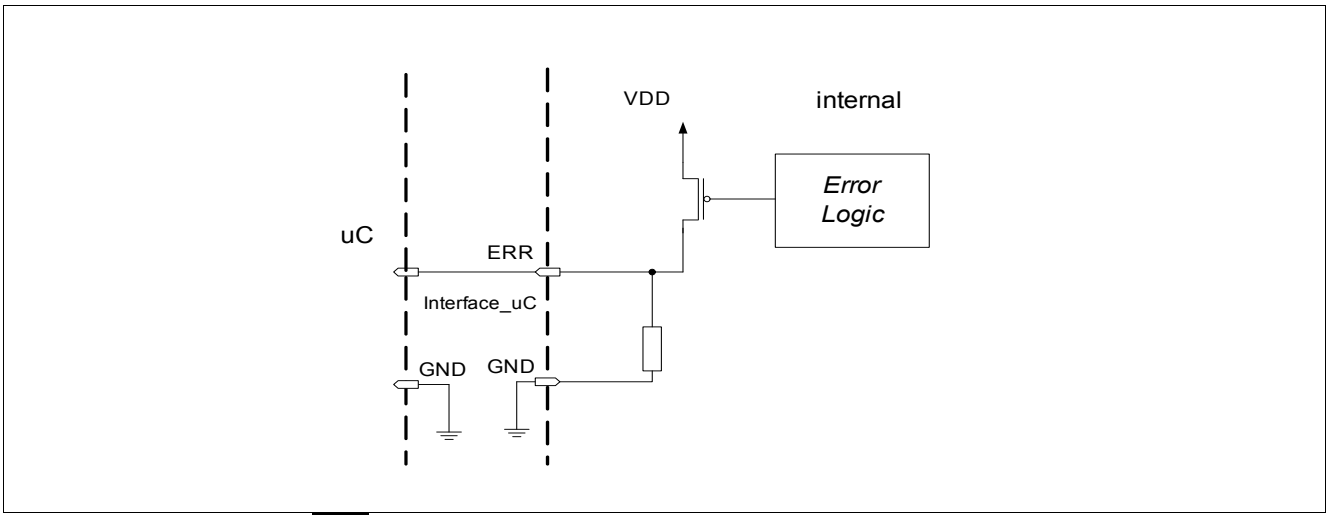


Figure 12 Structure of $\overline{ERR}$ output

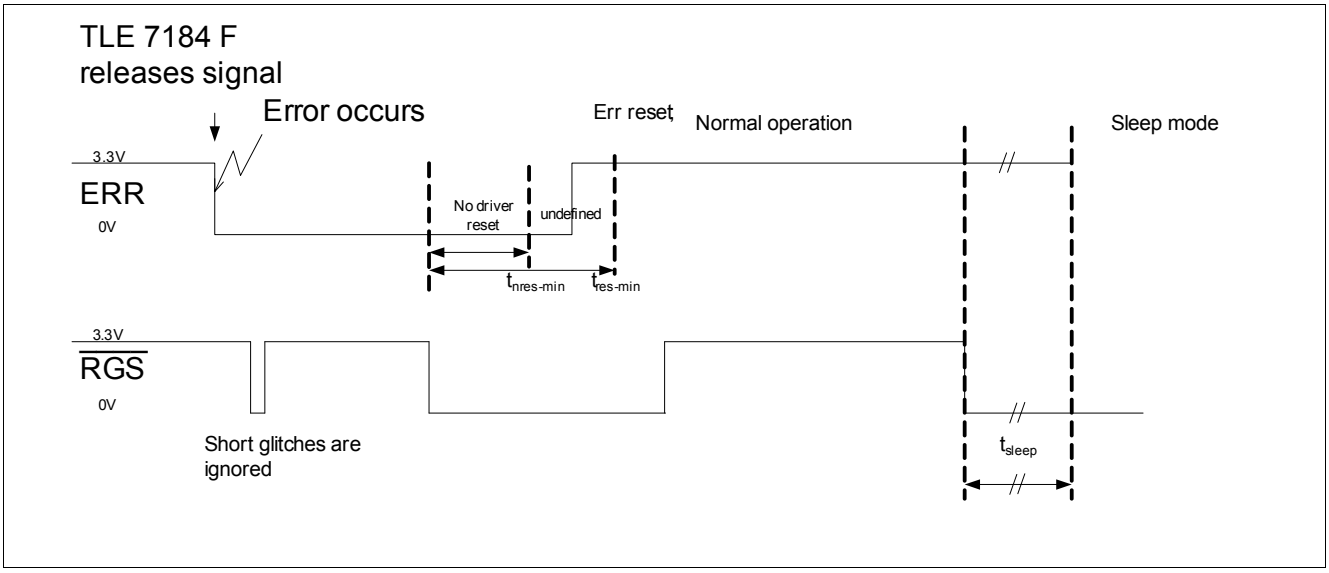


Figure 13 Enable / Disable timing

9.4 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

V_S = 7.0 to 33V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Dead time							
9.4.1	Programmable internal dead time	t_{DT}	0.095 0.29 0.85 1.2 2.1	0.14 0.42 1.21 1.88 3.62	0.18 0.55 1.55 2.6 5.1	µs	R_{DT}=0 Ω R_{DT}=10 kΩ R_{DT}=47 kΩ R_{DT}=100 kΩ R_{DT}=1000 kΩ
9.4.2	Max. internal dead time	t_{DT_MAX}	2.0	4.0	6.0	µs	DT pin open
9.4.3	Dead time deviation between channels	d_{tDT}	-20	–	20	%	–
			-15	–	15	%	R_{DT}<=47 kΩ
9.4.4	Dead time deviation between channels LSoff -> HS on	d_{tDTH}	-14	–	14	%	–
			-12	–	12	%	R_{DT}<=47 kΩ
9.4.5	Dead time deviation between channels HSoff -> LS on	d_{tDTL}	-14	–	14	%	–
			-12	–	12	%	R_{DT}<=47 kΩ
Short circuit protection							
9.4.6	Short circuit protection detection level	V_{SCPDL}	0.3	–	2	V	programmed by SCDL pin
9.4.7	Short circuit protection detection Accuracy	A_{SCP}	-20	–	+20	%	0.3V<= V_{SCDL}<0.9V
9.4.8	Short circuit protection detection Accuracy	A_{SCP}	-10	–	+10	%	0.9V<= V_{SCDL}<=2.0V
9.4.9	Filter time of short circuit protection	$t_{SCP(off)}$	2.3	–	4.3	µs	Ixx static on
9.4.10	Blanking time plus filter time of short circuit detection	t_{SCPTT}	4	–	8	µs	Ixx switching “off” to “on”
9.4.11	Internal pull-up resistor SCDL to V_{DD}	R_{SCDL}	180	300	420	kΩ	–
9.4.12	SCDL open pin detection level	V_{SCPOP}	2.0	–	2.5	V	–
9.4.13	Filter time of SCDL open pin	t_{SCPOP}	1	–	3.4	µs	–
9.4.14	SCDL open pin detection level hysteresis[2)]	V_{SCOPH}	–	0.3	–	V	–
Over- and Under Voltage monitoring							
9.4.15	Over Voltage shut down at IOV	V_{OVIOV}	4.15	–	4.4	V	IOV voltage increasing
9.4.16	Pull down resistor at IOV to GND	R_{IOV}	300	–	700	kΩ	–
9.4.17	Over Voltage shut down at VDH	V_{OVVDH}	33	–	37	V	VDH increasing
9.4.18	Over Voltage shut down filter time for IOV or VDH	t_{OV}	13	–	23	µs	–
9.4.19	Under Voltage diagnosis at VREG	V_{UVVR}	5.5	–	6.5	V	VREG decreasing

Electrical Characteristics - Protection and diagnostic functions (cont'd)

V_S = 7.0 to 33V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.4.20	Under Voltage diagnosis filter time for VREG	t_{UVVR}	10	–	30	µs	–
9.4.21	Under Voltage shut down at VREG	V_{VRSD}	1.5	–	2.3	V	VREG decreasing
9.4.22	Under Voltage lockout at VS	V_{VSLO}	4.4	5.0	5.5	V	V_{VS} decreasing
9.4.23	Under Voltage lockout filter time for VS	t_{UVLO}	1	–	3	µs	–
$\overline{\text{ERR}}$ pin[1]							
9.4.24	$\overline{\text{ERR}}$ output voltage	V_{ERR}	2.9	–	–	V	No external load
9.4.25	Rise time $\overline{\text{ERR}}$ (20 - 80% of internal 5V)	$t_{f(ERR)}$	–	–	3.5	µs	C_{LOAD}=1nF
9.4.26	Internal pull-down resistor $\overline{\text{ERR}}$ to GND	$R_{f(ERR)}$	21.2	–	60	kΩ	–
Reset and Enable							
9.4.27	Low time of uC $\overline{\text{RGS}}$ signal without reset	t_{nres}	–	–	0.5	µs	–
9.4.28	Low time of uC $\overline{\text{RGS}}$ pin necessary to trigger reset and to clear error registers	t_{res}	3	–	–	µs	–
Wake-up and go-to-sleep							
9.4.29	Low level input voltage of $\overline{\text{RGS}}$	V_{RGSLL}	–	–	1.6	V	–
9.4.30	High level input voltage of $\overline{\text{RGS}}$	V_{RGSHL}	2.8	–	–	V	–
9.4.31	Input hysteresis of $\overline{\text{RGS}}$[2]	d_{RGS}	100	–	–	mV	–
9.4.32	$\overline{\text{RGS}}$ pull-down resistors to GND	R_{RGS}	100	–	210	kΩ	–
9.4.33	Low level input voltage of $\overline{\text{INH}}$[3] for wake up	V_{INHL}	–	–	0.75	V	–
9.4.34	High level input voltage of $\overline{\text{INH}}$[3] for wake up	V_{INHH}	2.1	–	–	V	–
9.4.35	$\overline{\text{INH}}$ high time to guarantee wake-up	V_{IHhigh}	100	–	–	µs	–
9.4.36	$\overline{\text{INH}}$ pull-down resistors to GND	R_{INH}	100	–	210	kΩ	–
9.4.37	Wake up delay time	t_{wake}	9	–	17	ms	
9.4.38	$\overline{\text{RGS}}$ low time for go-to-sleep	t_{sleep}	20	–	50	µs	
9.4.39	V_{DD} voltage for changing from Go-to-Sleep Mode to Sleep Mode	$V_{DDsleep}$	1.5	–	2.3	V	–
9.4.40	V_{DD} Under Voltage Shut Down	$V_{UVSDVDD}$	1.5	–	2.3	V	–

1) $\overline{\text{ERR}}$ pin and Reset & Enable functional between V_{VS}=6 ... 7V, but characteristics might be out of specified range

2) Not subject to production test; specified by design

3) These levels are valid for wake up of the IC. The input levels for $\overline{\text{INH}}$ deciding the output state of $\overline{\text{INHD}}$ are shown in Chapter 8.4

Electrical Characteristics - Protection and diagnostic functions

V_S = 6.0 to 33V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Temperature monitoring							
9.4.41	Over Temperature shut down	$T_{j(SD)}$	160	170	180	°C	1)–
9.4.42	Analog temperature output at 25°C	V_{ATRT}	1.32	–	1.65	V	C_{load}<=1.5nF; T_j=25°C
9.4.43	Analog temperature output coefficient	K_{ATRT}	4.57	–	5.20	mV/K	C_{load}<=1.5nF 1)
9.4.44	Analog temperature output drift over lifetime[1)]	V_{ATRTd}	0	–	+6	mV	C_{load}<=1.5nF
9.4.45	Analog temperature range[1)]	T_{AT}	-40	–	175	°C	–
Over current detection							
9.4.46	Over current detection level in% of V_{VDD}	V_{OCTH}	92	–	96.5	%	–
9.4.47	Filter time for over current detection	t_{OC}	1.8	–	4.2	µs	–
Under Voltage monitoring VDD							
9.4.48	Under Voltage shut down at V_{DD}[2)]	V_{UVVDD}	2.4	–	2.85	V	V_{VDD} decreasing
9.4.49	Under Voltage shut down filter time	t_{UVVDD}	15	–	45	µs	–

1) Not subject to production test; specified by design

2) For Under Voltage detection level during go-to-sleep see $V_{DDsleep}$

10 Application Description

In the automotive sector there are more and more applications requiring high performance motor drives, such as HVAC fans, engine cooling fans, pumps etc.. In these applications 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

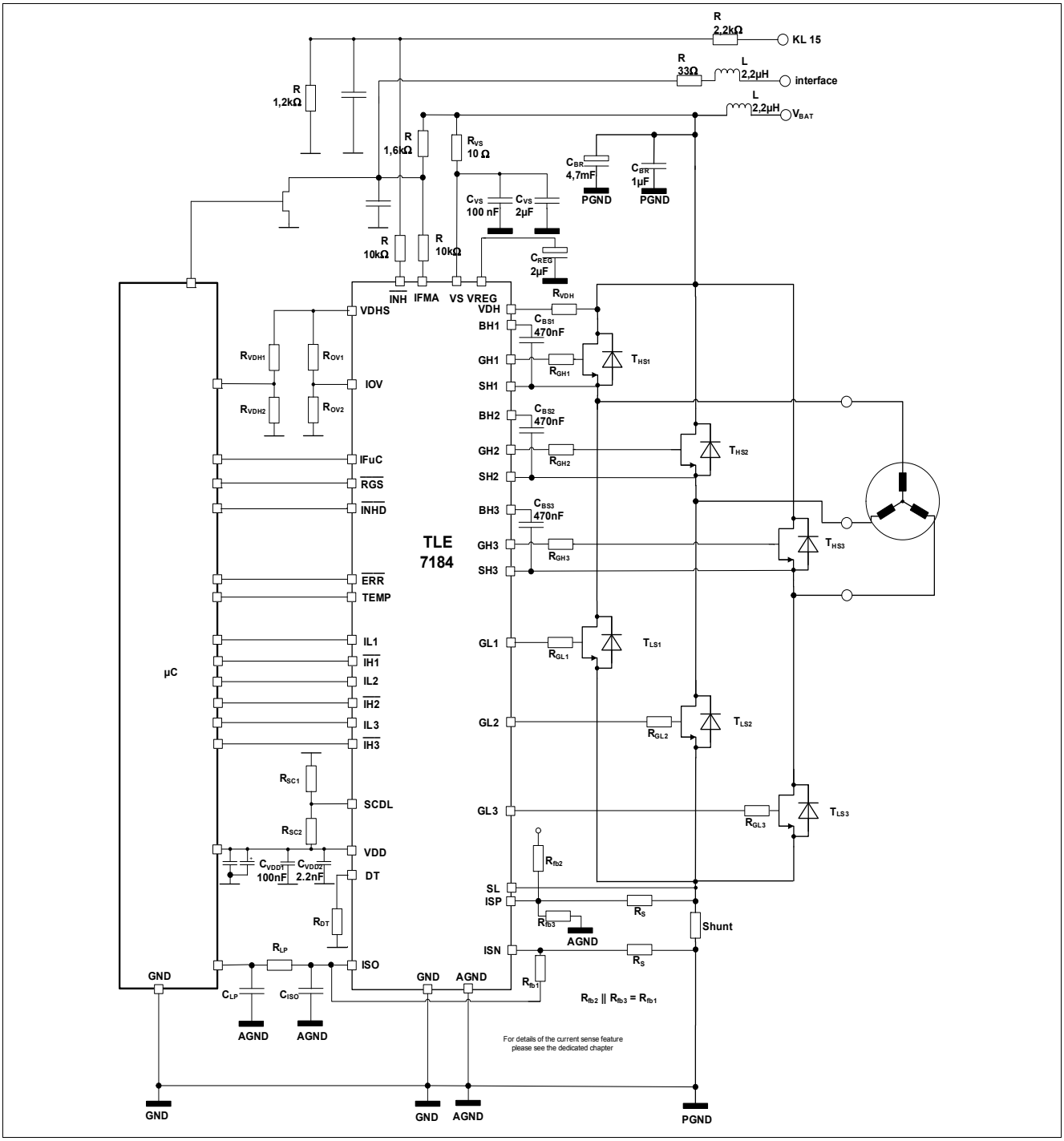


Figure 14 Application Circuit TLE7184F-3V

Note: This is a simplified example of an application circuit. The function must be verified in the real application

11 Package Outlines

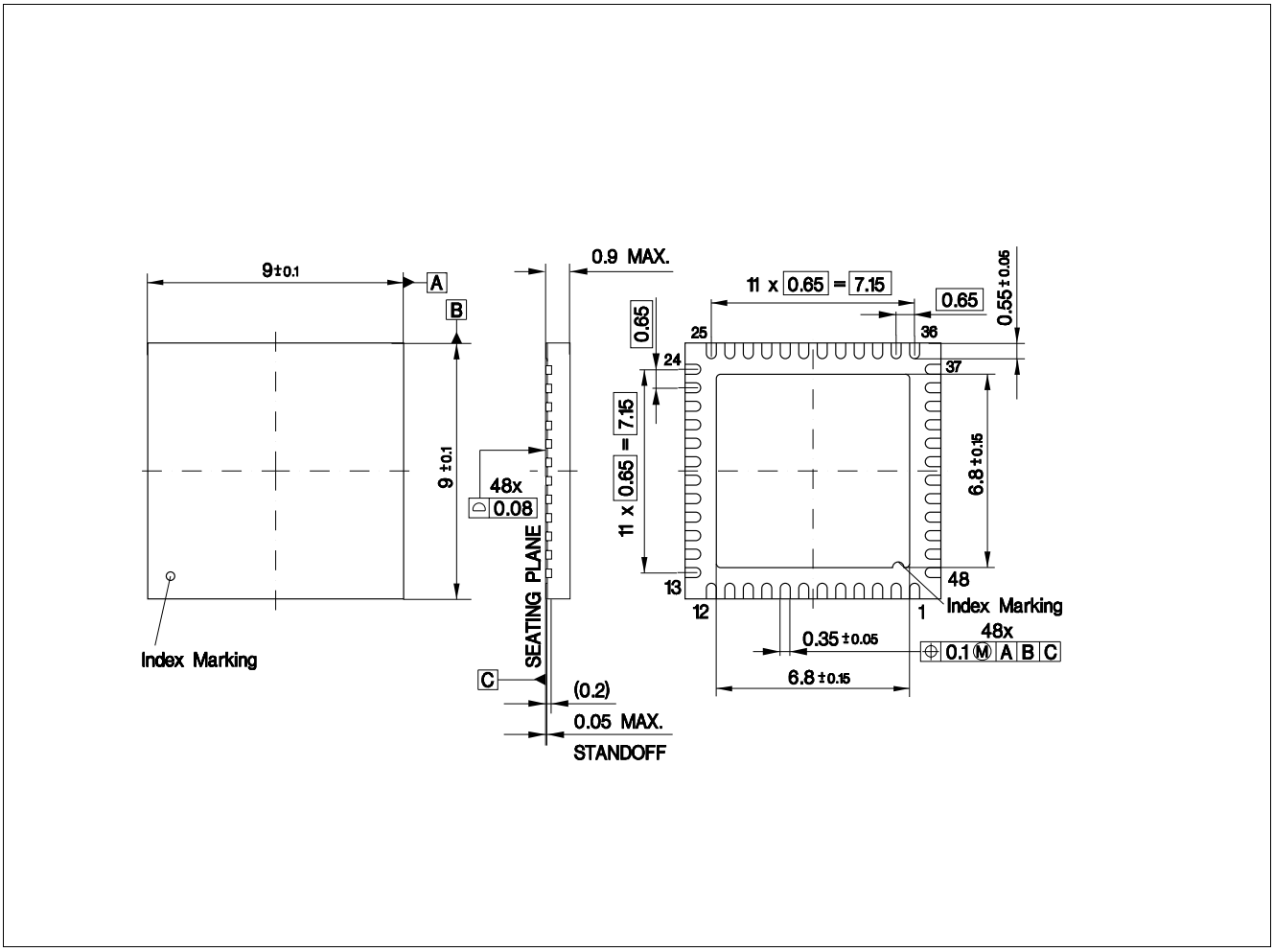


Figure 15 PG-VQFN-48

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

12 Revision History

Revision	Date	Changes
Rev.1.2	2016-01-27	- package adjustments
Rev.1.1	2011-08-03	- added figure VDD output voltage vs load current - added figure VDD output voltage vs supply voltage
Rev.1.0	2011-04-20	- $\overline{\text{INH}}$ high time to guarantee wake-up added - IFMA low time to guarantee wake-up added - Text Description improved - remaining OTPW text removed - Steady state differential input voltage range across VIN removed - SCDL open pin detection level hysteresis, footnote added
Rev.0.4	2011-03-17	- Common mode suppression, footnote added - High level input voltage $\overline{\text{INH}}$ (for $\overline{\text{INHD}}$=high) adapted - SCDL open pin detection level hysteresis, footnote added - Rise time $\overline{\text{ERR}}$ adapted - $\overline{\text{ERR}}$ output voltage adapted - Over temperature pre-warning removed
Rev.0.3	2011-03-14	- Voltage difference between ISP and ISN specified - Minimum buffer capacitor C_{VREG} specified - Description of SH currents added - Pull up and pull down resistors at IHx and ILx expanded - Propagation time tolerance reduced - Rise and fall times specified - Fig. 4 new - Fig. 5 updated - Pull up resistor at INHD expanded - Pull down resistor at ERR output expanded - Pull up resistor at IFuC output expanded - Matching of IFMA pull up / pull down resistors replaced by IFMA input current / VS - Limit the lower load current of VDD to 2mA - Dead time description improved - Short circuit detection accuracy improved - Analog temperature output at 25°C improved

Edition 2016-01-27

Published by
Infineon Technologies AG
81726 Munich, Germany

© 2016 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.