TLE 8110 EE

Smart Multichannel Low Side Switch with Parallel Control and SPI Interface

coreFLEX TLE8110EE

Data Sheet

Rev. 1.4, 2013-07-02

Automotive Power

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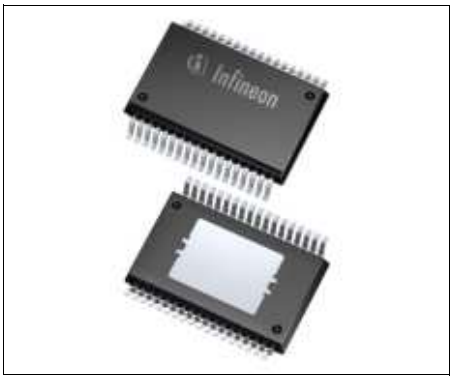
Smart Multichannel Low Side Switch with Parallel Control and SPI Interface
coreFLEX

TLE8110EE

AEC Qualified

RoHS

1 Overview



PG-DSO-36

Features

- Overvoltage, Overtemperature, ESD -Protection
- Direct Parallel PWM Control of all Channels
- safe*COMMUNICATION* (SPI and Parallel)
- Efficient Communication Mode: compact*CONTROL*
- Compatible with 3.3V- and 5V- Micro Controllers I/O ports
- clamp*SAFE* for highly efficient parallel use of the channels
- Green Product (RoHS compliant)
- AEC Qualified

Application

- Power Switch Automotive and Industrial Systems switching Solenoids, Relays and Resistive Loads

Description

10-channel Low-Side Switch in Smart Power Technology [SPT] with **S**erial **P**eripheral **I**nterface [SPI] and 10 open drain DMOS output stages. The TLE8110EE is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via Parallel Input Pins for PWM use or SPI Interface. The TLE8110EE is particularly suitable for Engine Management and Powertrain Systems.

Type	Package	Marking
TLE8110EE	PG-DSO-36	TLE8110EE

Table 1 Product Summary

Parameter	Symbol	Value	Unit
Analogue Supply voltage	V_{DD}	4.50 … 5.50	V
Digital Supply Voltage	V_{CC}	3.00 … 5.50	V
Clamping Voltage (CH 1-10)	$V_{DS(CL)typ}$	55	V
On Resistance typical at Tj=25°C and I_{Dnom}	R_{ON1-4}	0.30	Ω
	R_{ON5-6}	0.25	Ω
	R_{ON7-10}	0.60	Ω
On Resistance maximum at Tj=150°C and I_{Dnom}	R_{ON1-4}	0.60	Ω
	R_{ON5-6}	0.50	Ω
	R_{ON7-10}	1.20	Ω
Nominal Output current (CH 1-4)	I_{Dnom}	1.50	A
Nominal Output current (CH 5-6)	I_{Dnom}	1.70	A
Nominal Output current (CH 7-10)	I_{Dnom}	0.75	A
Output Current Shut-down Threshold (CH 1-4) min.	$I_{DSD(low)}$	2.60	A
Output Current Shut-down Threshold (CH 5-6) min.	$I_{DSD(low)}$	3.70	A
Output Current Shut-down Threshold (CH 7-10) min.	$I_{DSD(low)}$	1.70	A

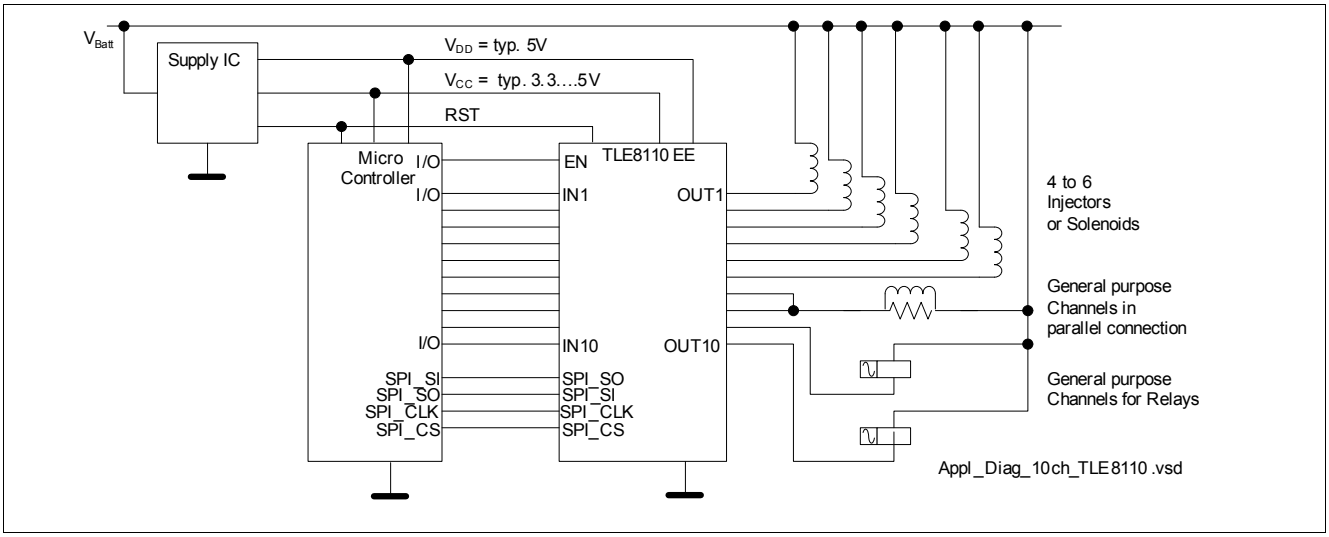


Figure 1 Block Diagram TLE8110EE

2 Block Diagram

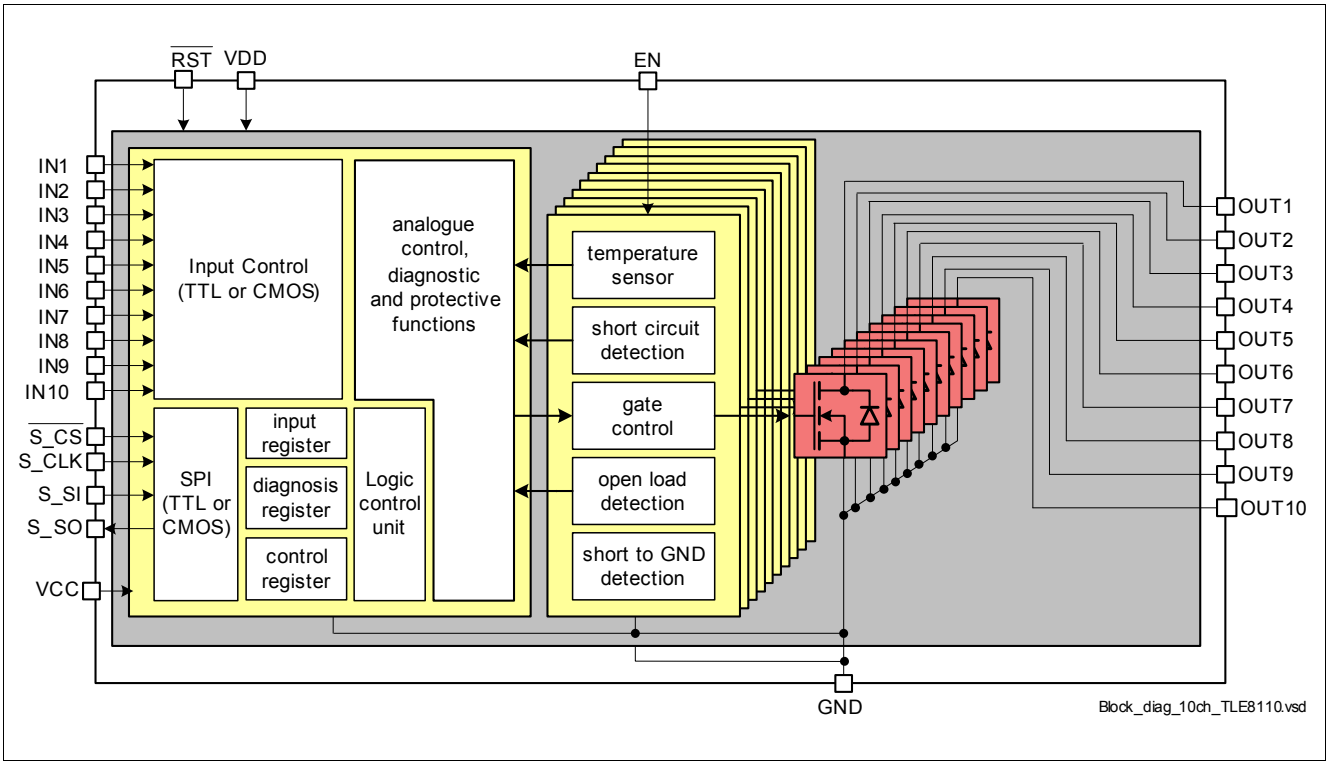


Figure 2 Block Diagram

2.1 Description

Communication

The TLE8110EE is a 10-channel low-side switch in PG-DSO-36 package providing embedded protection functions. The 16-bit serial peripheral interface (SPI) can be utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy-chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins [1].

The analogue and the digital part of the device is supplied by 5V. Logic Input and Output Signals are then compatible to 5V logic level [TTL - level]. Optionally, the logic part can be supplied with lower voltages to achieve signal compatibility with e.g. 3.3V logic level [CMOS - level].

The TLE8110EE is equipped with 10 parallel input pins that are routed to each output channel. This allows control of the channels for loads driven by Pulse Width Modulation (PWM). The output channels can also be controlled by SPI.

Reset

The device is equipped with one Reset Pin and one Enable. Reset [RST] serves the whole device, Enable [EN] serves only the Output Control Unit and the Power Stages.

1) Daisy Chain

Diagnosis

The device provides diagnosis of the load, including open load, short to GND as well as short circuit to V_{Batt} detection and over-load / over-temperature indication. The SPI diagnosis flags indicates if latched fault conditions may have occurred.

Protection

Each output stage is protected against short circuit. In case of over load, the affected channel is switched off. The switching off reaction time is dependent on two switching thresholds. Restart of the channel is done by clearing the Diagnosis Register [1)]. This feature protects the device against uncontrolled repetitive short circuits. The reaction to a short-circuit and over-temperature can be alternatively changed to further modes, such as semi- or auto - restart of the affected channel.

There is a temperature sensor available for each channel to protect the device in case of over temperature. In case of over temperature the affected channel is switched off and the Over-Temperature Flag is set. Restart of the channel is done by deleting the Flag. This feature protects the device against uncontrolled temperature toggling.

Parallel Connection of Channels

The device is featured with a central clamping structure, so-called *CLAMP*safe. This feature ensures a balanced clamping between the channels and allows in case of parallel connection of channels a high efficient usage of the channel capabilities. This parallel mode is additionally featured by best possible parameter- and thermal matching of the channels and by controlling the channels accordingly.

1) Restart after Clear

3 Pin Configuration

3.1 Pin Assignment

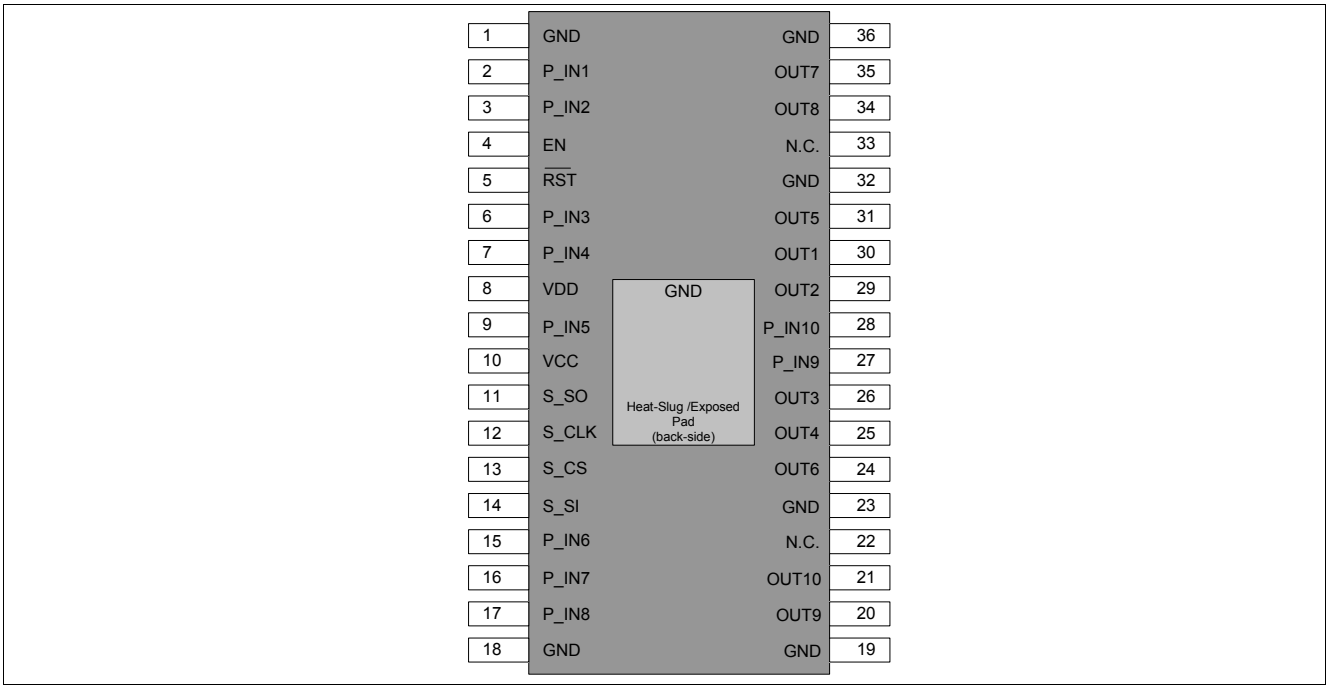


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	P_IN1	Parallel Input Pin 1. Default assignment to Output Channel 1.
3	P_IN2	Parallel Input Pin 2. Default assignment to Output Channel 2.
4	EN	Enable Input Pin. If not needed, connect with Pull-up resistor to VCC.
5	$\overline{\text{RST}}$	Reset Input Pin. (low active). If not needed, connect with Pull-up resistor to VCC.
6	P_IN3	Parallel Input Pin 3. Default assignment to Output Channel 3.
7	P_IN4	Parallel Input Pin 4. Default assignment to Output Channel 4.
8	VDD	Analogue Supply Voltage
9	P_IN5	Parallel Input Pin 5. Default assignment to Output Channel 5.
10	VCC	Digital Supply Voltage
11	S_SO	Serial Peripheral Interface [SPI], Serial Output
12	S_CLK	Serial Peripheral Interface [SPI], Clock Input
13	$\overline{\text{S_CS}}$	Serial Peripheral Interface [SPI], Chip Select (active Low)
14	S_SI	Serial Peripheral Interface [SPI], Serial Input
15	P_IN6	Parallel Input Pin 6. Default assignment to Output Channel 6.
16	P_IN7	Parallel Input Pin 7. Default assignment to Output Channel 7.
17	P_IN8	Parallel Input Pin 8. Default assignment to Output Channel 8.
18	GND	Ground

Pin	Symbol	Function
19	GND	Ground
20	OUT9	Drain of Power Transistor Channel 9
21	OUT10	Drain of Power Transistor Channel 10
22	N.C.	internally not connected, connect to Ground
23	GND	Ground
24	OUT6	Drain of Power Transistor Channel 6
25	OUT4	Drain of Power Transistor Channel 4
26	OUT3	Drain of Power Transistor Channel 3
27	P_IN9	Parallel Input Pin 9. Default assignment to Output Channel 9.
28	P_IN10	Parallel Input Pin 10. Default assignment to Output Channel 10.
29	OUT2	Drain of Power Transistor Channel 2
30	OUT1	Drain of Power Transistor Channel 1
31	OUT5	Drain of Power Transistor Channel 5
32	GND	Ground
33	N.C.	internally not connected, connect to Ground
34	OUT8	Drain of Power Transistor Channel 8
35	OUT7	Drain of Power Transistor Channel 7
36	GND	Ground
Cooling Tab	GND	Cooling Tab; internally connected to GND

3.3 Terms

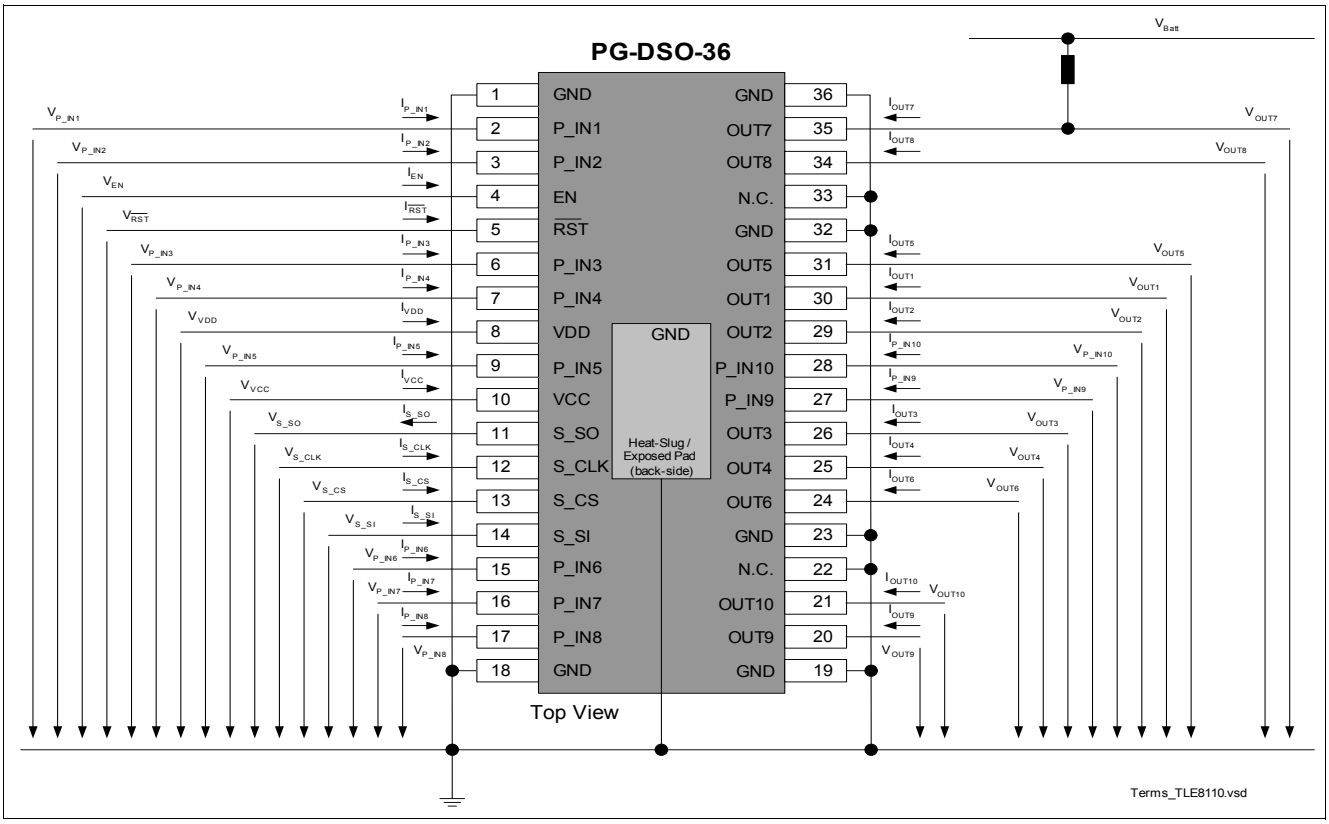


Figure 4 Terms

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltages						
4.1.1	Digital Supply voltage	V_{CC}	-0.3	5.5	V	permanent
4.1.2	Digital Supply voltage	V_{CC}	-0.3	6.2	V	t < 10s
4.1.3	Analogue Supply voltage	V_{DD}	-0.3	5.5	V	permanent
4.1.4	Analogue Supply voltage	V_{DD}	-0.3	6.2	V	t < 10s
Power Stages						
4.1.5	Load Current (CH 1 to 10)	I_{Dn}	-	$I_{DSD(low)}$	A	–
4.1.6	Reverse Current Output (CH 1-10)	I_{Dn}	$-I_{DSD(low)}$	-	A	–
4.1.7	Total Ground Current	I_{GND}	-20	20	A	–
4.1.8	Continuous Drain Source Voltage (Channel 1 to 10)	V_{DSn}	-0.3	45	V	–
4.1.9	maximum Voltage for short circuit protection on Output	V_{DSn}	-	24	V	one event on one single channel.
Clamping Energy - Single Pulse[2)3)]						
4.1.10	Single Clamping Energy Channel Group 1-4	E_{AS}	-	29	mJ	I_D = 2.6A 1 single pulse
4.1.11	Single Clamping Energy Channel Group 5-6	E_{AS}	-	31	mJ	I_D = 3.7A 1 single pulse
4.1.12	Single Clamping Energy Channel Group 7-10	E_{AS}	-	11	mJ	I_D = 1.7A 1 single pulse
Logic Pins (SPI, INn, EN, RST)						
4.1.13	Input Voltage at all Logic Pin	V_x	-0.3	5.5	V	permanent
4.1.14	Input Voltage at all Logic Pin	V_x	-0.3	6.2	V	t < 10s
4.1.15	Input Voltage at Pin 27, 28 (IN9, 10,)	V_x	-0.3	45	V	permanent
Temperatures						
4.1.16	Junction Temperature	T_j	-40	150	°C	–
4.1.17	Junction Temperature	T_j	-40	175	°C	max. 100hrs cumulative
4.1.18	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Robustness						
4.1.19	Electro Static Discharge Voltage “Human Body Model - HBM”	V_{ESD}	-4	4	kV	All Pins HBM[4)] 1.5KOhm, 100pF

Absolute Maximum Ratings[1] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.20	Electro Static Discharge Voltage "Charged Device Model - CDM"	V_{ESD}	-500	500	V	All Pins CDM[5]
4.1.21	Electro Static Discharge Voltage "Charged Device Model - CDM"	V_{ESD}	-750	750	V	Pin 1, 18, 19, 36 (corner pins) CDM[5]

1) Not subject to production test, specified by design.
2) One single channel per time.
3) Triangular Pulse Shape (inductance discharge): $I_D(t) = I_D(0)\cdot(1 - t / t_{pulse})$; $0 < t < t_{pulse}$.
4) ESD susceptibility, HBM according to EIA/JESD 22-A114-B
5) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101-C

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Supply Voltages						
4.2.1	Analogue Supply Voltage	V_{DD}	4.5	5.5	V	–
4.2.2	Digital Supply Voltage	V_{CC}	3	V_{DD}	V	–
4.2.3	Digital Supply Voltage	V_{CC}	V_{DD}	5.5	V	leakage Currents (I_{CC}) might increase if $V_{CC} > V_{DD}$.
Power Stages						
4.2.4	Ground Current	I_{GND_typ}	9		A	resistive loads[1]
Temperatures						
4.2.5	Junction Temperature	T_j	-40	150	°C	-
4.2.6	Junction Temperature	T_j	-40	175	°C	[1] for 100hrs

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point	R_{thJSP}	-	1.75	3.60	K/W	P_{vtot} = 3W[1)2)3)]
4.3.2	Junction to Ambient	R_{thJA}	-	25.00	-	K/W	P_{vtot} = 3W[1)2)3)]

1) Not subject to production test, specified by design.
2) Homogenous power distribution over all channels (All Power stages equally heated), dependent on cooling set-up.
3) Refer to ***Figure 5***

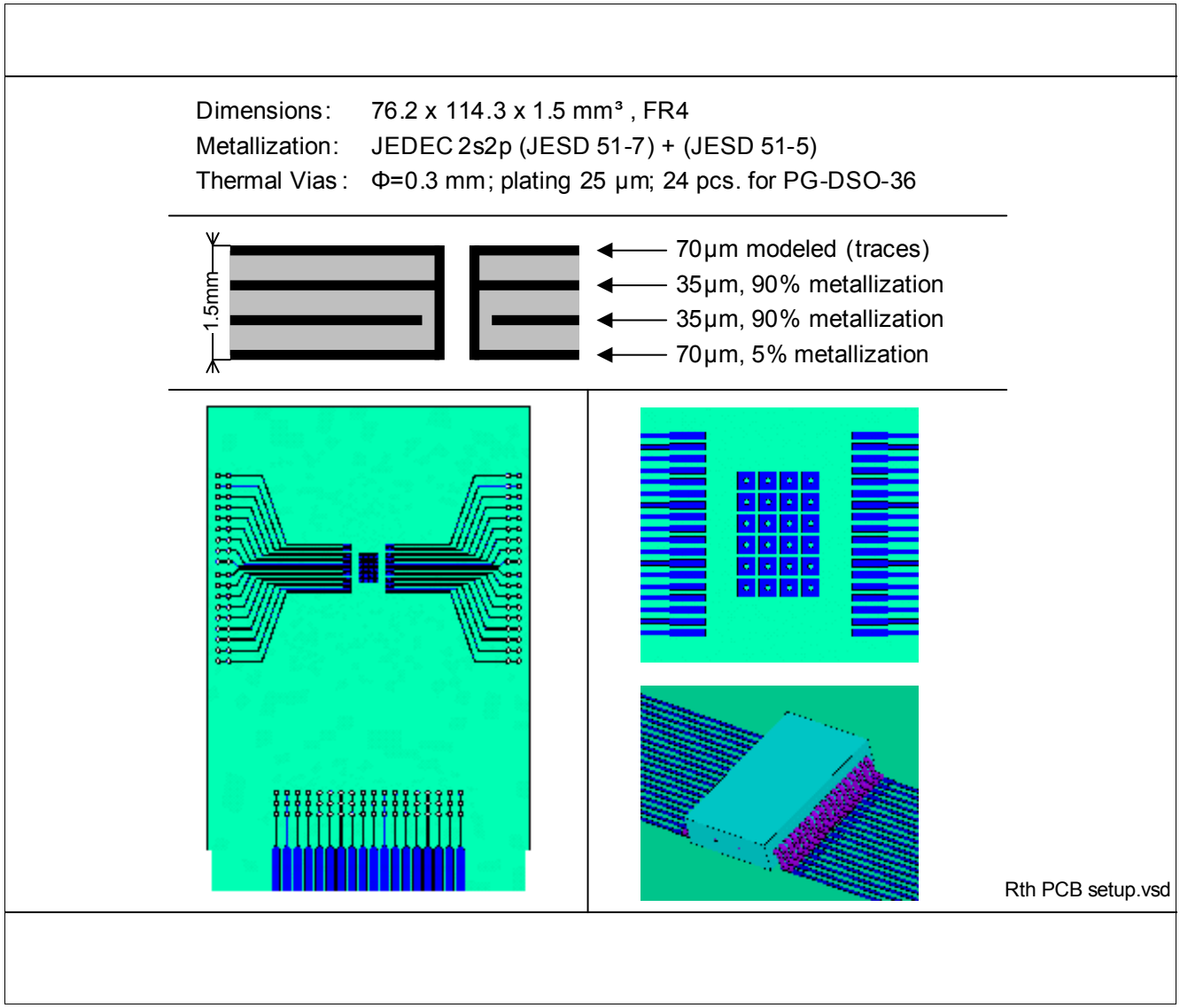


Figure 5 PG-DSO-36 PCB set-up

5 Power Supply

5.1 Description Power Supply

The TLE8110EE is supplied by analogue power supply line V_{DD} which is used for the analogue functions of the device, such as the gate control of the power stages. The digital power supply line V_{CC} is used to supply the digital part and offers the possibility to adapt the logic level of the serial output pins to lower logic levels.

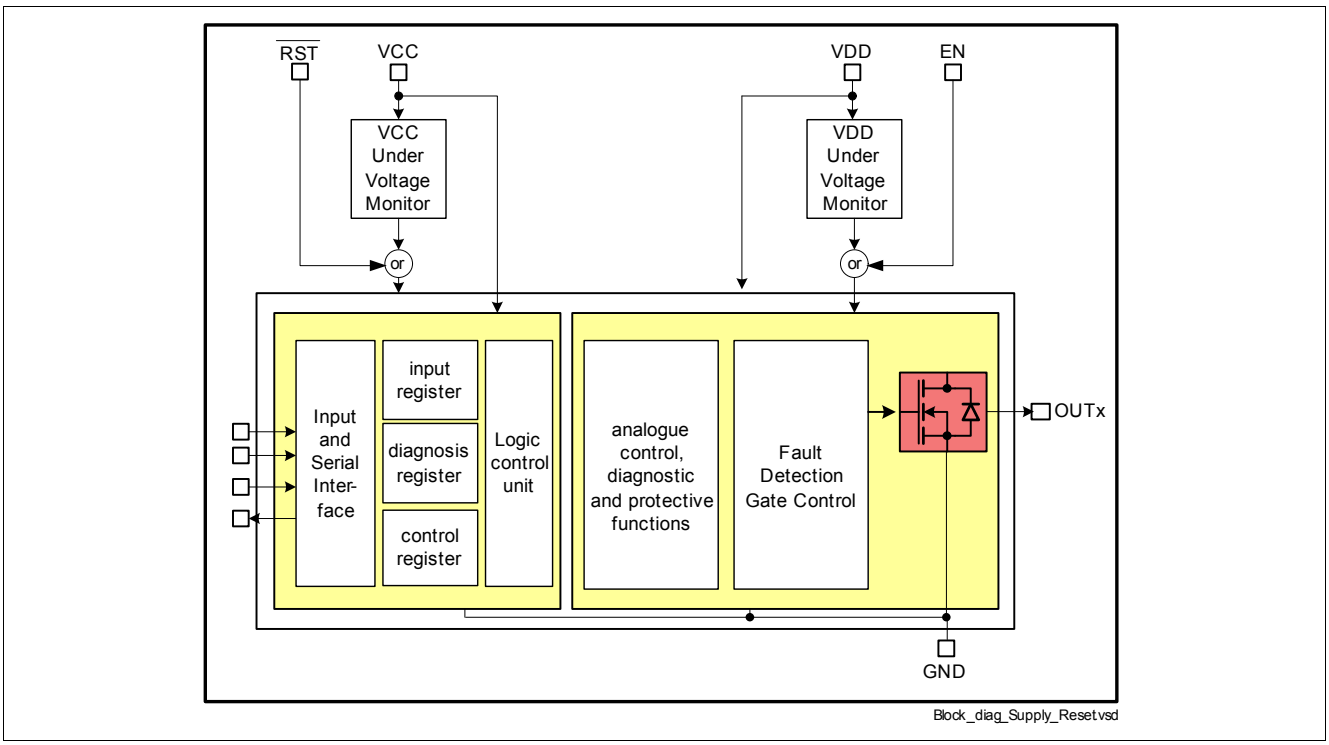


Figure 6 Block Diagram Supply and Reset

Description Supply

The Supply Voltage Pins are monitored during the power-on phase and under normal operating conditions for under voltage.

If during Power-on the increasing supply voltage exceeds the Supply Power-on Switching Threshold, the internal Reset is released after an internal delay has expired.

In case of under voltage, a device internal reset is performed. The Switching Threshold for this case is the Power-on Switching threshold minus the Switching Hysteresis.

In case of under voltage on the analogue supply line V_{DD} the outputs are turned off but the content of the registers and the functionality of the logic part is kept alive. In case of under voltage on the digital supply V_{CC} line, a complete reset including the registers is performed.

After returning back to normal supply voltage and an internal delay, the related functional blocks are turned on again. For more details, refer to the chapter “Reset”.

The device internal under-voltage set will set the related bits in SDS (Short Diagnosis and Device Status) to allow the micro controller to detect this reset. For more information, refer to the chapter “Control of the Device”.

5.2 Electrical Characteristics Power Supply

Electrical Characteristics: Power Supply

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Digital Supply and Power-on Reset							
5.2.1	Digital Supply Voltage	V_{CC}	3	-	5.5	V	
5.2.2 a)	Digital Supply Current during Reset (V_{CC} < V_{CCpo})	I_{CCstb}	-	15	20	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, Tj=85°C [1] V_{CC} = 2.0V V_{DD} > V_{CC}
b)			-	20	40	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, Tj=150°C V_{CC} = 2.0V V_{DD} > V_{CC}
5.2.3 a)	Digital Supply Current during Reset ($V_{\overline{RST}}$ < $V_{\overline{RSTI}}$)	I_{CCstb}	-	2	5	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, Tj=85°C[1] V_{DD} > V_{CC}
b)			-	5	15	µA	f_{SCLK} = 0Hz, S_CS = V_{CC}, Tj=150°C V_{DD} > V_{CC}
5.2.4 a)	Digital Supply Operating Current V_{CC} = 3.3V	I_{CC}	-	0.15	2	mA	f_{SCLK} = 0Hz, Tj=150°C. all Channels ON [1]
b)			-	0.5	5	mA	f_{SCLK} = 5MHz, Tj=150°C. all Channels ON [1)2)]
5.2.5 a)	Digital Supply Operating Current V_{CC} = 5.5V	I_{CC}	-	0.25	2	mA	f_{SCLK} = 0Hz, Tj=150°C. all Channels ON
b)			-	0.8	10	mA	f_{SCLK} = 5MHz, Tj=150°C. all Channels ON [1)2)]
5.2.6	Digital Supply Power-on Switching Threshold	V_{CCpo}	1.9	2.8	3	V	V_{CC} increasing
5.2.7	Digital Supply Switching Hysteresis	V_{CChy}	100	300	500	mV	[1]

Electrical Characteristics: Power Supply

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Analogue Supply and Power-on Reset							
5.2.8	Analogue Supply Voltage	V_{DD}	4.5	-	5.5	V	-
5.2.9 a)	Analogue Supply Current during Reset (V_{DD}< V_{DDpo})	I_{DDstb}	-	10	20	µA	f_{SCLK} = 0Hz, Tj=85°C 1) V_{DD} = 2V
b)			-	15	40	µA	f_{SCLK} = 0Hz, Tj=150°C V_{DD} = 2V
5.2.10 a)	Analogue Supply Current during Reset (V_{EN}< V_{ENI})	I_{DDstb}	-	1	5	µA	f_{SCLK} = 0Hz, Tj=85°C 1)
b)			-	2	15	µA	f_{SCLK} = 0Hz, Tj=150°C
5.2.11	Analogue Supply Operating Current	I_{DD}	-	8	25	mA	f_{SCLK} = 0...5MHz1) Tj=150°C all Channels ON
5.2.12	Analogue Supply Power-on Switching Threshold	V_{DDpo}	3	4.2	4.5	V	V_{DD} increasing
5.2.13	Analogue Supply Switching Hysteresis	V_{DDhy}	100	200	400	mV	1)
5.2.14	Analogue Supply Power-on Delay Time	t_{VDDpo}	-	100	200	µs	V_{DD} increasing 1)

1) Parameter not subject to production test. Specified by design.
2) C = 50pF connected to S_SO

6 Reset and Enable Inputs

6.1 Description Reset and Enable Inputs

The TLE8110EE contains one Reset- and one Enable Input Pin as can be seen in **Figure 6**.

Description:

Reset Pin [$\overline{\text{RST}}$] is the main reset and acts as the internal under voltage reset monitoring of the digital supply voltage V_{CC}: As soon as $\overline{\text{RST}}$ is pulled low, the whole device including the control registers is reset.

The Enable Pin [EN] resets only the Output channels and the control circuits. The content of the all registers is kept. This functions offers the possibility of a “soft” reset turning off only the Output lines but keeping alive the SPI communication and the contents of the control registers. This allows the read out of the diagnosis and setting up the device during or directly after Reset.

6.2 Electrical Characteristics Reset Inputs

Electrical Characteristics: $\overline{\text{Reset}}$ Inputs

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reset Input Pin [$\overline{\text{RST}}$]							
6.2.1	Low Level of $\overline{\text{RST}}$	V_{RSTl}	-0.3	-	V_{CC} *0.2	V	-
6.2.2	High Level of $\overline{\text{RST}}$	V_{RSTh}	V_{CC} *0.4	-	V_{CC}	V	-
6.2.3	$\overline{\text{RST}}$ Switching Hysteresis	V_{RSThy}	20	100	300	mV	1)
6.2.4	Reset Pin pull-down Current	$I_{RSTresh}$	20	40	85	µA	$V_{\overline{RST}}$=5V
		$I_{RSTresl}$	2.4	-	-	µA	$V_{\overline{RST}}$=0.6V 1)
6.2.5	Required Reset Duration time $\overline{\text{RST}}$	t_{RSTmin}	2	-	-	µs	1)
Enable Input Pin [EN]							
6.2.6	Low Level of EN	V_{ENl}	-0.3	-	V_{CC} *0.2	V	-
6.2.7	High Level of EN	V_{ENh}	V_{CC} *0.4	-	V_{CC}	V	-
6.2.8	EN Switching Hysteresis	V_{ENhy}	20	60	300	mV	1)
6.2.9	Enable Pin pull-down Current	I_{ENresh}	5	35	85	µA	$V_{\overline{EN}}$=5V
		I_{ENresl}	2.4	-	-	µA	$V_{\overline{EN}}$=0.6V 1)
6.2.10	Enable Reaction Time (reaction of OUTx)	t_{ENrr}	-	4	-	µs	1)
6.2.11	Required Enable Duration time EN	t_{ENmin}	2	-	-	µs	1)

1) Parameter not subject to production test. Specified by design.

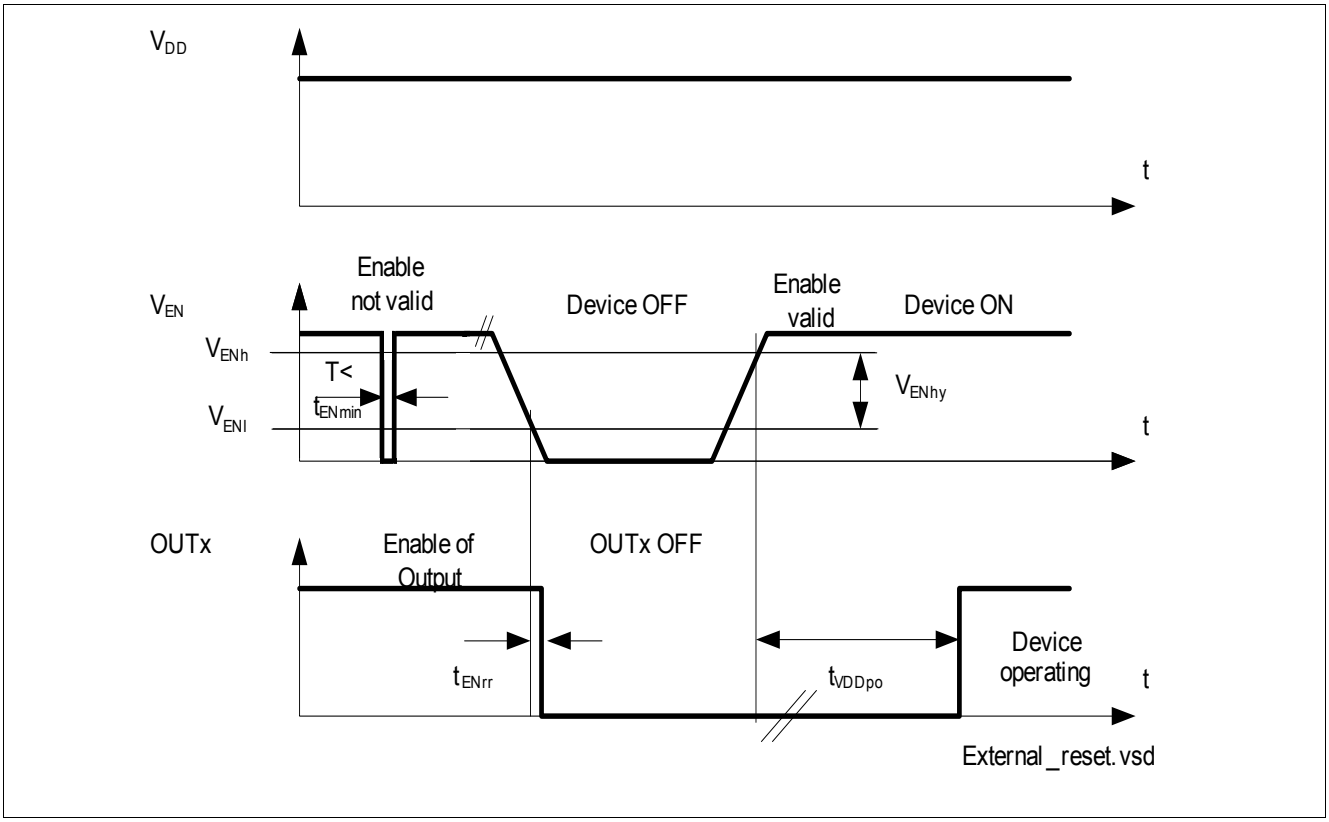


Figure 7 Timing

7 Power Outputs

7.1 Description Power Outputs

The TLE8110EE is a 10 channel low-side powertrain switch. The power stages are built by N-channel power MOSFET transistors. The device is a universal multichannel switch but mostly suited for the use in Engine Management Systems [EMS]. Within an EMS, the best fit of the channels to the typical loads is:

- Channel 1 to 4 for Injector valves or mid-sized solenoids with a nominal current requirement of 1.5A.
- Channel 5 to 6 for mid-sized solenoids or Injector valves with a nominal current requirement of 1.7A
- Channel 7 to 10 for small solenoids or relays with a nominal current requirement of 0.75A

Channel 1 to 10 provide enhanced clamping capabilities of typically 55V best suited for inductive loads such as injectors and valves. It is recommended in case of an inductive load, to connect an external free wheeling- or clamping diode, where-ever possible to reduce power dissipation.

All channels can be connected in parallel. Channels 1 to 4, 5 to 6 and 7 to 10 are prepared by matching for parallel connection with the possibility to use a high portion of the capability of each single channel also in parallel mode (refer to **Chapter 7.4**).

Channel 5 and 6 have a higher current shut down threshold to allow to connect in parallel mode a load with a high inrush-current, such as a lambda sensor heater.

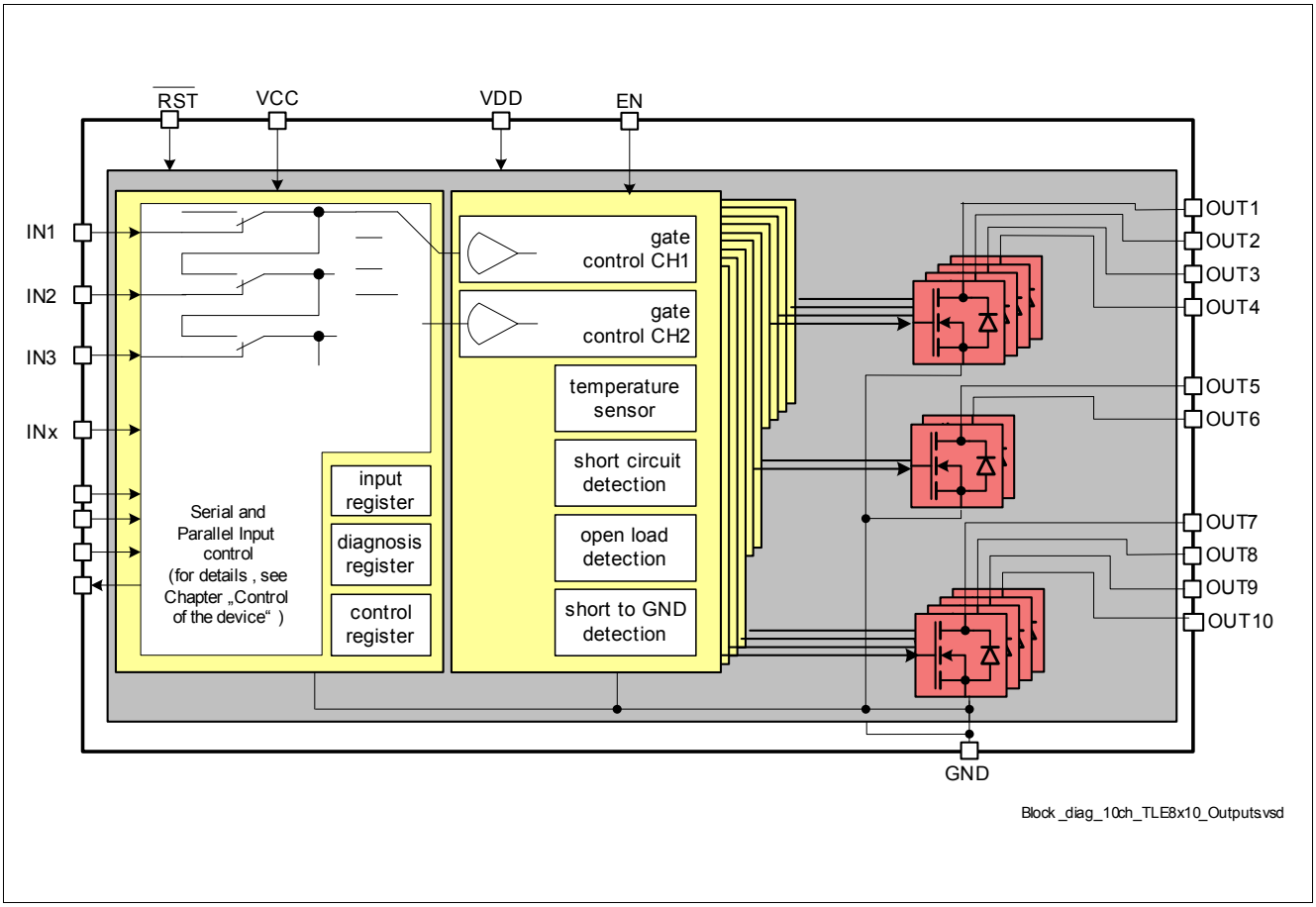


Figure 8 Block Diagram of Control and Power Outputs

7.2 Description of the Clamping Structure

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The clamping voltage is necessary to prevent destruction of the device, see **Figure 9** for the clamping circuit principle. Nevertheless, the maximum allowed load inductance is limited.

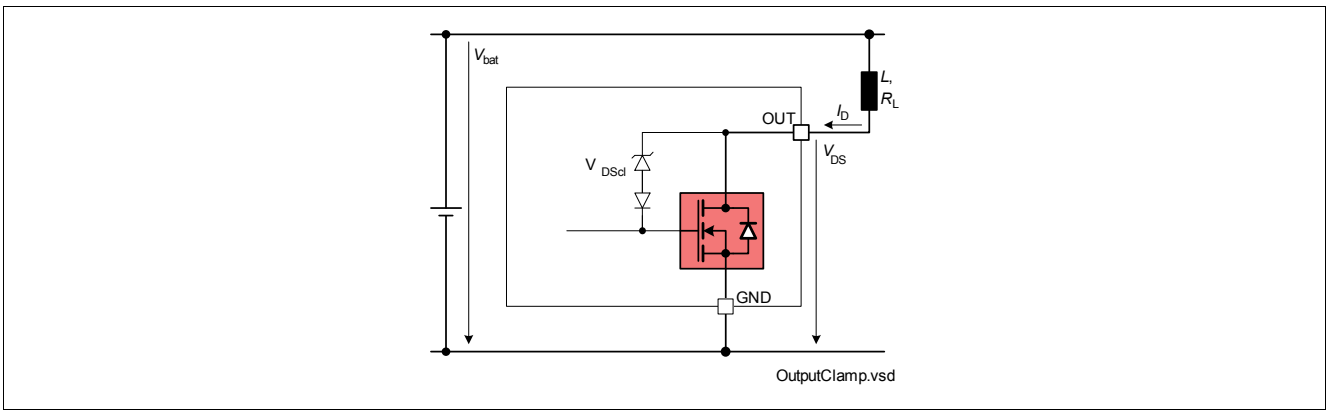


Figure 9 Internal Clamping Principle

Clamping Energy

During demagnetization of inductive loads, energy has to be dissipated in the device. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \frac{L_L}{R_L} \cdot \left[I_L - \frac{V_{DS(CL)} - V_{BAT}}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{V_{DS(CL)} - V_{BAT}}\right)\right] \quad (1)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

Attention: It is strongly recommended to measure the load Energy and Current under operating conditions, example of measurement setup is shown in Figure 10. Load small-signal parameters might not reflect the real load behavior under operating conditions, see Figure 11. For more details please refer to the Application Note "Switching Inductive Loads".

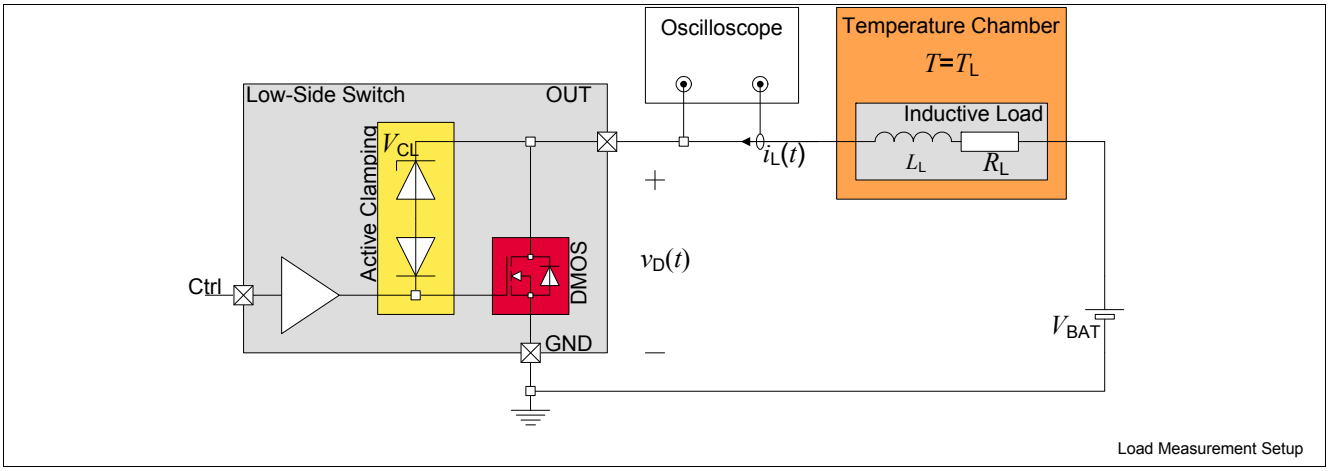


Figure 10 E_{CL} measurement setup

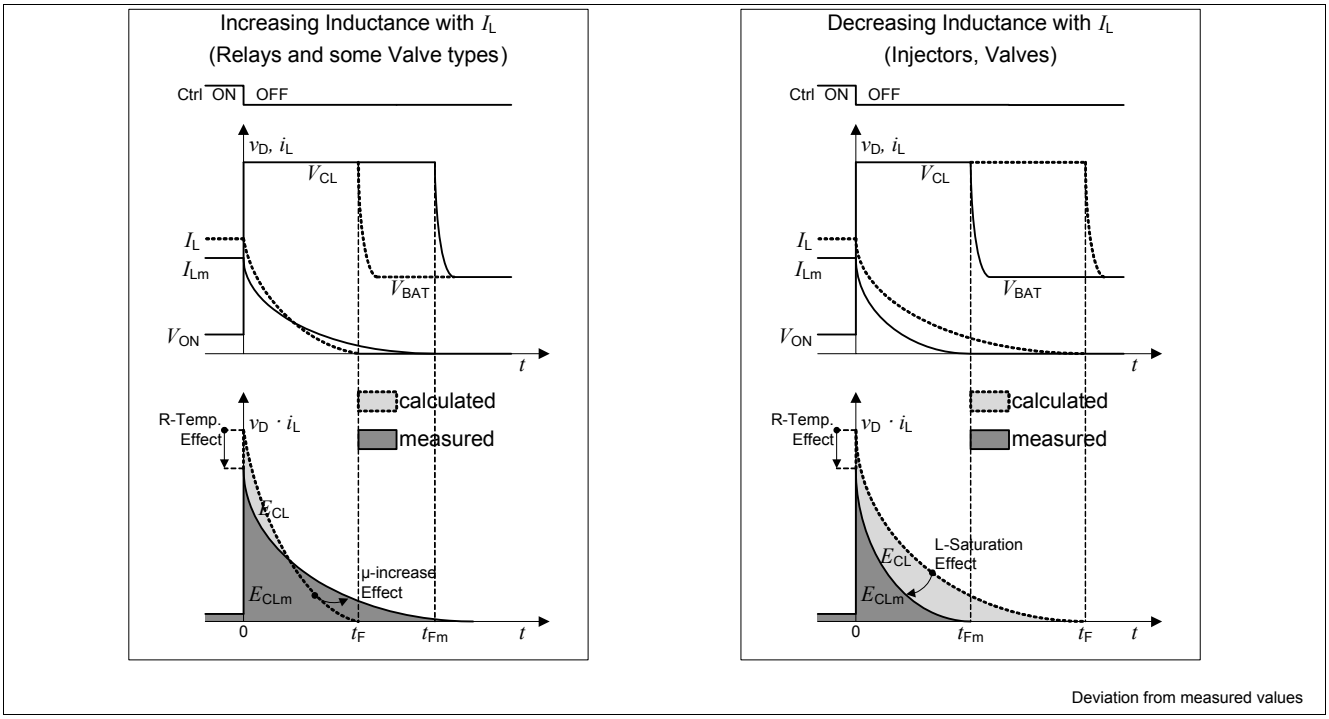


Figure 11 Deviation of calculation from measurement

7.3 Electrical Characteristics Power Outputs

Electrical Characteristics: Power Outputs

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Channel Resistance							
7.3.1	On State Resistance Channel Group 1-4	R_{DSon}	-	0.3	-	Ohm	I_{Dnom}=1,5A; Tj=25°C[1)]
			-	0.45	0.6	Ohm	I_{Dnom}=1,5A; Tj=150°C
7.3.2	On State Resistance Channel Group 5-6	R_{DSon}	-	0.25	-	Ohm	I_{Dnom}=1.7A; Tj=25°C[1)]
			-	0.35	0.5	Ohm	I_{Dnom}=1.7A; Tj=150°C
7.3.3	On State Resistance Channel Group 7-10	R_{DSon}	-	0.6	-	Ohm	I_{Dnom}=0.75A; Tj=25°C[1)]
			-	0.85	1.2	Ohm	I_{Dnom}=0.75A; Tj=150°C

Electrical Characteristics: Power Outputs (cont'd)

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Clamping Energy - Repetitive[1)2)3)4)]							
Channel Group 1-4							
7.3.4	Repetitive Clamping Energy	E_{AR}	-	-	11	mJ	I_D = 1.0A 10^9 cycles
			-	-	12	mJ	I_D = 2.1A 10^4 cycles
			-	-	15	mJ	I_D = 2.6A 10 cycles [5)]
Channel 5-6							
7.3.5	Repetitive Clamping Energy	E_{AR}	-	-	13	mJ	I_D = 1.3A 10^9 cycles
			-	-	15	mJ	I_D = 2.7A 10^4 cycles
			-	-	20	mJ	I_D = 3.2A 10 cycles [5)]
Channel 7-10							
7.3.6	Repetitive Clamping Energy	E_{AR}	-	-	4	mJ	I_D = 0.7A 10^9 cycles
			-	-	4	mJ	I_D = 1.4A 10^4 cycles
			-	-	5	mJ	I_D = 1.7A 10 cycles [5)]
Leakage Current							
7.3.7	Output Leakage Current in standby mode, Channel 1 to 4	I_{Doff}	-	-	3	µA	V_{DS}=13.5V; V_{DD}=5V, Tj=85°C[1)]
			-	-	8	µA	V_{DS}=13.5V; V_{DD}=5V, Tj=150°C
7.3.8	Output Leakage Current in standby mode, Channel 5 to 6	I_{Doff}	-	-	6	µA	V_{DS}=13.5V; V_{DD}=5V, Tj=85°C[1)]
			-	-	12	µA	V_{DS}=13.5V; V_{DD}=5V, Tj=150°C
7.3.9	Output Leakage Current in standby mode, Channel 7 to 10	I_{Doff}	-	-	2	µA	V_{DS}=13.5V; V_{DD}=5V, Tj=85°C[1)]
			-	-	5	µA	V_{DS}=13.5V; V_{DD}=5V, Tj=150°C

Electrical Characteristics: Power Outputs (cont'd)

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Clamping Voltage							
7.3.10	Output Clamping Voltage, Channel 1 to 10	V_{DScl}	45	55	60	V	
Timing							
7.3.11	Output Switching Frequency	f_{OUTx}	-	-	20	kHz	1) resistive load duty cycle > 25%.
7.3.12	Turn-on Time	t_{dON}	-	5	10	µs	V_{DS}=20% of V_{batt} V_{batt} = 13.5V, I_{DS1} to I_{DS6} = 1A, I_{DS7} to I_{DS10} = 0.5A, resistive load
7.3.13	Turn-off Time	t_{dOFF}	-	5	10	µs	V_{DS}=80% of V_{batt} V_{batt} = 13.5V, I_{DS1} to I_{DS6} = 1A, I_{DS7} to I_{DS10} = 0.5A resistive load

1) Parameter is not subject to production test, specified by design.

2) Either one of the values has to be considered as worst case limitation. Cumulative scenario and wide range of operating conditions are treated in the Application Note "Switching Inductive Loads - TLE8110 addendum".

3) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

4) Triangular Pulse Shape (inductance discharge): $I_D(t) = I_D(0) \cdot (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.

5) Repetitive operation not allowed. Starting T_j must be kept within specs. In case of high energy pulse an immediate switch-off strategy is recommended

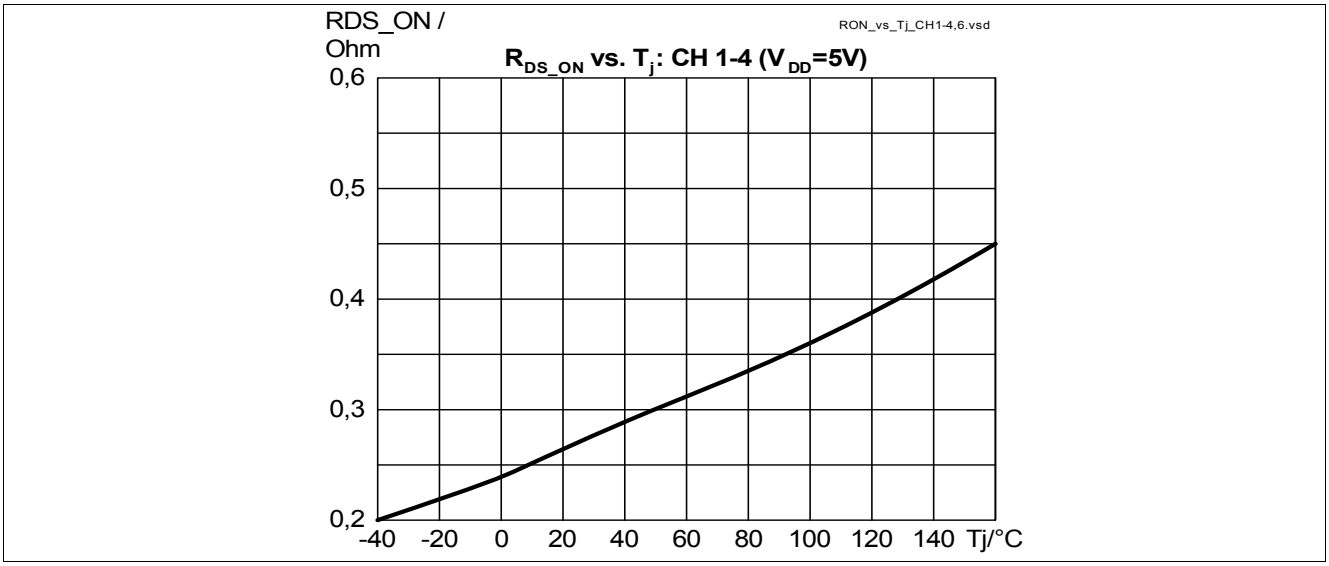


Figure 12 CH 1-4: typical behavior of RDS_ON versus the junction temperature Tj

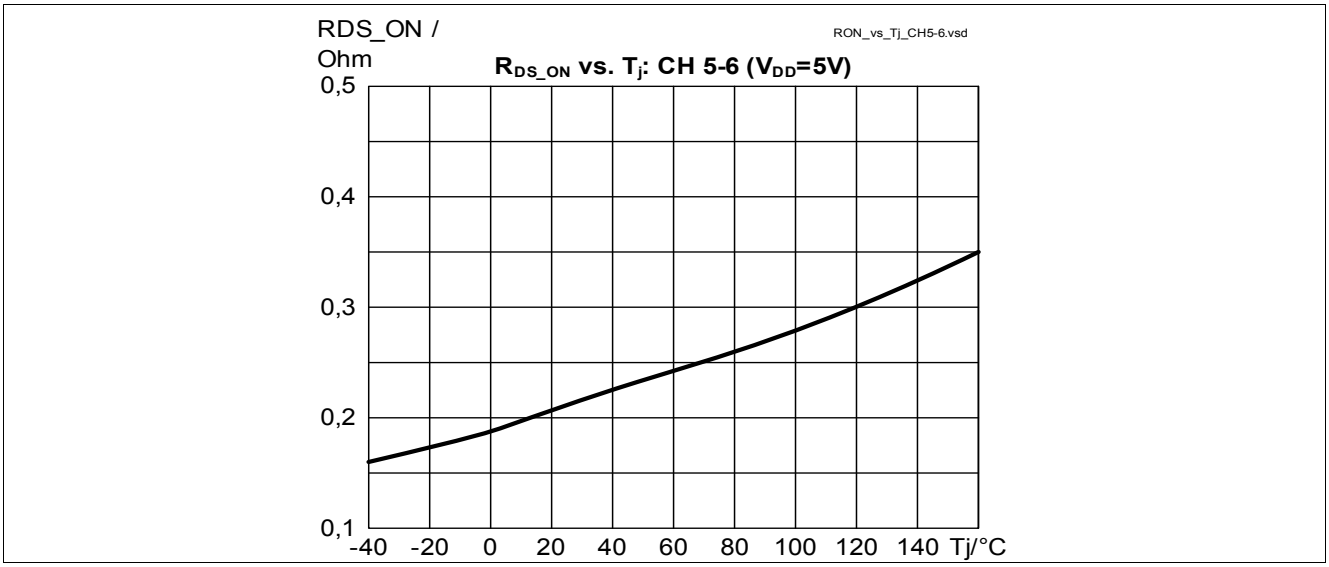


Figure 13 CH 5-6: typical behavior of RDS_ON versus the junction temperature Tj

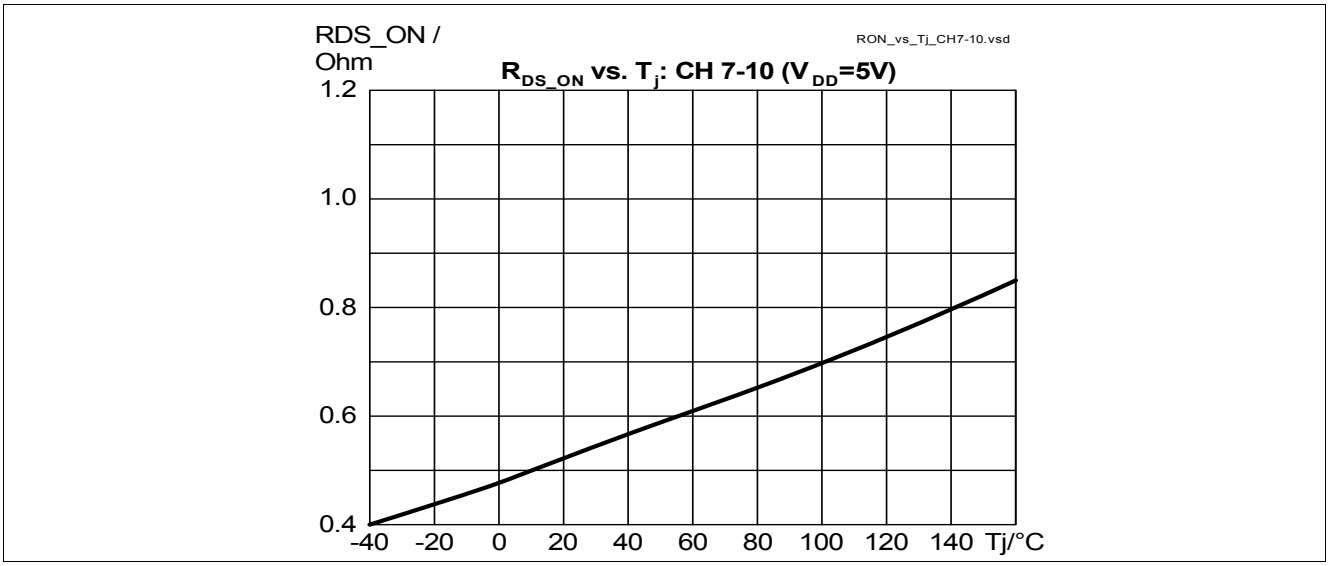


Figure 14 CH7-10: typical behavior of RDS_ON versus the junction temperature Tj

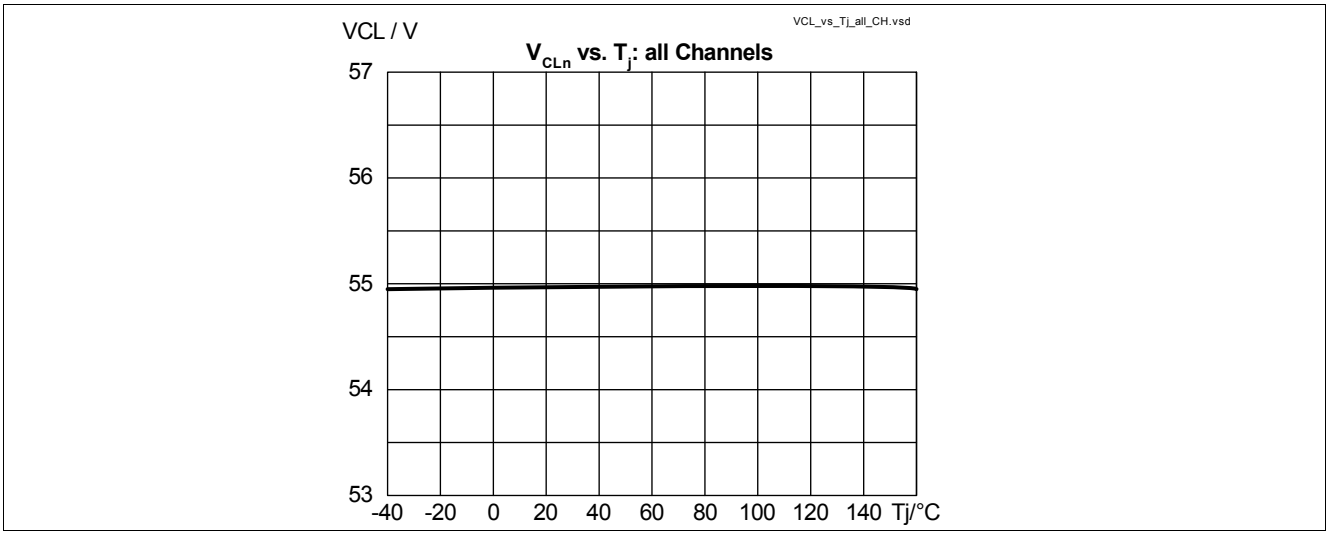


Figure 15 All Channels: typical behavior of the clamping voltage versus the junction temperature

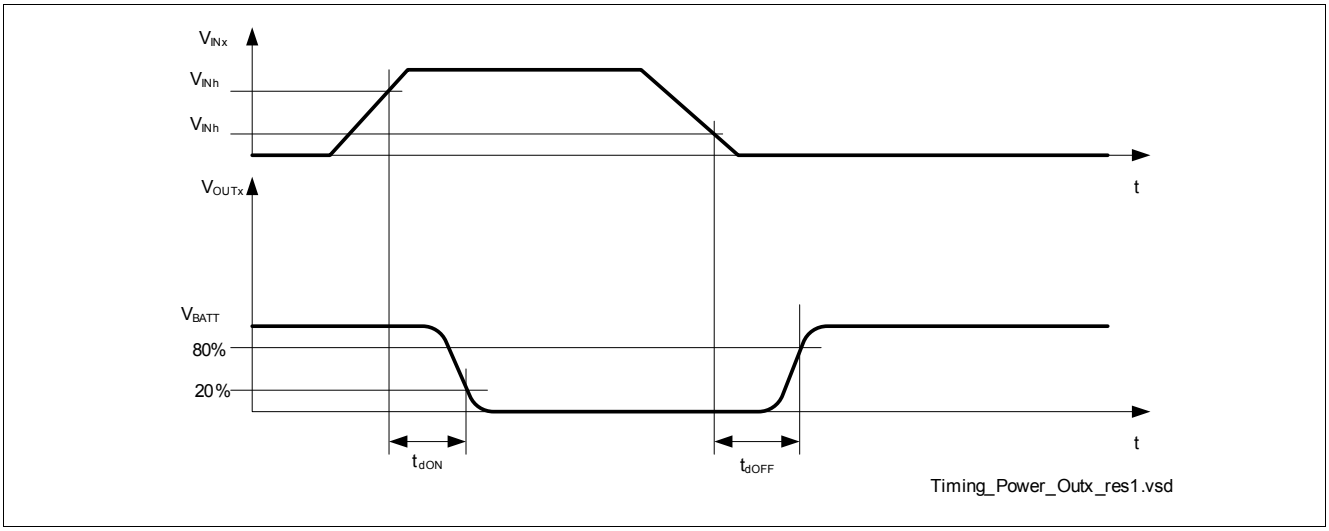


Figure 16 Timing of Output Channel switching (resistive load)

7.4 Parallel Connection of the Power Stages

The TLE8110EE is equipped with a structure which improves the capability of parallel-connected channels. The device can be “informed” via the PMx.PMx - bits (see chapter control of the device) which of the channels are connected in parallel. The input channels can be mapped to the parallel connected output channels in order to apply the PWM signals. This feature allows a flexible adaptation to different load situations within the same hardware setup.

In case of overload the ground current and the power dissipation is increasing. The application has to take into account that all maximum ratings are observed (e.g. operating temperature T_J and total ground current I_{GND}, see Maximum Ratings). In case of parallel connection of channels with or w/o PM-bit set, the defined maximum clamping energy must not be exceeded.

All stages are switched on and off simultaneously. The µC has to ensure that the stages which are connected in parallel have always the same state (on or off). The PM-bit should be set according to the parallel connected power stages in order to achieve the best possible performance.

The PM-bit is set to its default value in case of a Reset event (Reset pin Low or at Digital Supply undervoltage), that means the improved Parallel Mode is no longer active. In the event of reset the channels will be switched off causing the clamping energy to be dissipated with low performance of the current sharing as without PM-bit set, for more details please refer to the Application Note *Switching Inductive Loads - TLE8110 addendum*.

The performance during parallel connection of channels is specified by design and not subject to the production test. All channels at the same junction temperature level.

ON-Resistance

The typical ON-Resistance $R_{DSsum(typ)}$ of parallel connected channels is given by:

$$R_{DSsum(typ)} = \left[\frac{1}{R_{DSon,\,n(typ)}} + \frac{1}{R_{DSon,\,n+1(typ)}}\right]^{-1} \quad (2)$$

Table 2 Performance[1)2)3)4)] in case of Parallel Connection of Channels: related PM-Bit set

Pos.	Parameter	Symbol	Channels in Parallel			Unit	Conditions
			2x	3x	4x		
Channel Group 1-4							
7.4.1	Maximum overall current before reaching lower limit threshold	$I_{Dsum(low)}$	5.1	7.6	10.1	A	[1)]
7.4.2	Maximum overall Repetitive Clamping Energy	E_{ARsum}	37	-	-	mJ	I_D=1.0A 10^9 cycles
			17	38	69	mJ	I_D=1.75A 10^9 cycles
			-	23	42	mJ	I_D=2.5A 10^9 cycles
			-	-	33	mJ	I_D=3.0A 10^9 cycles
Channel Group 5-6							
7.4.3	Maximum overall current before reaching lower limit threshold	$I_{Dsum(low)}$	7.2	-	-	A	
7.4.4	Maximum overall Repetitive Clamping Energy	E_{ARsum}	43	-	-	mJ	I_D=1.3A 10^9 cycles
			21	-	-	mJ	I_D=2.2A 10^9 cycles
Channel Group 7-10							
7.4.5	Maximum overall current before reaching lower limit threshold	$I_{Dsum(low)}$	3.3	5.0	6.6	A	
7.4.6	Maximum overall Repetitive Clamping Energy	E_{ARsum}	15	-	-	mJ	I_D=0.7A 10^9 cycles
			6	15	30	mJ	I_D=1.2A 10^9 cycles
			-	9	18	mJ	I_D=1.6A 10^9 cycles
			-	-	11	mJ	I_D=2.1A 10^9 cycles

1) The performance during parallel connection of channels is specified by design and not subject to the production test.

2) Homogenous power distribution over all channels (all power stages equally heated), dependent on cooling set-up.

3) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

4) Triangular Pulse Shape (inductance discharge): $I_D(t) = I_D(0) \cdot (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.

Table 3 Performance[1)2)3)4)] in case of Parallel Connection of Channels: related PM-Bit NOT set

Pos.	Parameter	Symbol	Channels in Parallel			Unit	Conditions
			2x	3x	4x		
Channel Group 1-4							
7.4.1	Maximum overall current before reaching lower limit threshold	$I_{Dsum(low)}$	5.1	7.6	10.1	A	[1)]
7.4.2	Maximum overall Repetitive Clamping Energy	E_{ARsum}	18	-	-	mJ	I_D=1.0A 10^9 cycles
			8	13	19	mJ	I_D=1.75A 10^9 cycles
			-	8	11	mJ	I_D=2.5A 10^9 cycles
			-	-	9	mJ	I_D=3.0A 10^9 cycles
Channel Group 5-6							
7.4.3	Maximum overall current before reaching lower limit threshold	$I_{Dsum(low)}$	7.2	-	-	A	
7.4.4	Maximum overall Repetitive Clamping Energy	E_{ARsum}	22	-	-	mJ	I_D=1.3A 10^9 cycles
			11	-	-	mJ	I_D=2.2A 10^9 cycles
Channel Group 7-10							
7.4.5	Maximum overall current before reaching lower limit threshold	$I_{Dsum(low)}$	3.3	5.0	6.6	A	
7.4.6	Maximum overall Repetitive Clamping Energy	E_{ARsum}	7	-	-	mJ	I_D=0.7A 10^9 cycles
			3	4	7	mJ	I_D=1.2A 10^9 cycles
			-	3	4	mJ	I_D=1.6A 10^9 cycles
			-	-	3	mJ	I_D=2.1A 10^9 cycles

1) The performance during parallel connection of channels is specified by design and not subject to the production test.

2) Homogenous power distribution over all channels (all power stages equally heated), dependent on cooling set-up.

3) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

4) Triangular Pulse Shape (inductance discharge): $I_D(t) = I_D(0) \cdot (1 - t / t_{pulse})$; $0 < t < t_{pulse}$.

8 Diagnosis

8.1 Diagnosis Description

The TLE8110EE provides diagnosis information about the device and about the load. Following diagnosis flags have been implemented for each channel:

Diagnosis[1]	Symbol	DRn[1:0]x[2]	Device reaction	Confirmation Procedure[3]
Short to Ground	SCG	00_B	-	-
No Fault	OK	11_B	-	-
Open Load	OL	01_B	-	Chapter 8.1.1
Overcurrent / Overtemperature	OCT	10_B	Switch-off of related channel	Chapter 8.1.2

1) No priority scheme is implemented for the diagnosis detection, any new diagnosis entry will override the previous one
2) Diagnosis Register (A/B banks) bit configuration, see Chapter 12.3.2.1
3) For some diagnosis a confirmation procedure is required for a safe operation of the device, refer to Figure 17

Updating of the Diagnosis is based on a filter-dependent standard delay time (t_d) of 220µs max. This value is set as a default. Refer to Figure 18 for details.

If SCG or OL condition is asserted and before the Diagnosis Delay Time (t_d) is elapsed a condition change occurs, OL-to-SCG or SCG-to-OL, filter timer is not reset and latest condition before t_d expiration will be stored into the diagnosis register.

- Application Hint: It is recommended to avoid OFF periods of the channel shorter than $t_{d(max)}$ (220µs) in order to ensure the filter time is expired and the correct diagnosis information is stored.
- Application Hint: In specific application cases - such as driving Uni-Polar Stepper Motor - it might be possible, that reverse currents flow for a short time, which possibly can disturb the diagnosis circuit at neighboring channels and cause wrong diagnosis results of those channels. To reduce the possibility, that this effect appears in a certain timing range, the filter time of Channels 7 to 10 can be extended to typ. 2.5ms or typ. 5ms by setting the “Diagnosis Blind Time” - Bits (DBTx). If Channels 7 to 10 are used for driving loads causing reverse currents, they influence each other and additionally might affect Channels 5 and 6 . It is recommended to use the channels 7 + 8 and 9 + 10 as pairs for anti-parallel control signals, such as for the stepper motors. For logic setting details, see chapter “Control of the Device”.

8.1.1 Open Load diagnosis

If an OL is read out of the Diagnosis Register, the following procedure is required in order to confirm the channel status and ensure a safe operation of the device:

After reading the OL [01_B] in the diagnosis register (**Chapter 12.3.2**)

1. Switch-OFF for $t \geq t_{d(max)}$ the related channel (via serial or direct control, see **Chapter 12.3.3** and **Chapter 12.3.4**)
2. Read again the diagnosis register
   a) If OL is confirmed Then take actions according to system implementation
3. Continue normal operation

Refer to **Figure 17** for the procedure flow-chart.

8.1.2 Overcurrent / Overtemperature diagnosis

After an OCT assertion the related channel is switched OFF for safety reasons. If an OCT is read out of the Diagnosis Register, the following procedure is required in order to confirm the channel status and ensure a safe operation of the device:

After reading the OCT [10_B] in the diagnosis register (**Chapter 12.3.2**)

1. Set related bit DEVS.DCCx = 0 to disable OFF-diagnosis, see **Chapter 12.3.6**
2. Clear the Diagnosis issuing a DCC.DRxCL command, see **Chapter 12.3.2**
3. Switch-ON for $t \geq t_{OFFcl_l(max)}$ the related channel
4. Read again the diagnosis register
   a) If OCT is confirmed Then take actions according to system implementation
5. Set related bit DEVS.DCCx = 1 to enable OFF-diagnosis
6. Continue normal operation

Refer to **Figure 17** for the procedure flow-chart.

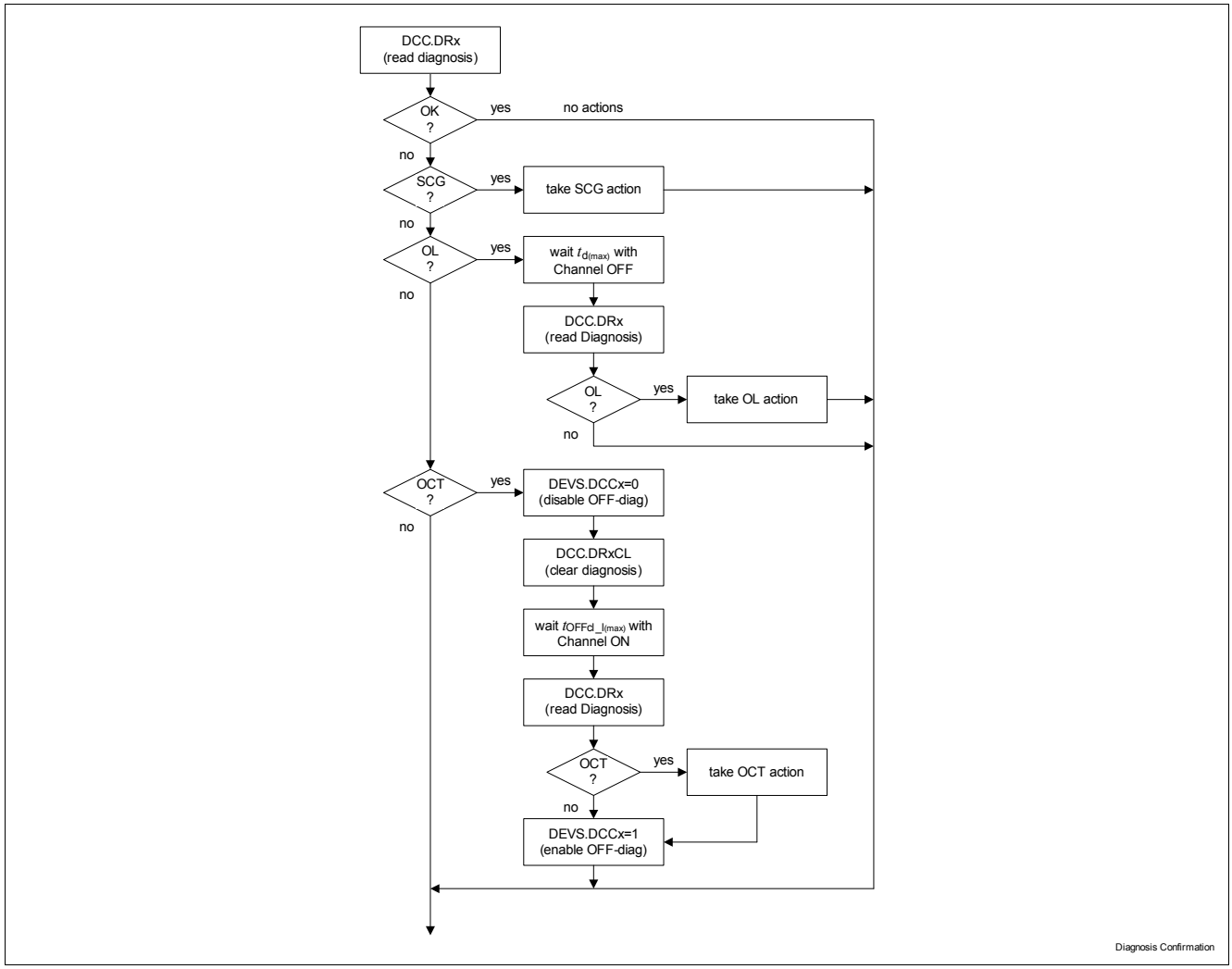


Figure 17 Diagnosis Confirmation procedure

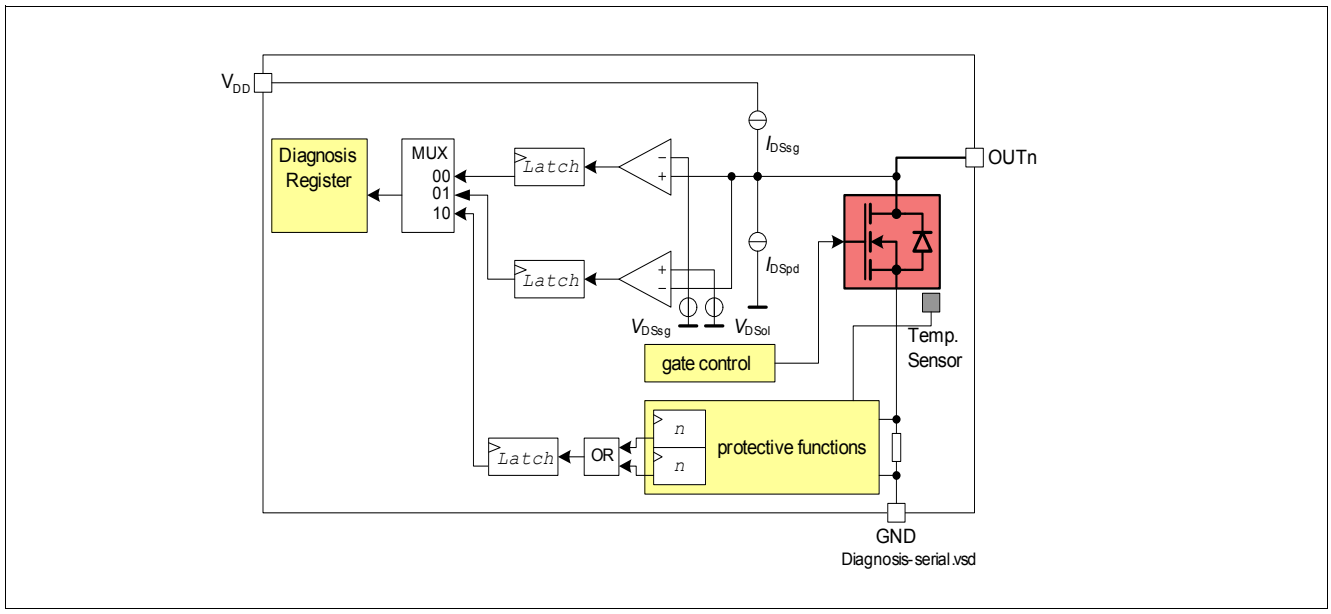


Figure 18 Block Diagram of Diagnosis

8.2 Electrical Characteristics Diagnosis

Electrical Characteristics: Diagnosis

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Open Load Diagnosis							
8.2.1	Open load detection threshold voltage	V_{DSol}	2.00	2.60	3.20	V	-
8.2.2	Output pull-down diagnosis current per channel (low level)	I_{Dpd}	50	90	150	µA	V_{DS} = 13.5 V
8.2.3	Open Load Diagnosis Delay Time (all channels)	t_d	100	-	220	µs	DEVS.DBT1=0 DEVS.DBT2=1 or 0
8.2.4 a)	Channel 7-10: Open Load Diagnosis Delay Time “Diagnosis Blind Time” see chapter “Control of the device” **Figure 19**, **Figure 20**	t_d	1.65	2.5	3.45	ms	DEVS.DBT1=1 DEVS.DBT2=0
b)			3.3	5	7.3	ms	DEVS.DBT1=1 DEVS.DBT2=1
Short to GND Diagnosis							
8.2.5	Short to ground detection threshold voltage	V_{DSsg}	1.00	1.50	2.00	V	-
8.2.6	Output diagnosis current for short to ground per channel (low level)	I_{Dsg}	-150	-100	-50	µA	V_{DS} = 0V
8.2.7	Short to GND Diagnosis Delay Time	t_d	100	-	220	µs	DEVS.DBT1=0 DEVS.DBT2=1 or 0
8.2.8 a)	Channel 7-10: Short to GND Diagnosis Delay Time. “Diagnosis Blind Time” see chapter “Control of the device”, **Figure 19**, **Figure 20**	t_d	1.65	2.5	3.45	ms	DEVS.DBT1=1 DEVS.DBT2=0
b)			3.3	5	7.3	ms	DEVS.DBT1=1 DEVS.DBT2=1

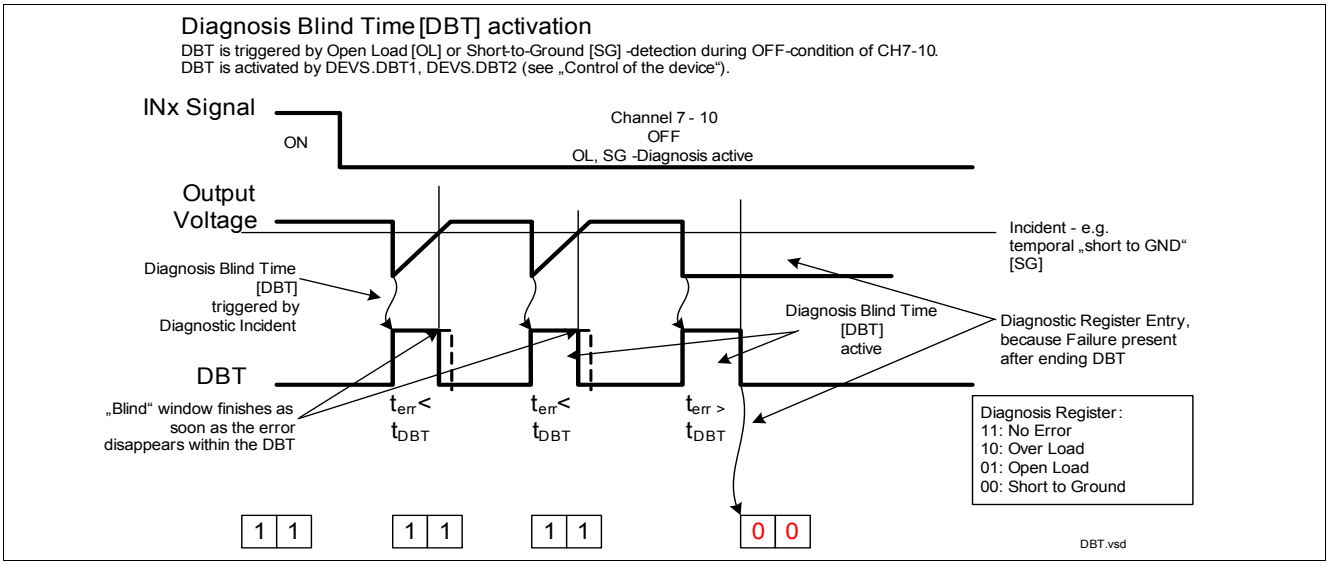


Figure 19 Diagnosis Blind Time

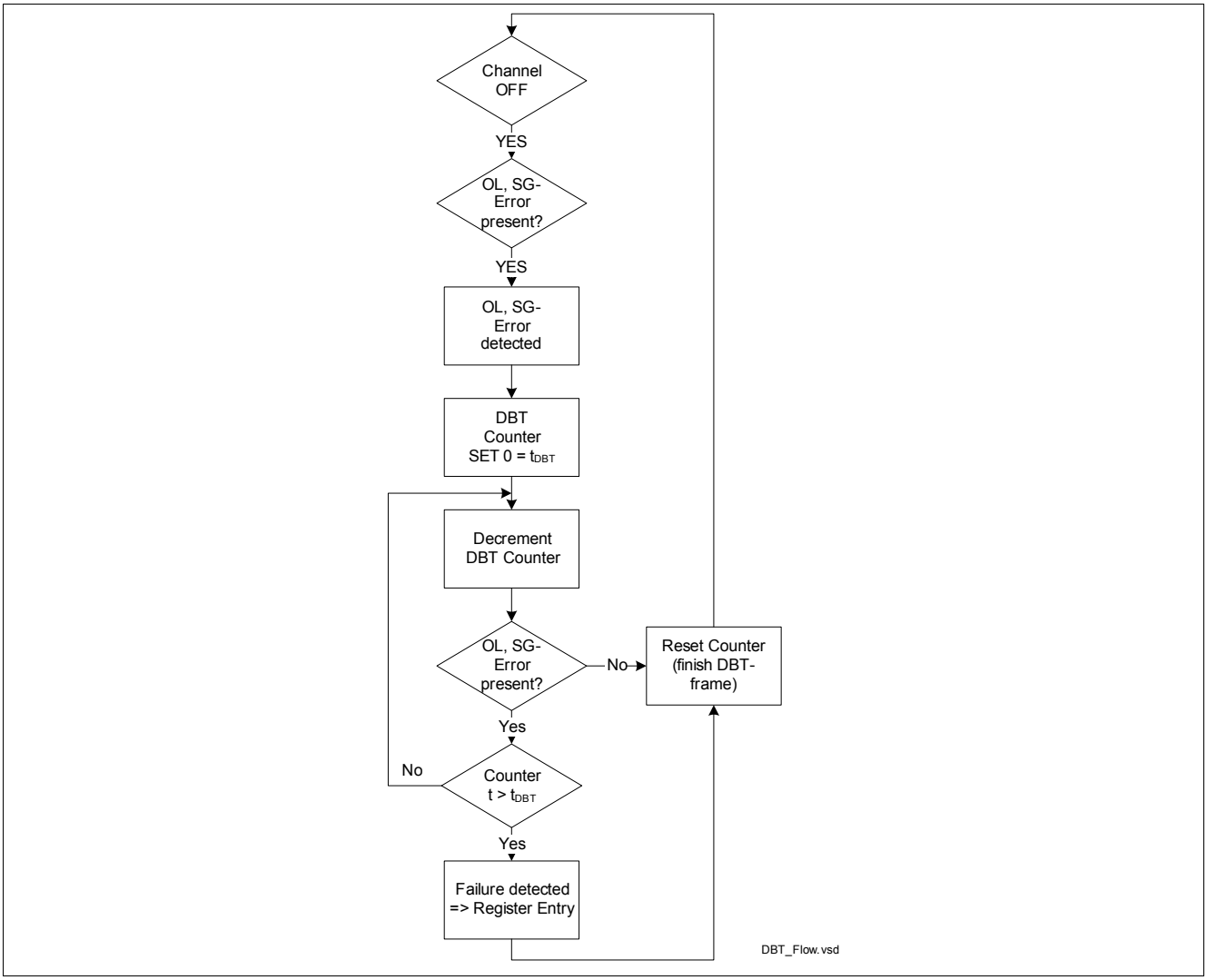


Figure 20 Diagnosis Blind Time - Logic Flow

9 Parallel Inputs

9.1 Description Parallel Inputs

There are 10 input pins available are on TLE8110EE to control the output stages.

Each input signal controls the output stages of its assigned channel. For example, IN1 controls OUT1, IN2 controls OUT2, etc.

A “Low”-Signal at INx switches the related Output Channel off. The zener diode protects the input circuit against ESD pulses.

For details about the Boolean operation, refer to the chapter “Control of the device”, for details about timing refer to **Figure 12**.

9.2 Electrical Characteristics Parallel Inputs

Electrical Characteristics: Parallel Inputs

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Parallel Inputs							
9.2.1	Low Level of parallel Input pin	V_{INxl}	-0.3	-	V_{CC}* 0.2	V	-
9.2.2	High Level of Parallel Input pin	V_{INxh}	V_{CC}* 0.4	-	V_{CC}	V	-
9.2.3	Parallel Input Pin Switching Hysteresis	V_{INxhy}	15	60	300	mV	1)
9.2.4 a)	Input Pin pull-down Current	I_{INxh}	20	40	85	µA	V_{INx}=5V
.....b)		I_{INxl}	2.4	-	-	µA	V_{INx}=0.6V 1)

1) Parameter not subject to production test. Specified by design.

10 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this Document. Fault conditions are considered “outside” the normal operating range. Protection functions are not designed for continuous repetitive operation.

There is an over load and over temperature protection implemented in the TLE8110EE.

If a protection function becomes active during the write cycle of Diagnosis Information into the Diagnosis Register, the information is latched and stored into the diagnosis register after the write process.

In order to achieve a maximum protection, the affected channel with over current or over temperature (OCT) is switched and latched OFF, channel can be turned ON again after the diagnosis register is cleared (**Chapter 12.3.2**) or if a different new diagnosis overrides the OCT.

For the failure condition of Reverse Currents, the device contains a “Reverse Current Protection Comparator” [RCP]. This RCP can optionally be activated by setting the DEVS.RCP Bit.
In case the comparator is activated, it detects a reverse current and switches ON the related output channel. The channel is kept ON up to a reverse current channel dependent threshold I_{RCP_off}. This threshold is defined by regulators target value to keep the output voltage at >/~-0.3V. If the current exceeds a defined value, the comparator switches OFF and other protection functions are protecting the circuit against reverse current. That means that at higher currents / or in case RCP is de-activated / not activated, the reverse current is flowing through the body diode of the DMOS. In that case, the voltage drops to typically -0.6V according the voltage of the body diode. In case the comparator threshold has been exceeded and the RCP has been switched OFF, the functions remains OFF until the reverse current arrives back to zero reverse current. Only then, the comparator can be activated again after a delay time $t_{RCP_on_delay}$.
This function reduces the un-wanted influence of a reverse current to the analogue part of the circuit (such as the diagnosis). For more details about the functionality, see **Figure 23** and **Figure 24** and concerning the settings and the related registers, refer to Chapter “Control of the Device”.

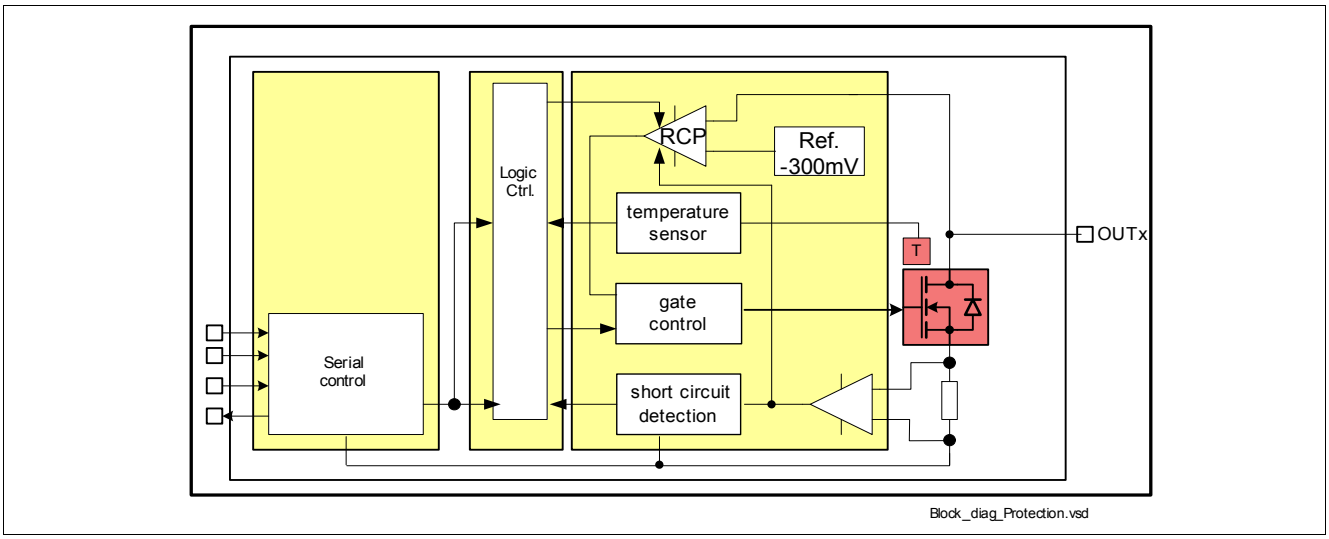


Figure 21 Block Diagram Protection Functions

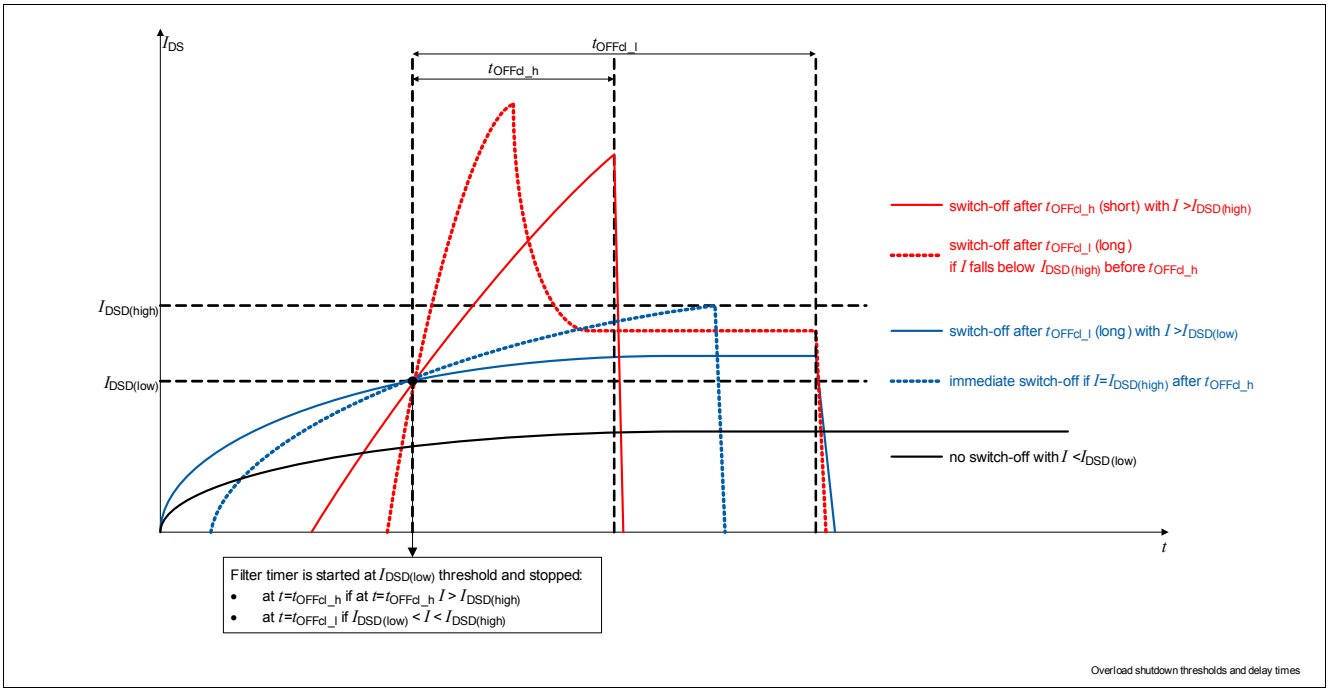


Figure 22 Overload shutdown thresholds and delay times

10.1 Electrical Characteristics Overload Protection Function

Electrical Characteristics: Overload Protection Function

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Over Current Protection							
10.1.1	Output Current Shut-down Threshold Low (Channel 1 to 4)	$I_{DSD(low)}$	2.6	3.8	5	A	-
10.1.2	Output Current Shut-down Threshold Low (Channel 5 to 6)	$I_{DSD(low)}$	3.70	4.85	6.00	A	-
10.1.3	Output Current Shut-down Threshold Low (Channel 7 to 10)	$I_{DSD(low)}$	1.7	2.3	2.9	A	-
10.1.4	Output Current Shut-down Threshold High (Channel 1 to 4)	$I_{DSD(high)}$	-	1.5 * $I_{DSD(low)}$	-	A	1)
10.1.5	Output Current Shut-down Threshold High (Channel 5 to 6)	$I_{DSD(high)}$	-	1.5 * $I_{DSD(low)}$	-	A	1)
10.1.6	Output Current Shut-down Threshold High (Channel 7 to 10)	$I_{DSD(high)}$	-	1.5 * $I_{DSD(low)}$	-	A	1)
10.1.7	Short Overload shutdown Delay Time (all Channels)	t_{OFFcl_h}	5	21	40	µs	valid for “Output Current Threshold High” 1)
10.1.8	Long Overload shutdown Delay Time (all Channels)	t_{OFFcl_l}	10	40	70	µs	valid for “Output Current Threshold Low”
Over Temperature Protection							
10.1.9	Thermal Shut Down Temperature	T_{jSD}	175	190	205	°C	1)
10.1.10	Thermal Shut Down Hysteresis	T_{jSDh}	10	-	20	K	1)

Electrical Characteristics: Overload Protection Function (cont'd)

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reverse Current Protection							
10.1.11	Reverse Current Comparator Switch-off Current level CH 1 - 4	I_{RCP_off}	-	-0.9	-	A	DEVS.RCP = 1[1)] Tj = 25°C
10.1.12	Reverse Current Comparator Switch-off Current level CH 5 - 6	I_{RCP_off}	-	-0.6	-	A	DEVS.RCP = 1[1)] Tj = 25°C
10.1.13	Reverse Current Comparator Switch-off Current level CH 7 - 10	I_{RCP_off}	-	-0.45	-	A	DEVS.RCP = 1[1)] Tj = 25°C
10.1.14	Reverse Current Comparator switch on delay time	$t_{RCP_on_delay}$	-	24	-	µs	DEVS.RCP = 1[1)] Tj = 25°C

1) Parameter not subject to production test. Specified by design.

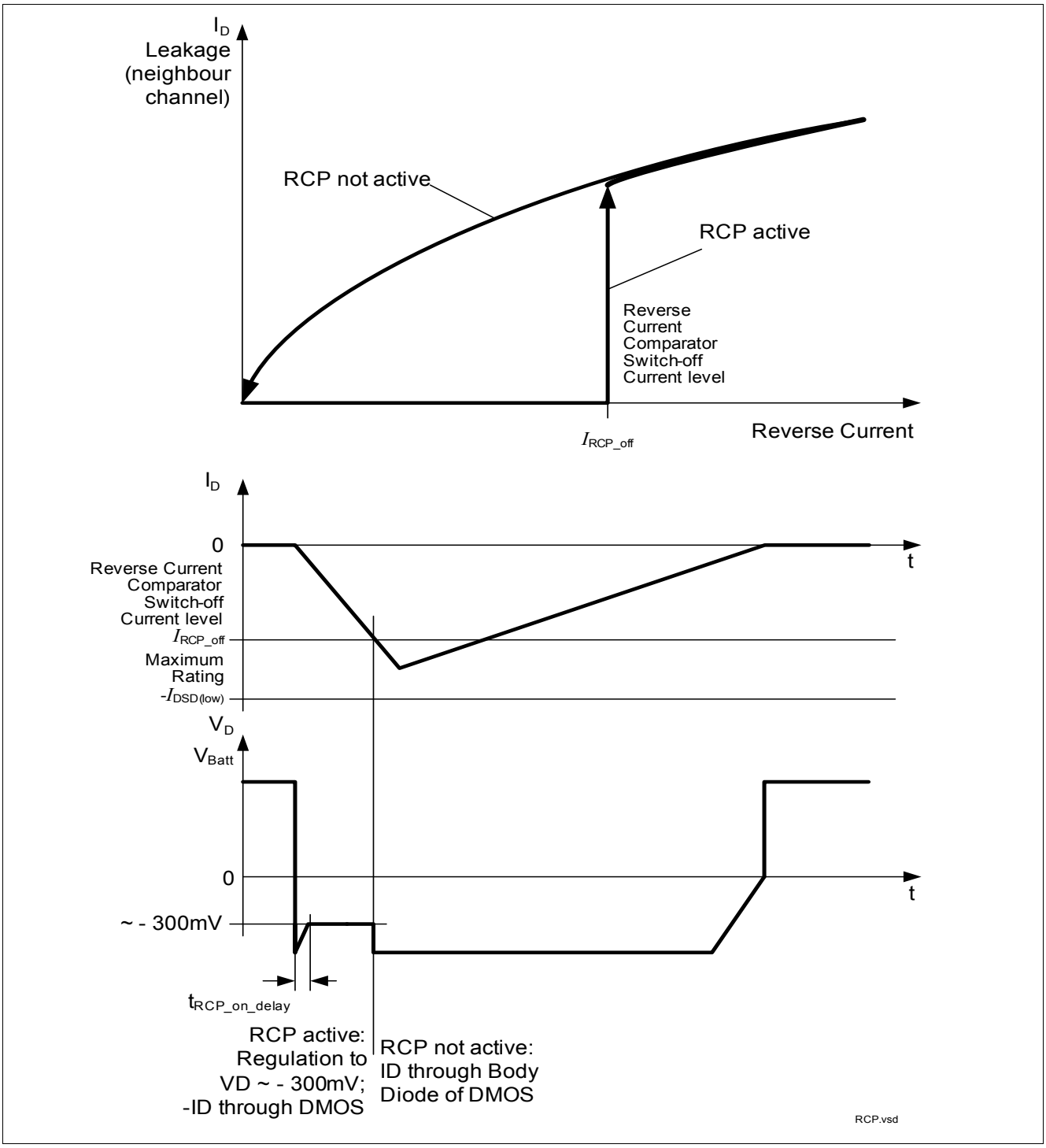


Figure 23 Reverse Current Protection Comparator 6

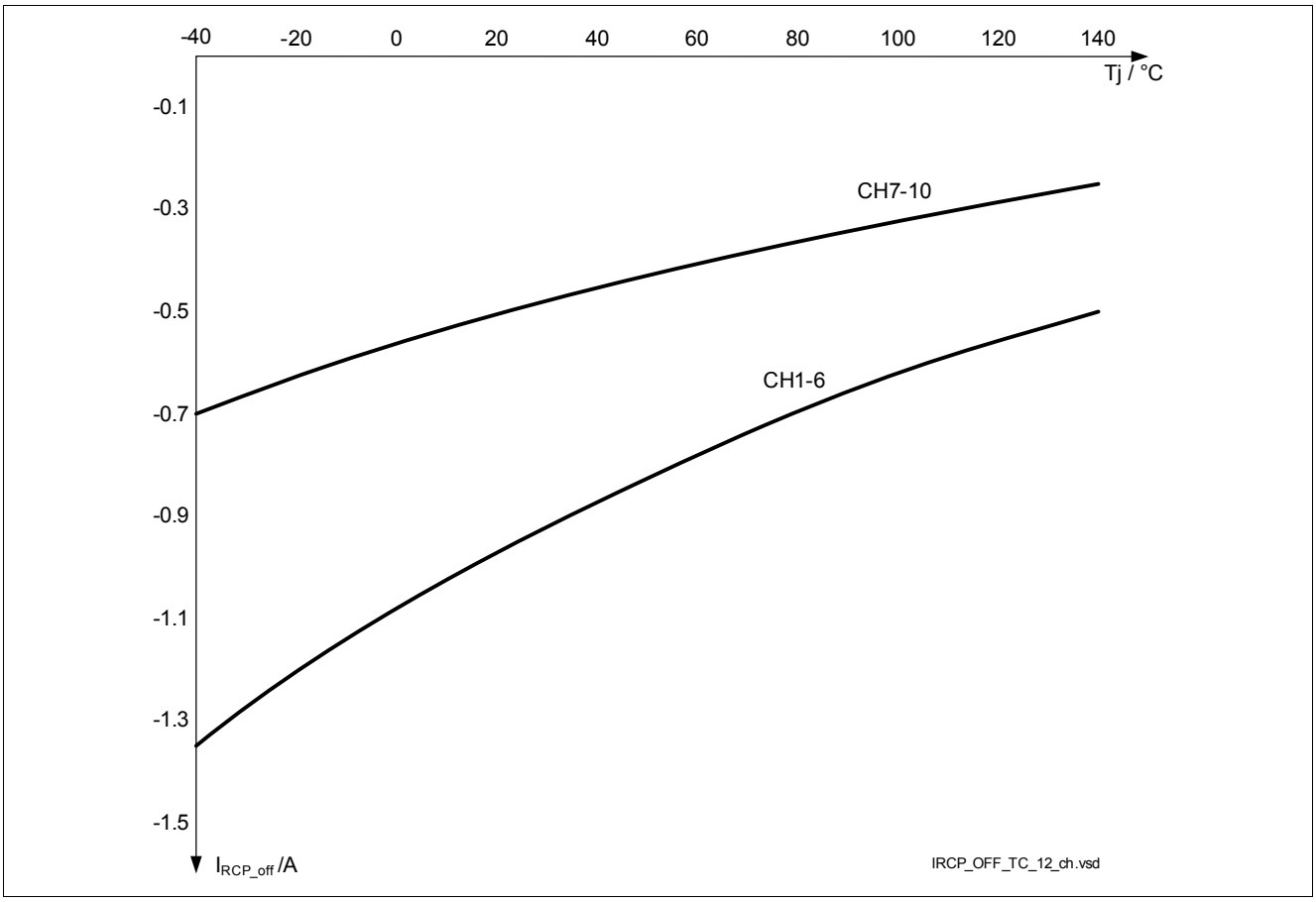


Figure 24 Reverse Current Protection Comparator (typical behavior vs junction temperature)

11 16 bit SPI Interface

11.1 Description 16 bit SPI Interface

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: S_SO, S_SI, S_CLK and $\overline{\text{S_CS}}$. Data is transferred by the lines S_SI and S_SO at the data rate given by S_CLK. The falling edge of $\overline{\text{S_CS}}$ indicates the beginning of a data access. Data is sampled in on line S_SI at the falling edge of S_CLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{\text{S_CS}}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. If in one transfer cycle not a multiple of 8 bits have been counted, the data frame is ignored. The interface provides daisy chain capability.

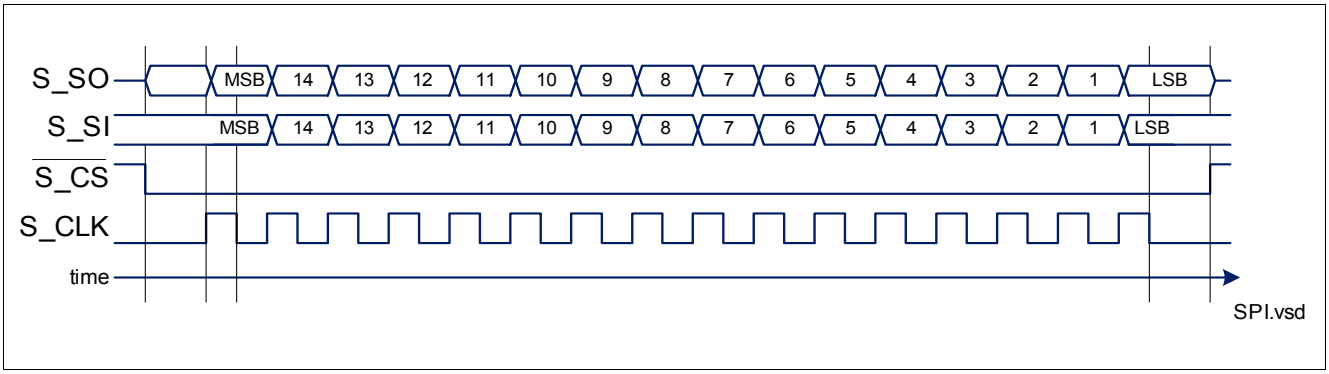


Figure 25 16 bit SPI Interface

The SPI protocol is described in Chapter “Control of the device”. Concerning Reset of the SPI, please refer to the chapter “Reset”

11.2 Timing Diagrams

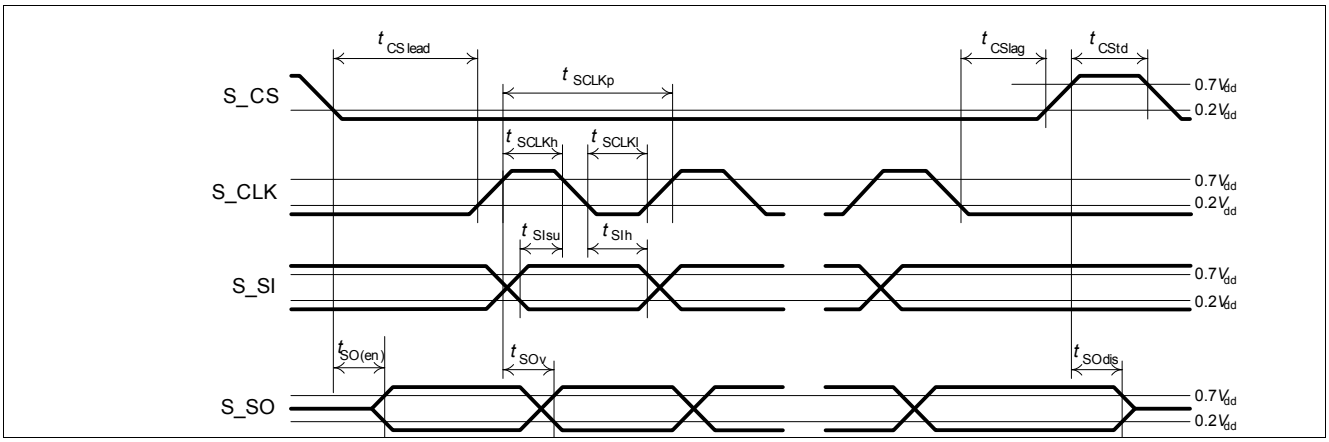


Figure 26 SPI timing diagram

11.3 Electrical Characteristics 16 bit SPI Interface

Electrical Characteristics: 16 bit SPI Interface

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
11.3.1	L level of pin $\overline{S_CS}$ S_CLK S_SI	V_{S_CSl} V_{S_CLKl} V_{S_Sll}	-0.3	-	V_{CC}* 0.2	V	-
11.3.2	H level of pin $\overline{S_CS}$ S_CLK S_SI	V_{S_CSh} V_{S_CLKh} V_{S_Slh}	V_{CC}* 0.4	-	V_{CC}	V	-
11.3.3	Hysteresis Input Pins	V_{S_CShy} V_{S_CLKhy} V_{S_Slhy}	20	100	300	mV	-
11.3.4 a)	Input Pin pull-down Current	I_{S_CLKh} I_{S_Slh}	20	40	85	µA	V_{IN}=5V
b)	S_CLK S_SI	I_{S_CLKl} I_{S_Sll}	2.4	-	-	µA	V_{IN}=0.6V[1)]
11.3.5 a)	Input Pin pull-up Current	I_{S_CSh}	-4	-	-	µA	V_{S_CS} = 2 V, V_{CC}=3.3V
b)	$\overline{S_CS}$	I_{S_CSl}	-20	-40	-85	µA	V_{S_CS} = 0 V, V_{CC}=5V
Output Characteristics (SO)							
11.3.6	L level output voltage	V_{S_SOl}	0	-	0.4	V	I_{S_SO} = -2 mA
11.3.7	H level output voltage	V_{S_SOh}	V_{cc} - 0.4 V	-	V_{cc}		I_{S_SO} = 1.5 mA
11.3.8	Output tristate leakage current	I_{S_SOoff}	-10	-	10	µA	V_{S_SO} = V_{cc}
Timings							
11.3.9	Serial clock frequency	f_{S_CLK}	0	-	5	MHz	-C_L = 50 pF [1)]
11.3.10	Serial clock period	$t_{S_CLK(P)}$	200	-	-	ns	[1)]
11.3.11	Serial clock high time	$t_{SCLK(H)}$	50	-	-	ns	[1)]
11.3.12	Serial clock low time	$t_{SCLK(L)}$	50	-	-	ns	[1)]
11.3.13	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	250	-	-	ns	[1)]
11.3.14	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	250	-	-	ns	[1)]
11.3.15	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	250	-	-	ns	[1)]
11.3.16	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	-	-	ns	[1)]
11.3.17	Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	-	-	ns	[1)]
11.3.18	Output enable time (falling $\overline{CS}$ to SO valid)	$t_{SO(en)}$	-	-	200	ns	C_L = 50 pF [1)]

Electrical Characteristics: 16 bit SPI Interface (cont'd)

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
11.3.19	Output disable time (rising $\overline{CS}$ to SO tri-state)	$t_{SO(dis)}$	-	-	200	ns	C_L = 50 pF 1)
11.3.20	Output data valid time with capacitive load	$t_{SO(v)}$	-	-	100	ns	C_L = 50 pF 1)
11.3.21	Diagnosis Clear-to-Read Idle Time	t_{Didle}	16	-	-	µs	1)
11.3.22	Diagnosis Overcurrent-to-Clear Idle Time	t_{OCidle}	12	-	-	µs	1)

1) Not subject to production test, specified by design.

12 Control of the device

This chapter describes the SPI-Interface signals, the protocol, registers and commands. Reading this chapter allows the Software Engineer to control the device. The chapter contains also some information about communication safety features of the protocol.

12.1 Internal Clock

The device contains an internal clock oscillator.

Electrical Characteristics: Internal Clock

3.0V < V_{CC} < 5.5V; 4.5V < V_{DD} < 5.5V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Parallel Inputs							
12.1.1	internal clock oscillator frequency	f_{int_osc}	-	500	-	kHz	1)

1) Parameter not subject to production test. Specified by design.

12.2 SPI Interface. Signals and Protocol

12.2.1 Description 16 bit SPI Interface Signals

$\overline{\text{S_CS}}$ - Chip Select:

The system micro controller selects the TLE8110EE by means of the $\overline{\text{S_CS}}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{\text{S_CS}}$ is in high state, any signals at the S_CLK and S_SI pins are ignored and S_SO is forced into a high impedance state.

$\overline{\text{S_CS}}$ High to Low transition: ⎺_

- The information to be transferred loaded into the shift register (16-bit Protocol).
-

$\overline{\text{S_CS}}$ Low to High transition: _/⎺

- Command decoding is only done, when after the falling edge of CS exactly a multiple (1, 2, 3, …) of eight S_CLK signals have been detected. (See Modulo-8 Counter: **Chapter 12.2.4.2**)

S_CLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (S_SI) transfers data is shifted into the register on the falling edge of S_CLK while the serial output (S_SO) shifts the information out on the rising edge of the serial clock. It is essential that the S_CLK pin is in low state whenever chip select CS makes any transition.

S_SI - Serial Input:

Serial input data bits are shifted in at this pin, the most significant bit first. The bit at the S_SI Pin is read on the falling edge of S_CLK.

S_SO Serial Output:

Data is shifted out serially at this pin, the most significant bit first. S_SO is in high impedance state until the $\overline{\text{S_CS}}$ pin goes to low state.The next bits will appear at the S_SO pin following the rising edge of S_CLK.

12.2.2 Daisy Chain

The SPI-Interface of TLE8110EE provides daisy chain capability, see **Chapter 12.2.3.4** for more details. In this configuration several devices are activated by the same $\overline{\text{S_CS}}$ signal. The S_SI line of one device is connected with the S_SO line of another device (see **Figure 27**), which builds a chain. The ends of the chain are connected with the output and input of the master device, S_SO and S_SI respectively. The master device provides the master clock CLK, which is connected to the S_CLK line of each device in the chain. By each clock edge on S_CLK, one bit is shifted into the S_SI. The bit shifted out can be seen at SO. After 16 S_CLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{\text{S_CS}}$ line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device 1 has been shifted in to device 2. Example: When using three devices in daisy chain, three times 16 bits have to be shifted through the devices. After that, the $\overline{\text{S_CS}}$ line must go high (see **Figure 27**).

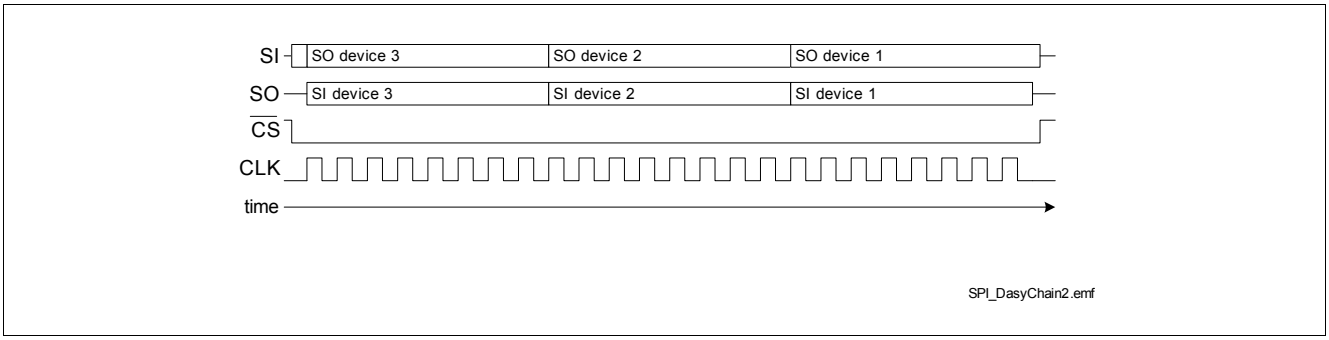


Figure 27 Principle example for Data Transfer in Daisy Chain Configuration

Note: Due to the integrated modulo 8 counter, 8 bit and 16 bit devices can be used in one daisy chain.

12.2.3 SPI Protocol

The device contains two protocol styles which are applied dependent of the used commands. There is the standard 16-bit protocol and the 2x8-bit protocol. Both protocols can appear also be mixed.

12.2.3.1 16-bit protocol

Each Cycle where a serial data or command frame is sent to the S_SI of the SPI interface, a data frame is returned at the same time by the S_SO The content of the S_SO frame is dependent on the previous command which has been sent to S_SI. Read Command (R/W = R) returns one cycle later the content of the addresses register. (see **Figure 28**).

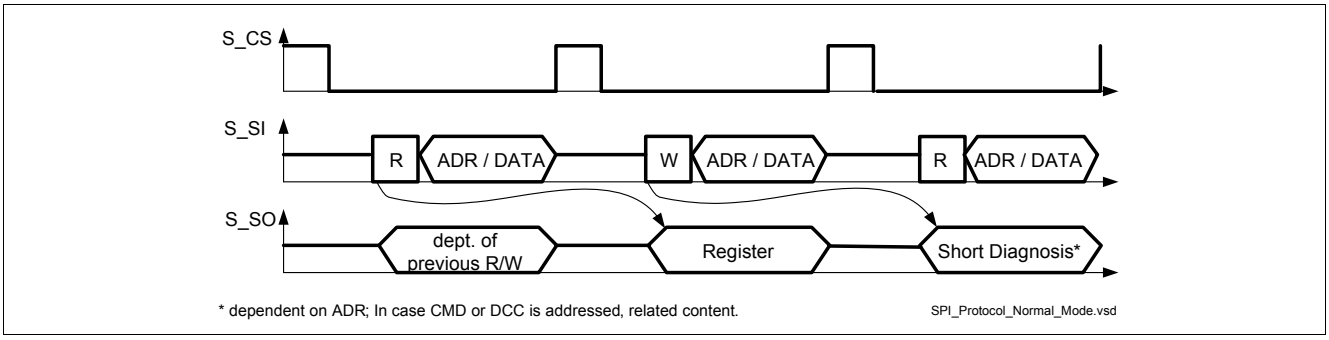


Figure 28 16-bit protocol

S_SI
Serial Input **Reset Value: N.A.**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{W}$/R	**ADDR**			**DATA / CMD**											

Field	Bits	Description
$\overline{W}$/R	15	**$\overline{W}$/R - $\overline{W}$rite / Read** 0 Write register: The register content of the addressed register will be updated after CS low → high transition. After sending a WRITE command, the device returns data according the addressed register 1 Read register: The register content of the addressed register will be sent in the next frame.
ADDR	14:12	**ADDR - Address** Pointer to register for read and write command
DATA/CMD	11:0	**DATA_CMD - Data / Command** Data written to or read from register selected by address ADDR

S_SO
Serial Output **Reset Value: xxxx xxxx xxxx $xxxx_B$ [1)]**

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAR	**ADDR**			**DATA**											

1) after reset is send a Short Diagnosis and Device Status CMD_CSDS, see **Chapter 12.3.1.2**.

Field	Bits	Description
PAR	15	**PAR - Parity Bit** 1: odd number of '1' in data and address field 0: even number of '1' in data and address field
ADDR	14:12	**Address** Address which has bin addressed
DATA	11:0	**Data** Content of Address or feedback Data

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame.

12.2.3.2 2x8-bit protocol

Each Cycle where a serial data or command frame is sent to the S_SI of the SPI interface, a data frame is returned at the same time by the S_SO. The content of the S_SO frame is dependent of the previous command which has been sent to S_SI and the content of the actual content of S_SI: The first Upper Byte send to S_SI controls the content of the Lower Byte actual returned by S_SO. The Lower Byte send to S_SI controls the Lower Byte in S_SO of the next frame. (see **Figure 29**).

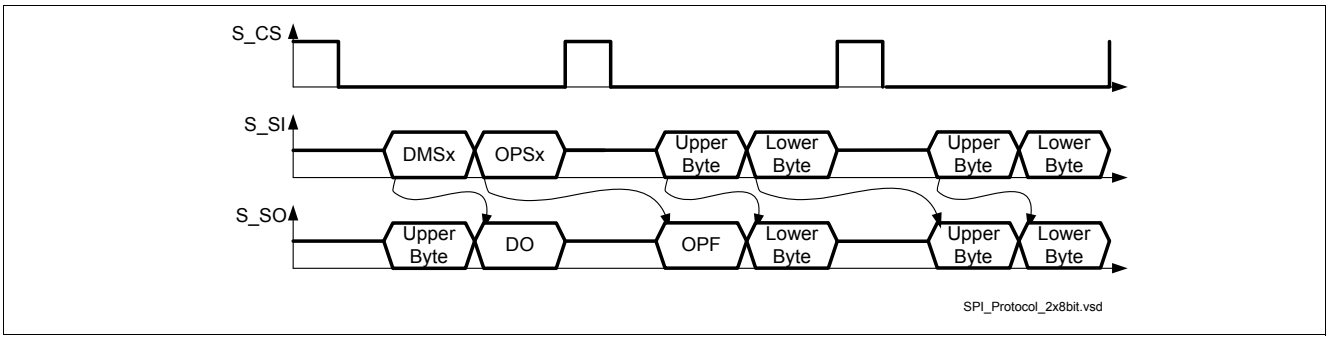
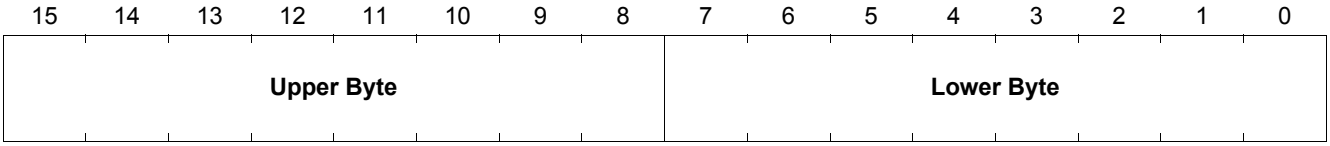


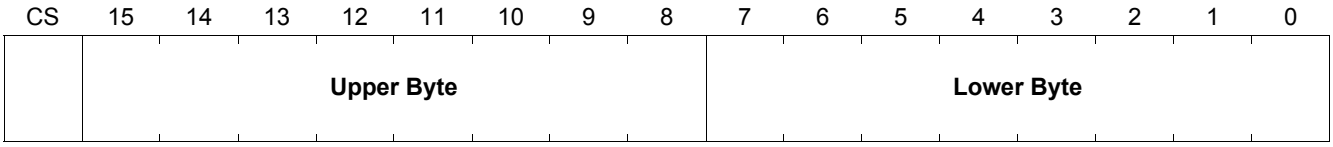
Figure 29 2x8-bit protocol

S_SI
Serial Input **Reset Value: N.A.**



Field	Bits	Description
Upper Byte	15:8	**Upper Byte** contains the command, which is performed after sending 8 bit to S_SI. The action out of this command is affecting the Lower Byte of S_SO of the actual communication frame.
Lower Byte	7:0	**Lower Byte** contains the command and data, which is performed at the end of the actual communication frame. The action out of this command is affection the Upper Byte of S_SO of next communication frame.

S_SO
Serial Output **Reset Value: xxxx xxxx xxxx $xxxx_B$ 1)**



1) after reset is send a Short Diagnosis and Device Status CMD_CSDS, see **Chapter 12.3.1.2**.

Field	Bits	Description
Upper Byte	15:8	**Upper Byte** contains the data according the command and data in the Lower Byte of the previous communication Frame.
Lower Byte	7:0	**Lower Byte** contains the data according the command in the Upper Byte of the actual communication frame

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame.

12.2.3.3 16- and 2x8-bit protocol mixed.

The 16-bit and 2x8-bit protocols are mixed according the used commands (see **Chapter 12.3.1**). Special care should be taken, changing from the 16-bit protocol to the 2x8-bit protocol. In this case, it is important to send a NOP command to S_SI. Otherwise, by sending instead a Command, a collision between the S_SO data in the following frame and the Lower Byte of the 2x8-bit protocol will happen (see **Chapter 12.2.3.2**).

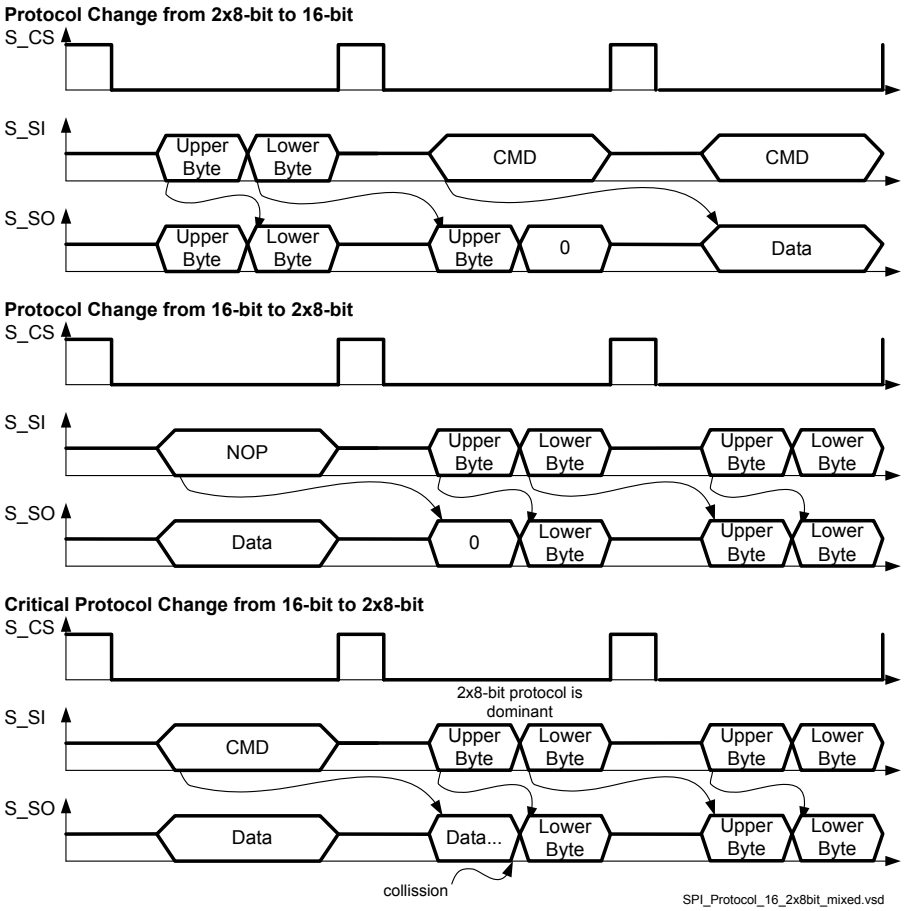


Figure 30 16-bit protocol

12.2.3.4 Daisy-Chain and 2x8-bit protocol

When using the TLE8110EE in a daisy-chain connection with other devices (TLE8110EE and non) special care has to be taken to avoid interference of 2x8-bit protocol with normal communication. Few simplified rules must be followed for a safe SPI communication in daisy-chain environment:

1. All TLE8110EE devices have to be routed at the beginning of the chain, other devices than TLE8110EE afterward
2. compactCONTROL commands (2x8-bit protocol) must not be addressed to TLE8110EE
3. The SPI frame of the daisy-chain must be extended of additional 8-bit (all zeros 00_H) at beginning of the frame
4. When a Read/Clear Diagnosis Register A command (DRA, DRACL) is addressed to TLE8110EE, a NOP command must be sent to the next TLE8110EE on the chain
5. When a Read/Clear Diagnosis Register A command (DRA, DRACL) is addressed to TLE8110EE, response of the next device on the chain must be ignored in the next SPI cycle

Details in **Figure 31** and **Figure 32**.

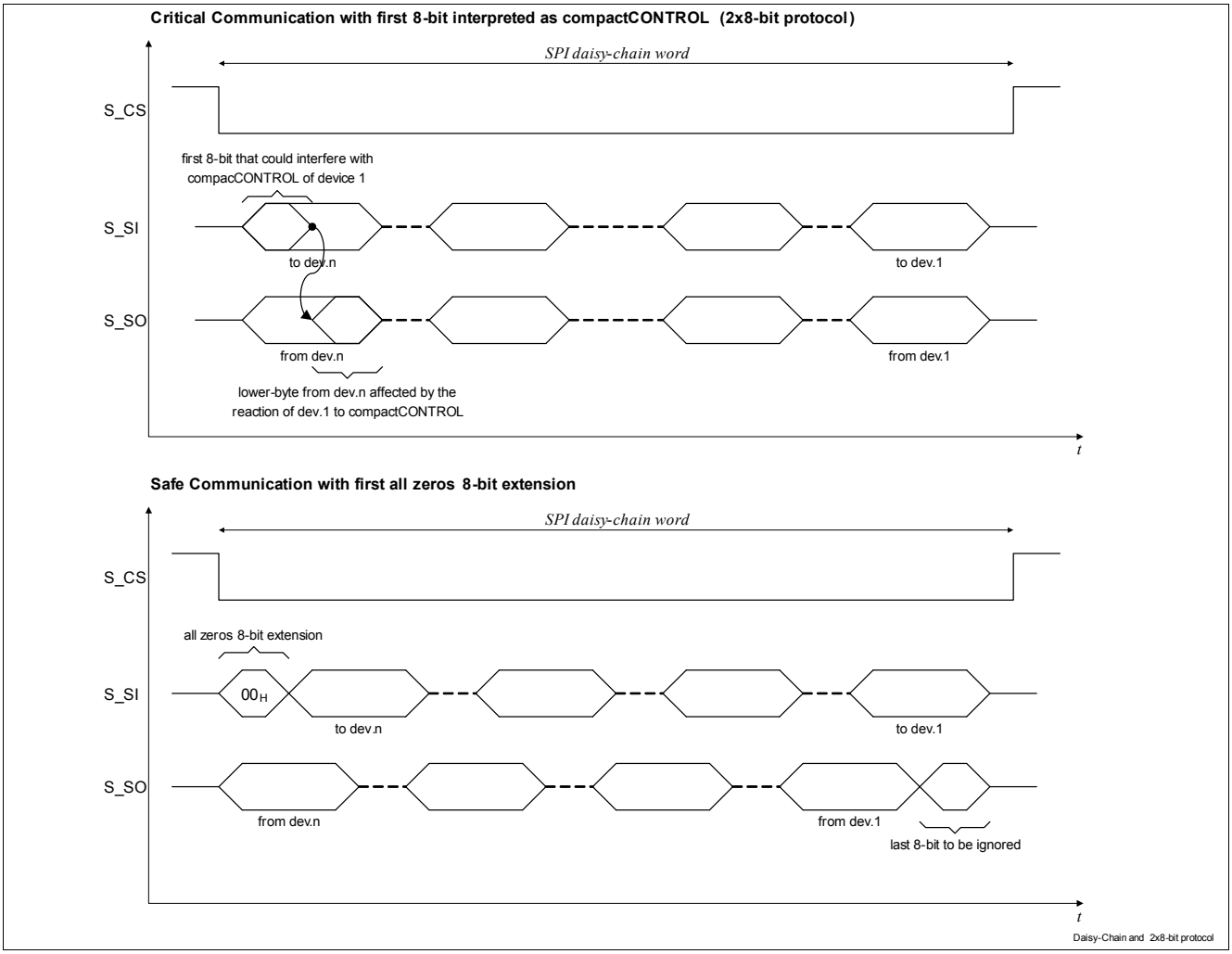


Figure 31 Daisy-Chain and 2x8-bit protocol

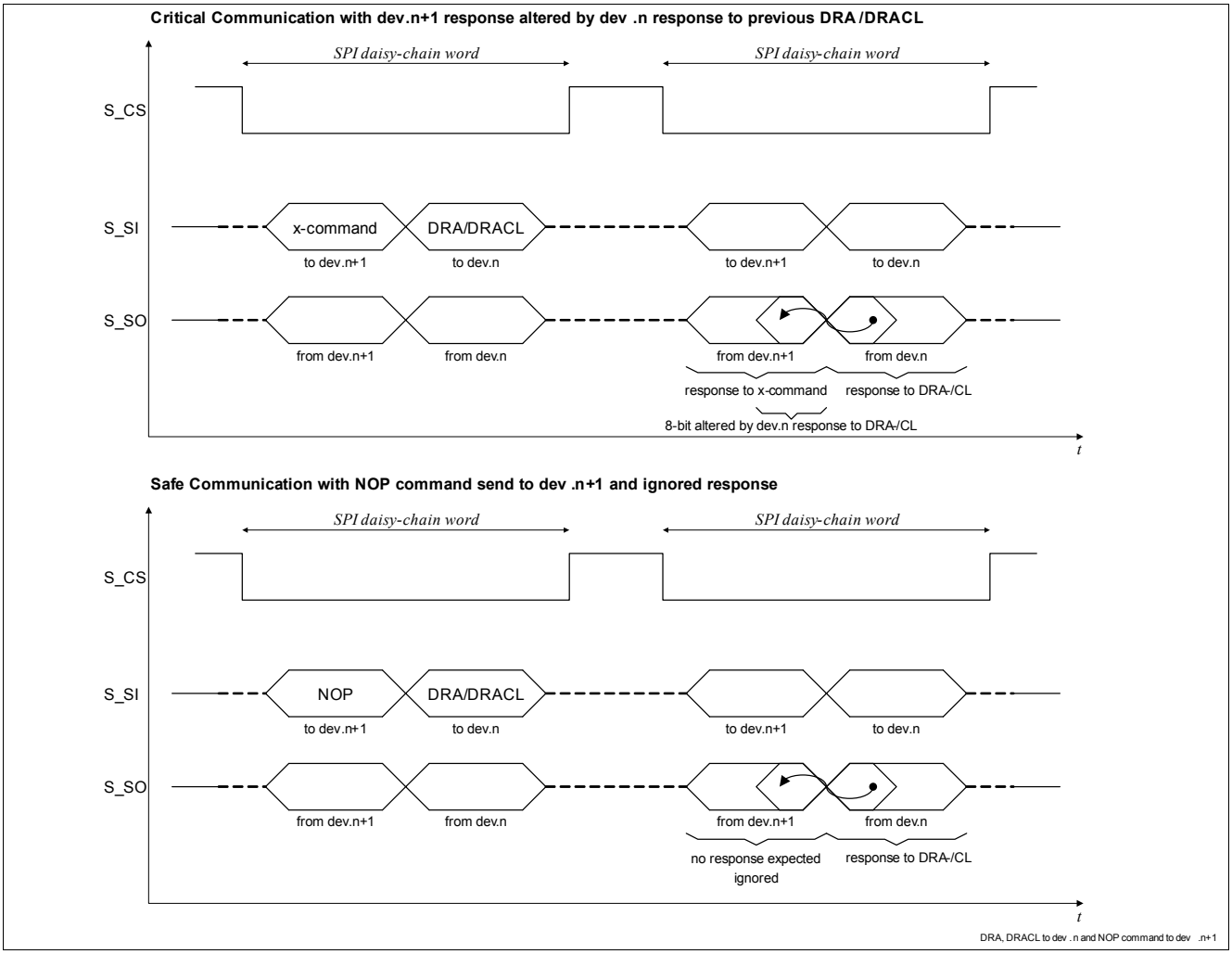


Figure 32 DRA, DRACL to dev.n and NOP command to dev.n+1

12.2.4 safeCOMMUNICATION

The device contains some safety features, which are improving the protection of the application against malfunction in case of disturbance of the communication between the Micro Controller and the Device:

12.2.4.1 Encoding of the commands

The Commands are encoded. In case other bit-patterns, then the defined once are received, the commands are ignored and the communication error can be read out with the command CMD_RSDS (see**Chapter 12.3.1.2**).

12.2.4.2 Modulo-8 Counter

The modulo is the integral remainder in integral division. In data communications, a modulo based approach is used to ensure that user information in SPI protocols is in the correct order. The device has a receiver-side counter, and a defined counter size. The modulo counter specifies the number of subsequent numbers available. In case of TLE8110EE Modulo 8 counter specifies 8 serial numbers. The modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. If in one transfer cycle not a multiple of 8 bits have been counted, the data frame is ignored and a Communication Error is indicated in the CMD_RSDS - Feedback (see**Chapter 12.3.1.2**).

12.3 Register and Command - Overview

This Chapter describes the Registers and Commands. The commands allow to carry through some actions, such as reading out or clearing the diagnosis or reading out the Input Pins.

Specially highlighted here should be the encoded CMD_DMSx/OPSx commands - compactCONTROL -, a highly efficient command-set to set a part of the output pins and read out the diagnosis at the same time. Included in this command set is the possibility to check, if the communication works well as also the possibility to read-out some of the parallel Input Pins INx. Using this compact command set can reduce the workload of the micro-controller during run-time significantly.

CMD_RSD is preformed and short diagnostics [SD] is returned after each Write Cycle to any of the writable registers.

After start-up of the device, the registers are loaded with the default settings as described below in the register descriptions. The Registers are cleared and set back to the default values, when a low signal is applied to the pin $\overline{\text{RST}}$ or an under-voltage condition appears at the supply pin V_{CC} what causes an under-voltage reset. If a low signal at pin EN is applied or an under-voltage condition appears at pin V_{DD}, the Registers are not cleared.

Table 1

Name	Type	Addr	Short Description	see:
CMD	W[1)]	000_B	Commands	Chapter 12.3.1
DCC	W[1)]	001_B	Diagnosis Registers and Compact Control	Chapter 12.3.2
OUTx	W/R	010_B	Output Control Register CHx.	Chapter 12.3.3
DEVS	W/R	011_B	Device Settings	Chapter 12.3.6
MSCS	W/R	100_B	reserved	
ISAx	W/R	101_B	Input or Serial Mode Register CHx Bank A	Chapter 12.3.4
ISBx	W/R	110_B	Input or Serial Mode Register CHx Bank B	Chapter 12.3.4
PMx	W/R	111_B	Parallel Mode Control of CHx with CHy	Chapter 12.3.5

1) if a read command is send, the command is ignored and S_SO returns a frame with ’0’.

Table 2

Register Overview

Name		Addr	11	10	9	8	7	6	5	4	3	2	1	0	def.[1)]
CMD	W[2)]	000_B	0	1	1	1	Command								---
DCC	W[2)]	001_B	Command												---
OUTx	W/R	010_B	1	1	OUT 10	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	C00h
DEVS	W/R	011_B	RCP	DBT2	DBT1	0	0	0	0	0	0	DCC 10	DCC 9	DCC 18	007h
MSCS	W/R	100_B	reserved												000h
ISAx	W/R	101_B	IS6		IS5		IS4		IS3		IS2		IS1		AAAh
ISBx	W/R	110_B	0	0	0	0	IS10		IS9		IS8		IS7		0AAh
PMx	W/R	111_B	0	0	0	0	PM91 0	PM89	PM78	PM56	0	PM34	PM23	PM12	000h

1) Default Values after Reset

2) if a read command is send, the command is ignored and S_SO returns a frame with ’0’.

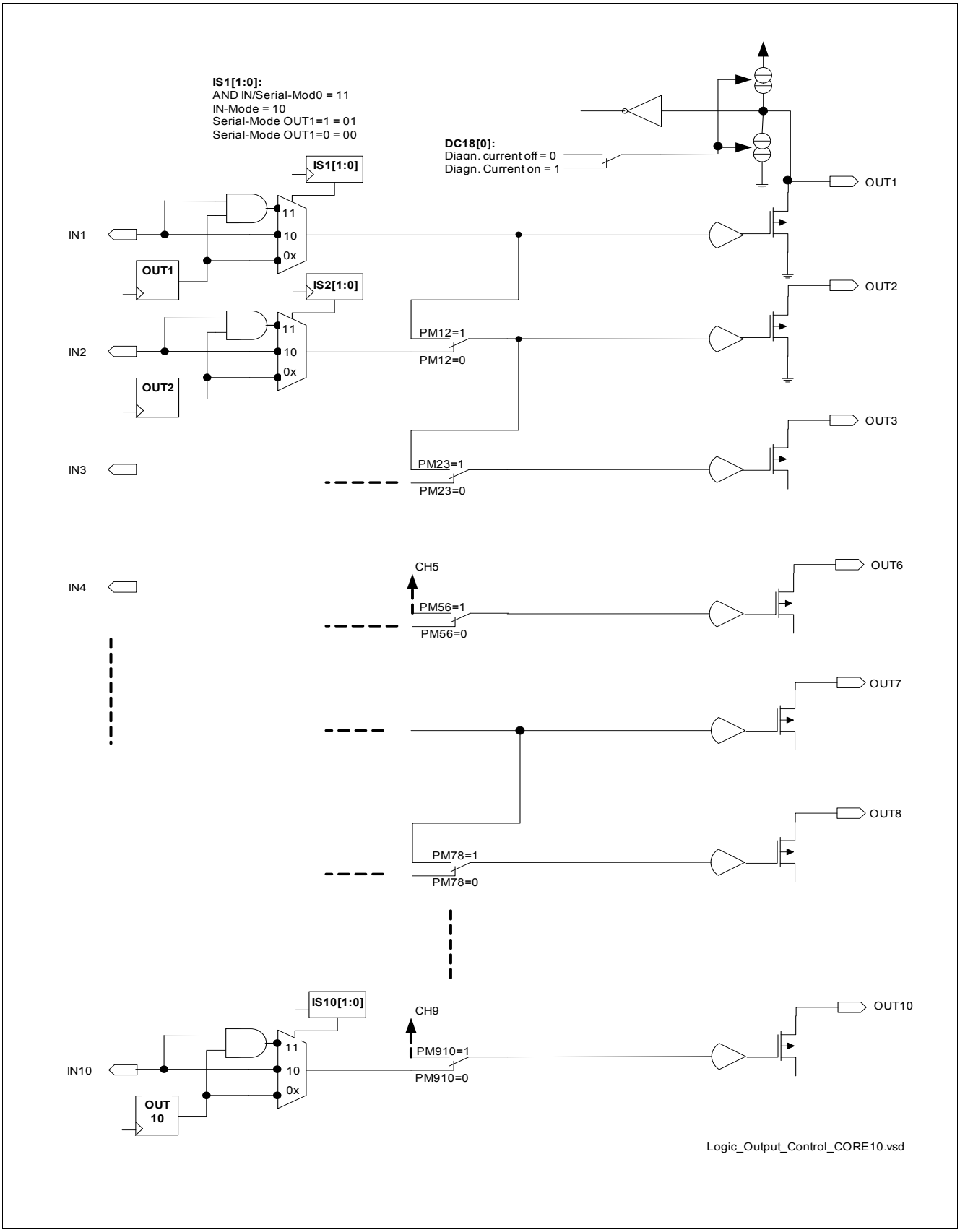


Figure 33 Logic Output Control Block Diagram TLE8110EE

12.3.1 CMD - Commands

By using the Address Range CMD[14:12]=’000’ commands can be send to the device. The Feedback of the commands is provided in the next SPI SO Frame.Details about the Feedback on each command is described in the Chapter 12.3.1.1.

It is possible to perform per each Communication Frame ONE Command out of Group-A (see following description of the Commands) and ONE Command out of Group-B at the same time. Performing more then one Command of one Group is not possible. For the case, this happens, the commands are ignored.

CMD **Command Register**	**Reset Value: N.A.**

Overview Commands

S_SI
SPI_Serial Input

CMD	11	10	9	8	7	6	5	4	3	2	1	0
RSD	0	1	1	1	0	0	0	0	0	0	0	1
RSDS	0	1	1	1	0	0	0	0	0	0	1	0
RPC	0	1	1	1	0	0	0	0	0	1	0	0
RINx	0	1	1	1	0	0	0	0	1	0	0	0
CSDS	0	1	1	1	0	0	0	1	0	0	0	0
NOP	0	1	1	1	0	0	0	0	0	0	0	0

Field	Command	Type	Description
Command Bits Group-B (Bits [7:4]) All other bit combinations are not valid. Command will be ignored then.			
NOP	0000	W	**NOP - no operation.** A frame with ’0000h’ will be returned
CMD_CSDS	0001	W	**CMD_CSDS - Command: Clear Short Diagnosis and Device Status** Clear the Device Status information. Performing this Clear Command clears the Information in the Reset and Communication Error Information as long as the incident is not present anymore. If the incident is still present, the related Bits remain setted. Performing this command does NOT clear the Diagnosis Registers. The Diagnosis Information is cleared by the Clear Diagnosis Commands. (see Chapter 12.3.2) SO returns a Frame with ’0000h’ after performing CMD_CSDS or in case this command is carried out together with a command out of Group-A, the feedback is according the Group-A command
Command Bits Group-A (Bits [3:0]) All other bit combinations are not valid. Command will be ignored then.			

Field	Command	Type	Description
CMD_NOP	0000	W	**NOP - no operation.** A frame with ’0000h’ will be returned
CMD_RINx	1000	W	**CMD_RINx - Command: Return Input Pin INx -Status** (**Chapter 12.3.1.4**)
CMD_RPC	0100	W	**CMD_RPC - Command: Return Pattern Check** (**Chapter 12.3.1.3**)
CMD_RSDS	0010	W	**CMD_RSDS - Command: Return Short Diagnosis and Device Status** **(Chapter 12.3.1.2)**
CMD_RSD	0001	W	**CMD_RSD - Command: Return Short Diagnosis** **(Chapter 12.3.1.1)**

12.3.1.1 CMD_RSD - Command: Return Short Diagnosis

The Command CMD_RSD offers the possibility to read out the OR-operated “short”-Diagnosis within one SO Feedback Frame. The data to be send is latched at the end of the command frame .

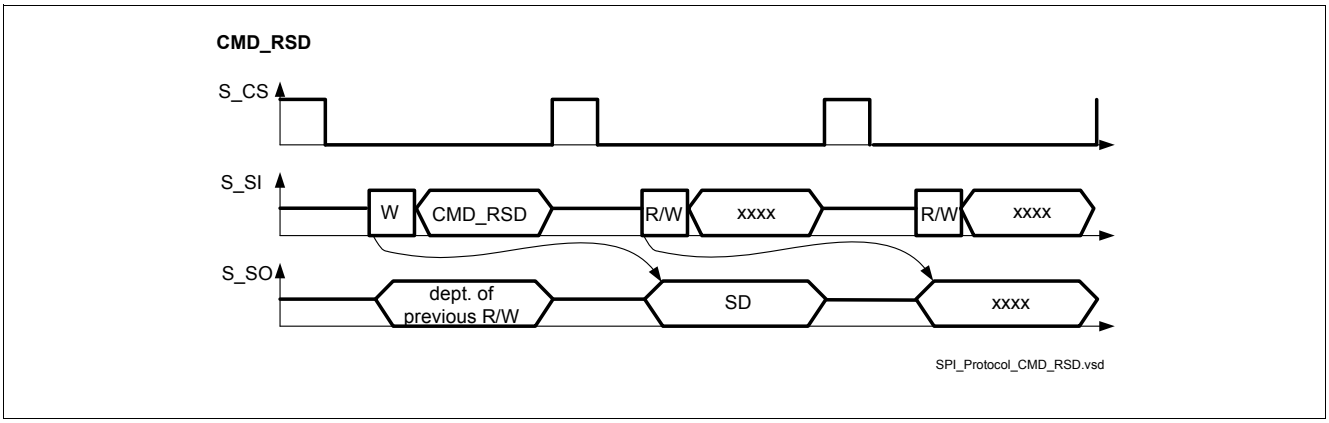


Figure 34 SPI Feedback on CMD_RSD

S_SO
SPI_Serial Output

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAR	0	0	0	0	0	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1

Field	Bits	Type	Description
-	-	-	**SD1-10 Short Diagnosis** 0 Normal Operation 1 Each SD-Bit contains the NAND-operated Diagnosis Error of each related Channel. Details can be read in diagnosis registers SD is returned after each Write Cycle to any of the writable registers.

12.3.1.2 CMD_RSDS - Command: Return Short Diagnosis and Device Status

The Command CMD_RSD offers the possibility to read out the OR-operated “short”-Diagnosis and the device Status - such as Reset-Information and Communication Error - within one SO Feedback Frame. The data to be send is latched at the end of the command frame .

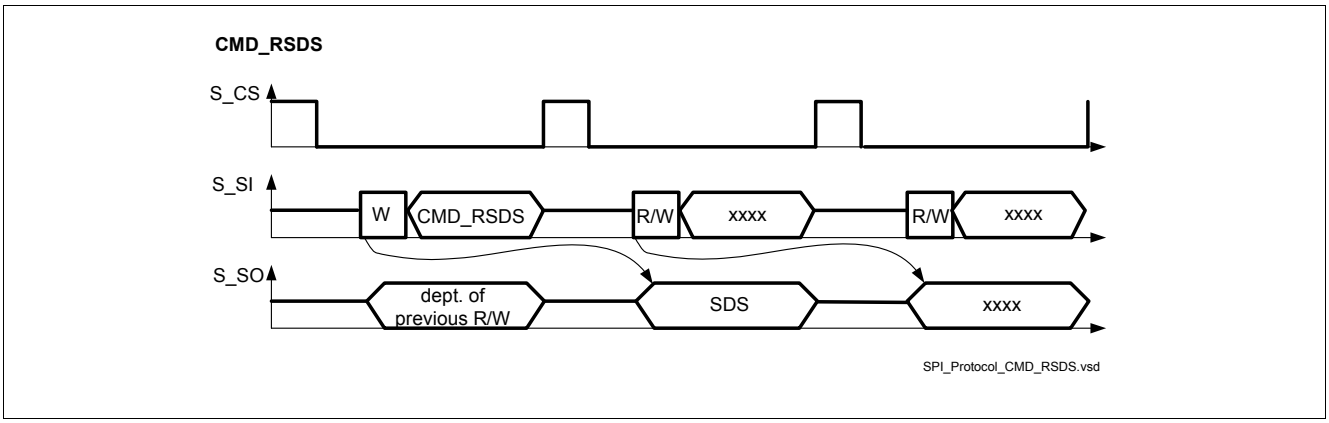


Figure 35 SPI Feedback on CMD_RSDS

S_SO
SPI_Serial Output

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAR	0	0	0	0	0	0	0	SDS8	SDS7	SDS6	SDS5	SDS4	SDS3	SDS2	SDS1

Field	Bits	Type	Description
-	7:0	-	**SDS - Short Diagnosis and Device Status**
-	0	-	**SDS1 - Diagnosis Error in Channel 1 to 6** 0 normal operation 1 diagnosis failure
-	1	-	**SDS2 - Diagnosis Error in Channel 7 to 10** 0 normal operation 1 diagnosis failure
-	2	-	**SDS3 - Under Voltage on VCC (Digital Supply Voltage)** see **Figure 36**
-	3	-	**SDS4 - Under Voltage on VDD (Analogue Supply Voltage)** see **Figure 36**
-	4	-	**SDS5 - Modulo Counter Error** 0 normal operation 1 Previous Modulo Counter Error
-	5	-	**SDS6 - Previous Communication Error - Encoded Command Ignored** 0 normal operation 1 Previous Communication Error - Encoded Command Ignored
-	6	-	**SDS7 - not used = '0'** always '0'
-	7	-	**SDS8 - not used = '0'** always '0'

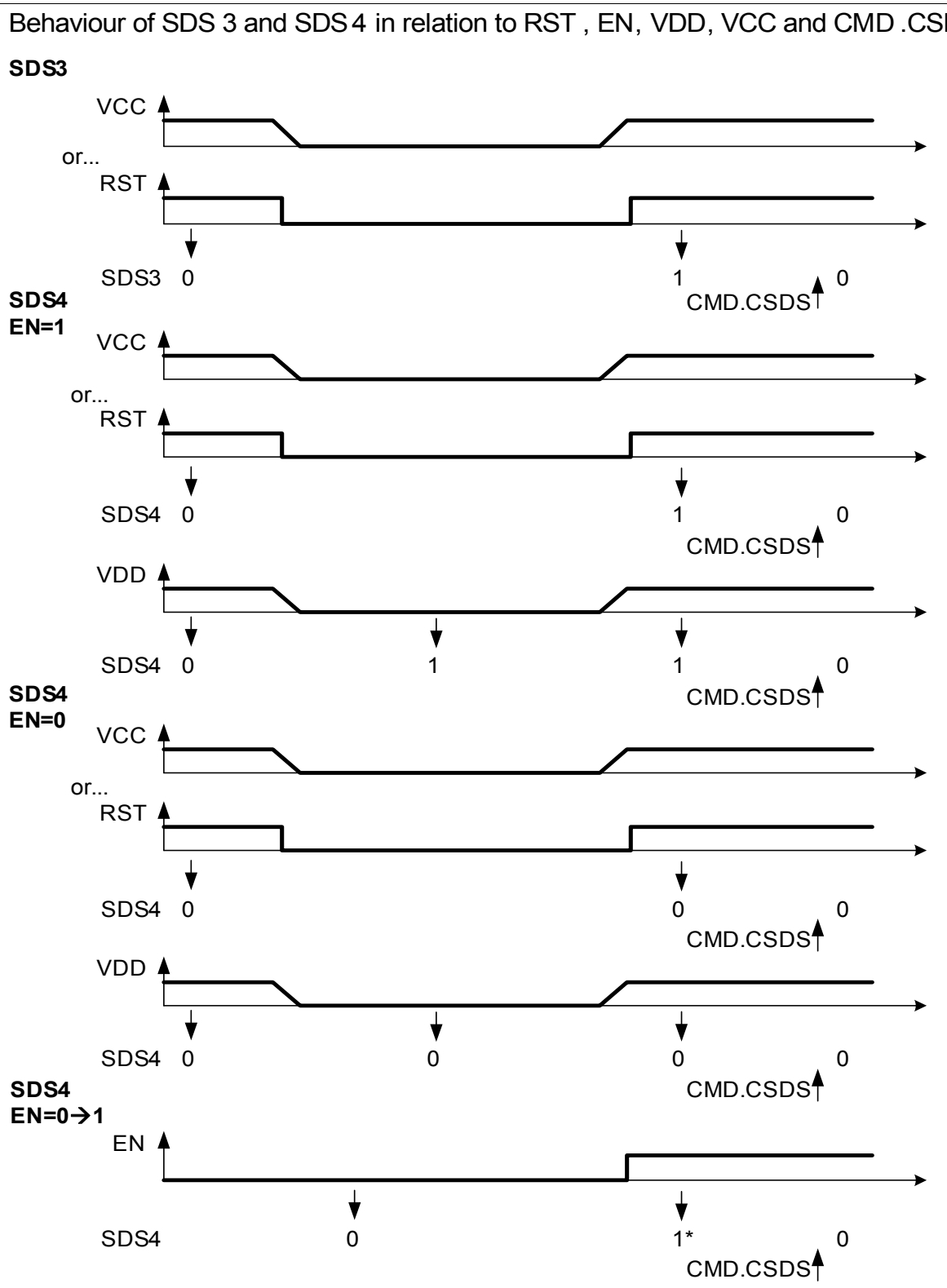


Figure 36 Behaviour of SDS3, 4

12.3.1.3 CMD_RPC - Command: Return Pattern Check

The Command CMD_RPC offers the possibility to get returned the previous Command to check if the communication works well. The data to be send is latched at the end of the command frame .

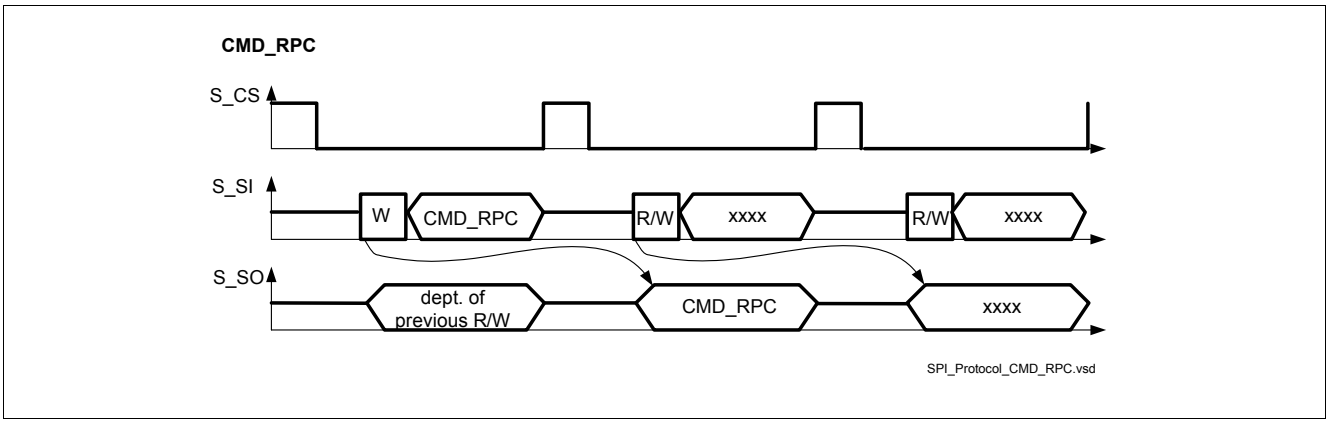


Figure 37 SPI Feedback on CMD_RPC

S_SO
SPI_Serial Output

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAR=0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	0

Field	Bits	Type	Description
-	-	-	**CMD_RPC is returned**

12.3.1.4 CMD_RINx - Command: Return Input Pin (INx) -Status

The Command CMD_RINx offers the possibility to read out the actual status of the Input Pins. This command allows to check the correct communication on the INx Pins. The data to be send is latched at the end of the command frame .

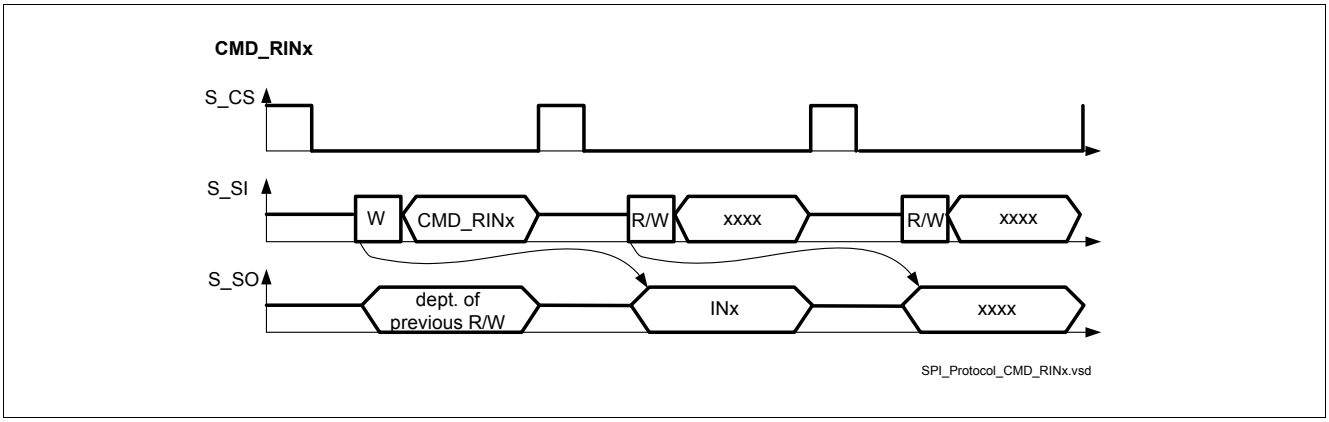


Figure 38 SPI Feedback on CMD_RINx

S_SO
SPI_Serial Output

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAR	0	0	0	0	0	IN10	IN9	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1

Field	Bits	Type	Description
-	-	-	**INx Input Pin Status** The Status of the INx Pins is read out at the moment of CS High-to-Low transition. Details see **Figure 39**. 0 INx = Low corresponding OFF 1 INx = High corresponding ON

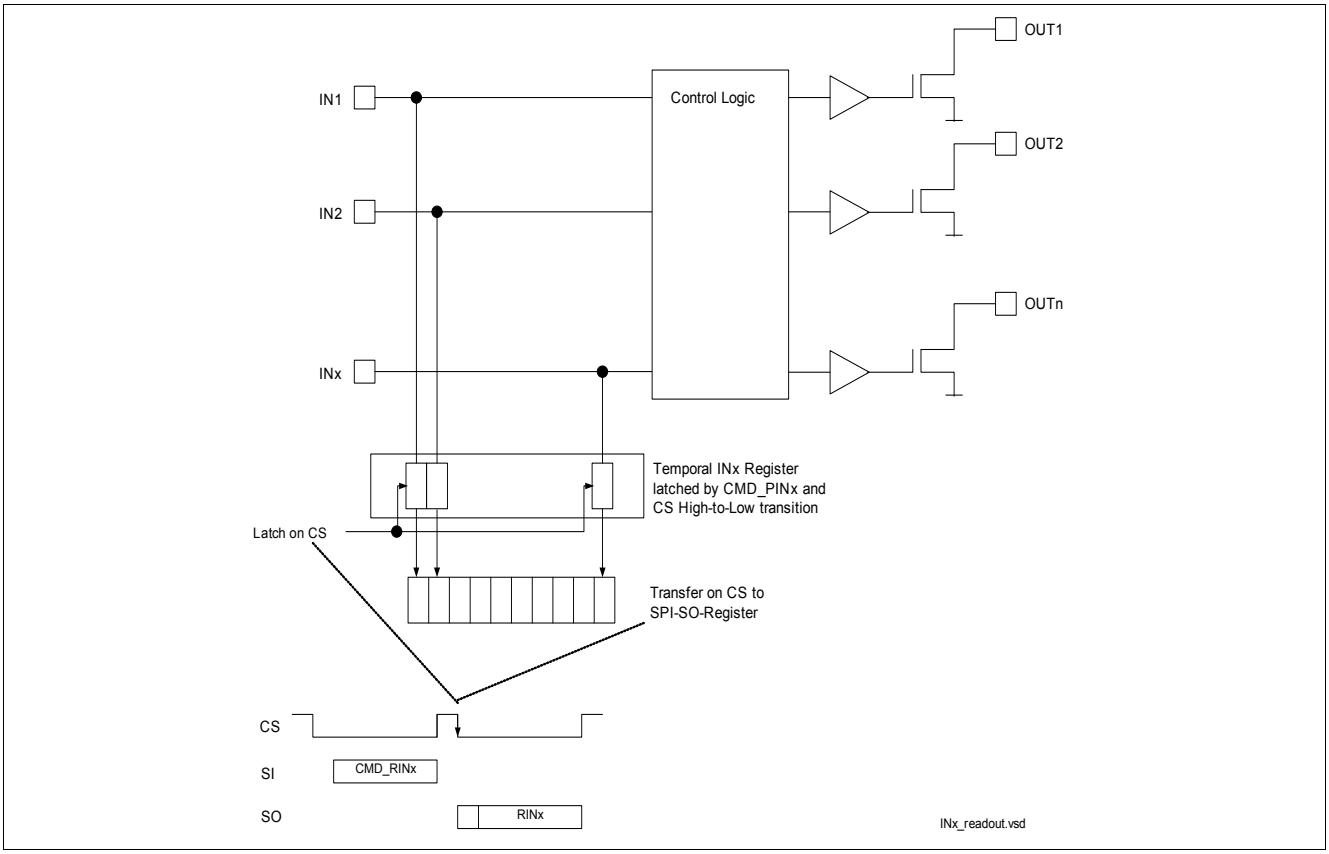


Figure 39 Read-out of INx Pins

12.3.2 DCC - Diagnosis Registers and compactCONTROL

The DCC - Diagnosis and Compact Control Set allows to read out and clear the Diagnosis Registers. Additionally this Command set offers the possibility to proceed with a compactCONTROL Mode using DMS - Diagnosis Mode Set and OPS - Output Pin Set Commands. This compactCONTROL Mode offers the possibility to Control the device with lowest work load on the micro controller side.

If any other pattern then the defined commands is received on S_SI, the command is ignored and rated as a Communication Error. In this case, this incident is reported in SDS (**Chapter 12.3.1.2**).

If an Error in the Output Channels is detected by the diagnosis circuit, the result is latched in the diagnosis registers related to each channel.

The Diagnosis Register is not deleted, when it is just read out. The Diagnosis Register byte can only be cleared by using the appropriated command. In this case, the complete Register Bank is cleared.

When issuing a Diagnosis Register Clear command (DRxCL or DMSCL), the idle time t_{Didle} needs to elapse, from the CS low-to-high transition of the clear command, before the register content is effectively cleared (**Figure 40**); this time has to be taken into account when trying to read the Diagnosis register content after a clear, see **Chapter 11.3** for t_{Didle} definition.

After an overcurrent entry is stored in the diagnosis register (OC), the idle time t_{OCidle} needs to elapse before a clear command can effectively clear the entry; if trying to clear the Diagnosis register after an OCT entry is read (**Figure 40**), this time has to be taken into account starting from the CS high-to-low transition of the previous read command, see **Chapter 11.3** for t_{OCidle} definition.

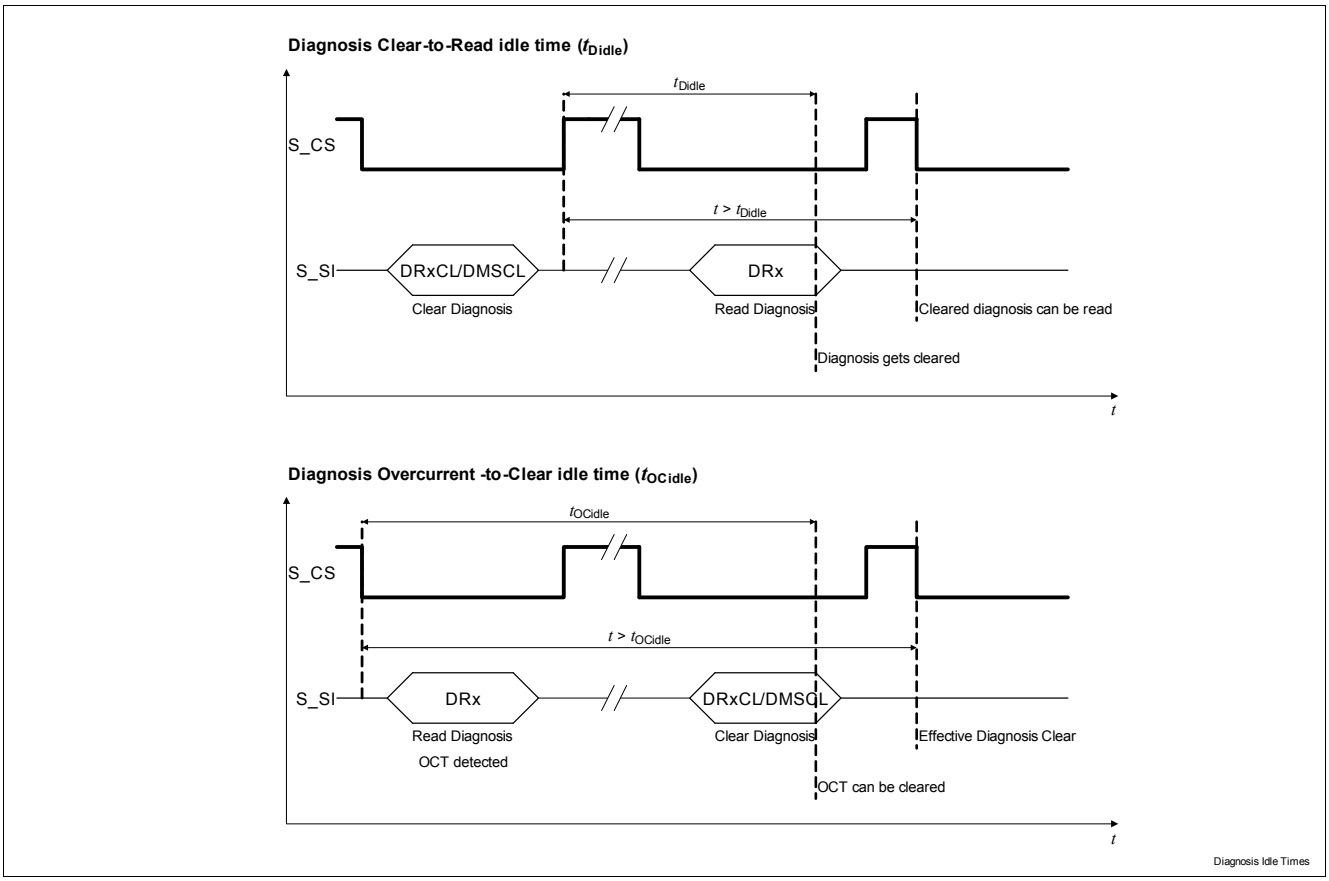


Figure 40 Diagnosis idle times

DCC **Diagnosis Registers and Compact Control**	**Reset Value: N.A.**

S_SI
SPI_Serial Input

DCC	11	10	9	8	7	6	5	4	3	2	1	0
DRA	0	1	0	1	0	0	0	0	0	0	0	0
DRB	0	1	1	0	0	0	0	0	0	0	0	0
DRACL	0	0	0	1	0	0	0	0	0	0	0	0
DRBCL	0	0	1	0	0	0	0	0	0	0	0	0
DMSCL/OPSx	1	0	0	0	OPSx							
DMS1/OPSx	1	0	1	1	OPSx							
DMS2/OPSx	1	1	0	1	OPSx							
DMS3/OPSx	1	1	1	0	OPSx							

DMSx/OPS1	1	DMSx	0	0	0	0	0	0	0	1
DMSx/OPS2	1	DMSx	0	0	0	0	0	0	1	0
DMSx/OPS3	1	DMSx	0	0	0	0	0	1	0	0
DMSx/OPS4	1	DMSx	0	0	0	0	1	0	0	0
DMSx/OPS5	1	DMSx	0	0	0	1	0	0	0	0
DMSx/OPS6	1	DMSx	0	0	1	0	0	0	0	0
DMSx/OPS7	1	DMSx	0	1	0	0	0	0	0	0
DMSx/OPS8	1	DMSx	1	0	0	0	0	0	0	0

Field	Bits	Type	Description
DCC_DRA	11:0	W	**DRA - Diagnosis Register A** (see **Chapter 12.3.2.1**) Read out Diagnosis Register A. Return the contents in the next SPI Frame. (see **Chapter 12.3.2.2**)
DCC_DRB	11:0	W	**DRB - Diagnosis Register B** (see **Chapter 12.3.2.1**) Read out Diagnosis Register B. Return the contents in the next SPI Frame. (see **Chapter 12.3.2.2**)
DCC_ DRACL	11:0	W	**DRACL - Diagnosis Register A Clear** Clear the contents of the Diagnosis Register A. Return the content present before the clear in the next SPI Frame. If the Diagnosis Error Remains, the Information remains.(see **Chapter 12.3.2.2**)
DCC_ DRBCL	11:0	W	**DRBCL - Diagnosis Register B Clear** Clear the contents of the Diagnosis Register B. Return the content present before the clear in the next SPI Frame. If the Diagnosis Error Remains, the Information remains. (see **Chapter 12.3.2.2**)
DCC_ DMSCL	11:8	W	**DMSCL/OPSx - Diagnosis Mode Set, Clear / Output Pins Set** On sending this command, the diagnosis registers DRA, DRB as well as the “virtual” Diagnosis Output Registers DO[7:0] (see **Chapter 12.3.2.3**) are cleared. Output Pin Settings are done according the content of OPSx. Returns the contents of cleared DR2 on SO in the 2nd byte of the actual communication frame and the Output Pin Feedback in the 1st Byte of the next frame. (see **Chapter 12.3.2.3**)
DCC_ DMS1	11:8	W	**DMS1/OPSx - Diagnosis Mode Set, Register1 / Output Pins Set** On sending this command, the diagnosis registers DR1 is selected. Output Pin Settings are done according the content of OPSx. Returns the contents of DR1 on SO in the 2nd byte of the actual communication frame and the Output Pin Feedback in the 1st Byte of the next frame. (see **Chapter 12.3.2.3**)
DCC_ DMS2	11:8	W	**DMS2/OPSx - Diagnosis Mode Set, Register2 / Output Pins Set** On sending this command, the diagnosis registers DR2 is selected. Output Pin Settings are done according the content of OPSx. Returns the contents of DR2 on SO in the 2nd byte of the actual communication frame and the Output Pin Feedback in the 1st Byte of the next frame. (see **Chapter 12.3.2.3**)

Field	Bits	Type	Description
DCC_ DMS3	11:8	W	**DMS3/OPSx - Diagnosis Mode Set, Register3 / Output Pins Set** On sending this command, the diagnosis registers DR3 is selected. Output Pin Settings are done according the content of OPSx. Returns the contents of DR3 on SO in the 2nd byte of the actual communication frame and the Output Pin Feedback in the 1st Byte of the next frame. (see **Chapter 12.3.2.3**)
DCC_ DMSx/OPSx	7:0	W	**DMSx/OPS1 - Diagnosis Mode Set x/ Output Pin Set Command 1** On sending this command, the diagnosis register is selected according DMSx. The Output Pins of Channel 7-10 are set according the following definitions. The OPSx are commands, no register. The commands are controlling the contents of ISA, ISB and OUTx. OPS[7:0] - Output Pin Set 0000 0001: CH7 input select, 1: parallel* / 0 : Serial 0000 0010: CH8 input select, 1: parallel* / 0 : Serial 0000 0100: CH9 input select, 1: parallel* / 0 : Serial 0000 1000: CH10 input select, 1: parallel* / 0 : Serial 0001 0000: CH7 output set, 1: ON / 0:OFF 0010 0000: CH8 output set, 1: ON / 0:OFF 0100 0000: CH9 output set, 1: ON / 0:OFF 1000 0000: CH10 output set, 1: ON / 0:OFF (*parallel controlled by INx) Sending OR operated combinations of above listed options (only OPSx) are possible in order to control more then one channel at the same time. If parallel mode Mode is selected (in “input select”), the serial settings (in “output select”) are ignored. In parallel Mode, the selected Channels are controlled via INx Pins. The default setting of ISB corresponds the command OPS[7:0] = xxxx 1111b. (parallel mode, status of the Outputs according signal on INx) Returns the contents the selected DRx register on SO in the 2nd byte of the actual communication frame and the Output Pin Feedback [OPF] in the 1st Byte of the next frame. (see **Chapter 12.3.2.3**)

12.3.2.1 DRx - Diagnosis Registers Contents

DRA[1:0]x / DRB[1:0]x **Diagnosis Register CHx Bank A and Bank B**	**Reset Value: 0000 0000 0000$_B$ = 000$_h$**

11	10	9	8	7	6	5	4	3	2	1	0
DRA[1]6	DRA[0]6	DRA[1]5	DRA[0]5	DRA[1]4	DRA[0]4	DRA[1]3	DRA[0]3	DRA[1]2	DRA[0]2	DRA[1]1	DRA[0]1

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	DRB[1]10	DRB[0]10	DRB[1]9	DRB[0]9	DRB[1]8	DRB[0]8	DRB[1]7	DRB[0]7

Field	Bits	Type	Description
DRA[1:0]x / DRB[1:0]x	1:0	R	**DRA[1:0]x / DRB[1:0]x** DRn[1]x/DRn[0]x = 11 no Error DRn[1]x/DRn[0]x = 10 Over Load, Shorted Load, Over temperature in ON-Mode DRn[1]x/DRn[0]x = 01 Open Load in OFF-Mode DRn[1]x/DRn[0]x = 00 Short to GND in OFF-Mode default DRx[1:0] = 11_B A new error on the same channel will overwrite older information. The diagnosis information which is returned by SO is latched when CS makes a High-to-Low transistion of the frame which sends out the register.

12.3.2.2 DRx - Return on DRx Commands

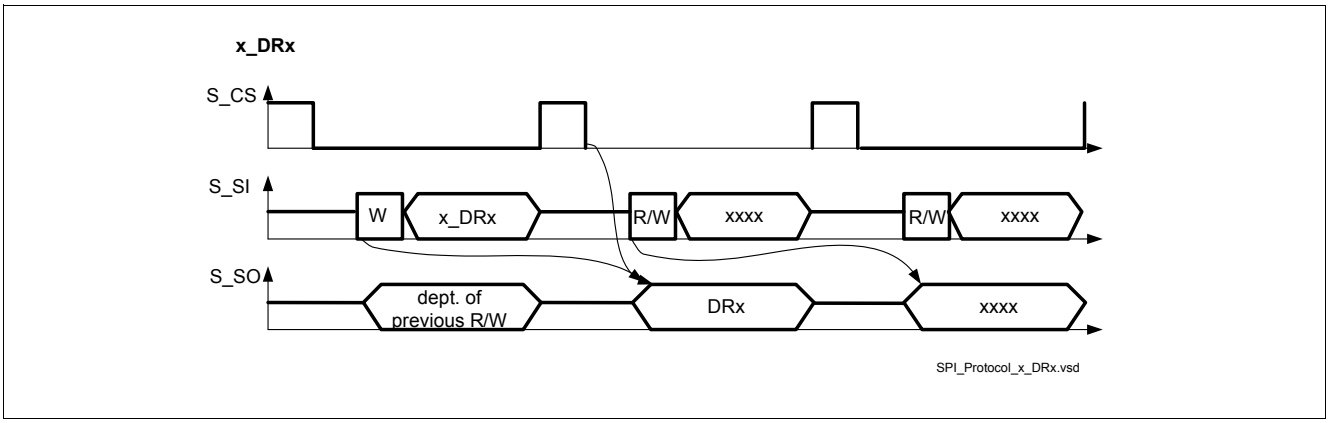


Figure 41 SPI Feedback on x_DRx commands

S_SO
SPI_Serial Output

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PAR	0	0	1	DRx [1]x	DRx [0]x	DRx [1]x	DRx [0]x	DRx [1]x	DRx [0]x	DRx [1]x	DRx [0]x	DRx [1]x	DRx [0]x	DRx [1]x	DRx [0]x

Field	Bits	Type	Description
-	-	-	**DRx Contents** 0 no Diagnosis Error 1 Diagnosis Error

12.3.2.3 DMSx/OPSx - Diagnosis Mode Set / Output Pin Set Commands

Protocol

Each Cycle where a serial data or command frame is sent to the Serial Input [SI] of the SPI interface, a data frame is returned immediately by the Serial Output [SO]. The content of the SO frame is dependent of the previous command which has been sent to SI and the content of the actual content of SI: The first Byte send by S_SI controls the content of the second byte actual returned by S_SO. The second Byte send by S_SI controls the first byte in S_SO of the next frame. (see **Figure 42**)

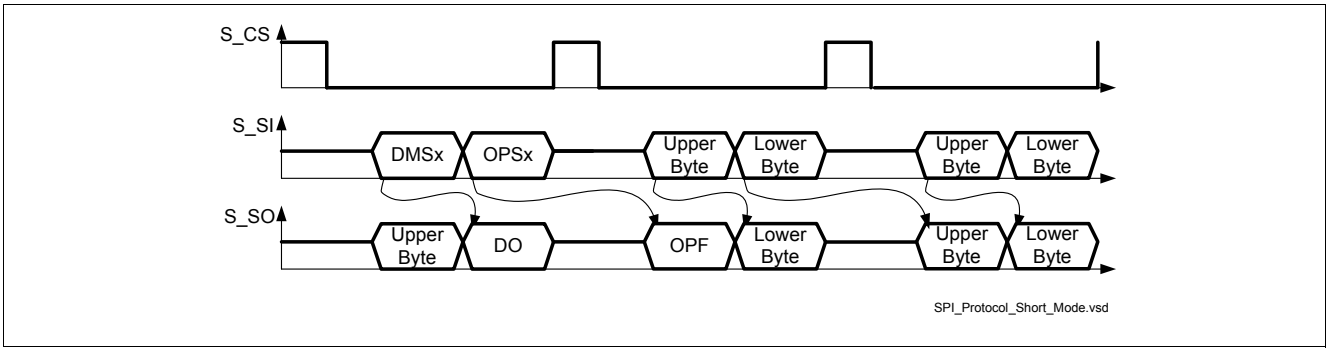


Figure 42 Data Transfer in Diagnosis and Compact Control

S_SI
SPI_Serial Input

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Diagnosis Mode Set DMS[4:0]								Output Pin Set OPS[7:0]							
-								serial mode selected				parallel or serial mode			
0	0	0	1	-	-	-	-	CH10: 1:ON 0:OFF	CH9: 1:ON 0:OFF	CH8: 1:ON 0:OFF	CH7: 1:ON 0:OFF	CH10: 0 = serial 1 = par.	CH9: 0 = serial 1 = par.	CH8: 0 = serial 1 = par.	CH7: 0 = serial 1 = par.

S_SO
SPI_Serial Output

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output Pin Set Feedback OPF[7:0]								Diagnosis Output DO[7:0]							

Diagnosis Register

Diagnosis Output Registers DO[7:0]

	7	6	5	4	3	2	1	0
Diag Register-1	DR4[1]	DR4[0]	DR3[1]	DR3[0]	DR2[1]	DR2[0]	DR1[1]	DR1[0]
Diag Register-2	DR1NA	DR3NA	1	1	DR6[1]	DR6[0]	DR5[1]	DR5[0]
Diag Register-3	DR10[1]	DR10[0]	DR9[1]	DR9[0]	DR8[1]	DR8[0]	DR7[1]	DR7[0]

Field	Bits	Type	Description
DO[7:0]	7:0	R	DO[7:0] - Diagnosis Output Contents according settings of DMS[4:0] Returned within the same frame as the pointer is send. DRx[1:0] definitions: see **Chapter 12.3.2.1**
DO[7:6] Diag Register-2	7:6	R	DO1NA: NAND-operated diagnosis of Diag Register-1 DO3NA: NAND-operated diagnosis of Diag Register-3 1: at least one diagnosis error is stored in the related Diag Register 0: no diagnosis error is stored in the related Diag Register.

Output Pin Feedback

Output Pin Feedback OPF[7:0]

15	14	13	12	11	10	9	8
OPF[7]	OPF[6]	OPF[5]	OPF[4]	OPF[3]	OPF[2]	OPF[1]	OPF[0]

Field	Bits	Type	Description
OPF[7:0]	15:8	R	OPF[7:0] - Output Pin Feedback Principally, OPF can return the previously send OPS word and the IN 10:7 -pin settings, dependent serial/parallel-setting of OPS: - If Serial Mode is selected by one or more OPS[3:0]-bits, the related OPF[7:4]-bits are returning the settings of OPS[7:4], send at the previous frame. - if parallel Mode is selected by one or more OPS[3:0]-bits, the related OPF[7:4]-bits are returning the condition available at the related IN 10:7 Pins at the moment of $\overline{S_CS}$ high-to-low transition. A mix of both modes is possible and depends on the channel related settings.

12.3.3 OUTx - Output Control Register CHx

The Output Control Register OUTx consists of 10 Bits to control the Output Channel. Each Bit switches ON/OFF the related Channel.

OUTx becomes only active when ISx[1:0] = 0x. For details refer to **Chapter 12.3.4**.

OUTx **Output Control Register**	**DATA** **Reset Value: 1100 0000 0000_B = $C00_h$**

11	10	9	8	7	6	5	4	3	2	1	0
1	1	OUT10	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3]	OUT2	OUT1

Field	Bits	Type	Description
OUTx[9:0]	9:0	R/W	**Data -** OUTx[9:0] OUTx = 0 According Channel is switched OFF OUTx = 1 According Channel is switched ON default (all channels OFF) OUT[9:0] = 00 0000 0000_B = 000_h
OUT[11:10]	11:10	R/W	**Data -** OUTx[11:10] bits are set to OUT[11:10] = 1.

12.3.4 ISx - INPUT or Serial Mode Control Register, Bank A and Bank B

The INPUT or Serial Control Register [ISx[1:0]] allows to define the way of controlling the Output Channels. There are 4 setting options possible:

- Standard Serial Control: The related Output Channel is set according the content of the OUTx Register. (**Chapter 12.3.3**)
- A further possibility is the control by the Input Pins
- The settings of the Parallel Mode Register PMx[0]. (**Chapter 12.3.5**)
- Additionally possible is the AND operation between the setting of the OUTx register and the PWM signal at the INPUT Pin.

ISAx **COMMAND**

INPUT or Serial Mode Control Register Bank A **Reset Value: 1010 1010 1010_B = AAA_h**

11	10	9	8	7	6	5	4	3	2	1	0
IS6		IS5		IS4		IS3		IS2		IS1	

ISBx **COMMAND**

INPUT or Serial Mode Control Register Bank B **Reset Value: 0000 1010 1010_B = $0AA_h$**

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	IS10		IS9		IS8		IS7	

Field	Bits	Type	Description
ISx[1:0]	11:0 ISAx 7:0 ISBx	R/W	**Command - IS[1:0]** ISx[1:0]= 0x: Serial Mode - The Channel is set ON/OFF by OUTx. 10: INPUT Mode - CHx ON/OFF according INx 11: AND operate Mode INx with OUTx -> CHx ON if OUTx & INx =1 default all Channels ISx[1:0] = 10_B

12.3.5 PMx - Parallel Mode Register CHx

The Parallel Mode Register PMx[1] allows to “inform” the device about externally parallel connected output channels. If a PMx bit is set, the “lower” related Input Channel controls the indicated Output Channels to achieve best possible matching and according to that highest efficiency of both channels. Additionally to that, the CLAMPsafe feature allows high matching during clamping.

PMx **COMMAND**

Parallel Mode Register CHx **Reset Value: 0000 0000 0000_B = 000_h**

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PM910	PM89	PM78	PM56	0	PM34	PM23	PM12

Field	Bits	Type	Description
PMx	11:8	R/W	0
PMx	7:0	R/W	**PMx - Parallel Mode Bit** 0 Direct Mode 1 Parallel Mode of Channel 1 with x+1 default PMx[0] = 0 Controlling Parallel Mode is possible between Channel 1 to 4, 5 to 6, 7 to 10. In between the groups, no parallel mode is supported but possible. In case Parallel Mode is chosen and a diagnosis error at only one of the channels is detected, the according diagnosis bit is set. This information mismatch can be caused by tolerance related in-balance of the channels connected together in parallel mode. The diagnosis bits should be or-operated by the Micro Controller side.

12.3.6 DEVS - Device Settings

This Register allows additional Device settings. For details refer also to the Chapter “Electrical Characteristics”.

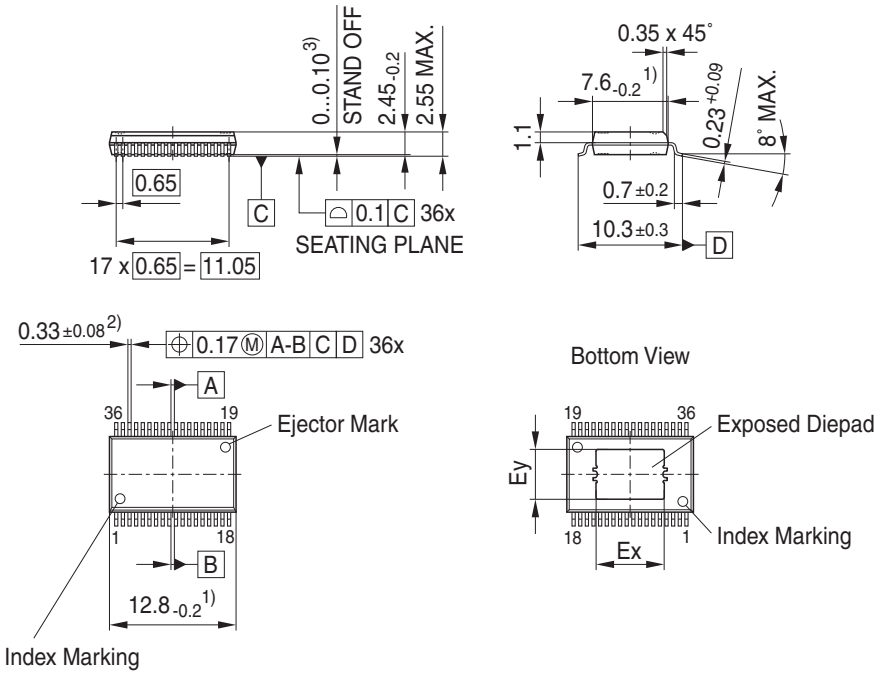
The Diagnosis Current Control register allow to select between different Diagnosis Modes. The Diagnosis Currents can be switched off to avoid glowing of any connected LEDs.

DEVS **Device Settings**	**COMMAND** **Reset Value: 0000 0000 0111_B = 007_h**

11	10	9	8	7	6	5	4	3	2	1	0
RCP	DBT2	DBT1	0	0	0	0	0	0	DCC10	DCC9	DCC18

Field	Bits	Type	Description
RCP	11	R/W	RCP - Reverse Current Protection 1: reverse current comp is enabled (valid for all Channels) 0: disabled **default: RCP = 0**
DBT2 DBT1	10 9	R/W	**DBT2,1 - Diagnosis Blind Time Channel 7 to 10** 0,0 standard Filter Time of typ. 150µs 1,0 standard Filter Time of typ. 150µs 0,1 OFF-state diagnosis Blind Time of typ. 2.5ms 1,1 OFF-state diagnosis Blind Time of typ. 5ms
DEVS[7:5]	7:5	R/W	Reserved, must be set to 0 default: 0
DEVS[4:3]	4:3	R/W	not used. set to ’0’
DCCx	2:0	R/W	**DCCx - Diagnosis Current Control** DCC18 switching ON/OFF diagnosis current of CH1-8 DCC9 switching ON/OFF diagnosis current of CH9 DCC10 switching ON/OFF diagnosis current of CH10 0 OFF-State Diagnosis (Detection of open load and short to GND) of CHx is switched OFF. ON state diagnosis (over current and over temperature detection) is still active. Diagnosis Current is switched OFF. 1 OFF-State (Detection of open load and short to GND) and ON-State (over current and over temperature detection) Diagnosis of CHx switched ON, Diagnosis Current is switched ON default DCC = 1

13 Package Outlines



Exposed Diepad Dimensions 4)			
Package	Leadframe	Ex	Ey
PG-DSO-36	A6901-C001	7	5.1

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side
3) Distance from leads bottom (= seating plane) to exposed diepad
4) Excluding the mold flash allowance of 0.3 max per side

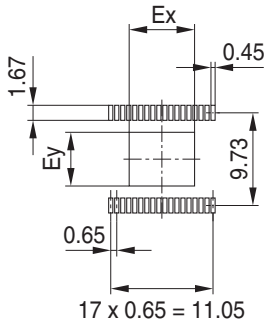


Figure 43 PG-DSO-36 Exposed Pad

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

14 Revision History

TLE8110EE

Revision History:	**2013-07-02**	Rev. 1.4
Rev. 1.4	Document Release	
	Added pin names to Pin Configuration picture, **Figure 3**	
	Improved definition of **Item 6.2.5**	
	Improved definition of **Item 6.2.11**	
Rev. 1.3.1	2011-05-26: Data Sheet Release	
	New detailed description of device diagnosis in **Chapter 8**, polling procedure provided	
	Load Clamping Energy measurement setup description added at **Chapter 7.2**	
	Removed LOTC-bit configuration/functionality, Parameters 10.1.9 and 10.2.12 with related footnote 2), both removed Figure. 20: Timing (CLn Over Current Latch...), removed **Chapter 12.3.2**, description reworked	
	Added **Figure 22** for Over-Current protection explanation	
	Added **Item 11.3.21**, **Item 11.3.22** for diagnosis clear/read delays	
	Chapter 12.3.2, added description of Diagnosis Clear/Read delays	
	Chapter 12.2.3.4 added to describe daisy-chain operation	
	TOR-bit Functionality Removed	
	Package name generalized to PG-DSO-36	
Rev. 1.3	2011-05-02: Added Reverse Current Comparator Functionality	
Rev. 1.2	2011-02-02: Removed Reverse Current Comparator Functionality	
Rev. 1.11	2011-02-02: footnote added for EAR specs	
	added footnotes [2) 3) 4) 5)] in **Chapter 7.3**	
Rev. 1.1	2011-01-10: EAS/EAR Spec Update for Single and Parallel Connection	
	Parallel Connection factors removed, parallel EAR spec cleaned/updated, **Chapter 7.4**	
	EAR Cumulative Scenario removed, **Chapter 7.2**	
	EAR ratings cleaned/updated, **Chapter 7.3**	
	EAS ratings cleaned/updated, **Chapter 4.1**	
Rev. 1.01	2010-12-01: Minor changes	
	Clamping Energy Formula reorganized in **Chapter 7.2**, Equation for RL=0 removed	
Rev. 1.0	2009-06-15: Data Sheet Release	

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