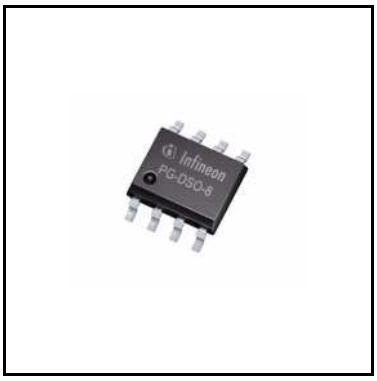
TLE8250GVIO

High Speed CAN-Transceiver



1 Overview

Quality Requirement Category: Automotive

Features

- Fully compatible to ISO 11898-2
- Wide common mode range for electromagnetic immunity (EMI)
- Very low electromagnetic emission (EME)
- Excellent ESD robustness
- Extended supply range at V_{CC} and V_{IO}
- Suitable for 5V and 3.3V microcontroller I/O voltages
- CAN Short-Circuit proof to ground, battery and V_{CC}
- TxD time-out function
- Low CAN bus leakage current in Power Down mode
- Over temperature protection
- Protected against automotive transients
- CAN data transmission rate up to 1 MBit/s
- V_{IO} input for voltage adaption to the micro controller supply
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Engine Control Unit (ECUs)
- Transmission Control Units (TCUs)
- Chassis Control Modules
- Electric Power Steering

Description

The TLE8250GVIO is a transceiver designed for CAN networks in automotive and industrial applications. As an interface between the physical bus layer and the CAN protocol controller, the TLE8250GVIO drives the signals to the bus and protects the microcontroller against disturbances coming from the network. Based on the high symmetry of the CANH and CANL signals, the TLE8250GVIO provides a very low level of electromagnetic emission (EME) within a broad frequency range. The TLE8250GVIO is integrated in a RoHS complaint PG-DSO-8 package and fulfills or exceeds the requirements of the ISO11898-2.

Overview

As a successor to the first generation of HS CAN transceivers, the TLE8250GVIO is fully pin and function compatible to his predecessor model, the TLE6250GV33. The TLE8250GVIO is optimized to provide an excellent passive behavior in Power Down mode. This feature makes the TLE8250GVIO extremely suitable for mixed supply CAN networks.

Based on the Infineon Smart Power Technology SPT, the TLE8250GVIO provides industry leading ESD robustness together with a very high electromagnetic immunity (EMI). The Infineon Smart Power Technology SPT allows bipolar and CMOS control circuitry in accordance with DMOS power devices to exist on the same monolithic circuit. The TLE8250GVIO and the Infineon SPT technology are AEC qualified and tailored to withstand the harsh conditions of the Automotive Environment.

Two different operation modes, additional Fail Safe features like a TxD time-out and the optimized output slew rates on the CANH and CANL signals are making the TLE8250GVIO the ideal choice for large CAN networks with high data rates.

Type	Package	Marking
TLE8250GVIO	PG-DSO-8	8250GVIO

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2 Block Diagram

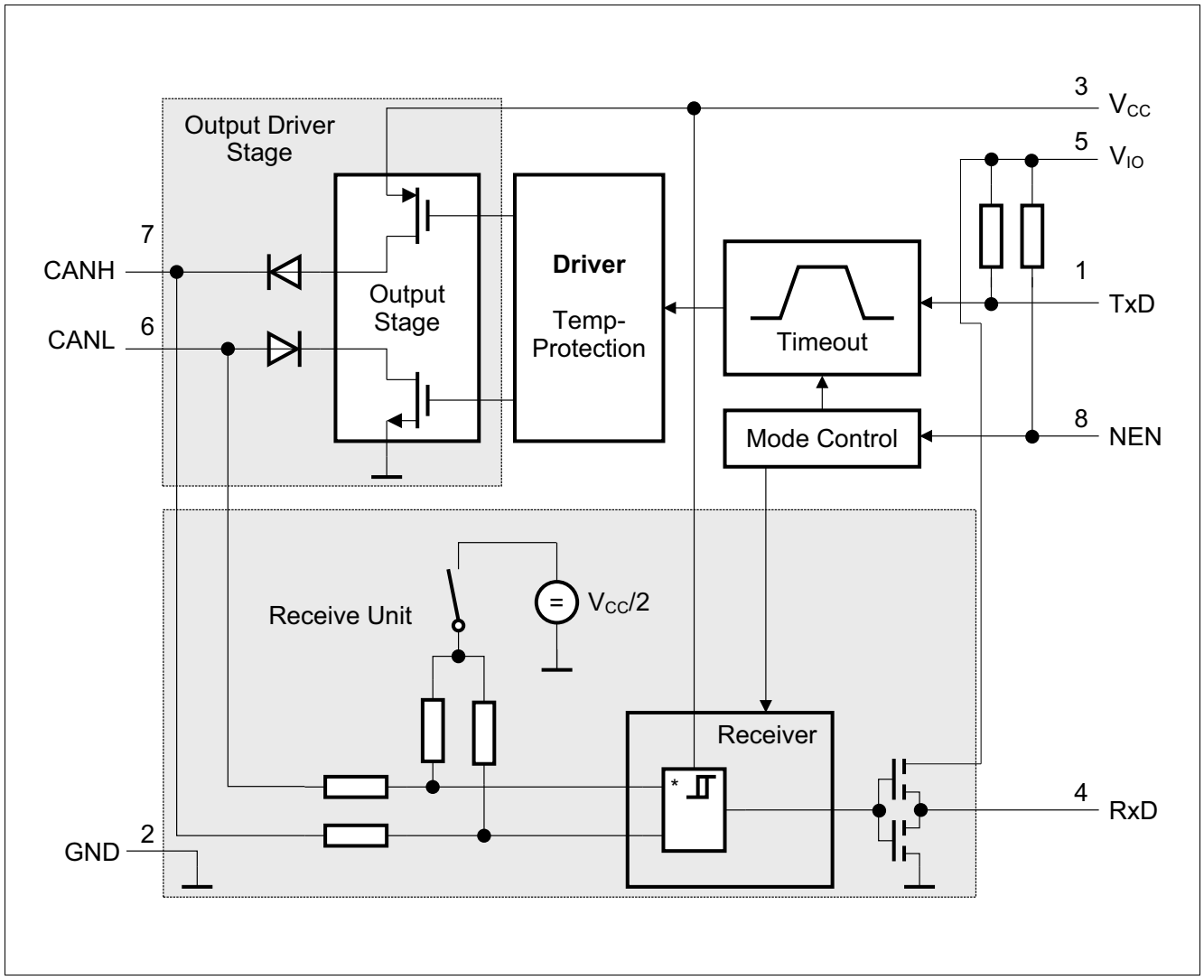


Figure 1 Block Diagram

Note: In comparison to the TLE6250GV33 the pin 8 (INH) was renamed to the term NEN, the function remains unchanged. NEN stands for Not ENable.

3 Pin Configuration

3.1 Pin Assignment

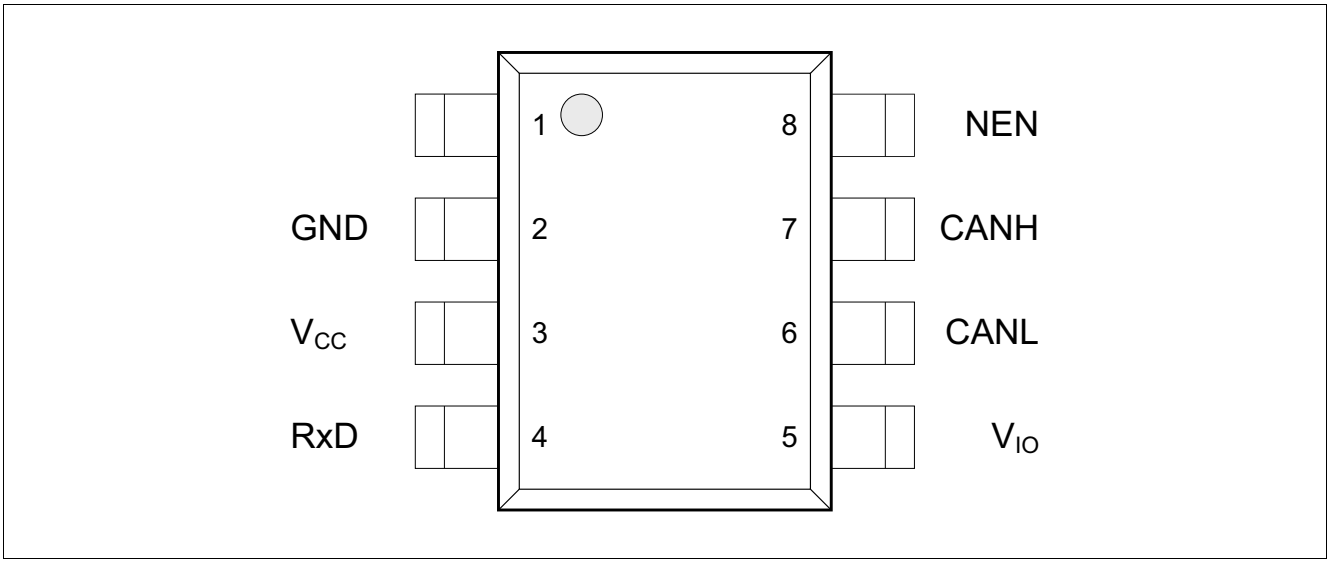


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Table 1 Pin Definition and Functions

Pin	Symbol	Function
1	TxD	**Transmit Data Input;** internal pull-up to V_{IO}, “Low” for “Dominant” state.
2	GND	**Ground**
3	V_{CC}	**Transceiver Supply Voltage;** 100 nF decoupling capacitor to GND required.
4	RxD	**Receive Data Output;** “Low” in “Dominant” state.
5	V_{IO}	**Digital Supply Voltage Input;** Supply voltage input to adapt the logical input and output voltage levels of the transceiver to the microcontroller supply. 100 nF decoupling capacitor to GND required.
6	CANL	**CAN Bus Low level I/O;** “Low “ in “Dominant” state.
7	CANH	**CAN Bus High level I/O;** “High” Sin “Dominant” state.
8	NEN	**Not ENable Input**[1]**;** internal pull-up to V_{IO}, “Low” for Normal Operation mode.

1) The naming of pin 8 is different between the TLE8250GVIO and its forerunner model the TLE6250GV33. The function of pin 8 remains the same.

4 Functional Description

CAN is a serial bus system that connects microcontrollers, sensor and actuators for real-time control applications. The usage of the Control Area Network (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7 layer OSI reference model the physical layer of a CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes inside the network. The physical layer specification of a CAN bus system includes all electrical and mechanical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed over the last years. The TLE8250GVIO is a High Speed CAN transceiver without any dedicated Wake-Up function. High Speed CAN Transceivers without Wake-Up function are defined by the international standard ISO 11898-2.

4.1 High Speed CAN Physical Layer

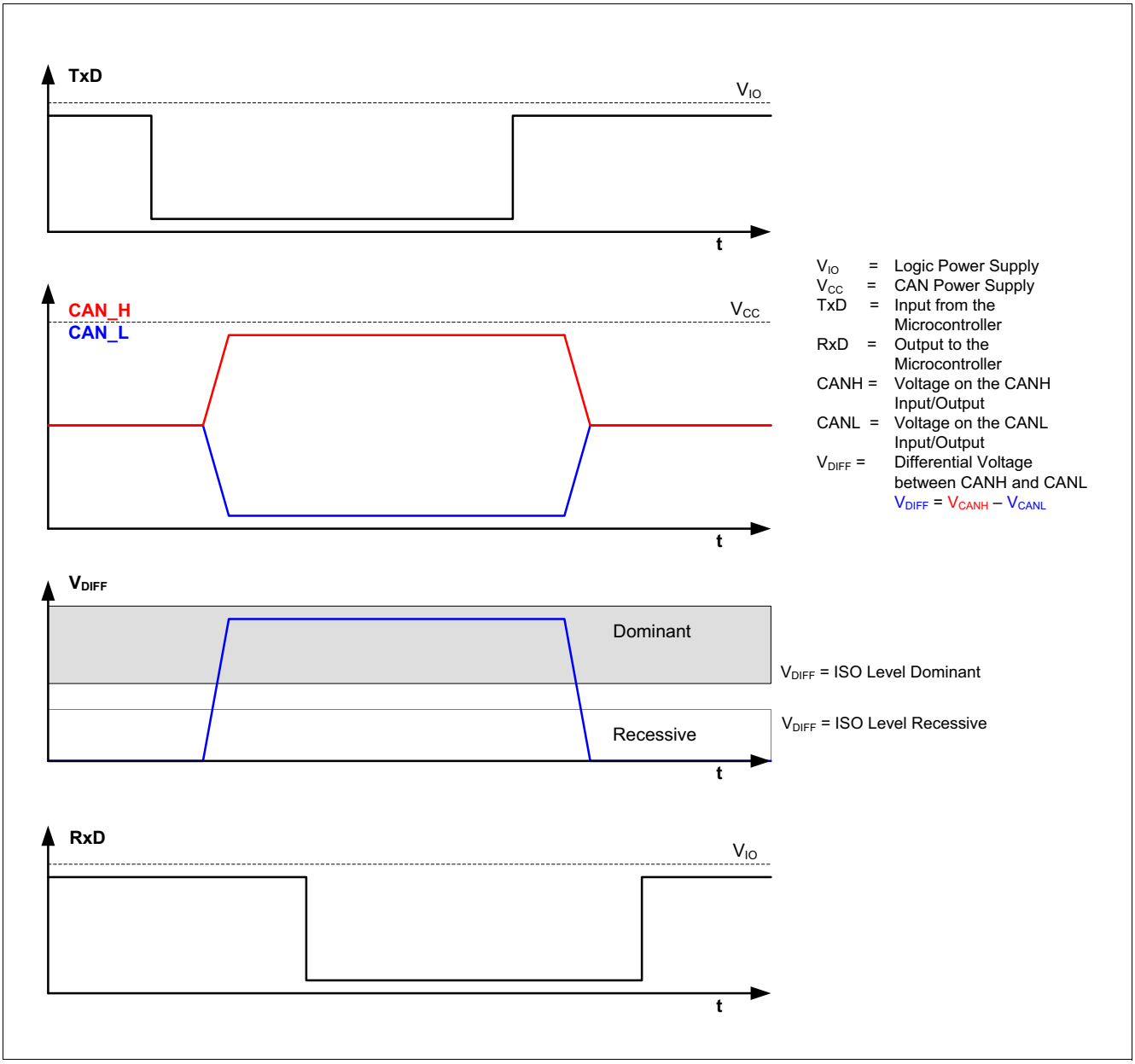


Figure 3 High Speed CAN Bus Signals and Logic Signals

The TLE8250GVIO is a High Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN network is a two wire, differential network which allows data transmission rates up to 1 MBit/s. Characteristic for a HS CAN network are the two signal states on the CAN bus: “Dominant” and “Recessive” (see **Figure 3**).

The pins CANH and CANL are the interface to the CAN bus and both pins operate as a input and as an output. The pins RxD and TxD are the interface to the microcontroller. The pin TxD is the serial data input from the CAN controller, the pin RxD is the serial data output to the CAN controller. As shown in **Figure 1**, the HS CAN transceiver TLE8250GVIO has a receive and a transmit unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time. The HS CAN transceiver TLE8250GVIO converts the serial data stream available on the transmit data input TxD, into a differential output signal on CAN bus, provided by the pins CANH and CANL. The receiver stage of the TLE8250GVIO monitors the data on the CAN bus and converts them to a serial, single ended signal on the RxD output pin. A logical “Low” signal on the TxD pin creates a “Dominant” signal on the CAN bus, followed by a logical “Low” signal on the RxD pin (see **Figure 3**). The feature, broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneous is essential to support the bit to bit arbitration inside CAN networks.

The voltage levels for HS CAN transceivers are defined by the ISO 11898-2 and the ISO 11898-5 standards. If a data bit is “Dominant” or “Recessive” depends on the voltage difference between pins CANH and CANL: $V_{DIFF} = V_{CANH} - V_{CANL}$.

In comparison to other differential network protocols the differential signal on a CAN network can only be larger or equal to 0 V. To transmit a “Dominant” signal to the CAN bus the differential signal V_{DIFF} is larger or equal to 1.5 V. To receive a “Recessive” signal from the CAN bus the differential V_{DIFF} is smaller or equal to 0.5 V.

Partially supplied CAN networks are networks where the CAN bus participants have different power supply conditions. Some nodes are connected to the power supply, some other nodes are disconnected from the power supply. Regardless, if the CAN bus participant is supplied or not supplied, each participant connected to the common bus media must not disturb the communication. The TLE8250GVIO is designed to support partially supplied networks. In Power Down mode, the receiver input resistors are switched off and the transceiver input is high resistive.

The voltage level on the digital input TxD and the digital output RxD is determined by the power supply level at the pin V_{IO}. Depending on voltage level at the V_{IO} pin, the signal levels on the logic pins (NEN, TxD and RxD) are compatible to microcontrollers with 5 V or 3.3 V I/O supply. Usually the V_{IO} power supply of the transceiver is connected to same power supply as I/O power supply of the microcontroller.

4.2 Operation Modes

Two different operation modes are available on TLE8250GVIO. Each mode with specific characteristics in terms of quiescent current or data transmission. For the mode selection the digital input pin NEN is used. **Figure 4** illustrates the different mode changes depending on the status of the NEN pin. After suppling V_{CC} and V_{IO} to the HS CAN transceiver, the TLE8250GVIO starts in Stand-By mode. The internal pull-up resistor is setting the TLE8250GVIO to Stand-By per default. If the microcontroller is up and running the TLE8250GVIO can change to operation mode within the time for mode change t_{Mode}.

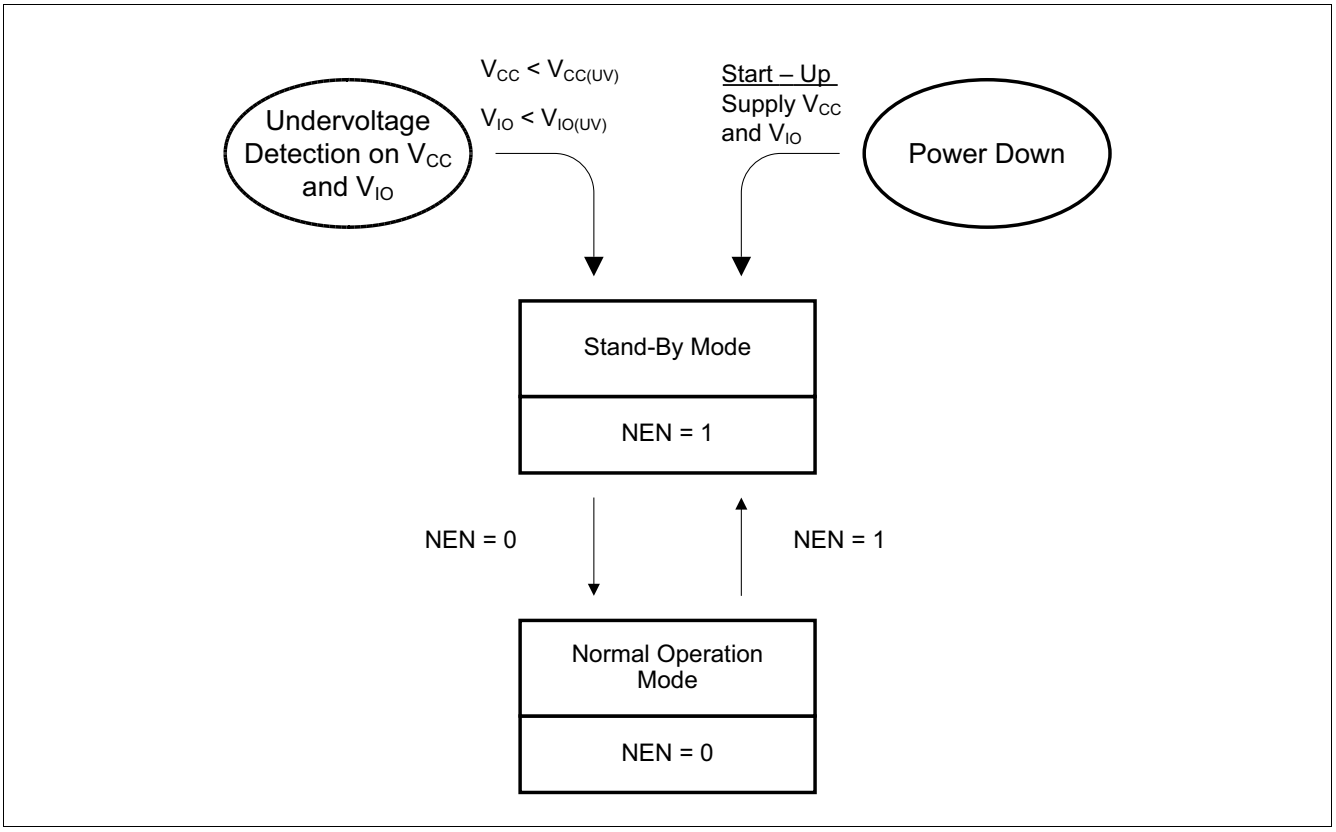


Figure 4 Operation Modes

The TLE8250GVIO has 2 major operation modes:

- Stand-By mode
- Normal Operation mode

Table 2 Operating modes

Mode	NEN	Bus Bias	Comments
Normal Operation	“Low”	$V_{CC}/2$	Output driver stage is active. Receiver unit is active.
Stand-By	“High”	Floating	Output driver stage is disabled. Receiver unit is disabled.
V_{CC} off	“Low” or “High”	Floating	Output driver stage is disabled. Receiver unit is disabled.

4.3 Normal Operation Mode

In Normal Operation mode the HS CAN transceiver TLE8250GVIO sends the serial data stream on the TxD pin to the CAN bus while at the same time the data available on the CAN bus are monitored to the RxD pin. In Normal Operation mode all functions of the TLE8250GVIO are active:

- The output driver stage is active and drives data from the TxD to the CAN bus.
- The receiver unit is active and provides the data from the CAN bus to the RxD pin.
- The bus basing is set to $V_{CC}/2$.
- The under-voltage monitoring on the power supply V_{CC} and on the power supply V_{IO} is active.

To enter the Normal Operation mode set the pin NEN to logical “Low” (see Table 2 or Figure 4). The NEN pin has an internal pull-up resistors to the power-supply V_{IO}.

4.4 Stand-By Mode

Stand-By mode is an idle mode of the TLE8250GVIO with optimized power consumption. In Stand-By mode the TLE8250GVIO can not send or receive any data. The output driver stage and the normal receiver unit are disabled. Both CAN bus pins, CANH and CANL are floating.

- The output driver stage is disabled.
- The receiver unit is disabled.
- The bus basing is floating.
- The under-voltage monitoring on the power supply V_{CC} and on the power supply V_{IO} is active.

To enter the Stand-By mode set the pin NEN to logical “High” (see Table 2 or Figure 4). The NEN pin has an internal pull-up resistor to the power-supply V_{IO}. In case the Stand-By mode will not be used in the application, the NEN pin needs to get connected to GND.

4.5 Power Down

Power Down mode means the TLE8250GVIO is not supplied. In Power Down the differential input resistors of the receiver stage are switched off. The CANH and CANL bus interface of the TLE8250GVIO acts as an high impedance input with a very small leakage current. The high ohmic input doesn’t influence the “Recessive” level of the CAN network and allows an optimized EME performance of the whole CAN network.

5 Fail Safe Functions

5.1 Short circuit protection

The CANH and CANL bus outputs are short-circuit-proof, either against GND or a positive supply voltage. A current limiting circuit protects the transceiver against damages. If the device is heating up due to a continuos short on CANH or CANL, the internal over-temperature protection switches off the bus transmitter.

5.2 Open Logic Pins

All logic input pins have internal pull-up resistor to V_{IO}. In case the V_{IO} supply is activated and the logical pins are open or floating, the TLE8250GVIO enters into the Stand-By mode per default. In Stand-By mode the output driver stage of the TLE8250GVIO is disabled, the bus biasing is shut off and the HS CAN TLE8250GVIO transceiver will not influence the data on the CAN bus.

5.3 TxD Time-Out function

The TxD Time-out feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously “Low”. A continuous “Low” signal on the TxD pin can have it’s root cause in a locked-up microcontroller or a short on the printed circuit board for example. In Normal Operation mode, a logical “Low” signal on the TxD pin for the time $t > t_{TxD}$ enables the TxD Time-out feature and the TLE8250GVIO disables the output driver stage (see Figure 5). The receive unit is still active and the data on the bus are still monitored by the RxD output pin.

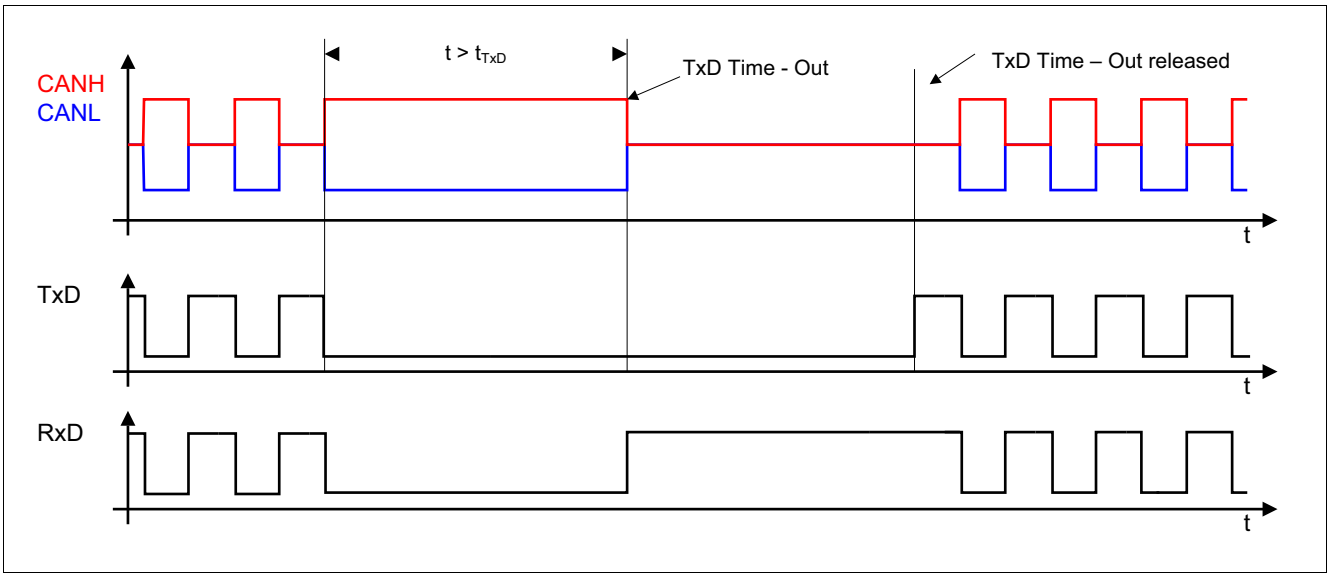
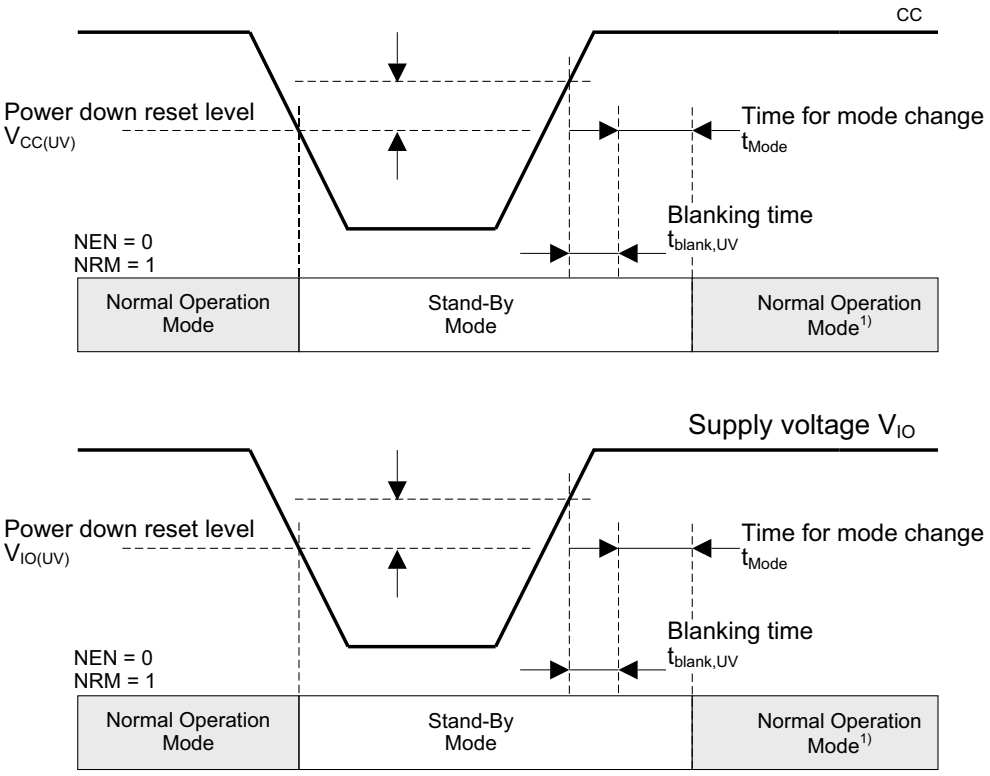


Figure 5 TxD Time-Out function

Figure 5 shows the way how the transmission stage is deactivated and activated again. A permanent “Low” signal on the TxD input pin activates the TxD time-out function and deactivates the transmitter output stage. To release the transmitter output stage after a TxD time-out event the TLE8250GVIO requires a signal change on the TxD input pin from logical “Low” to logical “High”.

5.4 Under-Voltage detection

The HS CAN Transceiver TLE8250GVIO is equipped with an under-voltage detection on the power supply V_{CC} and the power supply V_{IO}. In case of an under-voltage event on V_{CC} or V_{IO}, the under-voltage detection changes the operation mode of TLE8250GVIO to the Stand-By mode, regardless to the logical signal on the NEN pin (see Figure 6).If the transceiver TLE8250GVIO recovers from the under-voltage event, the operation mode returns to the programmed mode by the NEN pin.



1) Assuming the logical signal on the pin NEN keeps its values during the under-voltage event. In this case NEN remains „Low“.

Figure 6 Under-Voltage detection on V_{CC} and V_{IO}

5.5 Over-Temperature protection

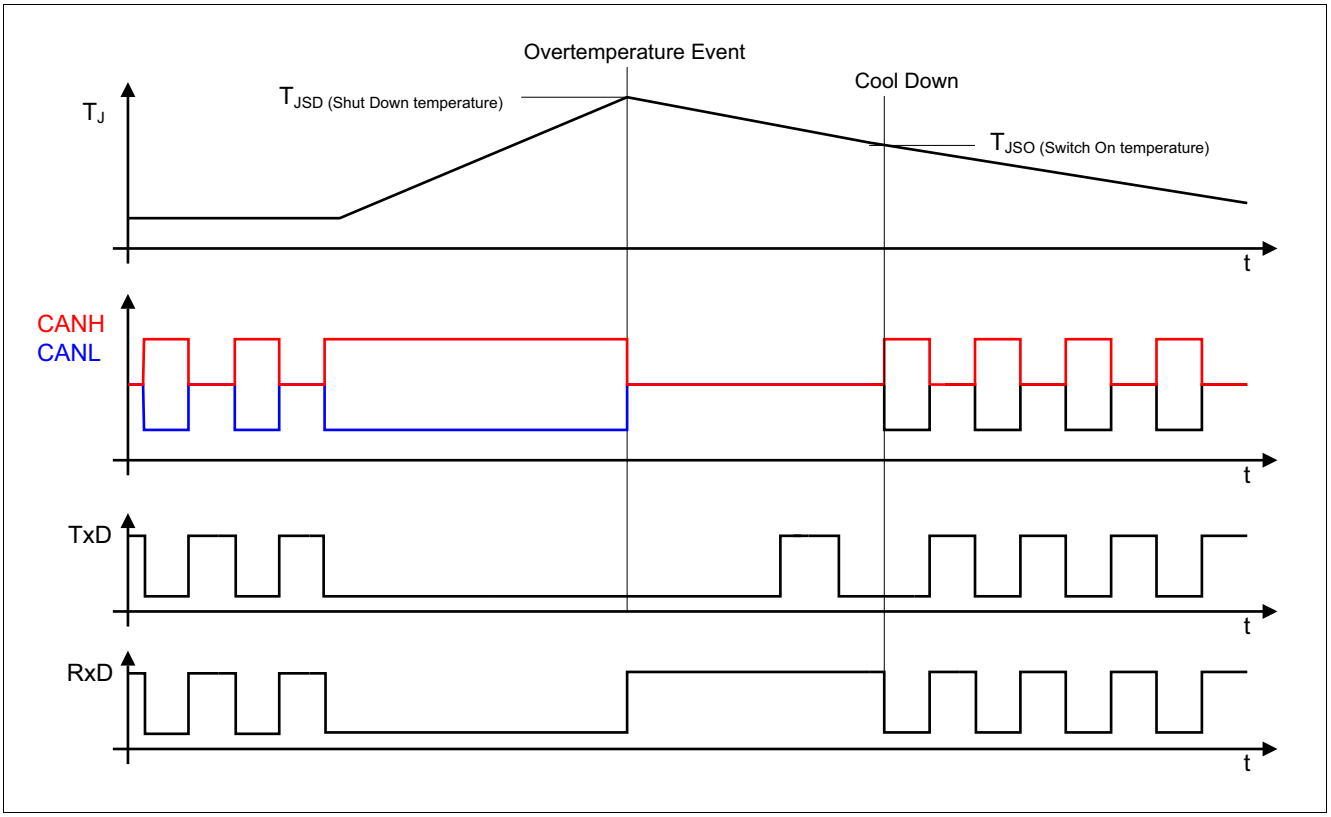


Figure 7 Over-Temperature protection

The TLE8250GVIO has an integrated over-temperature detection to protect the device against thermal overstress of the output driver stage. In case of an over-temperature event, the temperature sensor will disable the output driver stage (see **Figure 1**). After the device cools down the output driver stage is activated again (see **Figure 7**). Inside the temperature sensor a hysteresis is implemented.

6 General Product Characteristics

6.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings Voltages, Currents and Temperatures[1)]

All voltages with respect to ground; positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transceiver Supply Voltage	V_{CC}	-0.3	–	6.0	V	–	P_6.1.1
Logic Supply Voltage	V_{IO}	-0.3	–	6.0	V	–	P_6.1.2
CANH DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_6.1.3
CANL DC voltage versus GND	V_{CANL}	-40	–	40	V	–	P_6.1.4
Differential voltage between CANH and CANL	$V_{CAN\ diff}$	-40	–	40	V	–	P_6.1.5
Logic voltages at NEN, TxD, RxD	V_I	-0.3	–	6.0	V	–	P_6.1.6
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_6.1.7
Storage temperature	T_S	- 55	–	150	°C	–	P_6.1.8
ESD Resistivity							
ESD Resistivity at CANH, CANL versus GND	V_{ESD}	-8	–	8 –	kV	Human Body Model (100pF via 1.5 kΩ)[2)]	P_6.1.9
ESD Resistivity all other pins	V_{ESD}	-2	–	2 –	kV	Human Body Model (100pF via 1.5 kΩ)[2)]	P_6.1.10

1) Not subject to production test, specified by design

2) ESD susceptibility HBM according to EIA / JESD 22-A 114

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

6.2 Functional Range

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Transceiver Supply Voltage	V_{CC}	4.5	–	5.5	V	–	P_6.2.1
Logical Supply Voltage	V_{IO}	3.0	–	5.5	V	–	P_6.2.2
Thermal Parameters							
Junction temperature	T_j	-40	–	150	°C	[1)]	P_6.2.3

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

6.3 Thermal Characteristics

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 5 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance							
Junction to Ambient[1)]	R_{thJA}	–	130	–	K/W	[2)]	P_6.3.1
Thermal Shutdown Junction Temperature							
Thermal shutdown temp.	T_{JSD}	150	175	200	°C	–	P_6.3.2
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	P_6.3.3

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (TLE8250GVIO) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

7 Electrical Characteristics

7.1 Functional Device Characteristics

Table 6 Electrical Characteristics

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_J < +150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption on V_{CC}	I_{CC}	–	6	10	mA	"Recessive" state; $V_{TxD} = V_{IO}$	P_7.1.1
Current consumption on V_{CC}	I_{CC}	–	45	70	mA	"Dominant" state; V_{TxD} = 0 V	P_7.1.2
Current consumption	$I_{CC(STB)}$	–	7	15	µA	Stand-By mode; TxD = V_{IO}, NEN = "Low"	P_7.1.3
Current consumption	I_{IO}	–	–	1	mA	Normal Operation mode NEN = "Low"	P_7.1.4
Supply Resets							
V_{CC} under-voltage monitor	$V_{CC(UV)}$	1.3	3.2	4.3	V	–	P_7.1.5
V_{CC} under-voltage monitor hysteresis	$V_{CC(UV,H)}$	–	200	–	mV	1)	P_7.1.6
V_{IO} under-voltage monitor	$V_{IO(UV)}$	1.3	2.4	2.8	V	–	P_7.1.7
V_{IO} under-voltage monitor hysteresis	$V_{IO(UV,H)}$	–	200	–	mV	1)	P_7.1.8
V_{CC} and V_{IO} under-voltage blanking time	$t_{blank(UV)}$	–	15	–	µs	1)	P_7.1.9
Receiver Output: RxD							
HIGH level output current	$I_{RD,H}$	–	-4	-2	mA	V_{RxD} = 0.8 × V_{IO} V_{DIFF} < 0.5 V	P_7.1.10
LOW level output current	$I_{RD,L}$	2	4	–	mA	V_{RxD} = 0.2 × V_{IO} V_{DIFF} > 0.9 V	P_7.1.11
Transmission Input: TxD							
HIGH level input voltage threshold	$V_{TD,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	"Recessive" state	P_7.1.12
LOW level input voltage threshold	$V_{TD,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	"Dominant" state	P_7.1.13
TxD pull-up resistance	R_{TD}	10	25	50	kΩ	–	P_7.1.14
TxD input hysteresis	$V_{HYS(TxD)}$	–	200	–	mV	1)	P_7.1.15

Table 6 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_J < +150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TxD permanent dominant disable time	t_{TxD}	0.3	–	1.0	ms	–	P_7.1.16
Not Enable Input NEN							
HIGH level input voltage threshold	$V_{NEN,H}$	–	0.5 × V_{IO}	0.7 × V_{IO}	V	Stand-By mode;	P_7.1.17
LOW level input voltage threshold	$V_{NEN,L}$	0.3 × V_{IO}	0.4 × V_{IO}	–	V	Normal Operation mode;	P_7.1.18
NEN pull-up resistance	R_{NEN}	10	25	50	kΩ	–	P_7.1.19
NEN input hysteresis	$V_{HYS(NEN)}$	–	200	–	mV	1)	P_7.1.20
Bus Receiver							
Differential receiver threshold "Dominant"	$V_{DIFF,(D)}$	–	0.75	0.9	V	Normal Operation mode	P_7.1.21
Differential receiver threshold "Recessive"	$V_{DIFF,(R)}$	0.5	0.6	–	–	Normal Operation mode	P_7.1.22
Differential receiver input range - "Dominant"	$V_{diff,rdN}$	0.9	–	5.0	V	Normal Operation mode	P_7.1.23
Differential receiver input range - "Recessive"	$V_{diff,drN}$	-1.0	–	0.5	V	Normal Operation mode	P_7.1.24
Common Mode Range	CMR	-12	–	12	V	V_{CC} = 5 V	P_7.1.25
Differential receiver hysteresis	$V_{diff,hys}$	–	100	–	mV	1)	P_7.1.26
CANH, CANL input resistance	R_i	10	20	30	kΩ	"Recessive" state	P_7.1.27
Differential input resistance	R_{diff}	20	40	60	kΩ	"Recessive" state	P_7.1.28
Input resistance deviation between CANH and CANL	ΔR_i	-3	–	3	%	1) "Recessive" state	P_7.1.29
Input capacitance CANH, CANL versus GND	C_{IN}	–	20	40	pF	1) V_{TxD} = V_{CC}	P_7.1.30
Differential input capacitance	C_{InDiff}	–	10	20	pF	1) V_{TxD} = V_{CC}	P_7.1.31
Bus Transmitter							
CANL/CANH recessive output voltage	$V_{CANL/H}$	2.0	2.5	3.0	V	V_{TxD} = V_{IO}; no load	P_7.1.32
CANH, CANL recessive output voltage difference	V_{diff}	-500	–	50	mV	V_{TxD} = V_{IO}; no load	P_7.1.33
CANL dominant output voltage	V_{CANL}	0.5	–	2.25	V	4.75 V < V_{CC} < 5.25 V, V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω	P_7.1.34
CANH dominant output voltage	V_{CANH}	2.75	–	4.5	V	4.75 V < V_{CC} < 5.25 V, V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω	P_7.1.35

Table 6 Electrical Characteristics (cont'd)

4.5 V < V_{CC} < 5.5 V; 3.0 V < V_{IO} < 5.5 V; R_L = 60 Ω; -40°C < T_J < +150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH, CANL dominant output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$	V_{diff}	1.5	–	3.0	V	4.75 V < V_{CC} < 5.25 V, V_{TxD} = 0 V, 50 Ω < R_L < 65 Ω	P_7.1.36
Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	–	5.5	V	V_{TxD} = "Low"; V_{CC} = 5 V 50 Ω < R_L < 65 Ω	P_7.1.37
CANL short circuit current	I_{CANLsc}	50	100	200	mA	$V_{CANLshort}$ = 18 V	P_7.1.38
CANH short circuit current	I_{CANHsc}	-200	-100	-50	mA	$V_{CANHshort}$ = 0 V	P_7.1.39
Leakage current	$I_{CANHL,lk}$	-5	0	5	µA	V_{CC} = 0 V; V_{CANH} = V_{CANL}; 0 V < $V_{CANH,L}$ < 5 V	P_7.1.40
Dynamic CAN-Transceiver Characteristics							
Propagation delay TxD-to-RxD LOW ("Recessive" to "Dominant")	$t_{d(L),TR}$	–	–	255	ns	C_L = 100 pF; V_{CC} = 5 V; C_{RxD} = 15 pF	P_7.1.41
Propagation delay TxD-to-RxD HIGH ("Dominant" to "Recessive")	$t_{d(H),TR}$	–	–	255	ns	C_L = 100 pF; V_{CC} = 5 V; C_{RxD} = 15 pF	P_7.1.42
Propagation delay TxD LOW to bus "Dominant"	$t_{d(L),T}$	–	110	–	ns	C_L = 100 pF; V_{CC} = 5 V; C_{RxD} = 15 pF	P_7.1.43
Propagation delay TxD HIGH to bus "Recessive"	$t_{d(H),T}$	–	110	–	ns	C_L = 100 pF; V_{CC} = 5 V; C_{RxD} = 15 pF	P_7.1.44
Propagation delay bus "Dominant" to RxD "Low"	$t_{d(L),R}$	–	70	–	ns	C_L = 100 pF; V_{CC} = 5 V; C_{RxD} = 15 pF	P_7.1.45
Propagation delay bus "Recessive" to RxD "High"	$t_{d(H),R}$	–	100	–	ns	C_L = 100 pF; V_{CC} = 5 V; C_{RxD} = 15 pF	P_7.1.46
Time for mode change	t_{Mode}	–	–	10	µs	1)	P_7.1.47

1) Not subject to production test, specified by design

7.2 Diagrams

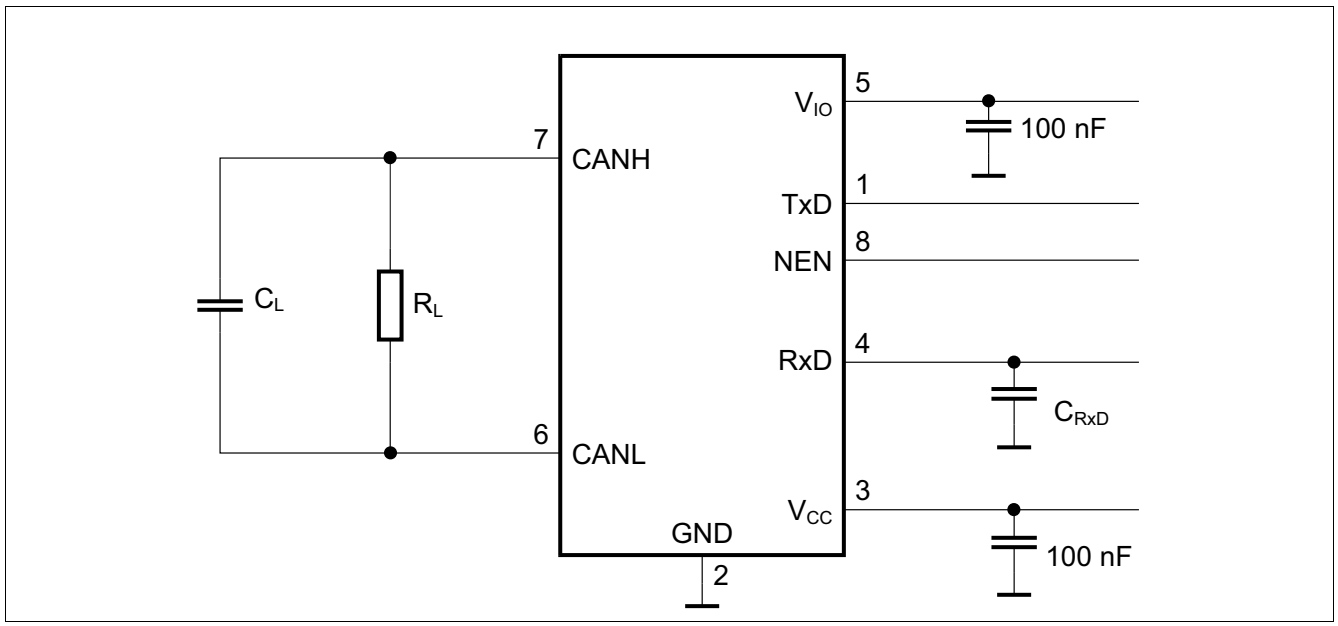


Figure 8 Simplified test circuit

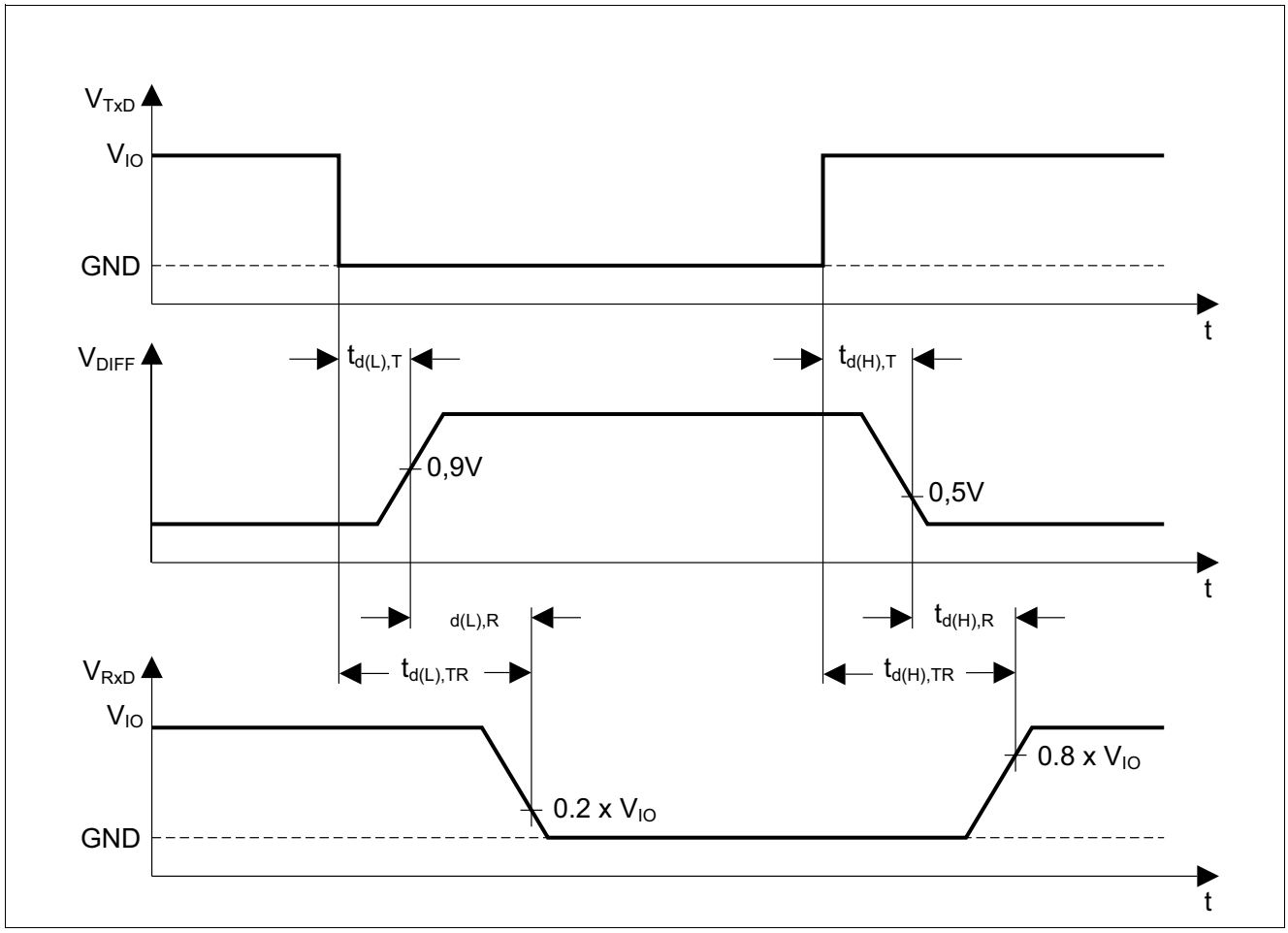


Figure 9 Timing diagram for dynamic characteristics

8 Application Information

8.1 Application Example

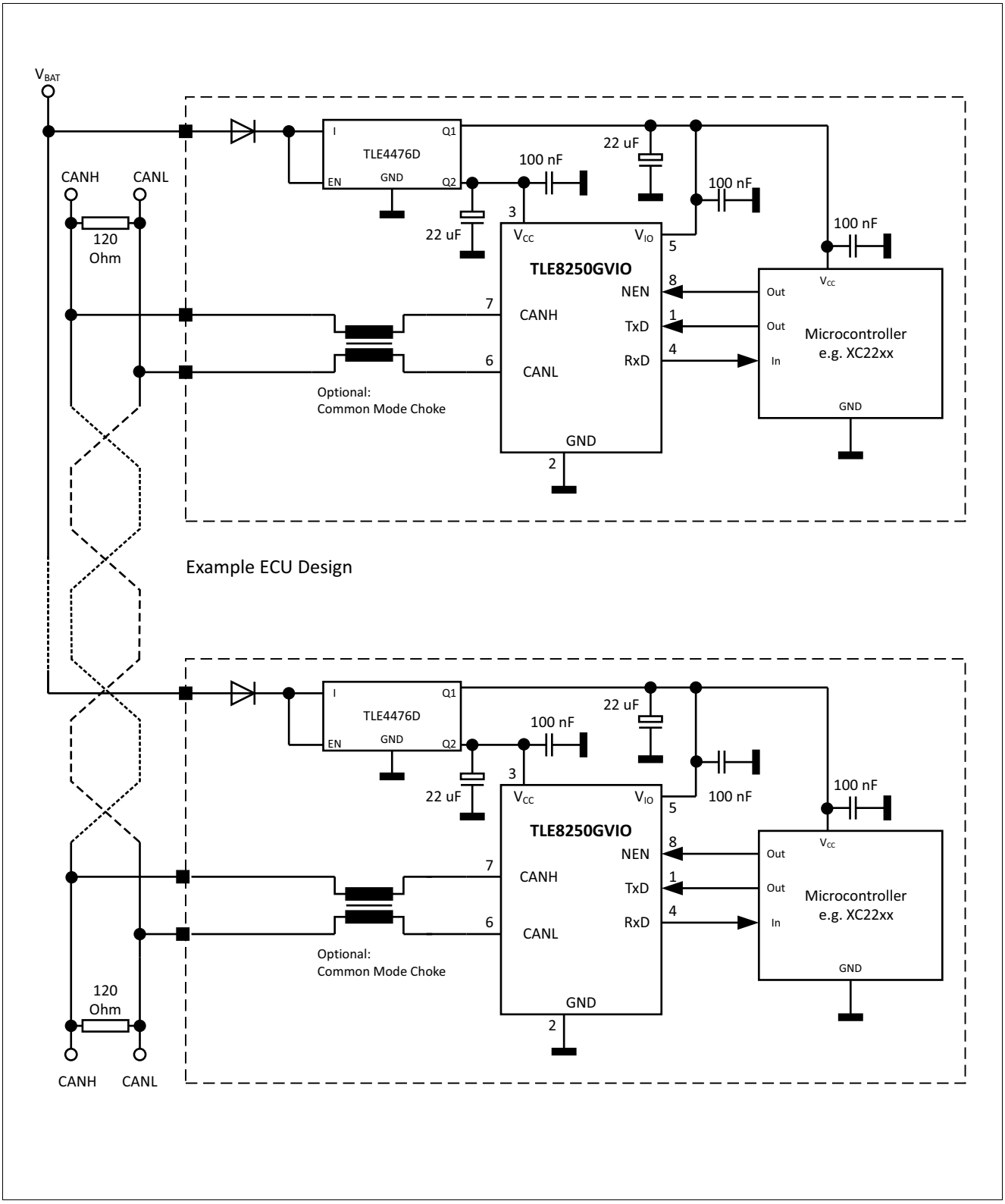


Figure 10 Simplified Application for the TLE8250GVIO

8.2 Output Characteristics of the RxD Pin

The RxD output pin is designed as a push-pull output stage (see Figure 1), meaning to produce a logical “Low” signal the TLE8250GVIO switches the RxD output to GND. Vice versa to produce a logical “High” signal the TLE8250GVIO switches the RxD output to V_{IO}.

The level $V_{RXD,H}$ for a logical “High” signal on the RxD output depends on the load at the RxD output pin and therefore on the RxD output current $I_{RD,H}$. The voltage level $V_{RxD,H}$ also depends on the voltage of the power supply V_{IO}. According to the operating range (see Table 4) the power supply V_{IO} can vary between 3.0 V and 5.5 V. At a V_{IO} supply of 5 V the output current of the RxD pin on the TLE8250GVIO is higher as in comparison for a V_{IO} supply of 3.3 V. For a load against the GND potential, the current $I_{RD,H}$ is flowing out of the RxD output pin.

Similar to the logical “High” signal, the level $V_{RXD,L}$ for a logical “Low” signal on the RxD output pin depends on the input current $I_{RD,L}$ and the power supply voltage V_{IO}. For a load against the power supply V_{IO} the current $I_{RD,L}$ is flowing into the RxD output pin.

Currents flowing into the device are marked positive inside the data sheet and currents flowing out of the device TLE8250GVIO are marked negative inside the data sheet (see Table 6).

The diagram in Figure 11 shows the output current capability of the RxD output pin depended on the chip temperature T_J at a V_{IO} power supply of 5.0 V. Figure 12 shows the output current capability of the RxD output pin at a V_{IO} power supply of 3.3 V.

Both diagrams show the output current for a logical “High” level $V_{RxD,H}$ = 4.6 V. The CAN transceiver TLE8250GVIO provides a logical “High” signal on the RxD output while the signal on the CAN bus is “Recessive” (see Figure 3):

- The curve **“VRxD,H = 4.6 V; typ. output current; VCC = 5.0 V; VIO =5.0 V;”** displays the typical output current at the RxD output pin of the TLE8250GVIO (see Figure 11).
  For this graph V_{CC} = 5.0 V and V_{IO} = 5.0 V.
- The curve **“VRxD,H = 4.6 V; typ. output current + 6 sigma; VCC = 5.0 V; VIO =5.0 V;”** displays the expected maximum value of the output current at the RxD output pin (see Figure 11).
  For this graph V_{CC} = 5.0 V and V_{IO} = 5.0 V.
- The curve **“VRxD,H = 4.6 V; typ. output current - 6 sigma; VCC = 5.0 V; VIO =5.0 V;”** displays the expected minimum value of the output current at the RxD output pin (see Figure 11).
  For this graph V_{CC} = 5.0 V and V_{IO} = 5.0 V.
- The curve **“VRxD,H = 4.6 V; typ. output current; VCC = 5.0 V; VIO =3.3 V;”** displays the typical output current at the RxD output pin of the TLE8250GVIO (see Figure 12).
  For this graph V_{CC} = 5.0 V and V_{IO} = 3.3 V.
- The curve **“VRxD,H = 4.6 V; typ. output current + 6 sigma; VCC = 5.0 V; VIO =3.3 V;”** displays the expected maximum value of the output current at the RxD output pin (see Figure 12).
  For this graph V_{CC} = 5.0 V and V_{IO} = 3.3 V.
- The curve **“VRxD,H = 4.6 V; typ. output current - 6 sigma; VCC = 5.0 V; VIO =3.3 V;”** displays the expected minimum value of the output current at the RxD output pin (see Figure 12).
  For this graph V_{CC} = 5.0 V and V_{IO} = 3.3 V.

The diagram in Figure 13 and the diagram in Figure 14 show the current capability of the RxD output pin depended on the chip temperature T_J. Figure 13 shows the current capability of the RxD output pin at a V_{IO} power supply of 5.0 V and Figure 14 shows the current capability of the RxD output pin at a V_{IO} power supply of 3.3 V.

Both diagrams show the output current for a logical “Low” level $V_{RxD,H}$ = 0.4 V. The CAN transceiver TLE8250GVIO provides a logical “Low” signal on the RxD output while the signal on the CAN bus is “Dominant” (see Figure 3):

- The curve **“VRxD,H = 0.4 V; typ. output current; VCC = 5.0 V; VIO =5.0 V;”** displays the typical output current at the RxD output pin of the TLE8250GVIO (see Figure 13).
  For this graph V_{CC} = 5.0 V and V_{IO} = 5.0 V.
- The curve **“VRxD,H = 0.4 V; typ. output current + 6 sigma; VCC = 5.0 V; VIO =5.0 V;”** displays the expected maximum value of the output current at the RxD output pin (see Figure 13).
  For this graph V_{CC} = 5.0 V and V_{IO} = 5.0 V.
- The curve **“VRxD,H = 0.4 V; typ. output current - 6 sigma; VCC = 5.0 V; VIO =5.0 V;”** displays the expected minimum value of the output current at the RxD output pin (see Figure 13).
  For this graph V_{CC} = 5.0 V and V_{IO} = 5.0 V.
- The curve **“VRxD,H = 0.4 V; typ. output current; VCC = 5.0 V; VIO =3.3 V;”** displays the typical output current at the RxD output pin of the TLE8250GVIO (see Figure 14).
  For this graph V_{CC} = 5.0 V and V_{IO} = 3.3 V.
- The curve **“VRxD,H = 0.4 V; typ. output current + 6 sigma; VCC = 5.0 V; VIO =3.3 V;”** displays the expected maximum value of the output current at the RxD output pin (see Figure 14).
  For this graph V_{CC} = 5.0 V and V_{IO} = 3.3 V.
- The curve **“VRxD,H = 0.4 V; typ. output current - 6 sigma; VCC = 5.0 V; VIO =3.3 V;”** displays the expected minimum value of the output current at the RxD output pin (see Figure 14).
  For this graph V_{CC} = 5.0 V and V_{IO} = 3.3 V.

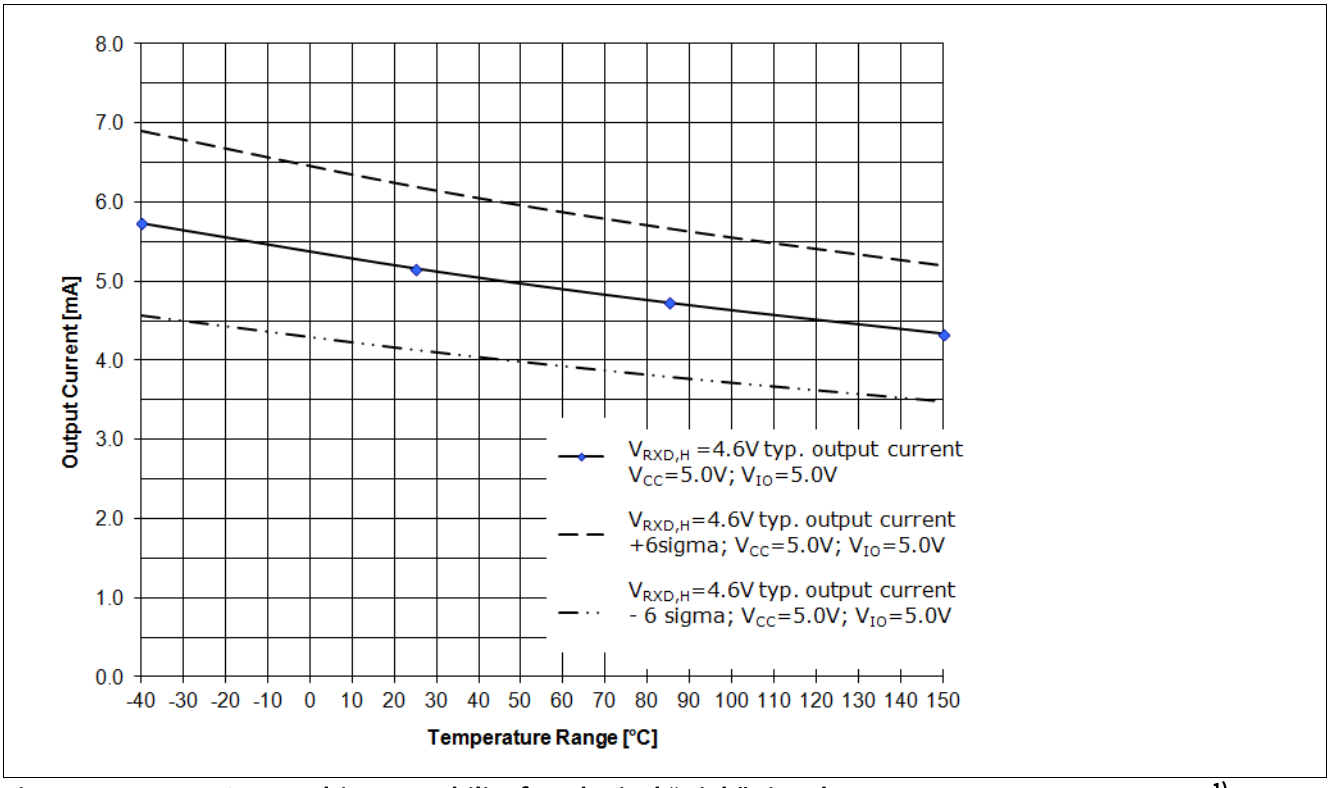


Figure 11 RxD Output driver capability for a logical “High” signal $V_{RxD,H}$=4.6 V, V_{CC}=5.0 V, V_{IO}=5.0 V[1)]

1) Characteristics generated by simulation and specified by design. Production test criteria is described in Table 6; Pos.: 7.1.10

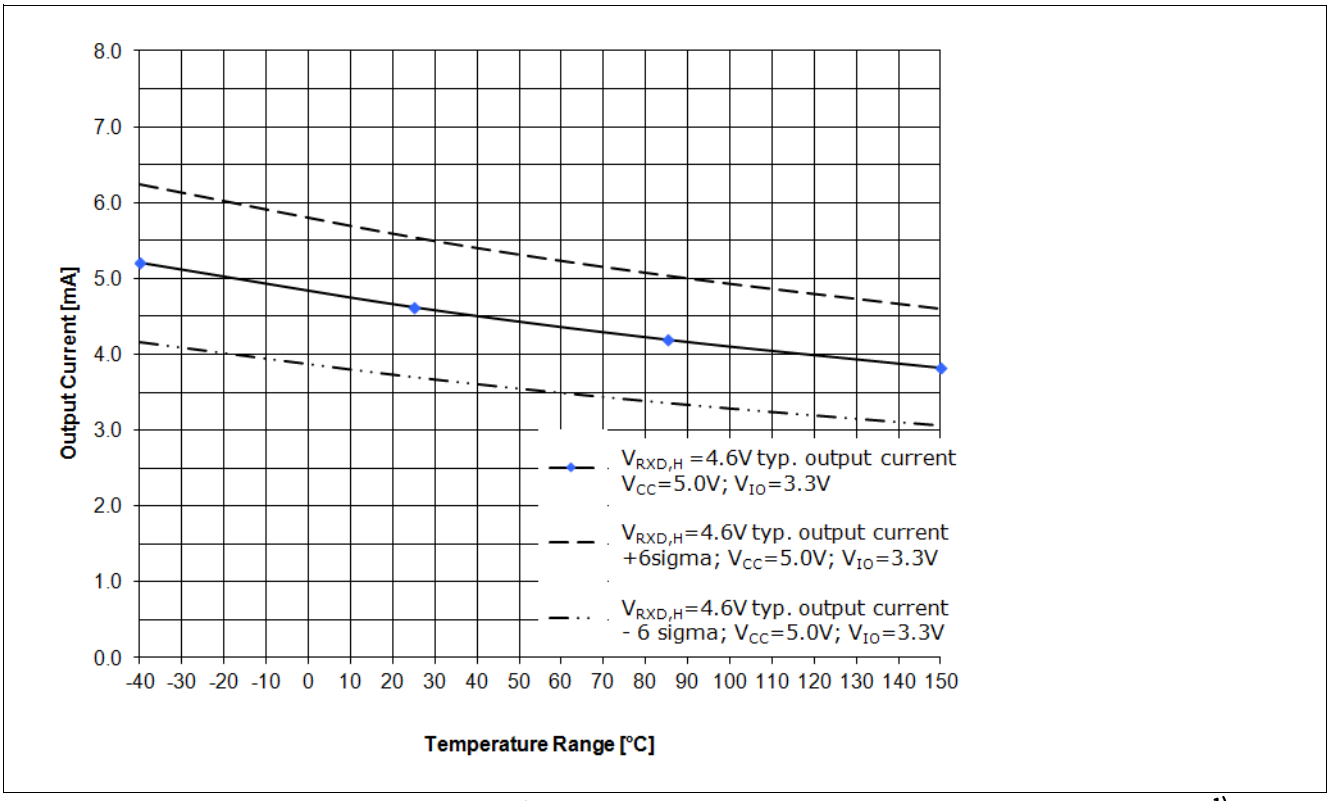


Figure 12 RxD Output driver capability for a logical "High" signal $V_{RxD,H}$=4.6 V, V_{CC}=5.0 V, V_{IO}=3.3 V[1)]

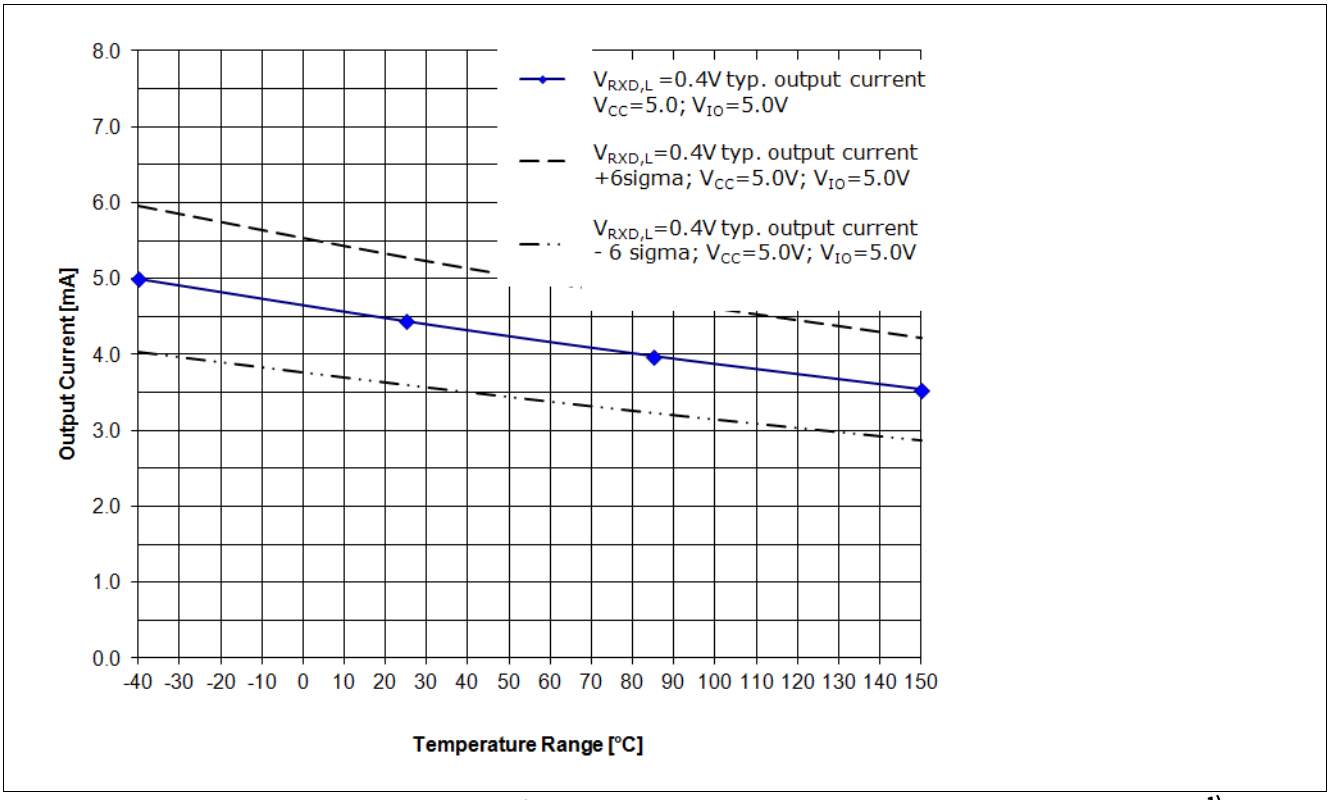


Figure 13 RxD Output driver capability for a logical "Low" signal $V_{RxD,H}$=0.4 V, V_{CC}=5.0 V, V_{IO}=5.0 V[1)]

1) Characteristics generated by simulation and specified by design. Production test criteria is described in Table 6; Pos.: 7.1.11

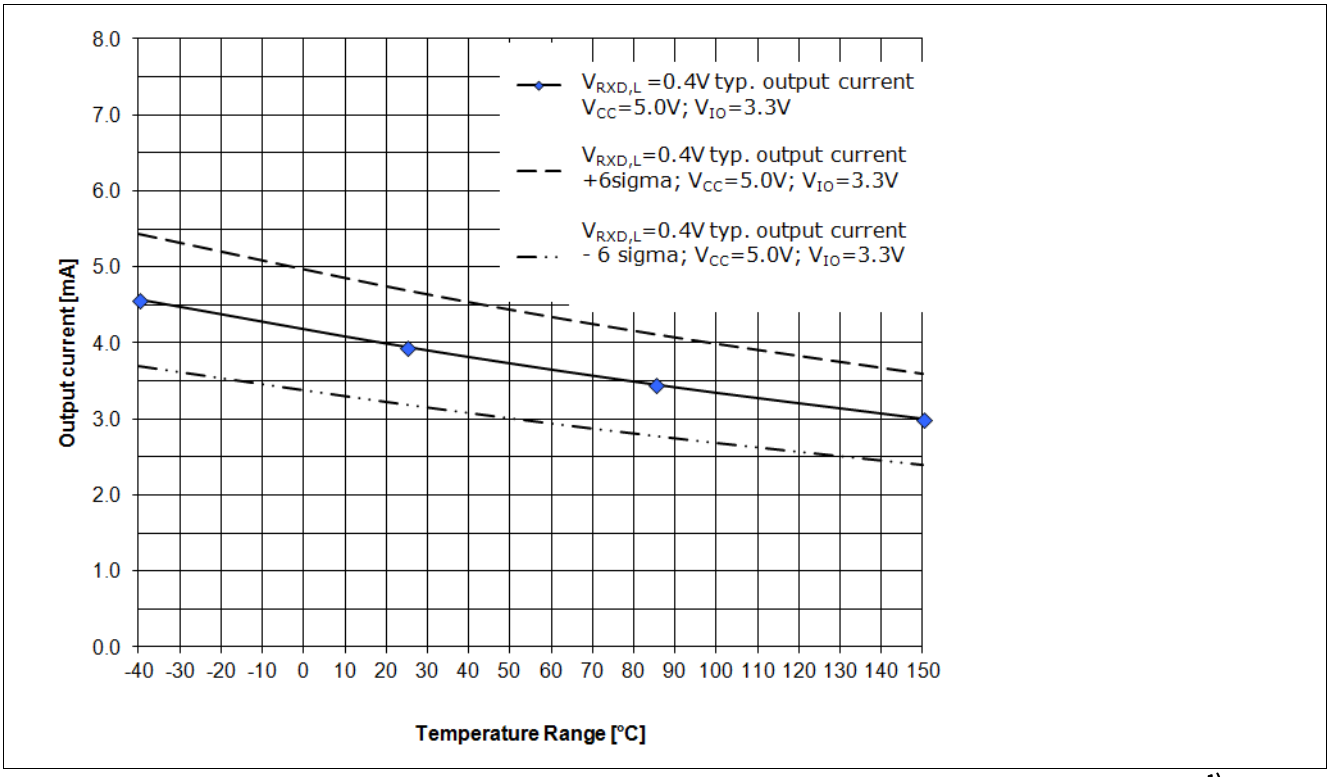


Figure 14 RxD Output driver capability for a logical "Low" signal $V_{RxD,H}$=0.4 V, V_{CC}=5.0 V, V_{IO}=3.3 V[1)]

8.3 Further Application Information

- Please contact us for information regarding the FMEA pin.
- Existing App. Note (Title)
- For further information you may contact http://www.infineon.com/transceiver

9 Package Outlines

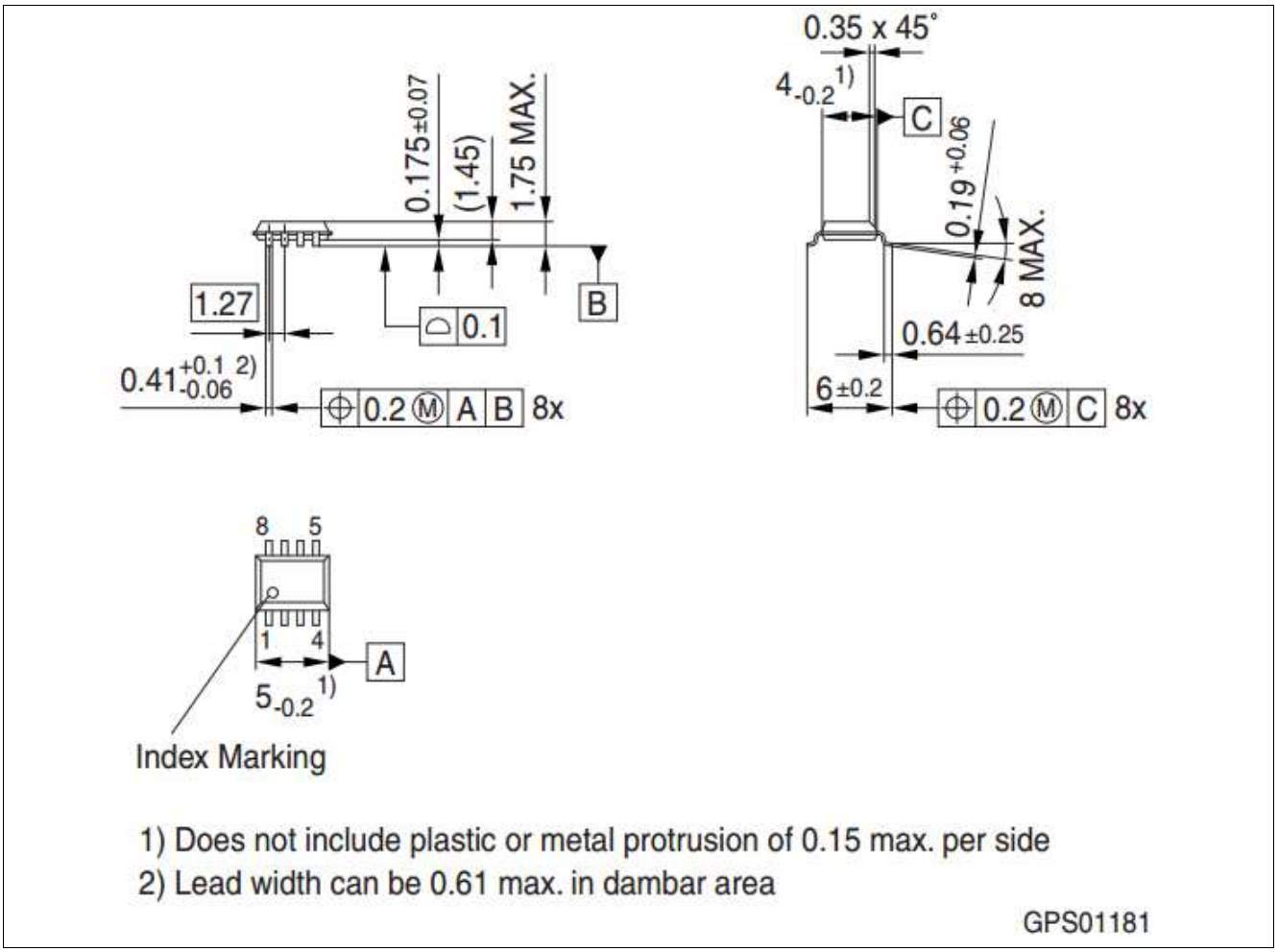


Figure 15 **PG-DSO-8** (Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision History

Revision	Date	Changes
1.11	2016-12-29	Update from Data Sheet Rev. 1.1: • new style template • editorial changes
1.1	2014-09-26	Update from Data Sheet Rev. 1.00: • All pages: Revision and date updated. Spelling and grammar corrected. • Cover page: Logo and layout updated. • Page 1, Overview: Feature list updated (“Extended supply range at V_{CC} and V_{IO}”). • Page 13, Table 4, P_6.2.1: Supply range updated (“4.5 V < V_{CC} < 5.5V”). • Page 13, Table 4, P_6.2.2: Supply range updated (“3.0 V < V_{IO} < 5.5V”). • Page 15, Table 6: Table header updated (“4.5 V < V_{CC} < 5.5V”). Table header updated (“3.0 V < V_{IO} < 5.5V”). • Page 16, Table 6, P_7.1.29: New parameter added. • Page 16, Table 6, P_7.1.30: New parameter added. • Page 16, Table 6, P_7.1.31: New parameter added. • Page 16, Table 6, P_7.1.34: Remark added (“4.75 V < V_{CC} < 5.25V”). • Page 16, Table 6, P_7.1.35: Remark added (“4.75 V < V_{CC} < 5.25V”). • Page 17, Table 6, P_7.1.36: Remark added (“4.75 V < V_{CC} < 5.25V”). • Page 19, Figure 10: Picture updated. • Page 20, Chapter 8.2: Description updated, renamed the term typical input current to typical output current. • Page 21ff, Figure 11, Figure 12, Figure 13, Figure 14: Picture updated • Page 25: Revision history updated
1.0	2010-09-02	Data Sheet created

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