Document Number: K21P80M50SF4
Rev. 4.1, 08/2013

# K21P80M50SF4

## K21 Sub-Family

Supports the following:
MK21DX128VLK5, MK21DX256VLK5, MK21DN512VLK5



### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 50 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - Up to 512 KB of program flash for devices without FlexNVM.
  - Up to 256 KB program flash for devices with FlexNVM.
  - 64 KB FlexNVM on FlexMemory devices
  - 4 KB FlexRAM on FlexMemory devices
  - Up to 64 KB RAM
  - Serial programming interface (EzPort)
- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - 16-channel DMA controller, supporting up to 63 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - Tamper detect and secure storage
  - Hardware random-number generator
  - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - General-purpose input/output
- Analog modules
  - 16-bit SAR ADC
  - Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two 2-channel general purpose timers, one with quadrature decoder functionality
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect
  - Two SPI modules
  - Two I2C modules
  - Four UART modules
  - I2S module

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

© 2012–2013 Freescale Semiconductor, Inc.

# Table of Contents


1 Ordering parts....3
1.1 Determining valid orderable parts....3
2 Part identification....3
2.1 Description....3
2.2 Format....3
2.3 Fields....3
2.4 Example....4
2.5 Small package marking....4
3 Terminology and guidelines....5
3.1 Definition: Operating requirement....5
3.2 Definition: Operating behavior....5
3.3 Definition: Attribute....6
3.4 Definition: Rating....6
3.5 Result of exceeding a rating....7
3.6 Relationship between ratings and operating requirements....7
3.7 Guidelines for ratings and operating requirements....8
3.8 Definition: Typical value....8
3.9 Typical value conditions....9
4 Ratings....9
4.1 Thermal handling ratings....9
4.2 Moisture handling ratings....10
4.3 ESD handling ratings....10
4.4 Voltage and current operating ratings....10
5 General....10
5.1 AC electrical characteristics....11
5.2 Nonswitching electrical specifications....11
5.2.1 Voltage and current operating requirements....11
5.2.2 LVD and POR operating requirements....12
5.2.3 Voltage and current operating behaviors....13
5.2.4 Power mode transition operating behaviors....13
5.2.5 Power consumption operating behaviors....14
5.2.6 EMC radiated emissions operating behaviors....18
5.2.7 Designing with radiated emissions in mind....19
5.2.8 Capacitance attributes....19
5.3 Switching specifications....19
5.3.1 Device clock specifications....19
5.3.2 General switching specifications....20
5.4 Thermal specifications....21
5.4.1 Thermal operating requirements....21
5.4.2 Thermal attributes....21
6 Peripheral operating requirements and behaviors....22
6.1 Core modules....22
6.1.1 JTAG electricals....22
6.2 System modules....25
6.3 Clock modules....25
6.3.1 MCG specifications....25
6.3.2 Oscillator electrical specifications....27
6.3.3 32 kHz oscillator electrical characteristics....30
6.4 Memories and memory interfaces....30
6.4.1 Flash electrical specifications....30
6.4.2 EzPort switching specifications....33
6.5 Security and integrity modules....34
6.5.1 DryIce Tamper Electrical Specifications....34
6.6 Analog....35
6.6.1 ADC electrical specifications....35
6.6.2 CMP and 6-bit DAC electrical specifications....39
6.7 Timers....42
6.8 Communication interfaces....42
6.8.1 USB electrical specifications....42
6.8.2 USB DCD electrical specifications....42
6.8.3 VREG electrical specifications....43
6.8.4 DSPI switching specifications (limited voltage range)....43
6.8.5 DSPI switching specifications (full voltage range)....45
6.8.6 I2C switching specifications....47
6.8.7 UART switching specifications....47
6.8.8 Normal Run, Wait and Stop mode performance over the full operating voltage range....47
6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range....49
7 Dimensions....51
7.1 Obtaining package dimensions....51
8 Pinout....51
8.1 K21 Signal Multiplexing and Pin Assignments....51
8.2 K21 Pinouts....54
9 Revision History....56

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK21 and MK21 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| K## | Kinetis family | • K21 |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | • N = Program flash only<br>• X = Program flash and FlexMemory |

*Table continues on the next page...*

| Field | Description | Values |
|---|---|---|
| FFF | Program flash memory size | • 32 = 32 KB<br>• 64 = 64 KB<br>• 128 = 128 KB<br>• 256 = 256 KB<br>• 512 = 512 KB<br>• 1M0 = 1 MB<br>• 2M0 = 2 MB |
| R | Silicon revision | • Z = Initial<br>• (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105<br>• C = –40 to 85 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• FT = 48 QFN (7 mm x 7 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm)<br>• MP = 64 MAPBGA (5 mm x 5 mm)<br>• LK = 80 LQFP (12 mm x 12 mm)<br>• LL = 100 LQFP (14 mm x 14 mm)<br>• MC = 121 MAPBGA (8 mm x 8 mm)<br>• LQ = 144 LQFP (20 mm x 20 mm)<br>• MD = 144 MAPBGA (13 mm x 13 mm) |
| CC | Maximum CPU frequency (MHz) | • 5 = 50 MHz<br>• 7 = 72 MHz<br>• 10 = 100 MHz<br>• 12 = 120 MHz<br>• 15 = 150 MHz<br>• 18 = 180 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 2.4 Example

This is an example part number:

MK21DX128VLK5

## 2.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| ## | Kinetis family | • 1# = K11/K12<br>• 2# = K21/K22 |
| C | Speed | • G = 50 MHz |
| F | Flash memory configuration | • G = 128 KB + Flex<br>• H = 256 KB + Flex<br>• 9 = 512 KB |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • MC = 121 MAPBGA |

This tables lists some examples of small package marking along with the original part numbers:

| Original part number | Alternate part number |
|---|---|
| MK21DX128VMC5 | M21GGVMC |
| MK21DX256VMC5 | M21GHVMC |
| MK21DN512VMC5 | M21G9VMC |

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/ pulldown current | 10 | 130 | µA |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

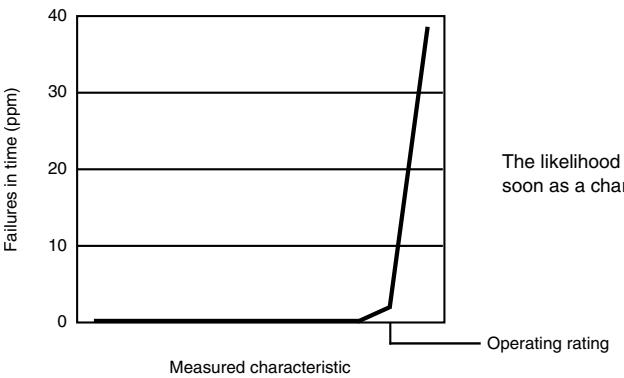
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

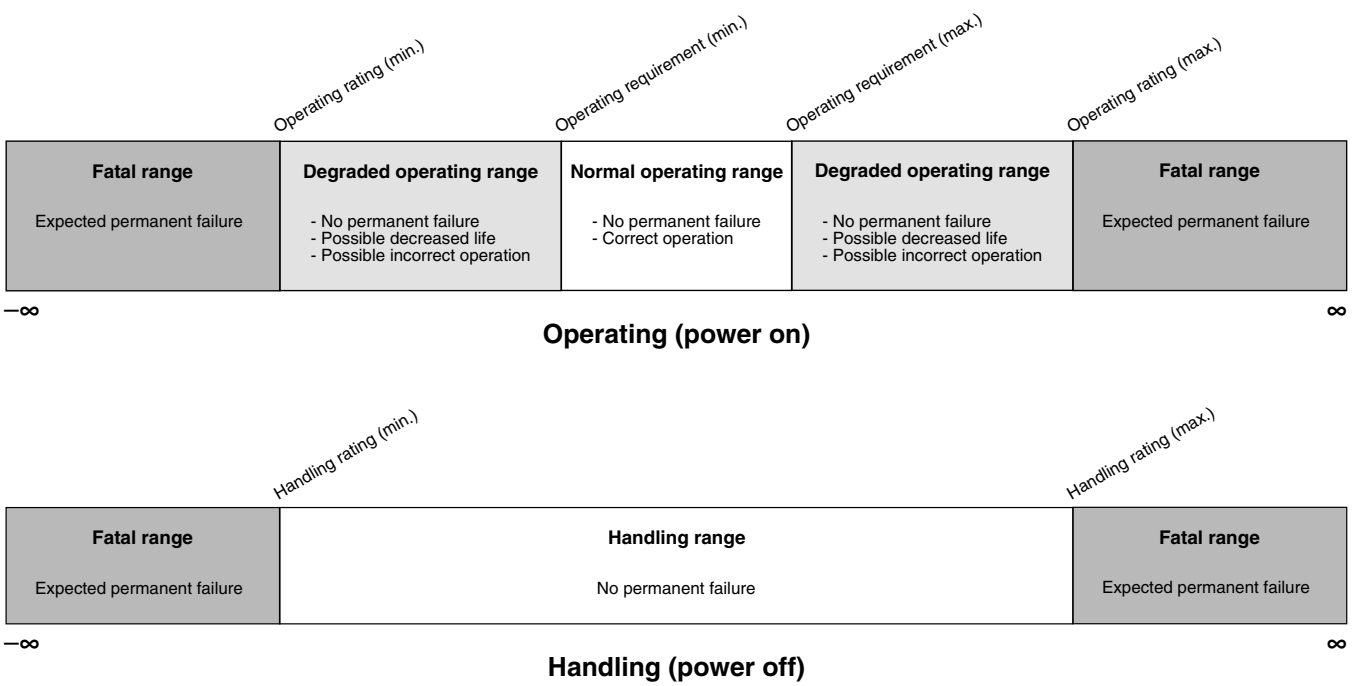
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 3.6 Relationship between ratings and operating requirements



## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

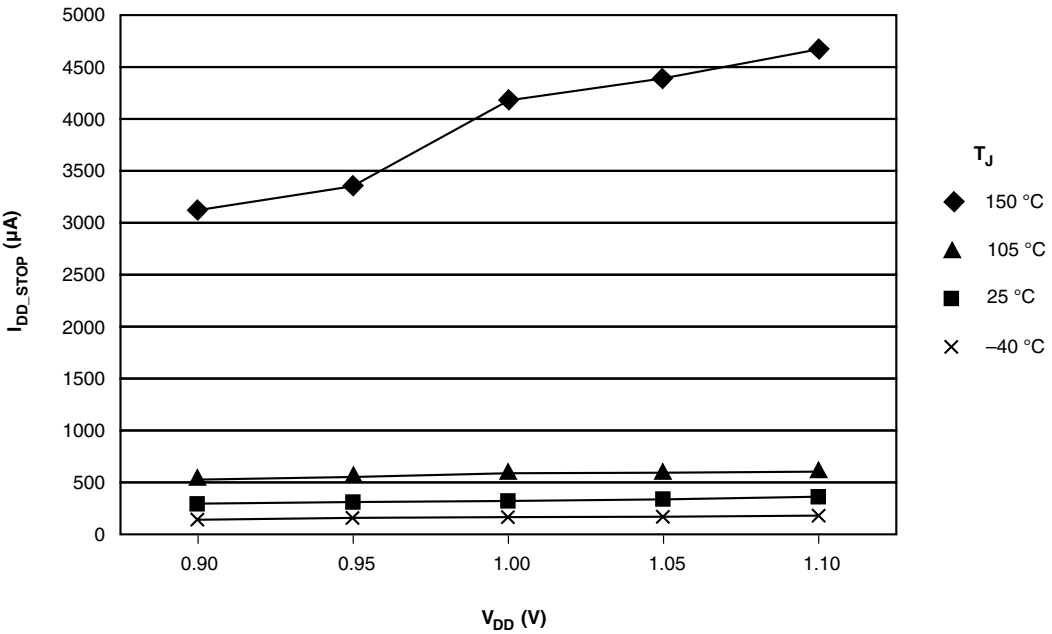
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 4 Ratings

## 4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 4.4 Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 155 | mA |
| $V_{DIO}$ | Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL) | –0.3 | | V |
| $V_{AIO}$ | Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Maximum current single pin limit (applies to all digital pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{USB0_DP}$ | USB0_DP input voltage | –0.3 | 3.63 | V |
| $V_{USB0_DM}$ | USB0_DM input voltage | –0.3 | 3.63 | V |
| VREGIN | USB regulator input | –0.3 | 6.0 | V |
| $V_{BAT}$ | RTC battery supply voltage | –0.3 | 3.8 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

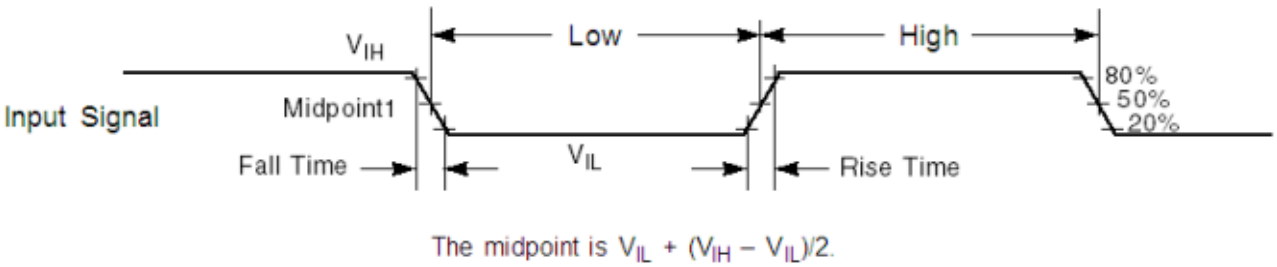



**Figure 1. Input signal measurement reference**

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{BAT}$ | RTC battery supply voltage | 1.71 | 3.6 | V | |
| $V_{IH}$ | Input high voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>0.7 × $V_{DD}$<br>0.75 × $V_{DD}$ | <br>—<br>— | <br>V<br>V | |
| $V_{IL}$ | Input low voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | <br>—<br>— | <br>0.35 × $V_{DD}$<br>0.3 × $V_{DD}$ | <br>V<br>V | |
| $V_{HYS}$ | Input hysteresis | 0.06 × $V_{DD}$ | — | V | |
| $I_{ICIO}$ | I/O pin DC injection current — single pin<br>• $V_{IN}$ < $V_{SS}$-0.3V (Negative current injection)<br>• $V_{IN}$ > $V_{DD}$+0.3V (Positive current injection) | <br>-3<br>— | <br>—<br>+3 | <br>mA | 1 |

*Table continues on the next page...*

**Table 1. Voltage and current operating requirements (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $I_{ICcont}$ | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins<br>• Negative current injection<br>• Positive current injection | <br><br>-25<br>— | <br><br>—<br>+25 | <br><br>mA | |
| $V_{RAM}$ | $V_{DD}$ voltage required to retain RAM | 1.2 | — | V | |
| $V_{RFVBAT}$ | $V_{BAT}$ voltage required to retain the VBAT register file | $V_{POR_VBAT}$ | — | V | |

1. All analog pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is less than $V_{AIO_MIN}$ or greater than $V_{AIO_MAX}$, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

## 5.2.2 LVD and POR operating requirements

**Table 2. $V_{DD}$ supply LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| $V_{LVW1H}$ | • Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | 80 | — | mV | |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | 60 | — | mV | |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising threshold is the sum of falling threshold and hysteresis voltage

**Table 3. VBAT power operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR_VBAT}$ | Falling VBAT supply POR detect voltage | 0.8 | 1.1 | 1.5 | V | |

## 5.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = - 9 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -3 mA | $V_{DD}$ – 0.5 | — | V | |
| | Output high voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 9 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 3 mA | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 0.6 mA | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) | | | | |
| | • @ full temperature range | — | 1.0 | µA | 1 |
| | • @ 25 °C | — | 0.1 | µA | |
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | µA | |
| $I_{OZ}$ | Total Hi-Z (off-state) leakage current (all input pins) | — | 4 | µA | |
| $R_{PU}$ | Internal pullup resistors | 22 | 50 | kΩ | 2 |
| $R_{PD}$ | Internal pulldown resistors | 22 | 50 | kΩ | 3 |

1. Tested by ganged leakage method
2. Measured at Vinput = $V_{SS}$
3. Measured at Vinput = $V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

**Table 5. Power mode transition operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.<br>• 1.71 V/($V_{DD}$ slew rate) ≤ 300 µs<br>• 1.71 V/($V_{DD}$ slew rate) > 300 µs | <br><br>—<br>— | <br><br>300<br>1.7 V / ($V_{DD}$ slew rate) | µs | 1 |
| | • VLLS0 → RUN | — | 135 | µs | |
| | • VLLS1 → RUN | — | 135 | µs | |
| | • VLLS2 → RUN | — | 85 | µs | |
| | • VLLS3 → RUN | — | 85 | µs | |
| | • LLS → RUN | — | 6 | µs | |
| | • VLPS → RUN | — | 5.2 | µs | |
| | • STOP → RUN | — | 5.2 | µs | |

1. Normal boot (FTFL_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash<br>• @ 1.8 V<br>• @ 3.0 V | <br>—<br>— | <br>12.98<br>12.93 | <br>14<br>13.8 | <br>mA<br>mA | 2 |

*Table continues on the next page...*

## Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | 3, 4 |
| | • @ 1.8 V | — | 17.04 | 19.3 | mA | |
| | • @ 3.0 V | | | | | |
| | • @ 25°C | — | 17.01 | 18.9 | mA | |
| | • @ 125°C | — | 19.8 | 21.3 | mA | |
| $I_{DD_WAIT}$ | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled | — | 7.95 | 9.5 | mA | 2 |
| $I_{DD_WAIT}$ | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 5.88 | 7.4 | mA | 5 |
| $I_{DD_STOP}$ | Stop mode current at 3.0 V | — | | | µA | |
| | • @ –40 to 25°C | | 320 | 436 | | |
| | • @ 50°C | | 360 | 489 | | |
| | • @ 70°C | | 410 | 620 | | |
| | • @ 105°C | | 610 | 1100 | | |
| $I_{DD_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled | — | 754 | — | µA | 6 |
| $I_{DD_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | 1.1 | — | mA | 7 |
| $I_{DD_VLPW}$ | Very-low-power wait mode current at 3.0 V | — | 437 | — | µA | 8 |
| $I_{DD_VLPS}$ | Very-low-power stop mode current at 3.0 V | — | | | µA | |
| | • @ –40 to 25°C | | 7.33 | 24.2 | | |
| | • @ 50°C | | 14 | 32 | | |
| | • @ 70°C | | 28 | 48 | | |
| | • @ 105°C | | 110 | 280 | | |
| $I_{DD_LLS}$ | Low leakage stop mode current at 3.0 V | — | | | µA | |
| | • @ –40 to 25°C | | 3.14 | 4.8 | | |
| | • @ 50°C | | 6.48 | 28.3 | | |
| | • @ 70°C | | 13.85 | 44.6 | | |
| | • @ 105°C | | 55.53 | 71.3 | | |
| $I_{DD_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | — | | | µA | |
| | • @ –40 to 25°C | | 2.19 | 3.4 | | |
| | • @ 50°C | | 4.35 | 4.35 | | |
| | • @ 70°C | | 8.92 | 24.6 | | |
| | • @ 105°C | | 35.33 | 45.3 | | |
| $I_{DD_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | — | | | µA | |
| | • @ –40 to 25°C | | 1.77 | 3.1 | | |
| | • @ 50°C | | 2.81 | 13.8 | | |
| | • @ 70°C | | 5.20 | 22.3 | | |
| | • @ 105°C | | 19.88 | 34.2 | | |

*Table continues on the next page...*

**Table 6. Power consumption operating behaviors (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 1.03<br>1.92<br>4.03<br>17.43 | 1.8<br>7.5<br>15.9<br>28.7 | µA | |
| $I_{DD_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 0.543<br>1.36<br>3.39<br>16.52 | 1.1<br>7.58<br>14.3<br>24.1 | µA | |
| $I_{DD_VLLS0}$ | Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 0.359<br>1.03<br>2.87<br>15.20 | 0.95<br>6.8<br>15.4<br>25.3 | µA | |
| $I_{DD_VBAT}$ | Average current when CPU is not accessing RTC registers at 3.0 V<br>• @ –40 to 25°C<br>• @ 50°C<br>• @ 70°C<br>• @ 105°C | — | 0.91<br>1.1<br>1.5<br>4.3 | 1.1<br>1.35<br>1.85<br>5.7 | µA | 9 |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32 kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

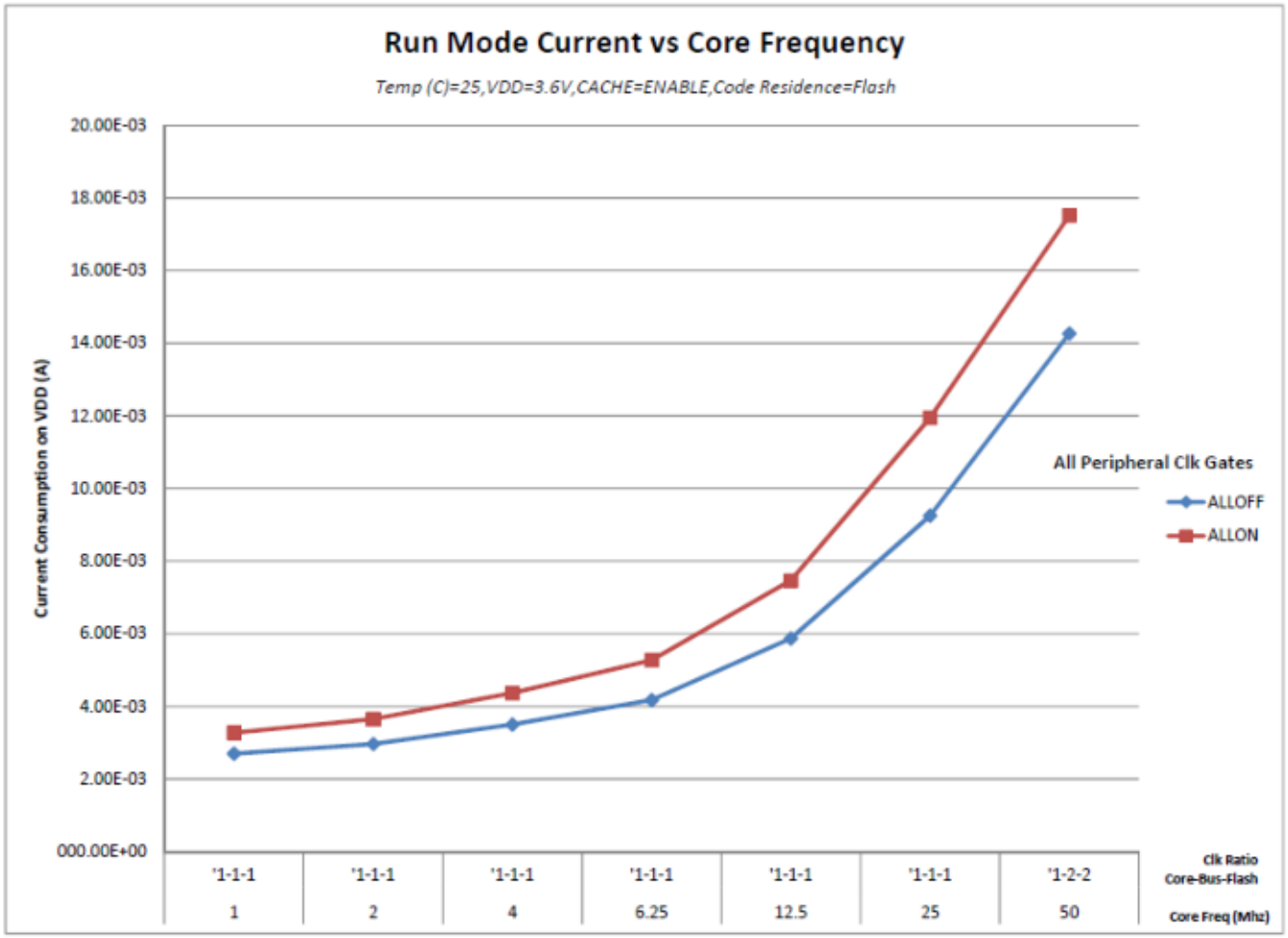



**Figure 2. Run mode supply current vs. core frequency**

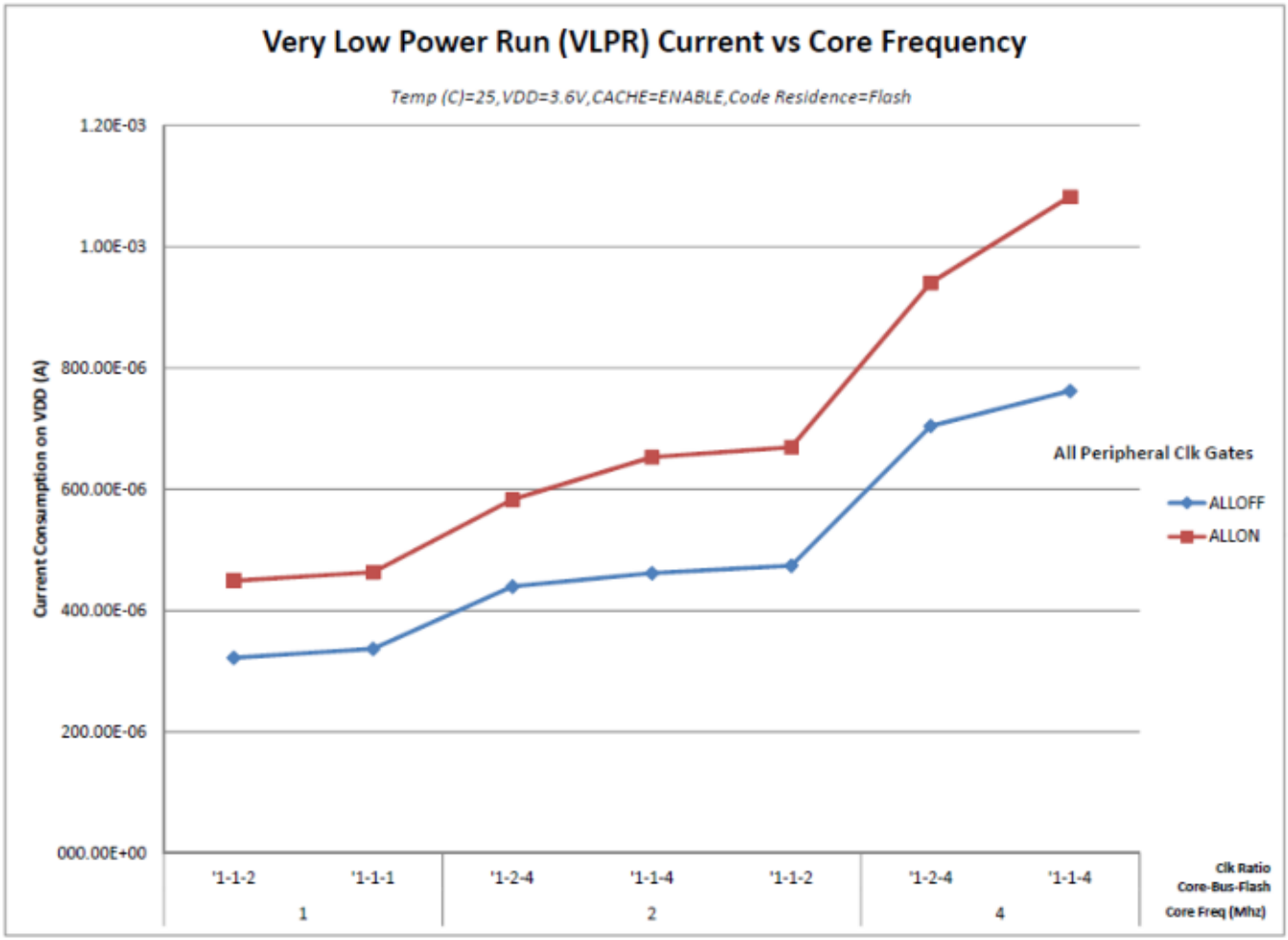



**Figure 3. VLPR mode supply current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

**Table 7. EMC radiated emissions operating behaviors [1]**

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{RE1}$ | Radiated emissions voltage, band 1 | 0.15–50 | 19 | dBµV | 2, 3 |
| $V_{RE2}$ | Radiated emissions voltage, band 2 | 50–150 | 21 | dBµV | |
| $V_{RE3}$ | Radiated emissions voltage, band 3 | 150–500 | 19 | dBµV | |
| $V_{RE4}$ | Radiated emissions voltage, band 4 | 500–1000 | 11 | dBµV | |
| $V_{RE_IEC}$ | IEC level | 0.15–1000 | L | — | 3, 4 |

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

3. $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, $f_{OSC}$ = 12 MHz (crystal), $f_{SYS}$ = 48 MHz, $f_{BUS}$ = 48MHz
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

### 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

### 5.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

**Table 9. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 50 | MHz | |
| | System and core clock when Full Speed USB in operation | 20 | — | MHz | |
| $f_{BUS}$ | Bus clock | — | 50 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 25 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |
| VLPR mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 4 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |
| $f_{LPTMR_pin}$ | LPTMR clock | — | 25 | MHz | |

*Table continues on the next page...*

**Table 9. Device clock specifications (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $f_{LPTMR_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz | |
| $f_{I2S_MCLK}$ | I2S master clock | — | 12.5 | MHz | |
| $f_{I2S_BCLK}$ | I2S bit clock | — | 4 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

**Table 10. General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path | 100 | — | ns | 3 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 50 | — | ns | 3 |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns | 3 |
| | Port rise and fall time (high drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br><br>—<br>—<br><br>—<br>— | <br><br><br>13<br>7<br><br>36<br>24 | <br><br><br>ns<br>ns<br><br>ns<br>ns | 4 |
| | Port rise and fall time (low drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br><br>—<br>—<br><br>—<br>— | <br><br><br>12<br>6<br><br>36<br>24 | <br><br><br>ns<br>ns<br><br>ns<br>ns | 5 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.

3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

# 5.4 Thermal specifications

## 5.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |

## 5.4.2 Thermal attributes

| Board type | Symbol | Description | 80 LQFP | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 50 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 35 | °C/W | 1, 3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 39 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 29 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 19 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 8 | °C/W | 5 |

*Table continues on the next page...*

| Board type | Symbol | Description | 80 LQFP | Unit | Notes |
|---|---|---|---|---|---|
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 2 | °C/W | 6 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 6 Peripheral operating requirements and behaviors

## 6.1 Core modules

### 6.1.1 JTAG electricals

**Table 12. JTAG limited voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 25 | |
| | • Serial Wire Debug | 0 | 50 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 20 | — | ns |
| | • Serial Wire Debug | 10 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |

*Table continues on the next page...*

## Table 12. JTAG limited voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |
| J11 | TCLK low to TDO data valid | — | 17 | ns |
| J12 | TCLK low to TDO high-Z | — | 17 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

## Table 13. JTAG full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 20 | |
| | • Serial Wire Debug | 0 | 40 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 25 | — | ns |
| | • Serial Wire Debug | 12.5 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.4 | — | ns |
| J11 | TCLK low to TDO data valid | — | 22.1 | ns |
| J12 | TCLK low to TDO high-Z | — | 22.1 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

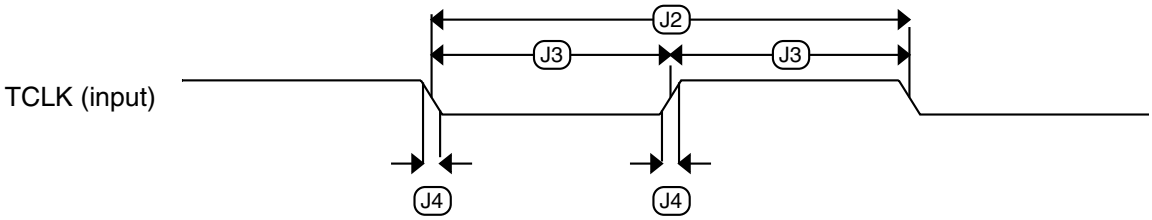



**Figure 4. Test clock input timing**

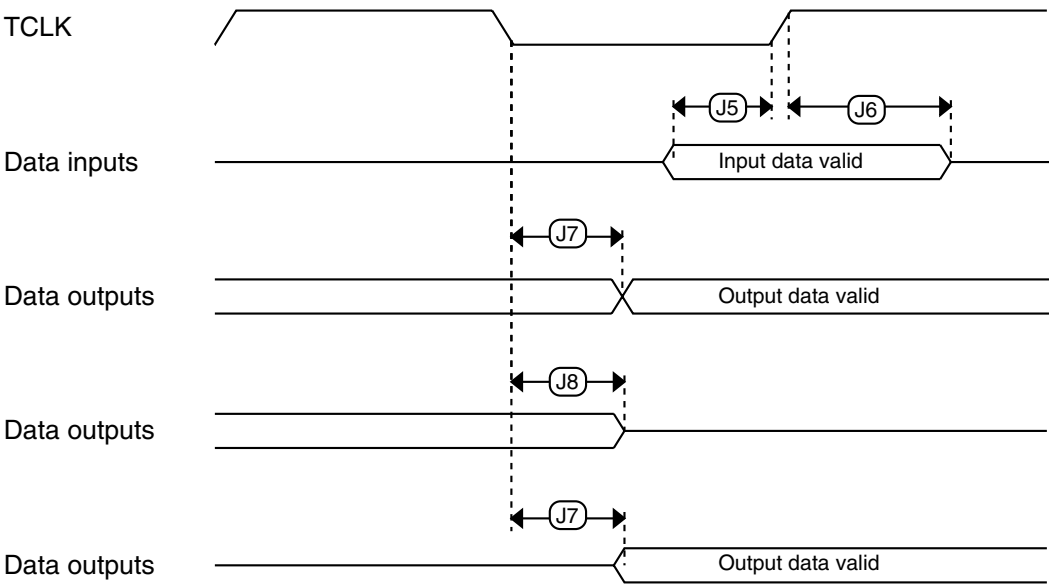



**Figure 5. Boundary scan (JTAG) timing**

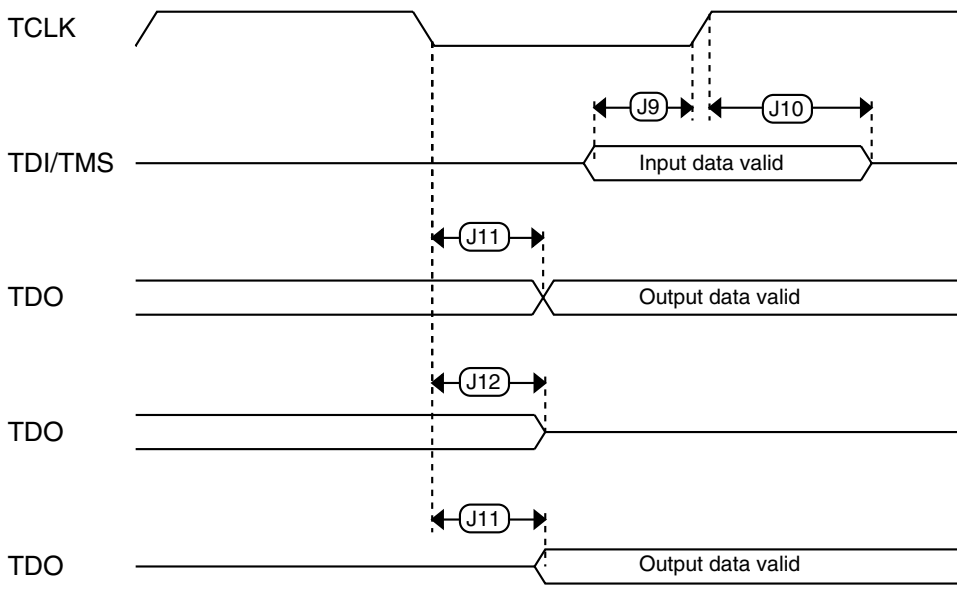



**Figure 6. Test Access Port timing**

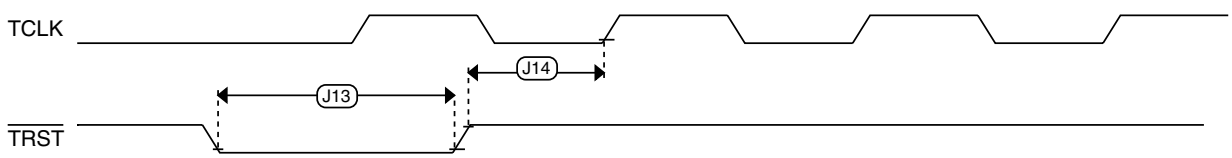



**Figure 7. $\overline{\text{TRST}}$ timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

**Table 14. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | | — | ± 0.2 | ± 0.5 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | ± 2 | $\%f_{dco}$ | 1, 2 |
| $\Delta f_{dco_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | | — | ± 0.3 | ±1 | $\%f_{dco}$ | 1, 2 |
| $f_{intf_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | | — | 4 | — | MHz | |
| $f_{intf_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints_t}$ | — | — | kHz | |
| $f_{loc_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | | (16/5) x $f_{ints_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00) 640 × $f_{fll_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS=01) 1280 × $f_{fll_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10) 1920 × $f_{fll_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11) 2560 × $f_{fll_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco_t_DMX32}$ | DCO output frequency | Low range (DRS=00) 732 × $f_{fll_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS=01) 1464 × $f_{fll_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) 2197 × $f_{fll_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) 2929 × $f_{fll_ref}$ | — | 95.98 | — | MHz | |

*Table continues on the next page...*

**Table 14. MCG specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $J_{cyc_fll}$ | FLL period jitter<br>• $f_{DCO}$ = 48 MHz<br>• $f_{DCO}$ = 98 MHz | —<br>— | 180<br>150 | —<br>— | ps | |
| $t_{fll_acquire}$ | FLL target frequency acquisition time | — | — | 1 | ms | 7 |
| PLL | | | | | | |
| $f_{vco}$ | VCO operating frequency | 48.0 | — | 100 | MHz | |
| $I_{pll}$ | PLL operating current<br>• PLL @ 96 MHz ($f_{osc_hi_1}$ = 8 MHz, $f_{pll_ref}$ = 2 MHz, VDIV multiplier = 48) | — | 1060 | — | µA | 8 |
| $I_{pll}$ | PLL operating current<br>• PLL @ 48 MHz ($f_{osc_hi_1}$ = 8 MHz, $f_{pll_ref}$ = 2 MHz, VDIV multiplier = 24) | — | 600 | — | µA | 8 |
| $f_{pll_ref}$ | PLL reference frequency range | 2.0 | — | 4.0 | MHz | |
| $J_{cyc_pll}$ | PLL period jitter (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | <br>—<br>— | <br>120<br>50 | <br>—<br>— | <br>ps<br>ps | 9 |
| $J_{acc_pll}$ | PLL accumulated jitter over 1µs (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | <br>—<br>— | <br>1350<br>600 | <br>—<br>— | <br>ps<br>ps | 9 |
| $D_{lock}$ | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll_lock}$ | Lock detector detection time | — | — | $150 \times 10^{-6} + 1075(1/f_{pll_ref})$ | s | 10 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco_t}$) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

### 6.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high-gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |
| $R_F$ | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | MΩ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | MΩ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | MΩ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |

*Table continues on the next page...*

**Table 15. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{pp}$[5] | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$ and $C_y$ can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 6.3.2.2 Oscillator frequency specifications

**Table 16. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that—it remains within the limits of DCO input clock frequency when divided by FRDIV.
3. Proper PC board layout procedures must be followed to achieve specifications.

4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

**NOTE**

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

## 6.3.3 32 kHz oscillator electrical characteristics

### 6.3.3.1 32 kHz oscillator DC electrical specifications

**Table 17. 32kHz oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BAT}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $R_F$ | Internal feedback resistor | — | 100 | — | MΩ |
| $C_{para}$ | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| $V_{pp}$[1] | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.3.2 32 kHz oscillator frequency specifications

**Table 18. 32 kHz oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc_lo}$ | Oscillator crystal | — | 32.768 | — | kHz | |
| $t_{start}$ | Crystal start-up time | — | 1000 | — | ms | 1 |
| $v_{ec_extal32}$ | Externally provided input clock amplitude | 700 | — | $V_{BAT}$ | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and $V_{IH}$ and $V_{IL}$ specifications do not apply. The voltage of the applied clock must be within the range of $V_{SS}$ to $V_{BAT}$.

# 6.4 Memories and memory interfaces

## 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversblk256k}$ | Erase Block high-voltage time for 256 KB | — | 104 | 904 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Read 1s Block execution time | | | | | |
| $t_{rd1blk64k}$ | • 64 KB data flash | — | — | 0.9 | ms | |
| $t_{rd1blk256k}$ | • 256 KB program flash | — | — | 1.7 | ms | |
| $t_{rd1sec2k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | |
| | Erase Flash Block execution time | | | | | 2 |
| $t_{ersblk64k}$ | • 64 KB data flash | — | 58 | 580 | ms | |
| $t_{ersblk256k}$ | • 256 KB program flash | — | 122 | 985 | ms | |
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| | Program Section execution time | | | | | |
| $t_{pgmsec512}$ | • 512 bytes flash | — | 2.4 | — | ms | |
| $t_{pgmsec1k}$ | • 1 KB flash | — | 4.7 | — | ms | |
| $t_{pgmsec2k}$ | • 2 KB flash | — | 9.3 | — | ms | |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | |
| $t_{ersall}$ | Erase All Blocks execution time | — | 250 | 2000 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |

*Table continues on the next page...*

## Table 20. Flash command timing specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Swap Control execution time | | | | | |
| $t_{swapx01}$ | • control code 0x01 | — | 200 | — | µs | |
| $t_{swapx02}$ | • control code 0x02 | — | 70 | 150 | µs | |
| $t_{swapx04}$ | • control code 0x04 | — | 70 | 150 | µs | |
| $t_{swapx08}$ | • control code 0x08 | — | — | 30 | µs | |
| | Program Partition for EEPROM execution time | | | | | |
| $t_{pgmpart64k}$ | • 64 KB FlexNVM | — | 138 | — | ms | |
| | Set FlexRAM Function execution time: | | | | | |
| $t_{setramff}$ | • Control Code 0xFF | — | 70 | — | µs | |
| $t_{setram32k}$ | • 32 KB EEPROM backup | — | 0.8 | 1.2 | ms | |
| $t_{setram64k}$ | • 64 KB EEPROM backup | — | 1.3 | 1.9 | ms | |
| | Byte-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr8bers}$ | Byte-write to erased FlexRAM location execution time | — | 175 | 260 | µs | 3 |
| | Byte-write to FlexRAM execution time: | | | | | |
| $t_{eewr8b32k}$ | • 32 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr8b64k}$ | • 64 KB EEPROM backup | | 475 | 2000 | µs | |
| | Word-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr16bers}$ | Word-write to erased FlexRAM location execution time | — | 175 | 260 | µs | |
| | Word-write to FlexRAM execution time: | | | | | |
| $t_{eewr16b32k}$ | • 32 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr16b64k}$ | • 64 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Longword-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr32bers}$ | Longword-write to erased FlexRAM location execution time | — | 360 | 540 | µs | |
| | Longword-write to FlexRAM execution time: | | | | | |
| $t_{eewr32b32k}$ | • 32 KB EEPROM backup | — | 630 | 2050 | µs | |
| $t_{eewr32b64k}$ | • 64 KB EEPROM backup | — | 810 | 2250 | µs | |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 6.4.1.3 Flash high voltage current behaviors

**Table 21. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 6.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Program Flash | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | Data Flash | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | FlexRAM as EEPROM | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | |
| | Write endurance | | | | | 3 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 35 K | 175 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 315 K | 1.6 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 1.27 M | 6.4 M | — | writes | |
| $n_{nvmwree4k}$ | • EEPROM backup to FlexRAM ratio = 4096 | 10 M | 50 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ $T_j$ ≤ °C.
3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

## 6.4.2 EzPort switching specifications

**Table 23. EzPort switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion | 2 x $t_{EZP_CK}$ | — | ns |
| EP3 | $\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup) | 5 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold) | 5 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 2 | — | ns |
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 5 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid | — | | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0 | — | ns |
| EP9 | $\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

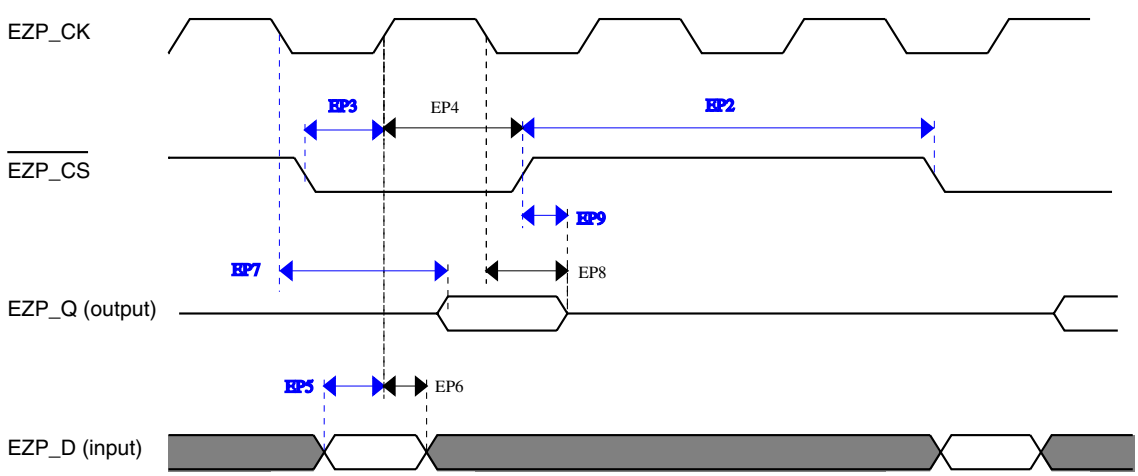



**Figure 8. EzPort Timing Diagram**

## 6.5 Security and integrity modules

### 6.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 24 and Table 25 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 6.6.1.1 16-bit ADC operating conditions

**Table 24. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 * VREFH<br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-bit / 10-bit / 12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 13-bit / 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |

*Table continues on the next page...*

## Table 24. 16-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $C_{rate}$ | ADC conversion rate | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

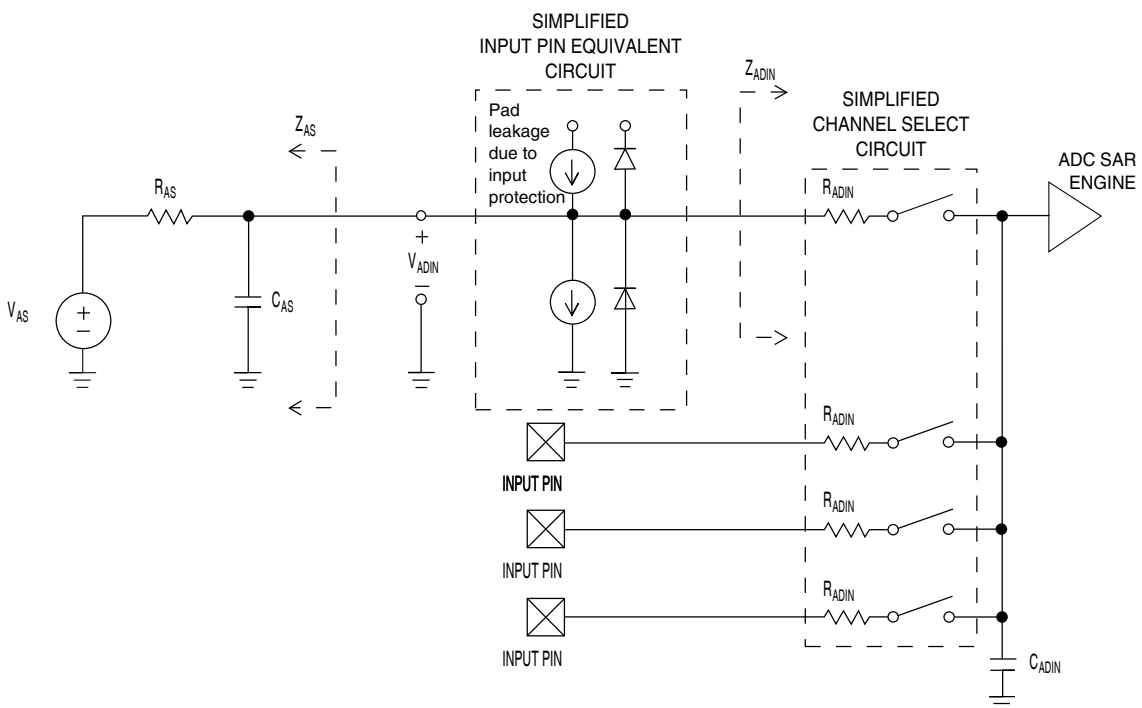



**Figure 9. ADC input impedance equivalency diagram**

### 6.6.1.2 16-bit ADC electrical characteristics

**Table 25. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)**

| Symbol | Description | Conditions[1]. | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA_ADC}$ | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| $f_{ADACK}$ | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0<br>• ADLPC = 1, ADHSC = 1<br>• ADLPC = 0, ADHSC = 0<br>• ADLPC = 0, ADHSC = 1 | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5 | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK}$ = 1/ $f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes<br>• <12-bit modes | —<br>— | ±4<br>±1.4 | ±6.8<br>±2.1 | LSB[4] | 5 |
| DNL | Differential non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±0.7<br>±0.2 | -1.1 to +1.9<br>-0.3 to 0.5 | LSB[4] | 5 |
| INL | Integral non-linearity | • 12-bit modes<br>• <12-bit modes | —<br>— | ±1.0<br>±0.5 | -2.7 to +1.9<br>-0.7 to +0.5 | LSB[4] | 5 |
| $E_{FS}$ | Full-scale error | • 12-bit modes<br>• <12-bit modes | —<br>— | -4<br>-1.4 | -5.4<br>-1.8 | LSB[4] | $V_{ADIN}$ = $V_{DDA}$<br>5 |
| $E_Q$ | Quantization error | • 16-bit modes<br>• ≤13-bit modes | —<br>— | -1 to 0<br>— | —<br>±0.5 | LSB[4] | |
| ENOB | Effective number of bits | 16-bit differential mode<br>• Avg = 32<br>• Avg = 4<br>16-bit single-ended mode<br>• Avg = 32<br>• Avg = 4 | <br>12.8<br>11.9<br><br>12.2<br>11.4 | <br>14.5<br>13.8<br><br>13.9<br>13.1 | <br>—<br>—<br><br>—<br>— | <br>bits<br>bits<br><br>bits<br>bits | 6 |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode<br>• Avg = 32<br>16-bit single-ended mode<br>• Avg = 32 | <br>—<br><br>— | <br>–94<br><br>-85 | <br>—<br><br>— | <br>dB<br><br>dB | 7 |

*Table continues on the next page...*

## Table 25. 16-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Symbol | Description | Conditions[1]. | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| SFDR | Spurious free dynamic range | 16-bit differential mode<br>• Avg = 32 | 82 | 95 | — | dB | 7 |
| | | 16-bit single-ended mode<br>• Avg = 32 | 78 | 90 | — | dB | |
| $E_{IL}$ | Input leakage error | | $I_{In} \times R_{AS}$ | | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 |
| $V_{TEMP25}$ | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

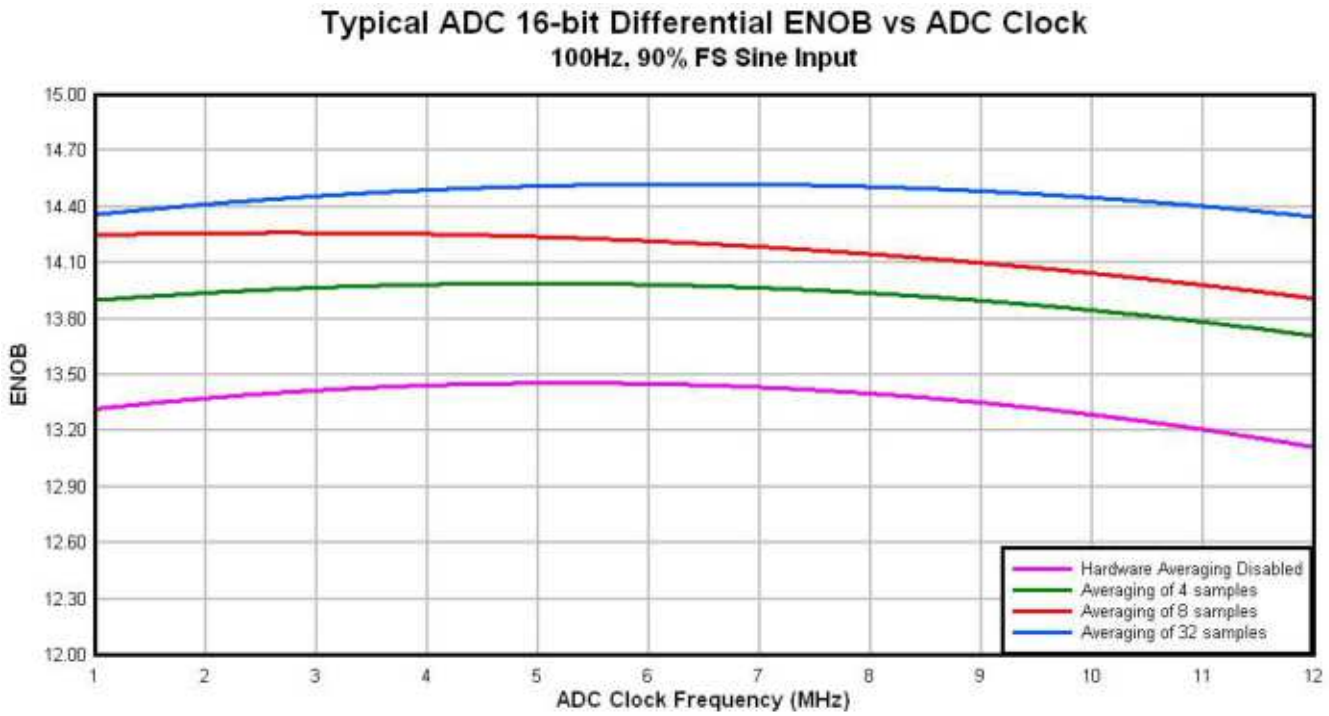



**Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

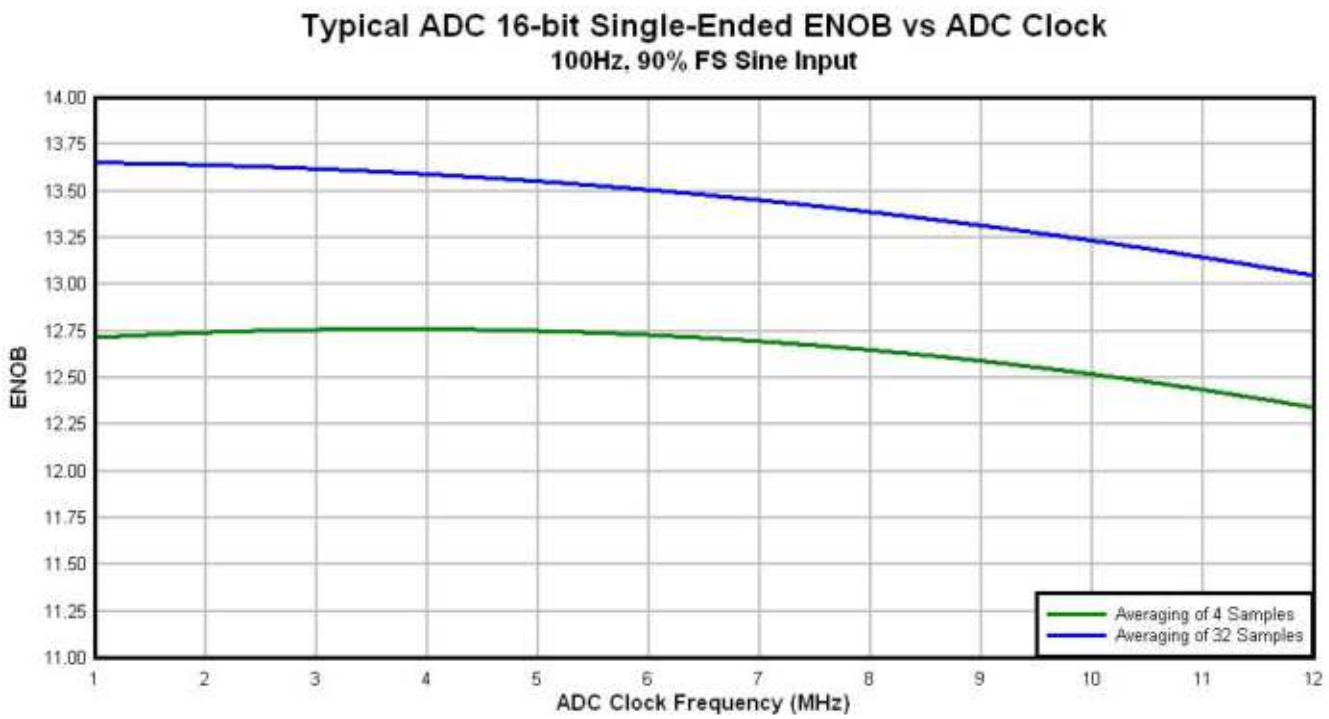



**Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

## 6.6.2 CMP and 6-bit DAC electrical specifications

### Table 26. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

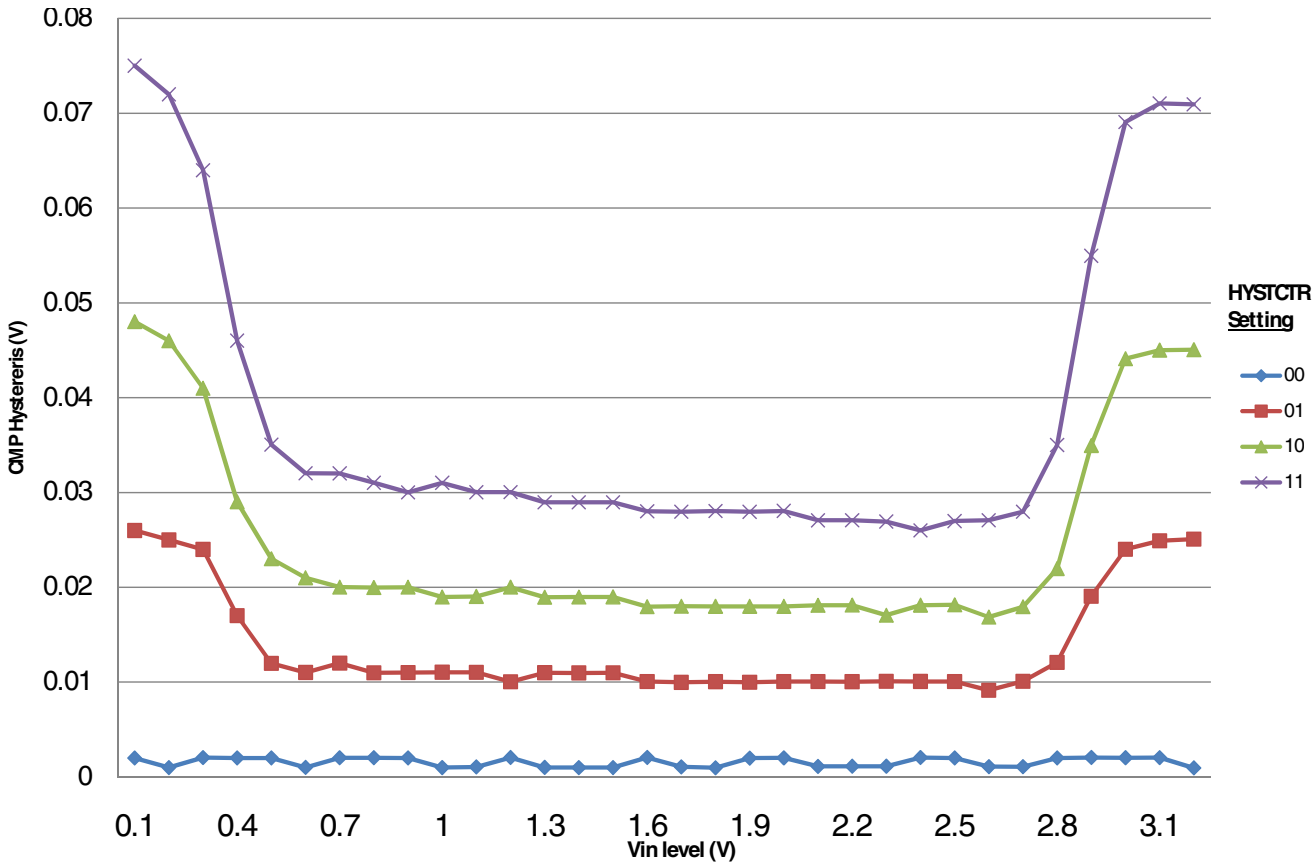



**Figure 12. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

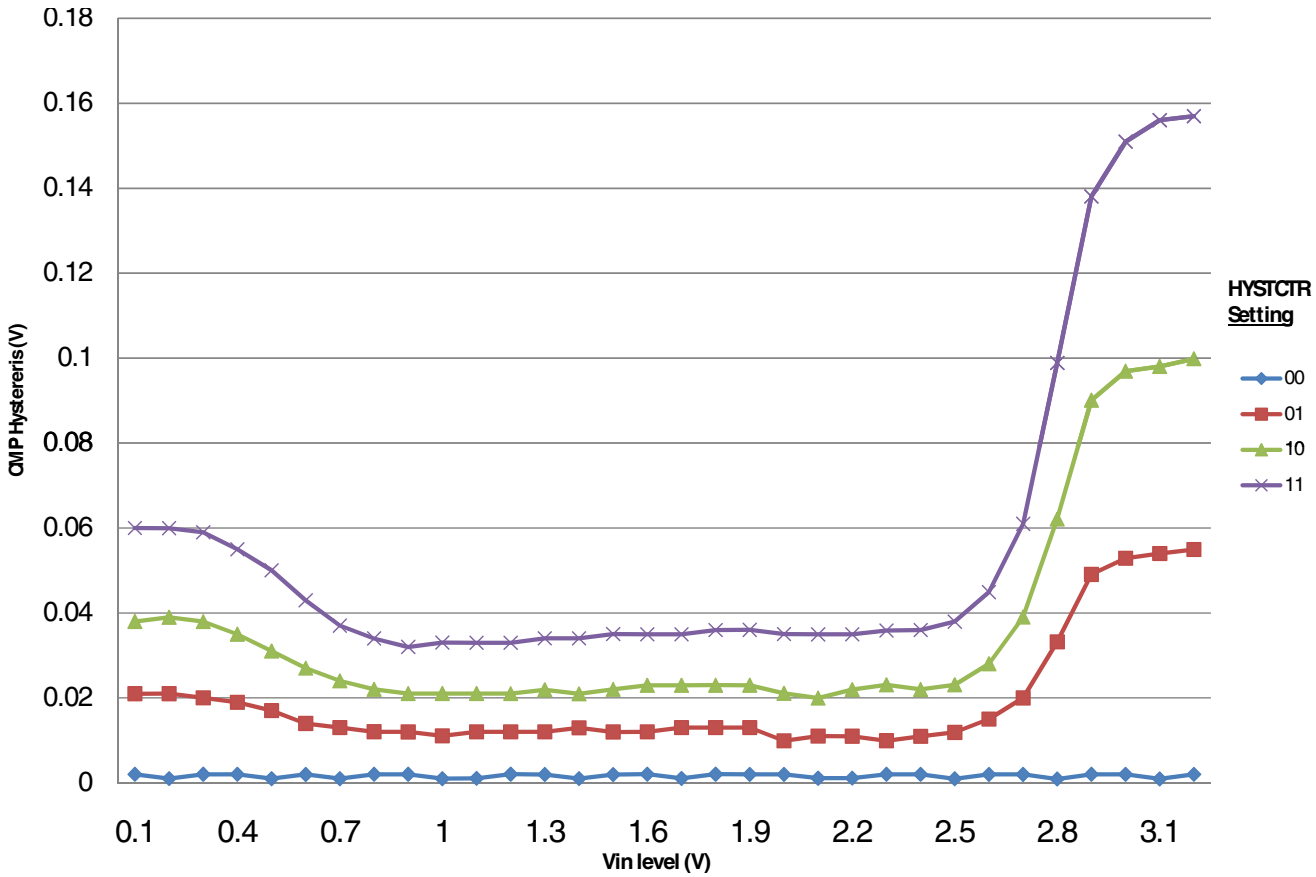



**Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

## 6.7 Timers

See General switching specifications.

## 6.8 Communication interfaces

### 6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

## 6.8.2 USB DCD electrical specifications

**Table 27. USB DCD electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DP_SRC}$ | USB_DP source voltage (up to 250 µA) | 0.5 | — | 0.7 | V |
| $V_{LGC}$ | Threshold voltage for logic high | 0.8 | — | 2.0 | V |
| $I_{DP_SRC}$ | USB_DP source current | 7 | 10 | 13 | µA |
| $I_{DM_SINK}$ | USB_DM sink current | 50 | 100 | 150 | µA |
| $R_{DM_DWN}$ | D- pulldown resistance for data pin contact detect | 14.25 | — | 24.8 | kΩ |
| $V_{DAT_REF}$ | Data detect voltage | 0.25 | 0.33 | 0.4 | V |

## 6.8.3 VREG electrical specifications

**Table 28. VREG electrical specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| VREGIN | Input supply voltage | 2.7 | — | 5.5 | V | |
| $I_{DDon}$ | Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V | — | 125 | 186 | µA | |
| $I_{DDstby}$ | Quiescent current — Standby mode, load current equal zero | — | 1.1 | 10 | µA | |
| $I_{DDoff}$ | Quiescent current — Shutdown mode<br>• VREGIN = 5.0 V and temperature=25 °C<br>• Across operating voltage and temperature | <br>—<br>— | <br>650<br>— | <br>—<br>4 | <br>nA<br>µA | |
| $I_{LOADstby}$ | Maximum load current — Standby mode | — | — | 1 | mA | |
| $V_{Reg33out}$ | Regulator output voltage — Input supply (VREGIN) > 3.6 V<br>• Run mode<br>• Standby mode | <br>3<br>2.1 | <br>3.3<br>2.8 | <br>3.6<br>3.6 | <br>V<br>V | |
| $V_{Reg33out}$ | Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode | 2.1 | — | 3.6 | V | 2 |
| $C_{OUT}$ | External output capacitor | 1.76 | 2.2 | 8.16 | µF | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | mΩ | |
| $I_{LIM}$ | Short circuit current | — | 315 | — | mA | |

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to $I_{Load}$.

## 6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 29. Master mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 25 | MHz | |
| DS1 | DSPI_SCK output cycle time | 2 x $t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns | |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | ($t_{BUS}$ x 2) – 2 | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 2 | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 15 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

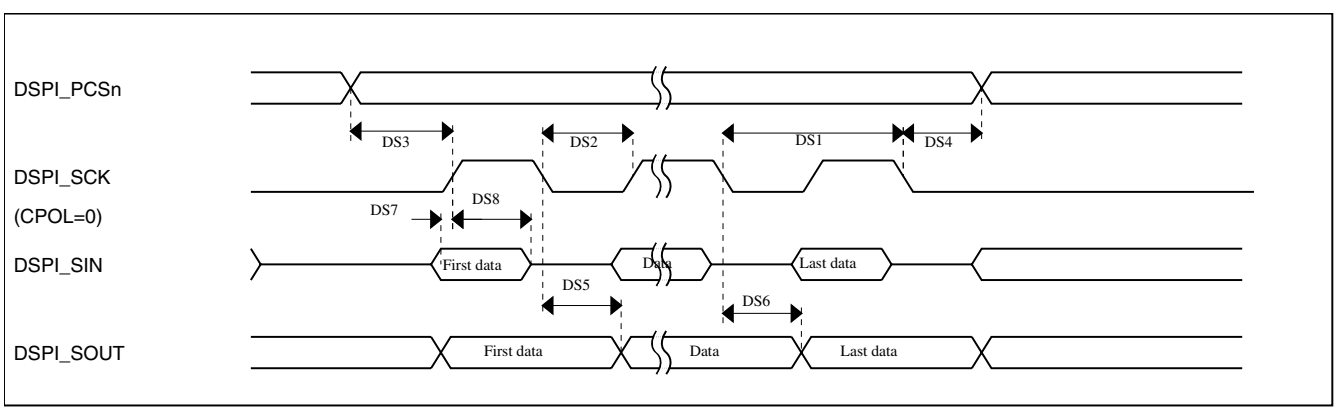



**Figure 14. DSPI classic SPI timing — master mode**

**Table 30. Slave mode DSPI timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 12.5 | MHz |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns |

*Table continues on the next page...*

**Table 30. Slave mode DSPI timing (limited voltage range) (continued)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 14 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 14 | ns |

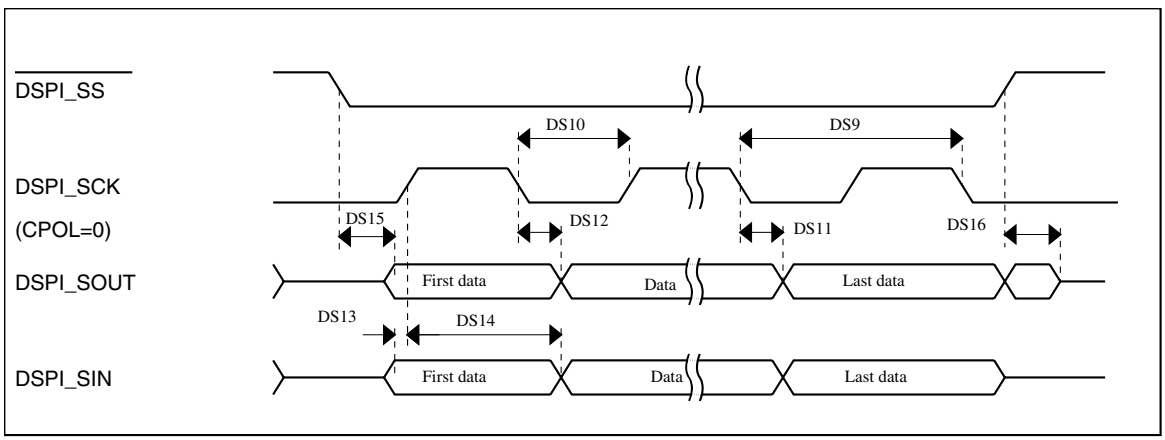



**Figure 15. DSPI classic SPI timing — slave mode**

## 6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 31. Master mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 12.5 | MHz | |
| DS1 | DSPI_SCK output cycle time | 4 x $t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2}$) + 4 | ns | |
| DS3 | DSPI_PCS*n* valid to DSPI_SCK delay | ($t_{BUS}$ x 2) – 4 | — | ns | 2 |

*Table continues on the next page...*

## Table 31. Master mode DSPI timing (full voltage range) (continued)

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| DS4 | DSPI_SCK to DSPI_PCS*n* invalid delay | ($t_{BUS}$ x 2) – 4 | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -4.5 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 20.5 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

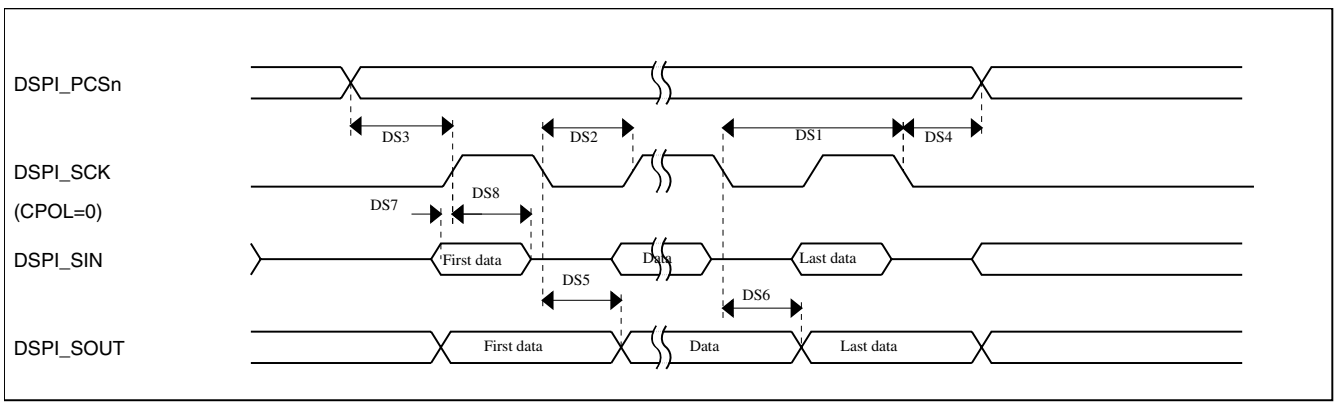



**Figure 16. DSPI classic SPI timing — master mode**

## Table 32. Slave mode DSPI timing (full voltage range)

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6.25 | MHz |
| DS9 | DSPI_SCK input cycle time | 8 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2)}$ + 4 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 20 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 19 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 19 | ns |

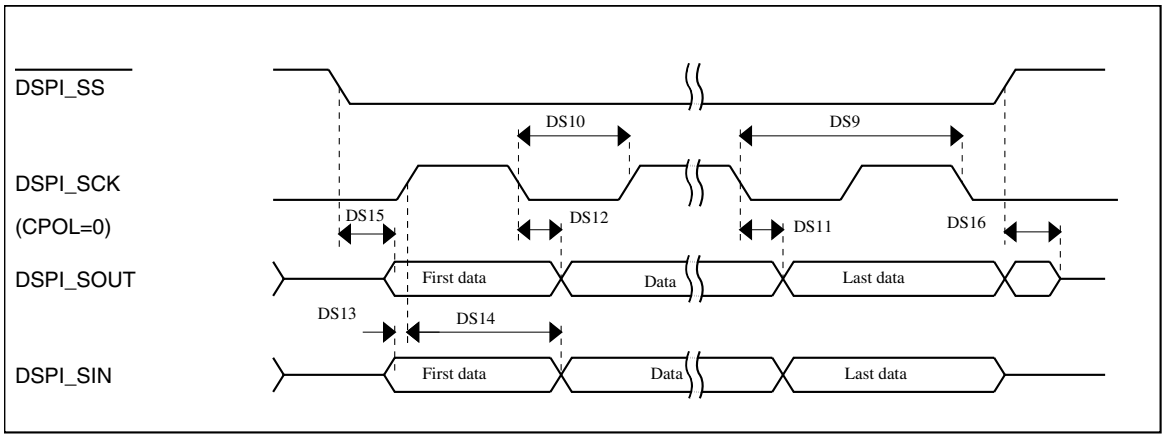



**Figure 17. DSPI classic SPI timing — slave mode**

## 6.8.6 I²C switching specifications

See General switching specifications.

## 6.8.7 UART switching specifications

See General switching specifications.

## 6.8.8 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 33. I2S/SAI master mode timing**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK (as an input) pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |

*Table continues on the next page...*

## Table 33. I2S/SAI master mode timing (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 25 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

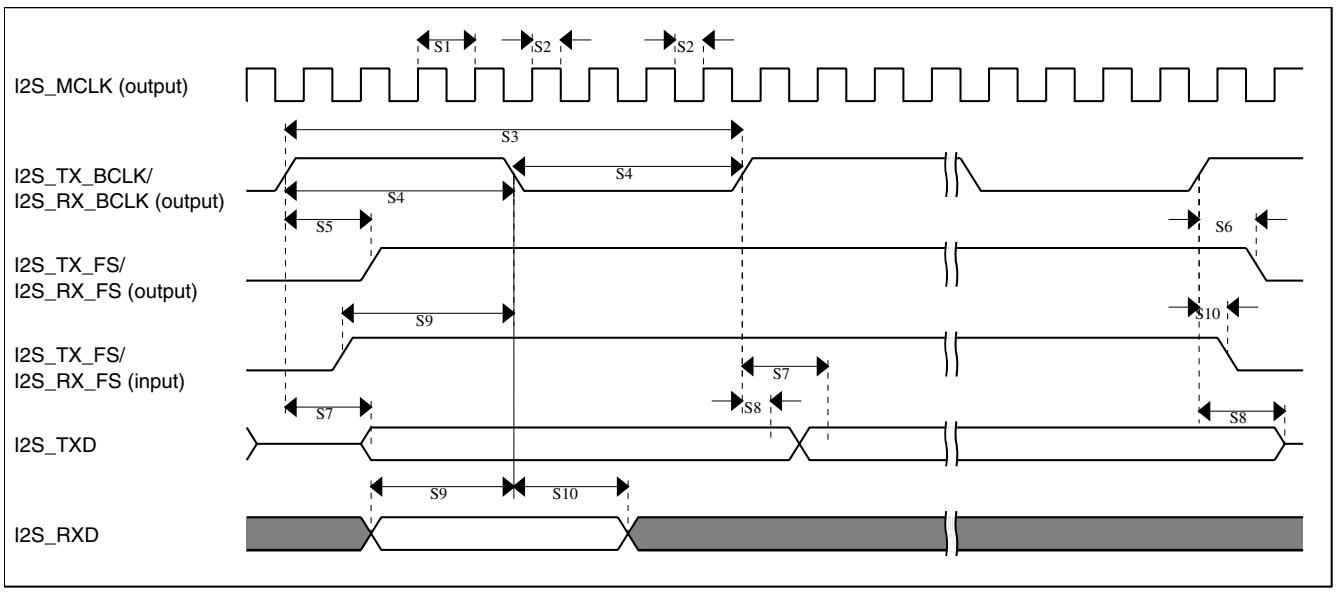



**Figure 18. I2S/SAI timing — master modes**

## Table 34. I2S/SAI slave mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 29 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 10 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 21 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

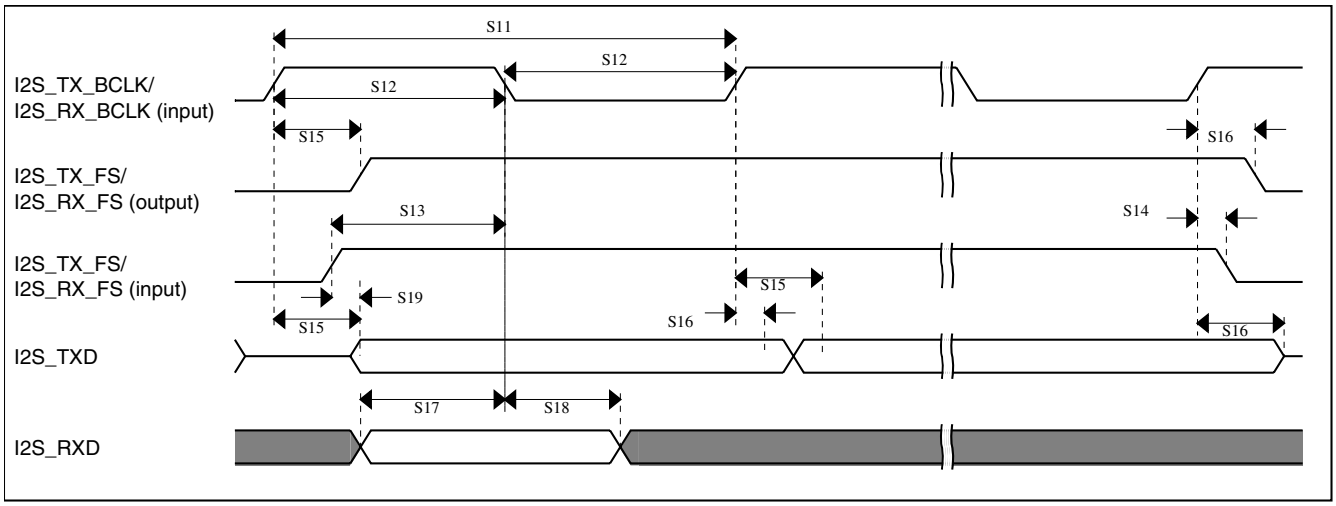



**Figure 19. I2S/SAI timing — slave modes**

## 6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 35. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 75 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

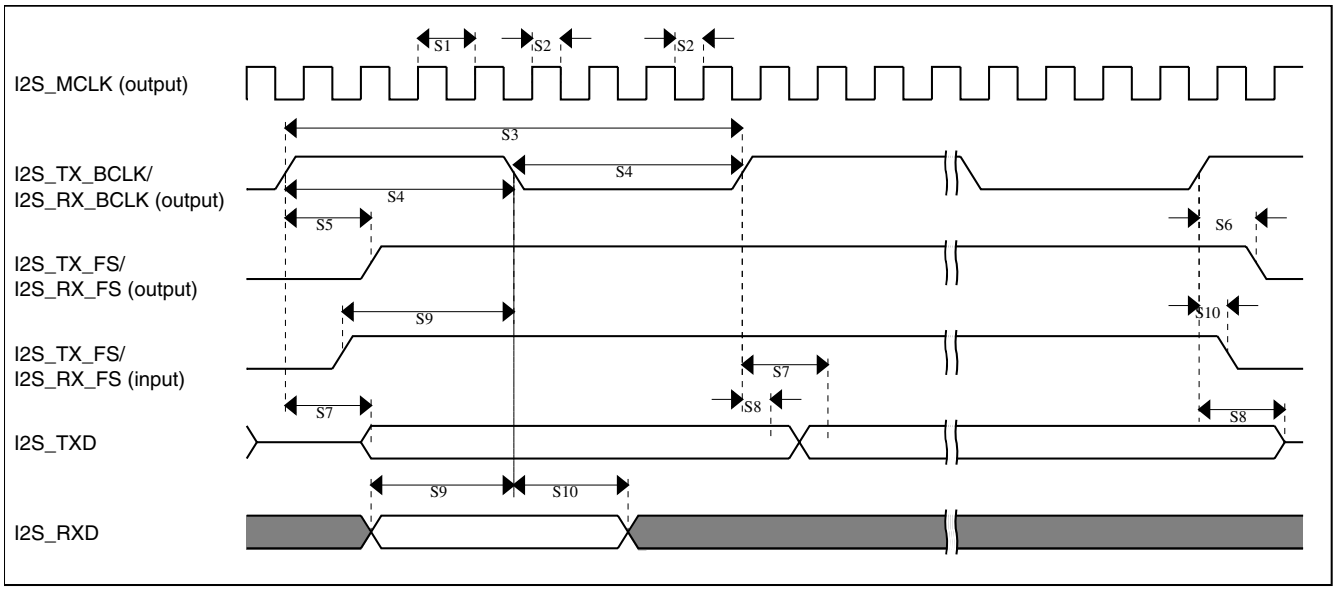



**Figure 20. I2S/SAI timing — master modes**

## Table 36. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 87 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 72 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

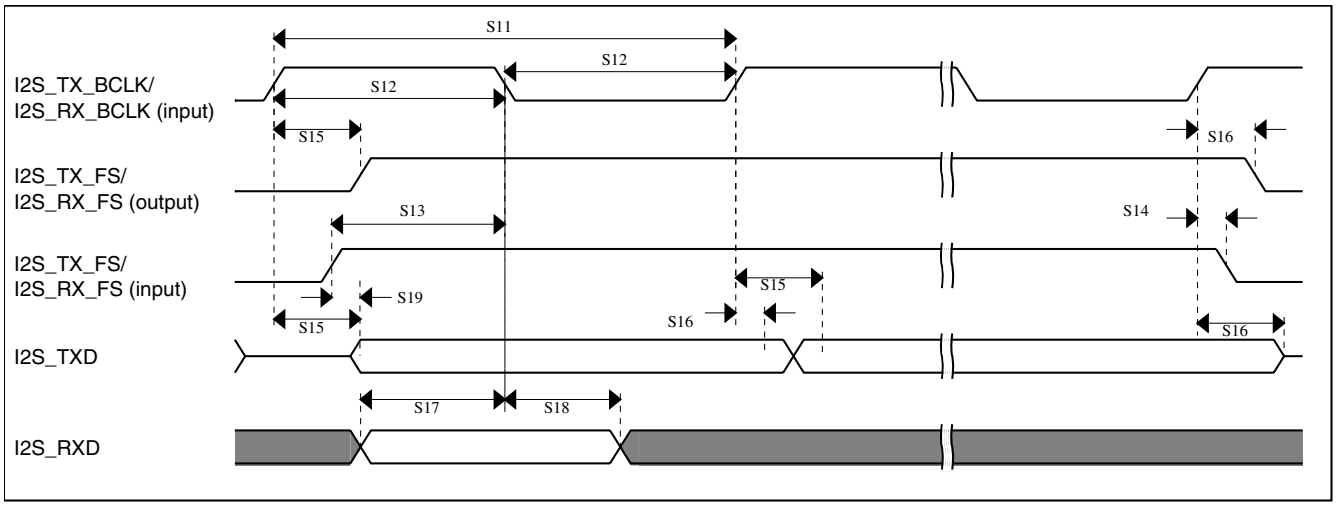



**Figure 21. I2S/SAI timing — slave modes**

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 80-pin LQFP | 98ASS23174W |

# 8 Pinout

## 8.1 K21 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**

- The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11,

K12, K21, and K22 devices and are not present on K10 and K20 devices.

- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT4, and for K22F devices, this signal is on ALT7.
- The FTM0_CH2 signal on PTC5/LLWU_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0_SCL signal on PTD2/LLWU_P13 and I2C0_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

| 80 LQFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ADC0_SE10 | ADC0_SE10 | PTE0 | SPI1_PCS1 | UART1_TX | | TRACE_CLKOUT | I2C1_SDA | RTC_CLKOUT | |
| 2 | ADC0_SE11 | ADC0_SE11 | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | | TRACE_D3 | I2C1_SCL | SPI1_SIN | |
| 3 | ADC0_DP1 | ADC0_DP1 | PTE2/ LLWU_P1 | SPI1_SCK | UART1_CTS_b | | TRACE_D2 | | | |
| 4 | ADC0_DM1 | ADC0_DM1 | PTE3 | SPI1_SIN | UART1_RTS_b | | TRACE_D1 | | SPI1_SOUT | |
| 5 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | | TRACE_D0 | | | |
| 6 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | | | | | |
| 7 | VDD | VDD | | | | | | | | |
| 8 | VSS | VSS | | | | | | | | |
| 9 | USB0_DP | USB0_DP | | | | | | | | |
| 10 | USB0_DM | USB0_DM | | | | | | | | |
| 11 | VOUT33 | VOUT33 | | | | | | | | |
| 12 | VREGIN | VREGIN | | | | | | | | |
| 13 | ADC0_DP0 | ADC0_DP0 | | | | | | | | |
| 14 | ADC0_DM0 | ADC0_DM0 | | | | | | | | |
| 15 | ADC0_DP3 | ADC0_DP3 | | | | | | | | |
| 16 | ADC0_DM3 | ADC0_DM3 | | | | | | | | |
| 17 | VDDA | VDDA | | | | | | | | |
| 18 | VREFH | VREFH | | | | | | | | |
| 19 | VREFL | VREFL | | | | | | | | |

| 80 LQFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|
| 20 | VSSA | VSSA | | | | | | | | |
| 21 | TAMPER0/ RTC_WAKEUP_ B | TAMPER0/ RTC_WAKEUP_ B | | | | | | | | |
| 22 | TAMPER1 | TAMPER1 | | | | | | | | |
| 23 | XTAL32 | XTAL32 | | | | | | | | |
| 24 | EXTAL32 | EXTAL32 | | | | | | | | |
| 25 | VBAT | VBAT | | | | | | | | |
| 26 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | | PTA0 | UART0_CTS_b/ UART0_COL_b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| 27 | JTAG_TDI/ EZP_DI | | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| 28 | JTAG_TDO/ TRACE_SWO/ EZP_DO | | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_SWO | EZP_DO |
| 29 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_RTS_b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| 30 | NMI_b/ EZP_CS_b | | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| 31 | DISABLED | | PTA5 | USB_CLKIN | FTM0_CH2 | | | I2S0_TX_BCLK | JTAG_TRST_b | |
| 32 | DISABLED | | PTA12 | | FTM1_CH0 | | | I2S0_TXD0 | FTM1_QD_PHA | |
| 33 | DISABLED | | PTA13/ LLWU_P4 | | FTM1_CH1 | | | I2S0_TX_FS | FTM1_QD_PHB | |
| 34 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | | | I2S0_RX_BCLK | I2S0_TXD1 | |
| 35 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | | | I2S0_RXD0 | | |
| 36 | DISABLED | | PTA16 | SPI0_SOUT | UART0_CTS_b/ UART0_COL_b | | | I2S0_RX_FS | I2S0_RXD1 | |
| 37 | DISABLED | | PTA17 | SPI0_SIN | UART0_RTS_b | | | I2S0_MCLK | | |
| 38 | VDD | VDD | | | | | | | | |
| 39 | VSS | VSS | | | | | | | | |
| 40 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| 41 | XTAL0 | XTAL0 | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPTMR0_ALT1 | | |
| 42 | RESET_b | RESET_b | | | | | | | | |
| 43 | ADC0_SE8 | ADC0_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_PHA | | |
| 44 | ADC0_SE9 | ADC0_SE9 | PTB1 | I2C0_SDA | FTM1_CH1 | | | FTM1_QD_PHB | | |
| 45 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | UART0_RTS_b | | | FTM0_FLT3 | | |
| 46 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | UART0_CTS_b/ UART0_COL_b | | | FTM0_FLT0 | | |
| 47 | DISABLED | | PTB10 | SPI1_PCS0 | UART3_RX | | | FTM0_FLT1 | | |
| 48 | DISABLED | | PTB11 | SPI1_SCK | UART3_TX | | | FTM0_FLT2 | | |
| 49 | DISABLED | | PTB12 | UART3_RTS_b | FTM1_CH0 | FTM0_CH4 | | FTM1_QD_PHA | | |
| 50 | DISABLED | | PTB13 | UART3_CTS_b | FTM1_CH1 | FTM0_CH5 | | FTM1_QD_PHB | | |
| 51 | DISABLED | | PTB16 | SPI1_SOUT | UART0_RX | | | EWM_IN | FTM_CLKIN0 | |

| 80 LQFP | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|
| 52 | DISABLED | | PTB17 | SPI1_SIN | UART0_TX | | | EWM_OUT_b | FTM_CLKIN1 | |
| 53 | DISABLED | | PTB18 | | FTM2_CH0 | I2S0_TX_BCLK | | | | |
| 54 | DISABLED | | PTB19 | | FTM2_CH1 | I2S0_TX_FS | | | | |
| 55 | ADC0_SE14 | ADC0_SE14 | PTC0 | SPI0_PCS4 | PDB0_EXTRG | | | I2S0_TXD1 | | |
| 56 | ADC0_SE15 | ADC0_SE15 | PTC1/ LLWU_P6 | SPI0_PCS3 | UART1_RTS_b | FTM0_CH0 | | I2S0_TXD0 | | |
| 57 | ADC0_SE4b/ CMP1_IN0 | ADC0_SE4b/ CMP1_IN0 | PTC2 | SPI0_PCS2 | UART1_CTS_b | FTM0_CH1 | | I2S0_TX_FS | | |
| 58 | CMP1_IN1 | CMP1_IN1 | PTC3/ LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | CLKOUT | I2S0_TX_BCLK | | |
| 59 | VSS | VSS | | | | | | | | |
| 60 | VDD | VDD | | | | | | | | |
| 61 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | | CMP1_OUT | | |
| 62 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | I2S0_RXD0 | | CMP0_OUT | FTM0_CH2 | |
| 63 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_SOUT | PDB0_EXTRG | I2S0_RX_BCLK | | I2S0_MCLK | | |
| 64 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | USB_SOF_OUT | I2S0_RX_FS | | | | |
| 65 | CMP0_IN2 | CMP0_IN2 | PTC8 | | | I2S0_MCLK | | | | |
| 66 | CMP0_IN3 | CMP0_IN3 | PTC9 | | | I2S0_RX_BCLK | | FTM2_FLT0 | | |
| 67 | DISABLED | | PTC10 | I2C1_SCL | | I2S0_RX_FS | | | | |
| 68 | DISABLED | | PTC11/ LLWU_P11 | I2C1_SDA | | I2S0_RXD1 | | | | |
| 69 | DISABLED | | PTC12 | | | | | | | |
| 70 | DISABLED | | PTC13 | | | | | | | |
| 71 | DISABLED | | PTC16 | | UART3_RX | | | | | |
| 72 | DISABLED | | PTC17 | | UART3_TX | | | | | |
| 73 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART2_RTS_b | | | | | |
| 74 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | UART2_CTS_b | | | | | |
| 75 | DISABLED | | PTD2/ LLWU_P13 | SPI0_SOUT | UART2_RX | I2C0_SCL | | | | |
| 76 | DISABLED | | PTD3 | SPI0_SIN | UART2_TX | I2C0_SDA | | | | |
| 77 | ADC0_SE21 | ADC0_SE21 | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_RTS_b | FTM0_CH4 | | EWM_IN | | |
| 78 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI0_PCS2 | UART0_CTS_b/ UART0_COL_b | FTM0_CH5 | | EWM_OUT_b | | |
| 79 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI0_PCS3 | UART0_RX | FTM0_CH6 | | FTM0_FLT0 | | |
| 80 | ADC0_SE22 | ADC0_SE22 | PTD7 | CMT_IRO | UART0_TX | FTM0_CH7 | | FTM0_FLT1 | | |

## 8.2 K21 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

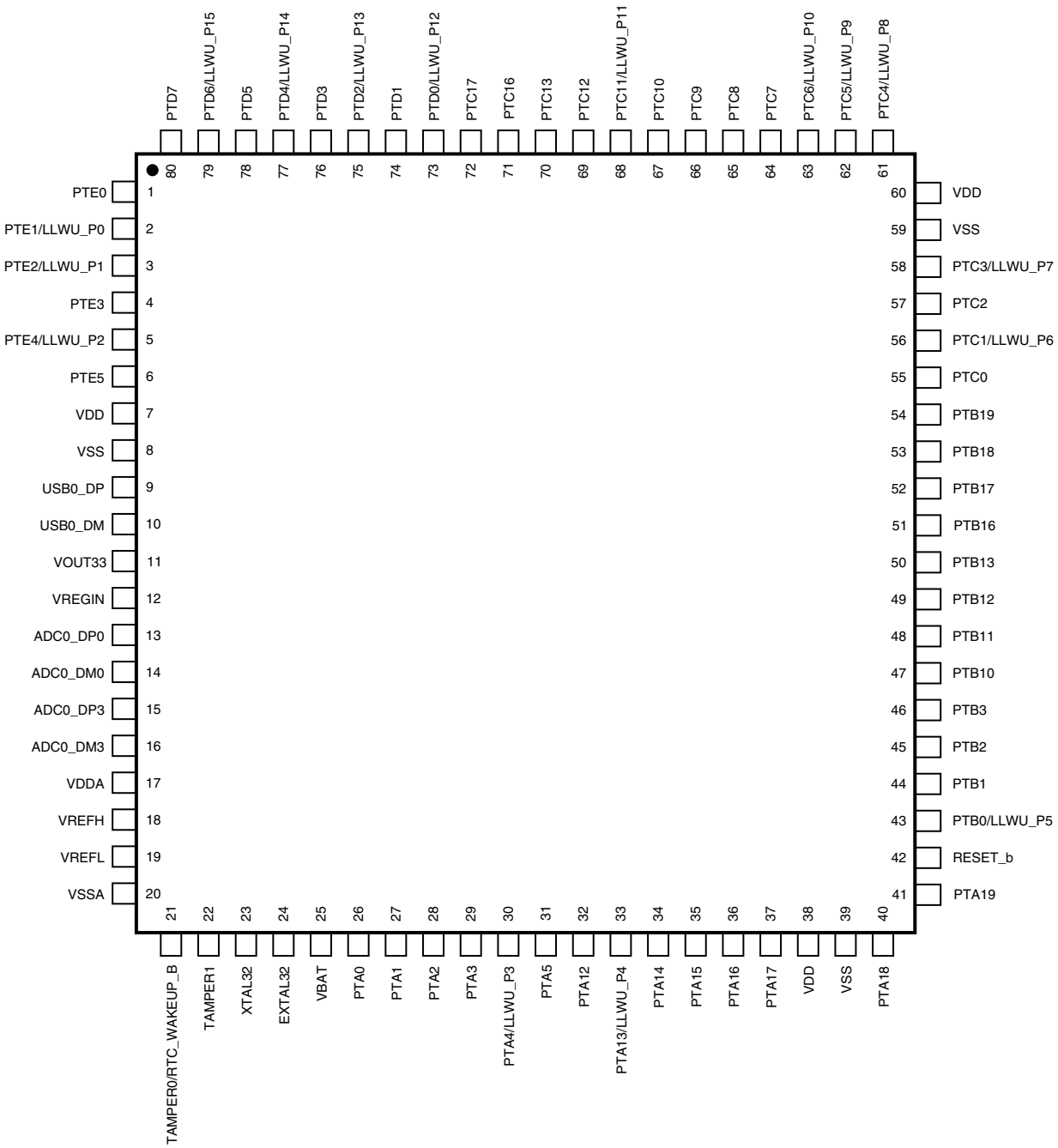



**Figure 22. K21 80 LQFP Pinout Diagram**

# 9 Revision History

The following table provides a revision history for this document.

**Table 37. Revision History**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 1 | 6/2012 | Alpha customer release. |
| 1.1 | 6/2012 | In Table 6, "Power consumption operating behaviors", changed the units of $I_{DD_VLLS2}$, $I_{DD_VLLS1}$, $I_{DD_VLLS0}$, and $I_{DD_VBAT}$ from nA to µA. |
| 2 | 7/2012 | • Updated section "Power consumption operating behaviors".<br>• Updated section "Flash timing specifications — program and erase".<br>• Updated section "Flash timing specifications — commands".<br>• Removed the 32K ratio from "Write endurance" in section "Reliability specifications".<br>• Updated IDDstby maximum value in section "VREG electrical specifications".<br>• Added the charts in section "Diagram: Typical IDD_RUN operating behavior". |
| 3 | 8/2012 | • Updated section "Power consumption operating behaviors".<br>• Updated section "EMC radiated emissions operating behaviors".<br>• Updated section "MCG specifications".<br>• Added applicable notes in section "Signal Multiplexing and Pin Assignments". |
| 4 | 12/2012 | • Updated section "Power consumption operating behaviors"<br>• Updated section "MCG specifications"<br>• Updated section "16-bit ADC operating conditions" |
| 4.1 | 08/2013 | • Added section "Small package marking"<br>• To section "MCG Specifications", added row for "Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C" |




***How to Reach Us:***

**Home Page:**
freescale.com

**Web Support:**
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale, the Freescale logo, Energy Efficient Solutions logo, and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM and Cortex are the registered trademarks of ARM Limited.
© 2012-2013 Freescale Semiconductor, Inc.

Document Number: K21P80M50SF4
Rev. 4.1
08/2013

