# 3A, 2.4MHz, Low-Voltage, I²C Programmable Buck Regulator

## Features

- 2.7 to 5.5V Input Voltage Range
- 0.6 to 3.345V Programmable Output Voltage
  - 6.25mV steps below 1.39375V
  - 15mV steps above 1.44V
- 3.0A Output Current
- ±1% Accuracy at $T_A$ = +25°C
  - ±2.5% over line/load/temp/setting
- Fast Transient Response
- Dynamic Voltage Scaling (DVS) with 8 ramp rates
- Soft-Start with 10 ramp rates
- 89% Peak Efficiency at Vout = 1.15625V
- 2.4MHz with Auto-Skip at light loads
  - Programmable forced-PWM mode
- 48uA typ. No-Load Supply Current in Skip Mode
- Tiny External Components
  - L = 330 or 470nH (2012 or 2016 metric size)
  - Cin = 10µF (0402), Cout = 2x22µF (2x0402)
- Over-Current, Short-Circuit, Under/Over-$V_{IN}$, and Thermal Shutdown Protections
- 1MHz I²C Interface
- Open-Drain $\overline{IRQ}$ Output Flag
- -40°C to 85°C Operating Temperature Range
- 15-bump Pb-free WLCSP (0.4mm pitch)
  - 1.340 x 2.045mm (0.6mm height)
  - Pin/Register Compatible with FAN53526

## Brief Description

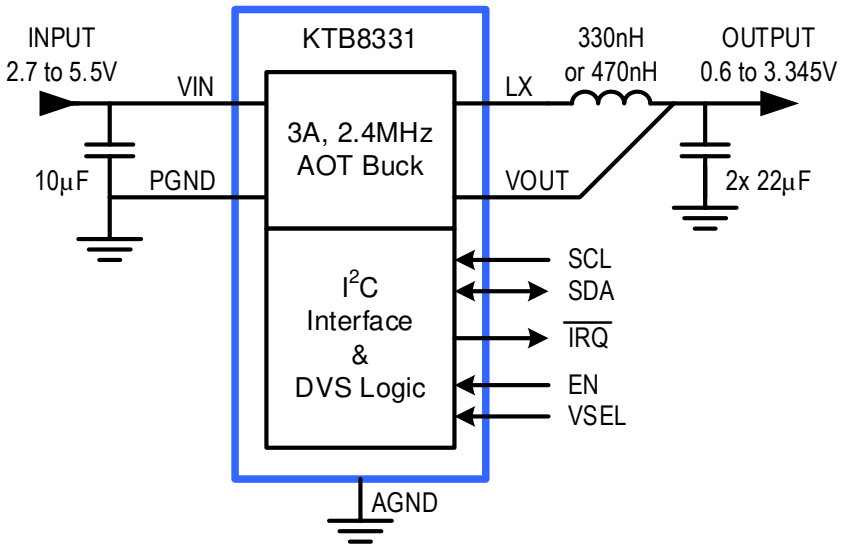
The KTB8331 is a precision adaptive-on-time (AOT) buck switching regulator with class-leading accuracy, transient response, efficiency, and solution size optimized for mobile and non-mobile application. It is I²C programmable for output voltages in the 0.6V to 3.345V range. It features soft-start and DVS with multiple programmable ramp rates. Versions with various default settings can be ordered. The features and performance make the KTB8331 suitable for a variety of applications including CPU/GPU core, DSP and baseband, DDR memory, VIO, and sensor/analog power.

The KTB8331 is available in RoHS and Green compliant 15-bump 1.340mm x 2.045mm x 0.6mm wafer-level chip-scale package (WLCSP).

## Applications

- CPU, GPU, AP, DSP, FPGA, I/O, XCVR Power
- HDD, LPDDR3, LPDDR4 Memory Power
- Tablets, Netbooks, Ultra-Books
- Smartphones, Mobile Internet Devices, IoT
- DSC, Drones, Gaming Consoles, Accessories

## Typical Application Schematic

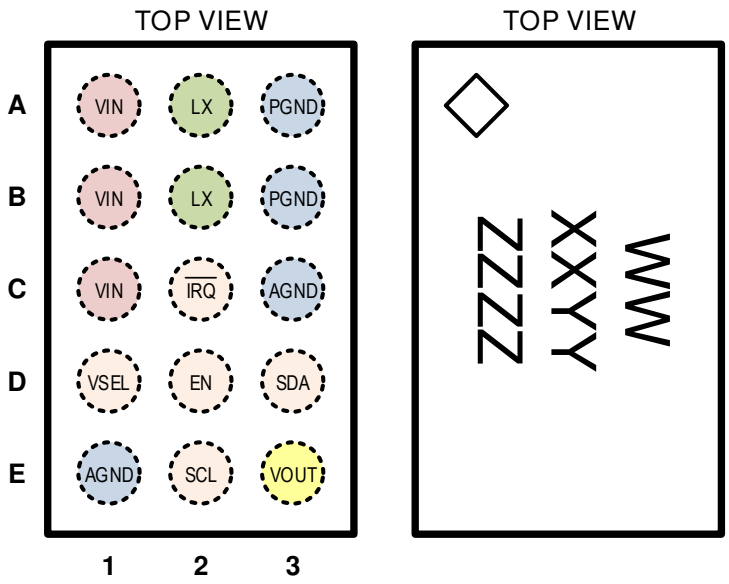


## Pin Descriptions

| Pin # | Name | Function |
|---|---|---|
| A1, B1, C1 | VIN | Voltage Input for buck regulator and IC power |
| A3, B3 | PGND | Power Ground for buck regulator |
| C3, E1 | AGND | Analog Ground for IC power |
| A2, B2 | LX | Inductor Connection for buck regulator |
| E3 | VOUT | Output Voltage sense input |
| D2 | EN | Chip Enable logic input |
| E2 | SCL | $I^2C$ Clock digital input |
| D3 | SDA | $I^2C$ Data digital I/O |
| C2 | $\overline{IRQ}$ | Interrupt Request open-drain output. If not used, tie to AGND or PGND. |
| D1 | VSEL | DVS Voltage Select and Auto-Skip vs. Forced-PWM Mode Select logic input |

## Pinout Diagram

**WLCSP-15**




15-Bump 1.340mm x 2.045mm x 0.62mm
WLCSP Package, 0.4mm pitch

**Top Mark**
WW = Device Code,
XX = Date Code, YY = Assembly Code,
ZZZZ = Serial Number

## Absolute Maximum Ratings[1]

($T_A$ = 25°C unless otherwise noted)

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{IN}$ | VIN to AGND | -0.3 to 6 | V |
| $V_{PGND}$ | PGND to AGND | -0.3 to 0.3 | V |
| $V_{LX}$[2] | LX to PGND | -0.3 to ($V_{IN}$+0.3) | V |
| $V_{OUT}$ | VOUT to AGND | -0.3 to ($V_{IN}$+0.3) | V |
| $V_{IO}$ | SCL, SDA, VSEL to AGND | -0.3 to 6 | V |
| | EN, $\overline{IRQ}$ to AGND | -0.3 to $V_{IN}$ | V |
| $I_{LX}$ | LX Continuous Current | 3.2 | $A_{RMS}$ |
| | LX Peak Current (1ms maximum) | 9.6 | $A_{PEAK}$ |
| $T_J$ | Operating Junction Temperature Range | -40 to 150 | °C |
| $T_S$ | Storage Temperature Range | -55 to 150 | °C |
| $T_{LEAD}$ | Maximum Soldering Temperature (at leads, 10 sec) | 260 | °C |

## ESD Ratings[3]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{ESD_HBM}$ | JEDEC JS-001-2017 ESD Human Body Model (all pins) | ±2 | kV |

## Thermal Capabilities[4]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance – Junction to Ambient | 77 | °C/W |
| $P_D$ | Maximum Power Dissipation at $T_A$ = 25°C | 1.62 | W |
| $\Delta P_D/\Delta_T$ | Derating Factor Above $T_A$ = 25°C | -13 | mW/°C |

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Absolute Maximum Rating for VLX is a DC voltage rating. During normal switching operation, short-duration voltage spikes beyond the DC rating are expected and normal for all DC-DC switching regulators.
3. ESD Ratings conform to JEDEC industry standards. Some pins may actually have higher performance.
4. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

## Ordering Information

| Part Number[5] | Marking[6] | Default Output Voltage & Mode[7] | | 7-bit I²C Slave Address | Package |
|---|---|---|---|---|---|
| | | (VSEL = 1) | (VSEL = 0) | | |
| KTB8331AEDAA-TR | QKXXYYZZZZ | 1.15625V Forced-PWM | 1.15625V Auto-Skip | 1100 000=0x60h | WLCSP15 |
| *KTB8331BEDAA-TR* | *QLXXYYZZZZ* | *3.300V Forced-PWM* | *3.150V Auto-Skip* | *1100 000=0x60h* | *WLCSP15* |
| *KTB8331CEDAA-TR* | *QMXXYYZZZZ* | *1.000V Forced-PWM* | *0.900V Auto-Skip* | *1100 000=0x60h* | *WLCSP15* |
| KTB8331DEDAA-TR | QNXXYYZZZZ | 0.600V Forced-PWM | 0.600V Auto-Skip | 1010 000=0x50h | WLCSP15 |
| KTB8331EEDAA-TR | QOXXYYZZZZ | 1.125V Forced-PWM | 1.125V Auto-Skip | 1010 111=0x57h | WLCSP15 |
| KTB8331FEDAA-TR | QUXXYYZZZZ | 0.950V Forced-PWM | 0.950V Auto-Skip | 1010 000=0x50h | WLCSP15 |
| KTB8331GEDAA-TR | QVXXYYZZZZ | 1.800V Forced-PWM | 1.800V Auto-Skip | 1010 000=0x50h | WLCSP15 |
| KTB8331HEDAA-TR | QWXXYYZZZZ | 3.300V Forced-PWM | 3.300V Auto-Skip | 1010 000=0x50h | WLCSP15 |
| KTB8331JEDAA-TR | RAXXYYZZZZ | 0.750V Forced-PWM | 0.750V Auto-Skip | 1010 001=0x51h | WLCSP15 |
| KTB8331KEDAA-TR | RBXXYYZZZZ | 1.200V Forced-PWM | 1.200V Auto-Skip | 1100 000=0x60h | WLCSP15 |
| KTB8331LEDAA-TR | RCXXYYZZZZ | 1.05V Forced-PWM | 1.05V Auto-Skip | 1100 000=0x60h | WLCSP15 |
| KTB8331MEDAA-TR | RJXXYYZZZZ | 1.081V Auto-Skip | 1.125V Auto-Skip | 1100 000=0x60h | WLCSP15 |

5. For part numbers in *Italic*, please contact your local sales representative for availability.

6. “WW” is the device ID, “XX” is the date code, “YY” is the assembly code, and “ZZZZ” is the serial number.

7. For part numbers in *Italic*, please contact your local sales representative for availability.

## Electrical Characteristics[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and $V_{IN}$ = 2.7V to 5.5V. *Typ* values are specified at +25°C with $V_{IN}$ = 3.6V.

### Supply Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Supply Operating Range | | 2.7 | | 5.5 | V |
| $V_{UVLO}$ | Under-Voltage Lockout Threshold | $V_{IN}$ rising<br>$V_{IN}$ hysteresis | 2.4 | 2.55<br>200 | 2.7 | V<br>mV |
| $V_{OVP}$ | Over-Voltage Protection Threshold | $V_{IN}$ rising | 5.5 | 5.75 | 5.9 | V |
| | | $V_{IN}$ hysteresis | | 200 | | mV |
| $I_{IN}$ | No-Load Supply Current | EN = 1, $V_{IN}$ = 3.6V, $V_{OUT}$ ≤2.5V, Skip | | 48 | 80 | µA |
| | | EN = 1, $V_{IN}$ = 3.6V, Forced-PWM | | 16 | | mA |
| $I_{SHDN}$ | Shutdown Supply Current | EN = 0, $T_A$ = 25°C | | 0.2 | 1 | µA |
| | | EN = 1, ENn[0]=0, $T_A$ = 25°C | | 0.2 | 1.5 | µA |

### Logic Pin Specifications (EN, VSEL, $\overline{IRQ}$)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input Logic High (EN, VSEL) | | 1.15 | | | V |
| $V_{IL}$ | Input Logic Low (EN, VSEL) | | | | 0.4 | V |
| $I_{I_LK}$ | Input Logic Leakage (EN, VSEL) | $T_A$ = 25°C, $V_I$ = 0V or $V_{IN}$ | -1 | ±0.01 | 1 | µA |
| $R_{I_PD}$ | Input Logic Pull-Down (EN, VSEL) | only connected when $V_I \le V_{IL}$<br>(disconnected when $V_I \ge V_{IH}$) | | 250 | | kΩ |
| $V_{OL}$ | Output Logic Low ($\overline{IRQ}$) | $I_{O_SINK}$ = 1mA | | 0.18 | 0.4 | V |
| $I_{O_LK}$ | Output Logic Leakage ($\overline{IRQ}$) | $T_A$ = 25°C, $V_O$ = high-Z or $V_{IN}$ | | 0.01 | 1 | µA |

### Thermal Shutdown Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{J_SHDN}$ | IC Junction Thermal Shutdown[9] | $T_J$ rising | | 140 | | °C |
| | | Hysteresis | | 20 | | °C |

(continued next page)

8. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

9. Guaranteed by design, characterization and statistical process control methods; not production tested.

## Electrical Characteristics (continued)[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and $V_{IN}$ = 2.7V to 5.5V. *Typ* values are specified at +25°C with $V_{IN}$ = 3.6V.

### I²C-Compatible Interface Specifications (SCL, SDA), see Figure 1

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input Logic High Threshold | | 1.1 | | | V |
| $V_{IL}$ | Input Logic Low Threshold | | | | 0.4 | V |
| $V_{OL}$ | SDA Output Logic Low | $I_{SDA}$ = 3mA | | | 0.4 | V |
| $t_1$ | SCL clock period[9] | | 2.5 | | | µs |
| $t_2$ | Data in setup time to SCL high[9] | | 100 | | | ns |
| $t_3$ | Data out stable after SCL low[9] | | 0 | | | ns |
| $t_4$ | SDA low setup time to SCL low (Start)[9] | | 100 | | | ns |
| $t_5$ | SDA high hold time after SCL high (Stop)[9] | | 100 | | | ns |

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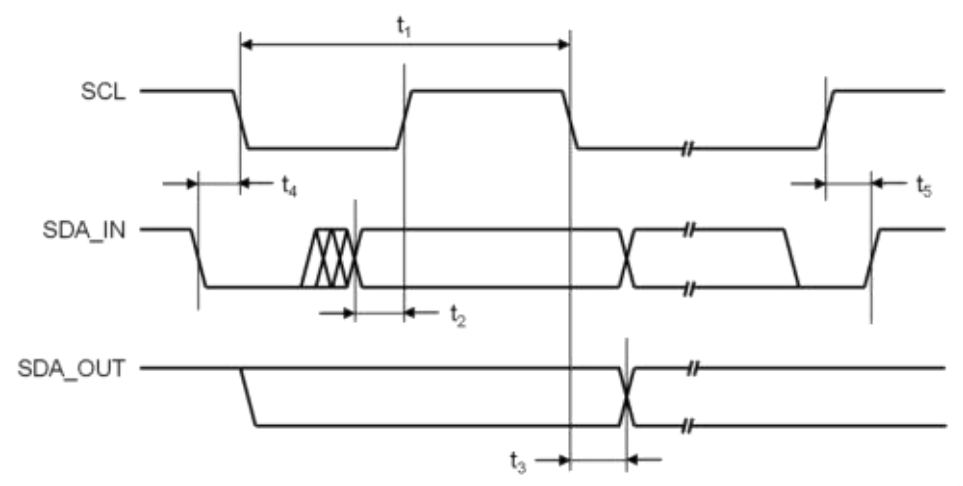



**Figure 1. I²C Compatible Interface Timing**

## Electrical Characteristics (continued)[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and $V_{IN}$ = 2.7V to 5.5V. *Typ* values are specified at +25°C with $V_{IN}$ = 3.6V.

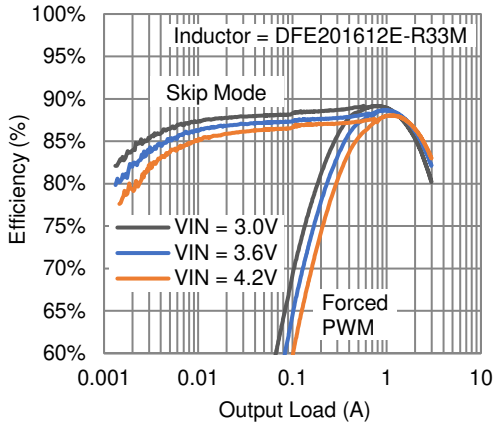
### Buck Regulator Specifications

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage Setting Range | Low Range (G=1), RANGE[0]=0 | 0.600 | | 1.39375 | V |
| | | High Range (G=2.4), RANGE[0]=1 | 1.440 | | 3.345 | V |
| $V_{OUT_STEP}$ | Output Voltage Setting Step Size | Low Range (G=1), RANGE[0]=0 | | 6.25 | | mV |
| | | High Range (G=2.4), RANGE[0]=1 | | 15 | | mV |
| $V_{OUT_ACC}$ | Output Voltage DC Accuracy | $T_A$ = 25°C, $V_{OUT}$ = 1.15625V, FPWM | -1 | ±0.2 | 1 | % |
| | | FPWM over line/load/temp/setting | -2.5 | ±1 | 2.5 | % |
| | | Auto-Skip over line/setting | | ±1 | | % |
| $V_{OUT_LOAD}$ | Output Voltage Load Regulation[9] | $I_{LOAD}$ = 1A to 3A, FPWM | | -0.01 | | %/A |
| $V_{OUT_LINE}$ | Output Voltage Line Regulation[9] | $V_{IN}$ = 2.7V to 5.5V, $I_{LOAD}$ = 1.5A | | ±0.01 | | %/V |
| $V_{OUT_TRAN}$ | Output Voltage Transient Response[9] | $I_{LOAD}$ = 10mA↔1.5A, $t_r = t_f$ = 200ns, $V_{OUT}$ = 1.15625V | | ±50 | | mV |
| $I_{OUT_MAX}$ | Maximum Output Current | | 3 | | | A |
| $I_{LX_PEAK}$ | LX Peak Current Limit | | 4 | 4.6 | 5.5 | A |
| $I_{LX_VALLEY}$ | LX Valley Current Limit | | 3 | 4.3 | 5.5 | A |
| $I_{LX_LEAK}$ | LX Leakage Current | $V_{LX}$ = 0V or 5.5V, $T_A$ = 25°C | | 0.1 | 1 | µA |
| $R_{DSON_MS}$ | Main Switch On-Resistance | MOSFET + metal + bumps | | 50 | | mΩ |
| $R_{DSON_SR}$ | Synch. Rectifier On-Resistance | MOSFET + metal + bumps | | 30 | | mΩ |
| $R_{LX_DIS}$ | LX Active Discharge Resistance | EN = 0 or ENn[0] = 0, DIS[0] = 1 | | 133 | | Ω |
| $t_{SS_DELAY}$ | Soft-Start Ramp Delay[9] | Hardware enable, EN=0→1 | | 350 | | µs |
| | | Software enable, ENn[0] = 0→1 | | 315 | | µs |
| $dV/dt_{SS}$ | Soft-Start Ramp Rates | 10 programmable rates | 1.5625 | | 30 | mV/µs |
| $t_{DVS_DELAY}$ | DVS Ramp Delay[9] | Hardware DVS, VSEL = 0↔1 | | 3 | | µs |
| | | Software DVS, by I²C command | | <10 | | µs |
| $dV/dt_{DVS}$ | DVS Ramp Rates | 8 programmable rates | 3.125 | | 25 | mV/µs |
| $V_{OUT_POK}$ | $V_{OUT}$ Power OK Threshold | Percentage of $V_{OUT}$ setting, falling | | 88 | | % |
| | | Percentage of $V_{OUT}$ setting, rising | | 92 | | % |

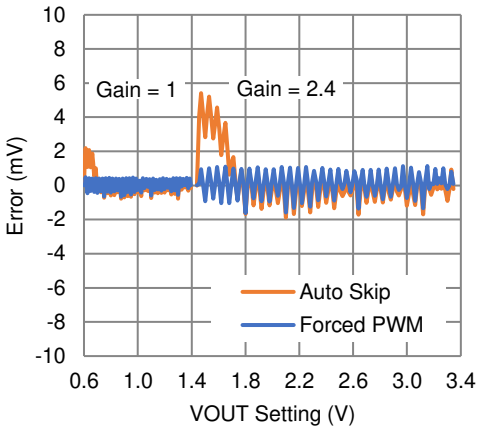
## Typical Characteristics

Unless otherwise noted, $V_{IN}$ = $V_{EN}$ = 3.6V, L = 330nH, $C_{IN}$ = 10µF, $C_{OUT}$ = 2x 22µF, and $T_A$ = 25°C.

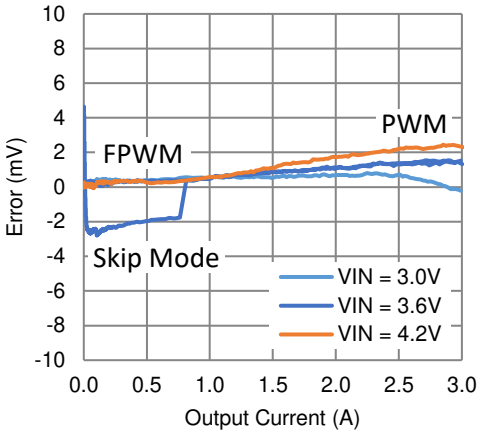
**Efficiency vs. Load at $V_{OUT}$ = 1.15625V**



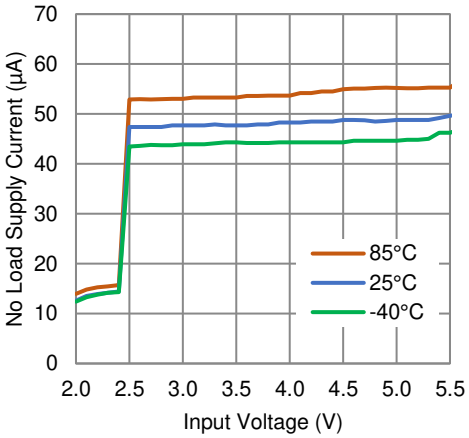

**$V_{OUT}$ Accuracy vs. $V_{OUT}$ Setting**
($I_{OUT}$ = 10mA)



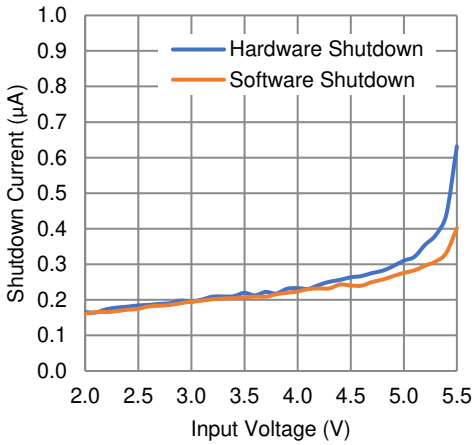

**$V_{OUT}$ Accuracy vs. Load**
($V_{OUT}$ = 1.15625V)



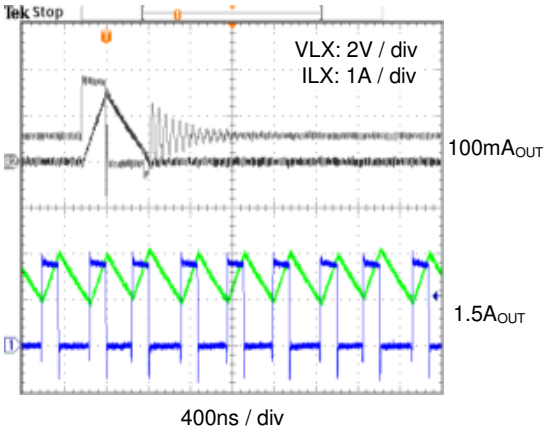

**Supply Current vs. $V_{IN}$**
($V_{OUT}$ = 1.15625V, No Load, Mode = Auto)




**Shutdown Supply Current vs. $V_{IN}$**



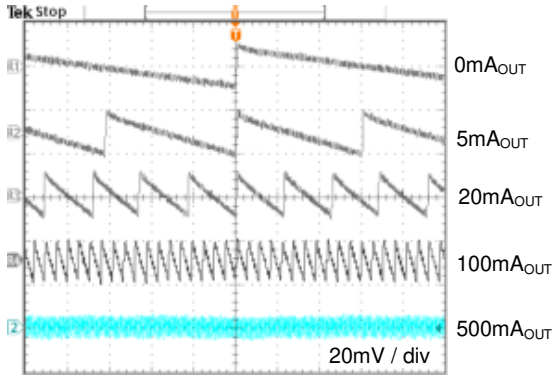

**$V_{LX}$ and $I_{LX}$ Switching Waveforms**
($V_{OUT}$ = 1.15625V, Mode = Auto)



## Typical Characteristics (continued)

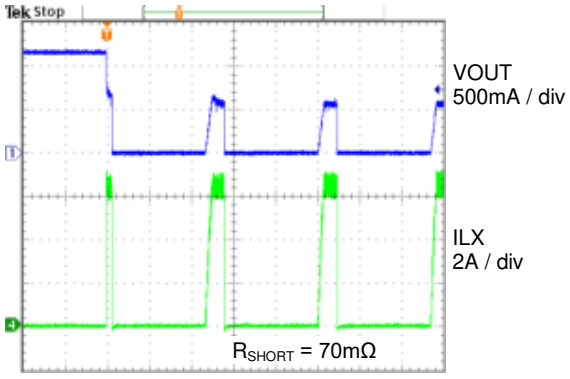
Unless otherwise noted, $V_{IN}$ = $V_{EN}$ = 3.6V, L = 330nH, $C_{IN}$ = 10µF, $C_{OUT}$ = 2x 22µF, and $T_A$ = 25°C.

**$V_{OUT}$ Ripple Waveforms**
($V_{OUT}$ = 1.15625V, Mode = Auto)




20µs / div

**Short-Circuit Protection**

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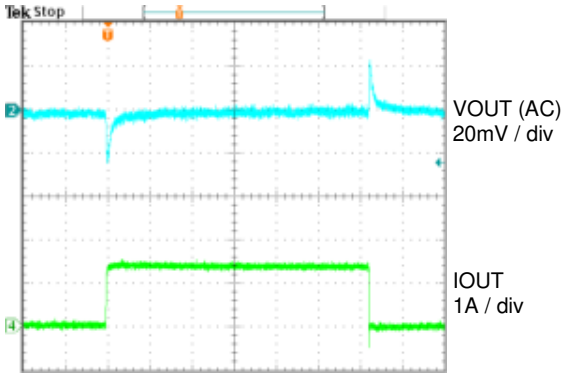
**Load Transient Response**
($V_{OUT}$ = 1.15625V, Load = 10mA-1.5A, Mode = FPWM)

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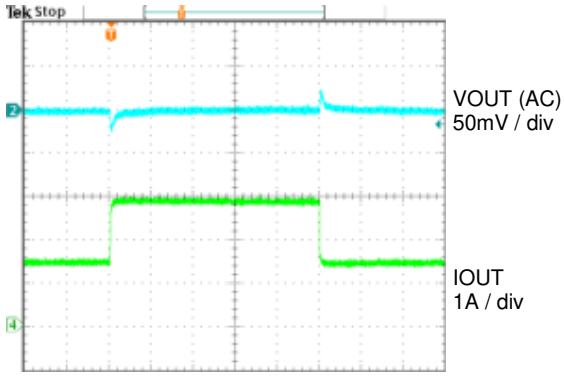
**Load Transient Response**
($V_{OUT}$ = 1.15625V, Load = 1.5A-3A, Mode = Auto)

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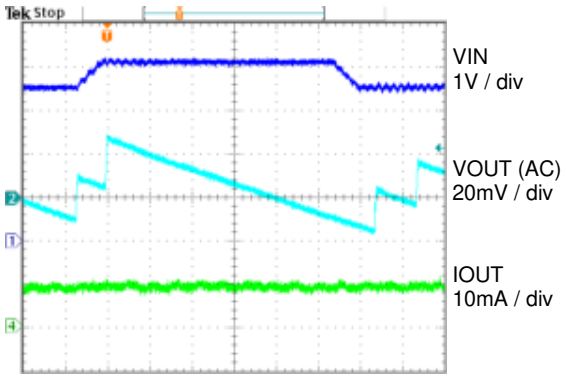
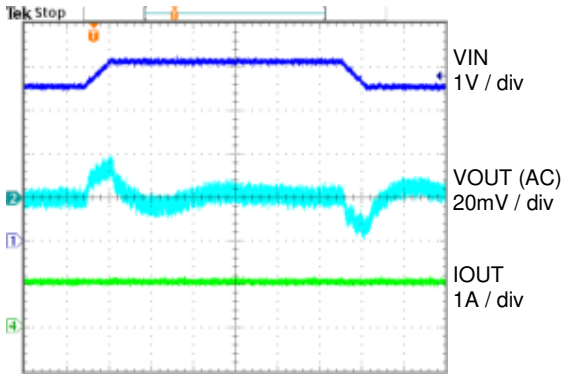
**Line Transient Response**
($V_{OUT}$ = 1.15625V, Mode = Auto)




20µs / div

**Line Transient Response**
($V_{OUT}$ = 1.15625V, Mode = FPWM)

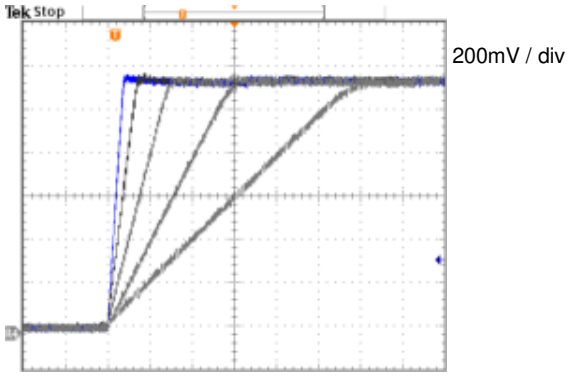



20µs / div

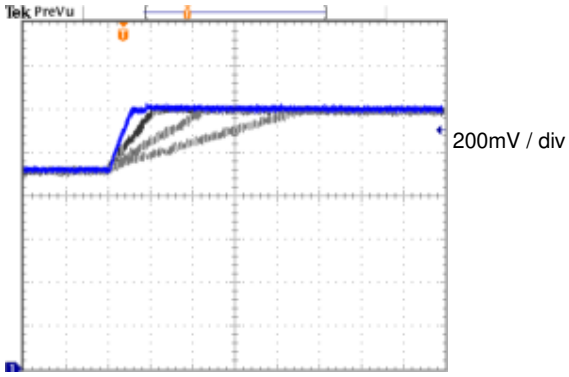
## Typical Characteristics (continued)

Unless otherwise noted, $V_{IN}$ = $V_{EN}$ = 3.6V, L = 330nH, $C_{IN}$ = 10µF, $C_{OUT}$ = 2x 22µF, and $T_A$ = 25°C.

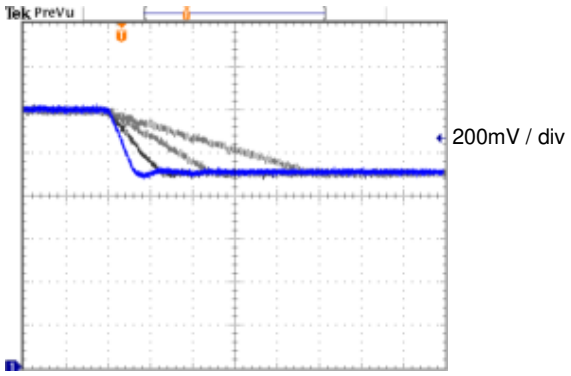
**Buck Enable Soft-Start Rates**
($V_{OUT}$ = 1.15625V)



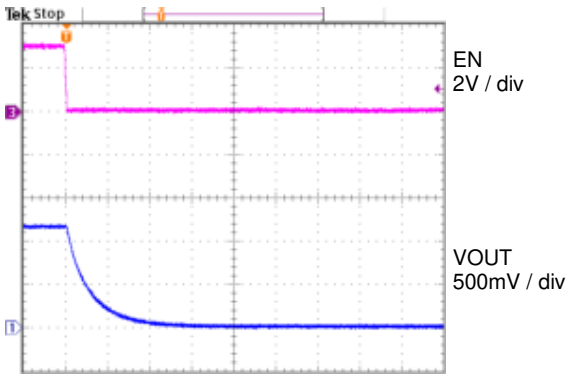

**DVS Positive Ramp-Up Rates**
($V_{OUT}$ = 0.9-1.2V)



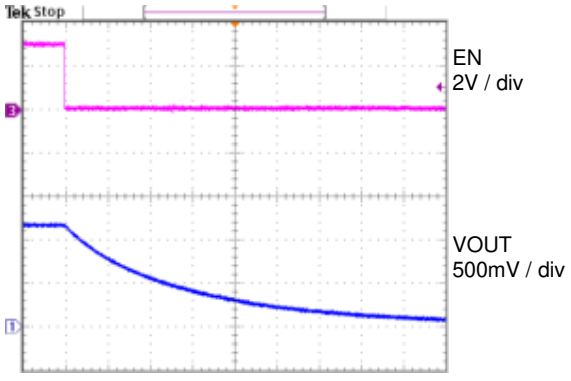

**DVS Negative Ramp-Down Rates**
($V_{OUT}$ = 1.2-0.9V)




**Buck Shutdown**
($V_{OUT}$ = 1.15625V, Active Discharge Enabled)




**Buck Shutdown**
($V_{OUT}$ = 1.15625V, Active Discharge Disabled)



## Functional Description

The KTB8331 is a highly efficient, high-performance, small buck regulator that operates from an input voltage of 2.7V to 5.5V and can output up to 3A. It integrates the main switch, synchronous rectifier switch, PWM control circuitry, $V_{OUT}$ setting DAC, various protection features, and an I²C serial interface to configure the output voltage, dynamic voltage scaling (DVS), control modes, and interrupts.

### Control Scheme

The KTB8331 uses a proprietary adaptive on-time (AOT) PWM control scheme to maintain a nearly constant switching frequency as input voltage and output voltage vary. Compared to typical current-mode PWM schemes, the AOT control scheme provides quick response to line and load transients with excellent stability and wide bandwidth, thereby minimizing output voltage droop and soar for dynamic loads, even with minimal output capacitance. The adaptive on-time approximates fixed-frequency switching without using a fixed clock oscillator, which eliminates the need to wait for the next clock before responding to a load transient.

The KTB8331 feedback loop also adds a proprietary, internally-compensated, integrating error amplifier to remove the output voltage offset normally associated with other AOT, constant on-time (COT), and hysteretic architectures.

### Shutdown Mode

When the EN pin is low, the KTB8331 buck is in shutdown mode and draws very little current. In shutdown, the I²C is still active, allowing read and write commands, as long as $V_{IN}$ is above $V_{UVLO}$. Similarly, register contents are retained during shutdown (and even when $V_{IN}$ is a little below $V_{UVLO}$), as long as $V_{IN}$ is above $V_{POR}$=1.8V.

### Hardware Enable

The KTB8331 buck regulator is turned on and off via hardware enable using the EN pin or via software enable using I²C commands. The default register settings allow simple hardware control. For hardware enable, drive the EN pin high. For hardware disable, drive the EN pin low.

### Software Enable

For software enable/disable control, first write 0 into the EN0 bit (B7) of the VSEL0 configuration register (0x00), and/or write 0 into the EN1 bit (B7) of the VSEL1 configuration register (0x01). The VSEL pin determines which register is used. Then bring the EN pin high. After that, write 1 into the corresponding EN0 or EN1 bit to enable the buck, and write 0 to disable the buck.

### Soft-Start

The KTB8331 buck contains soft-start circuitry to ramp up $V_{OUT}$ slowly in order to reduce inrush current at $V_{IN}$ and prevent the inductor current from reaching the peak current limit ($I_{LX_PEAK}$) during startup. The soft-start ramp rates are I²C programmable using the SLEW[2:0] bits (B6:4) in the CONTROL configuration register (0x02).

The default register setting provides the slowest ramp rate to accommodate cold startup with certain processor cores. Once the processor is warm, faster ramps may be used. The slower rates are also better for applications with large amounts of total output capacitance. The inductor's average current during soft-start is given by:

$$I_{L_SS} = C_{OUT} \times (dV/dt_{SS}) + I_{LOAD_SS}$$

where $dV/dt_{SS}$ is the soft-start ramp rate and $I_{LOAD_SS}$ is the load current during soft-start. Choose a ramp rate that keeps the inductor current average below 3A, or even lower. As an example, if $I_{LOAD_SS}$ = 0, the fastest ramp rate of $dV/dt_{SS}$ = 30mV/µs is still slow enough for $I_{L_SS}$ ≤ 3A with $C_{OUT}$ ≤ 100µF. But if $I_{LOAD_SS}$ = 1.5A and $C_{OUT}$ = 300µF, choose a $dV/dt_{SS}$ < 5mV/µs.

### Setting the Output Voltage

The KTB8331 has two independent output voltage ranges. The low range is $V_{OUT}$ = 0.6V to 1.39375V in 6.25mV steps. The high range is $V_{OUT}$ = 1.44V to 3.345V in 15mV steps. The range is I²C programmable using the RANGE bit (B3) in the CONTROL configuration register (0x02). The default range setting is factory trimmed to match the default output voltage setting – see the *Ordering Information* section.

After the correct range is selected, the KTB8331 register map contains two voltage setting registers to facilitate hardware control of DVS using the VSEL pin. The first output voltage setting is I²C programmable using the VOUT_VSEL0[6:0] bits (B6:0) in the VSEL0 configuration register (0x00). The second output voltage setting is I²C programmable using the VOUT_VSEL1[6:0] bits (B6:0) in the VSEL1 configuration register (0x01). The output voltage setting is given by:

$$V_{OUT} = G \times (600mV + 6.25mV \times VOUT_VSELn)$$

where G = 1.0 when the RANGE bit is 0, and G = 2.4 when the RANGE bit is 1. VOUT_VSELn is the decimal equivalent of the binary bits of VOUT_VSEL0[6:0] or VOUT_VSEL1[6:0]. The default voltage settings are factory trimmed, and several versions are available – see the *Ordering Information* section.

Note: Before toggling the RANGE bit, the buck converter VOUT must be disabled either by setting EN pin to low or by setting both registers VSEL0/VSEL1 and EN0/EN1 bits to 0.

## Dynamic Voltage Scaling (DVS)

Dynamic Voltage Scaling (DVS) is used to slew the output voltage between two voltage settings contained in the VSEL0 and VSEL1 registers – see *Setting the Output Voltage* section. The VSEL pin selects which register is used. Or, as an alternative method, I²C commands can be used by simply connecting the VSEL pin to ground and dynamically writing a new setting into the VSEL0 register.

In either method, all DVS output voltage transitions are slew-rate-controlled by an on-chip up/down counter and DAC. The DVS slew rate is I²C programmable using the SLEW[2:0] bits (B6:4) in the CONTROL configuration register (0x02). DVS slewing is only supported within a single output voltage range; slewing between a voltage in the low range and a voltage in the high range is ***not*** supported.

## Forced-PWM vs. Auto-Skip Modes

The KTB8331 has two ways to control light-load switching behavior – Forced-PWM mode and Auto-Skip mode. In Forced-PWM, the switching frequency remains nearly constant. This mode is helpful for applications that are noise sensitive.

In Auto-Skip mode, the KTB8331 transitions automatically between PWM switching at heavy loads and Skip/PFM switching at light loads. Auto-Skip mode is helpful for applications that need high efficiency at light loads. While skipping, single pulses are evenly spaced, resulting in the lowest output ripple and noise when compared to competing “pulse-grouping” or “burst mode” devices. Furthermore, the PFM frequency during single-pulse skipping remains above the audio frequency band (20Hz to 20kHz) down to very light loads – see the *Typical Operating Characteristics* section.

The switching mode is I²C programmable using the MODE[1:0] bits (B1:0) in the CONTROL configuration register (0x02). The MODE[1:0] bits work together with the VSEL pin to independently set the switching mode for the VOUT_VSEL0[6:0] and VOUT_VSEL1[6:0] output voltage settings. The default mode settings are factory trimmed, and several versions are available – see the *Ordering Information* section.

## Active Discharge

When the KTB8331 buck is disabled, an active discharge feature connects an on-chip resistor ($R_{LX_DIS}$) between the LX and PGND pins. This resistor discharges the output capacitor through the inductor. By default, this feature is enabled; however, it can be disabled for applications that require a high impedance at the output during shutdown. Enable and disable the active discharge feature via I²C commands by writing the DIS bit (B7) in the CONTROL configuration register (0x02).

## POR and Software Register Reset

The KTB8331 does NOT contain non-volatile memory for the register settings. When $V_{IN}$ rises above $V_{POR}$=1.8V, either at initial power up or after a temporary $V_{IN}$ droop below $V_{POR}$, a Power-On Reset (POR) circuit resets all registers to their factory default settings. Thereafter, as long as $V_{IN}$ remains above $V_{POR}$, the I²C registers contents are retained, regardless if the buck is enabled or disabled. However, to reliably read or write to the I²C registers, $V_{IN}$ should be above $V_{UVLO}$.

To reset the registers manually via software, use I²C to write a 1 to the RESET bit (B2) in the CONTROL configuration register (0x02). This resets nearly all registers to their default settings. There are a few exceptions, as makes logical sense; refer to the CONTROL register description.

## Internal Status Monitor

The KTB8331 contains a MONITOR status register (0x05), which can be read to check the present status of the IC. The register has individual bits for the status of $V_{OUT}$ power-OK, $V_{IN}$ under-voltage lockout, $V_{IN}$ over-voltage protection, $V_{OUT}$ positive slew, $V_{OUT}$ negative slew, software reset event latch, over-temperature thermal shutdown, and buck enable. Refer to the MONITOR register description for more details.

## Interrupt Register and IRQ\ Flag

The KTB8331 contains an interrupt mask register, an interrupt latch register, and an interrupt request flag pin (IRQ\) to inform a host processor that one or more status changes have occurred. The INTMASK mask register (0x06) and the INTLATCH interrupt register (0x07) both partially mirror the MONITOR status register bits. However, the enable (nEN_INT) interrupt has logic inversion (in comparison to the MONITOR status register) to indicate that the buck was ***disabled***.

Only unmasked events are latched into the INTLATCH register. By default, all interrupts are masked and need to be unmasked before they can be latched. The IRQ\ pin pulls active low while any bit in the INTLATCH register is a 1. Reading the INTLATCH register resets and clears the register, thereby releasing the IRQ\ pin. However, if an unmasked event is still on-going, it will not clear, and the IRQ\ pin will remain low.

This IRQ\ flag remain active during UVLO events as long as $V_{IN}$ is above $V_{POR}$=1.8V. However, the IRQ\ flag is always cleared if $V_{IN}$ falls below $V_{POR}$ due to power-on reset (POR) of all registers.

## Input Under-Voltage Lockout (UVLO)

When the input voltage ($V_{IN}$) is below the under-voltage lockout threshold ($V_{UVLO}$), the buck is disabled. The I²C registers and all logic pins remain functional during UVLO, so long as $V_{IN}$ remains above $V_{POR}$=1.8V. Exiting UVLO does ***not*** reset any registers. When $V_{IN}$ rises above $V_{UVLO}$, either at initial power up or after a temporary $V_{IN}$ droop below $V_{UVLO}$, and if the buck is enabled, the programmed soft-start ramp begins.

The UVLO status is reflected in the MONITOR register. UVLO events do ***not*** reset the registers to their defaults. $V_{IN}$ must fall below $V_{POR}$ to reset the registers.

## Input Over-Voltage Protection (OVP)

When the input voltage ($V_{IN}$) is above the over-voltage protection threshold ($V_{OVP}$), the buck is disabled. The I²C registers and all logic pins remain functional during OVP. When $V_{IN}$ returns below $V_{OVP}$, and if the buck is enabled, the programmed soft-start ramp begins.

Just like UVLO, the OVP status is reflected in the MONITOR register.

## Inductor Over-Current Protection (OCP)

Inductor peak current limit ($I_{LX_PEAK}$) and valley current limit ($I_{LX_VALLEY}$) protect the buck and inductor during over-current faults. The current limits control the buck's switching on a cycle-by-cycle basis and have a higher priority than the voltage regulation threshold.

During sustained over-current faults, the output voltage typically droops below the regulation threshold. The POK_STAT bit (B7) in the MONITOR register (0x05) indicates when $V_{OUT}$ is okay (***above*** the $V_{OUT_POK}$ threshold).

## Output Short-Circuit Protection (SCP) and Hiccup Mode

During a short-circuit event at the buck's output, the inductor experiences a very low discharge voltage during the switching cycle's off-time ($t_{OFF}$, when the synchronous rectifier switch is on). In this case, the inductor current ramps down very slowly. In order to prevent inductor current runaway, the valley current limit ($I_{LX_VALLEY}$) extends $t_{OFF}$, keeping the inductor current well controlled.

If an over-current fault or short-circuit event persists for more than 250µs, the buck enters hiccup mode and pause all switching. After about 5ms, the buck attempts to soft-start. If the fault persists, the buck once again enters hiccup mode and periodically re-attempts soft-start until the fault is removed. The low duty-factor during hiccup mode prevents the IC from getting hot.

### Thermal Shutdown Over-Temperature (OT)

Over-temperature (OT) protection occurs if the die junction temperature exceeds the thermal shutdown threshold ($T_{J_SHDN}$). During thermal shutdown, the buck pauses all switching until the die temperature cools. Once cooled, the buck re-starts with the programmed soft-start ramp.

The OT status is reflected in the MONITOR register and, if unmasked, latched into the INTLATCH register.

### Trim Options

The KTB8331 is factory trimmed using one-time programmable (OTP) registers. Standard versions are available for various default output voltage settings and modes – see the *Ordering Information* section. Contact a Kinetic Technologies representative regarding versions with other default settings or I²C slave addresses.

## I²C Interface Description

### I²C Serial Data Bus

The KTB8331 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The KTB8331 operates as a slave on the I²C bus. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The KTB8331 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 2:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus Not Busy**
Both data and clock lines remain HIGH.

**Start Data Transfer**
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

**Stop Data Transfer**
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

**Data Valid**
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

**Acknowledge**
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

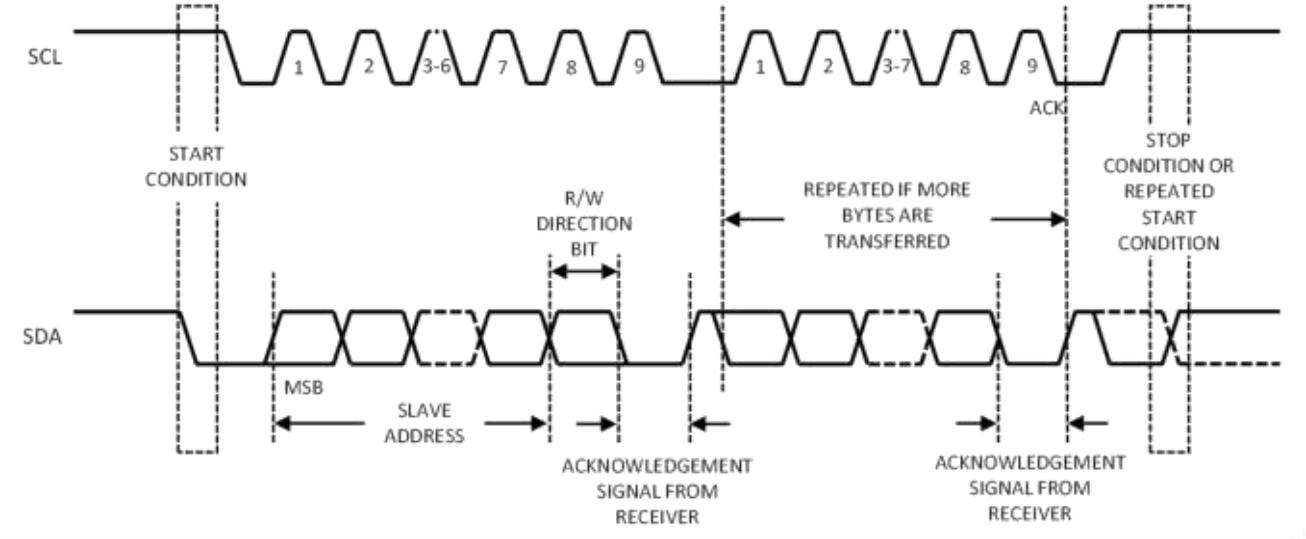



**Figure 2. Data Transfer on I²C Serial Bus**

The KTB8331 7-bit slave device address is listed in the Ordering Information table in page 3.

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

## I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 3 shows the sequence of the I²C write cycle.

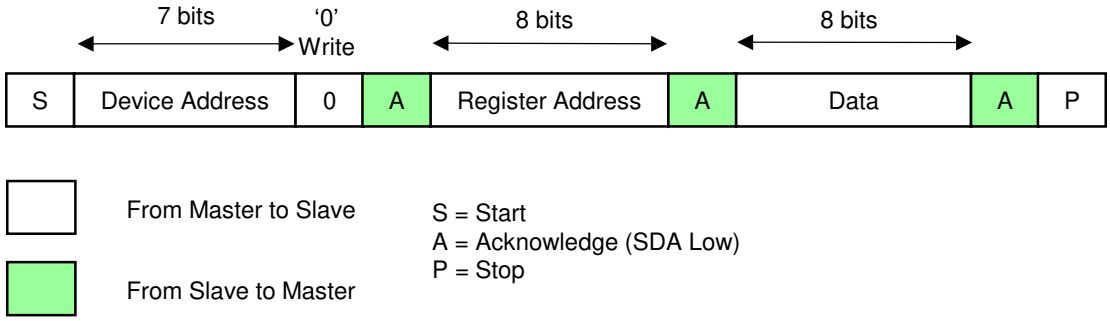



**Figure 3. I²C Write Cycle**

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generate stop condition to finish the write cycle.

## I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 4 shows the steps of the I²C read cycle.

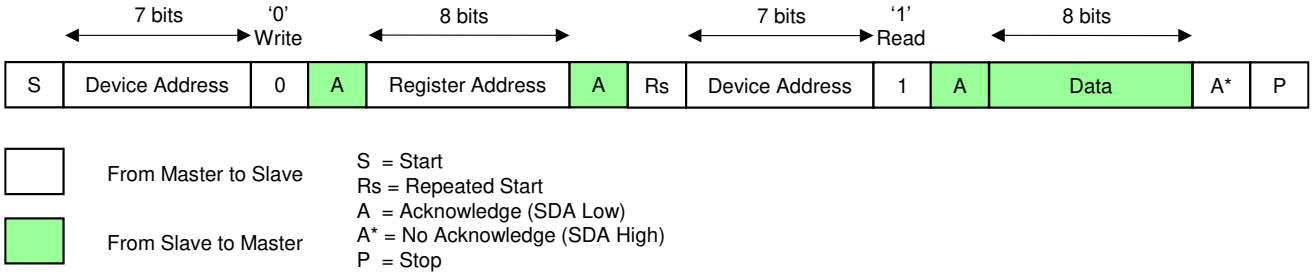



**Figure 4. I²C Read Cycle**

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generate stop condition to finish the read cycle.

# I²C Registers

## I²C Slave Address

| Options[10] | 7-Bit Address | Write Address | Read Address | Bits 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|
| KTB8331A/B/C/K/L/M | 0x60 | 0xC0 | 0xC1 | 1 1 0 0 0 0 0 *R/W̄* |
| KTB8331D/F/G/H | 0x50 | 0xA0 | 0xA1 | 1 0 1 0 0 0 0 *R/W̄* |
| KTB8331E | 0x57 | 0xAE | 0xAF | 1 0 1 0 1 1 1 *R/W̄* |
| KTB8331J | 0x51 | 0xA2 | 0xA3 | 1 0 1 0 0 0 1 *R/W̄* |

## I²C Register Map

| Hex Address | Name | Type | Access | Default Reset | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | VSEL0 | Config | R/W | 1xxx xxxx | EN0 | VOUT_VSEL0[6:0] | | | | | | |
| 0x01 | VSEL1 | Config | R/W | 1xxx xxxx | EN1 | VOUT_VSEL1[6:0] | | | | | | |
| 0x02 | CONTROL | Config | R/W | 1000 x0xx | DIS | SLEW[2:0] | | | RANGE | RESET | MODE[1:0] | |
| 0x03 | ID1 | Data | R | 1010 0010 | VENDOR[2:0] | | | DIE_ID[4:0] | | | | |
| 0x04 | ID2 | Status | R | 0000 xxxx | RSVD | RSVD | RSVD | RSVD | DIE_REV[3:0] | | | |
| 0x05 | MONITOR | Status | R | 0000 0000 | POK _STAT | UVLO _STAT | OVP _STAT | POS _STAT | NEG _STAT | RESET _STAT | OT _STAT | EN _STAT |
| 0x06 | INTMASK | Mask | R/W | 1111 1111 | RSVD | RSVD | RSVD | POS _INTM | NEG _INTM | RESET _INTM | OT _INTM | nEN _INTM |
| 0x07 | INTLATCH | Intrrpt | R/C | 0000 0000 | RSVD | RSVD | RSVD | POS _INT | NEG _INT | RESET _INT | OT _INT | nEN _INT |

Register contents are reset in hardware to their default values by $V_{IN}$ power-on reset. Additionally, most registers can be reset in software by writing 1 to the RESET bit (B2) in the CONTROL register (0x02). Default Reset bits marked with lower-case "x" in the register map and register details tables depend upon the ordered part# suffix and die revision; please see the *Ordering Information* section. Upper-case "X" used elsewhere in the tables designates "don't care".

## VSEL0 Configuration Register

Register Address 0x00

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 7 | EN0 | R/W | 1 | Software Buck Enable. When EN pin is low, the regulator is off. When EN pin is high and VSEL pin is low, the EN0 bit takes precedent. |
| 6:0 | VOUT_VSEL0[6:0] | R/W | xxx xxxx | Sets the nominal $V_{OUT}$ regulation voltage when VSEL pin is low. When RANGE bit is low, the $V_{OUT}$ range is from 0.600 to 1.39375V. When RANGE bit is high, the $V_{OUT}$ range is from 1.440 to 3.345V. $$V_{OUT} = G \times (600mV + 6.25mV \times VOUT_VSEL0)$$ where G = 1.0 when RANGE bit is low, and G = 2.4 when RANGE bit is high. |

| EN pin | VSEL pin | EN0 bit | Regulator |
|---|---|---|---|
| 0 | X | X | off |
| 1 | 0 | 0 | off |
| 1 | 0 | 1 | on |

[10] For Alternate 1/2/3 Slave Addresses, please contact a Kinetic Technologies representative.

## VSEL1 Configuration Register

Register Address 0x01

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Default Reset</th><th>Description</th></tr>
<tr><td>7</td><td>EN1</td><td>R/W</td><td>1</td><td>Software Buck Enable. When EN pin is low, the regulator is off. When EN pin is high and VSEL pin is high, the EN1 bit takes precedent.
<table>
<tr><th>EN pin</th><th>VSEL pin</th><th>EN1 bit</th><th>Regulator</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>off</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>off</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>on</td></tr>
</table></td></tr>
<tr><td>6:0</td><td>VOUT_VSEL1[6:0]</td><td>R/W</td><td>xxx xxxx</td><td>Sets the nominal $V_{OUT}$ regulation voltage when VSEL pin is high. When RANGE bit is low, the $V_{OUT}$ range is from 0.600 to 1.39375V. When RANGE bit is high, the $V_{OUT}$ range is from 1.440 to 3.345V.<br>$$V_{OUT} = G \times (600mV + 6.25mV \times VOUT_VSEL1)$$<br>where G = 1.0 when RANGE bit is low, and G = 2.4 when RANGE bit is high.</td></tr>
</table>

## CONTROL Configuration Register

Register Address 0x02

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Default Reset</th><th>Description</th></tr>
<tr><td>7</td><td>DIS</td><td>R/W</td><td>1</td><td>Active Discharge of LX when regulator is disabled. Discharging LX will discharge $C_{OUT}$ through the inductor.<br>0 = $V_{OUT}$ is high impedance when disabled.<br>1 = $V_{OUT}$ is discharged through an internal pull-down resistor when disabled.</td></tr>
<tr><td>6:4</td><td>SLEW[2:0]</td><td>R/W</td><td>000</td><td>Slew Rate Control for soft-start and DVS ramp-up/down rates. Works in conjunction with the RANGE bit.
<table>
<tr><th>RANGE bit</th><th>SLEW bits</th><th>Soft-Start</th><th>DVS</th><th>$f_{STEP}$</th></tr>
<tr><td>0</td><td>000</td><td>1.5625mV/µs</td><td>3.125mV/µs</td><td>500kHz</td></tr>
<tr><td>0</td><td>001</td><td>3.125mV/µs</td><td>3.125mV/µs</td><td>500kHz</td></tr>
<tr><td>0</td><td>010</td><td>3.125mV/µs</td><td>6.25mV/µs</td><td>1MHz</td></tr>
<tr><td>0</td><td>011</td><td>6.25mV/µs</td><td>6.25mV/µs</td><td>1MHz</td></tr>
<tr><td>0</td><td>100</td><td>6.25mV/µs</td><td>12.5mV/µs</td><td>2MHz</td></tr>
<tr><td>0</td><td>101</td><td>12.5mV/µs</td><td>12.5mV/µs</td><td>2MHz</td></tr>
<tr><td>0</td><td>110</td><td>12.5mV/µs</td><td>25mV/µs</td><td>4MHz</td></tr>
<tr><td>0</td><td>111</td><td>25mV/µs</td><td>25mV/µs</td><td>4MHz</td></tr>
<tr><td>1</td><td>000</td><td>1.875mV/µs</td><td>3.75mV/µs</td><td>250kHz</td></tr>
<tr><td>1</td><td>001</td><td>3.75mV/µs</td><td>3.75mV/µs</td><td>250kHz</td></tr>
<tr><td>1</td><td>010</td><td>3.75mV/µs</td><td>7.5mV/µs</td><td>500kHz</td></tr>
<tr><td>1</td><td>011</td><td>7.5mV/µs</td><td>7.5mV/µs</td><td>500kHz</td></tr>
<tr><td>1</td><td>100</td><td>7.5mV/µs</td><td>15mV/µs</td><td>1MHz</td></tr>
<tr><td>1</td><td>101</td><td>15mV/µs</td><td>15mV/µs</td><td>1MHz</td></tr>
<tr><td>1</td><td>110</td><td>15mV/µs</td><td>25mV/µs</td><td>2MHz</td></tr>
<tr><td>1</td><td>111</td><td>30mV/µs</td><td>25mV/µs</td><td>2MHz</td></tr>
</table></td></tr>
</table>

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 3 | RANGE | R/W | x | Sets the $V_{OUT}$ range. Also influences the DVS ramp-up/down slew rate (see SLEW[2:0] above).<br>**RANGE bit** / **G** / **$V_{OUT(min)}$** / **$V_{OUT(max)}$** / **$V_{OUT(step)}$**<br>0 / 1.0 / 0.600V / 1.39375V / 6.25mV<br>1 / 2.4 / 1.440V / 3.345V / 15mV<br>$V_{OUT} = G \times (600mV + 6.25mV \times VOUT_VSELn)$<br>where G = 1.0 when RANGE bit is low, and G = 2.4 when RANGE bit is high.<br>Note: Before toggling the RANGE bit, the buck converter VOUT must be disabled either by setting EN pin to low or by setting both registers VSEL0/VSEL1 and EN0/EN1 bits to 0. |
| 2 | RESET | R/W | 0 | Software Reset to default register settings. Writing 1 resets ***nearly*** all the registers. The RESET bit always reads back as 0. Before self-clearing, the software reset event is latched into the RESET_STAT bit (B2) in the MONITOR register (0x05) and also into the RESET_INT bit (B2) in the INTLATCH register (0x07) if unmasked.<br>Items that are ***NOT*** reset by the RESET bit are:<br>1. RESET_STAT bit in the MONITOR register<br>2. RESET_INT bit in the INTLATCH register |
| 1:0 | MODE[1:0] | R/W | xx | Auto-Skip vs. Forced-PWM mode control. Works in conjunction with the VSEL pin. Auto-Skip automatically uses PWM in continuous conduction at heavy loads and PFM pulse-skipping in discontinuous conduction at light loads.<br>**VSEL pin** / **MODE bits** / **Operating Mode**<br>0 / X0 / Auto-Skip<br>0 / X1 / Forced-PWM<br>1 / 0X / Auto-Skip<br>1 / 1X / Forced-PWM |

## ID1 Data Register

Register Address 0x03

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 7:5 | VENDOR[2:0] | R | 101 | Vendor Identification<br>101 = Kinetic Technologies |
| 4:0 | DIE_ID[4:0] | R | 0 0010 | Die Type Identification<br>0 0010 = KTB8331 |

## ID2 Status Register

Register Address 0x04

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 7 | RSVD | R | 0 | Reserved. Always reads back as 0. |
| 6 | RSVD | R | 0 | Reserved. Always reads back as 0. |
| 5 | RSVD | R | 0 | Reserved. Always reads back as 0. |
| 4 | RSVD | R | 0 | Reserved. Always reads back as 0. |
| 3:0 | DIE_REV[3:0] | R | xxxx | Die Revision Identification |

## MONITOR Status Register

Register Address 0x05

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 7 | POK_STAT | R | 0 | $V_{OUT}$ Power OK Status<br>0 = $V_{OUT}$ is below POK comparator threshold<br>1 = $V_{OUT}$ is above POK comparator threshold<br>During normal operation, the POK_STAT bit is 1. During disabled, soft-start or overload conditions, the POK_STAT bit is 0. |
| 6 | UVLO_STAT | R | 0 | $V_{IN}$ Under-Voltage Status<br>0 = $V_{IN}$ is above the UVLO comparator threshold<br>1 = $V_{IN}$ is below the UVLO comparator threshold<br>During normal operation or when disabled, the UVLO_STAT bit is 0. During low input voltage conditions, the buck is disabled by the UVLO comparator and the UVLO_STAT bit is set to 1 (so long as $V_{IN}$ remains above $V_{POR}$=1.8V). |
| 5 | OVP_STAT | R | 0 | $V_{IN}$ Over-Voltage Status<br>0 = $V_{IN}$ is below the OVP comparator threshold<br>1 = $V_{IN}$ is above the OVP comparator threshold<br>During normal operation or when disabled, the OVP_STAT bit is 0. During high input voltage conditions, the buck is disabled by the OVP comparator and the OVP_STAT bit is set to 1. |
| 4 | POS_STAT | R | 0 | $V_{OUT}$ Positive Slew Status<br>0 = $V_{OUT}$ is at its set value<br>1 = $V_{OUT}$ is slewing in the positive direction towards it set value<br>During normal operation, the POS_STAT bit is 0. During soft-start or positive DVS slew transitions, the POS_STAT bit is 1. |
| 3 | NEG_STAT | R | 0 | $V_{OUT}$ Negative Slew Status<br>0 = $V_{OUT}$ is at its set value<br>1 = $V_{OUT}$ is slewing in the negative direction towards it set value<br>During normal operation, the NEG_STAT bit is 0. During negative DVS slew transitions, the NEG_STAT bit is 1. |
| 2 | RESET_STAT | R/C | 0 | Software Reset Status Latch<br>0 = software reset was not performed since this bit was cleared<br>1 = software reset was performed since this bit was cleared<br>The RESET_STAT bit is set to 1 when a software reset is written to the RESET bit (B2) in the CONTROL register. The RESET_STAT bit is ***NOT*** reset by the software reset. Instead, it is cleared (reset to 0) after the RESET_STAT bit is read or whenever chip power is removed ($V_{IN}$<$V_{POR}$). |
| 1 | OT_STAT | R | 0 | Over-Temperature Status<br>0 = the die is not in thermal shutdown<br>1 = the die is in thermal shutdown<br>During normal operation, the OT_STAT bit is 0. During thermal shutdown, the OT_STAT bit is 1. |
| 0 | EN_STAT | R | 0 | Enable Status<br>0 = the buck is disabled by hardware or software<br>1 = the buck is enabled by hardware or software<br>During normal operation, the EN_STAT bit is 1. During hardware or software disabled conditions, the EN_STAT bit is 0. |

## INTMASK Mask Register

Register Address 0x06

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 7:5 | RSVD | R/W | 111 | RSVD |
| 4 | POS_INTM | R/W | 1 | POS Interrupt Mask<br>0 = the interrupt is not masked<br>1 = the interrupt is masked |
| 3 | NEG_INTM | R/W | 1 | NEG Interrupt Mask<br>0 = the interrupt is not masked<br>1 = the interrupt is masked |
| 2 | RESET_INTM | R/W | 1 | RESET Interrupt Mask<br>0 = the interrupt is not masked<br>1 = the interrupt is masked |
| 1 | OT_INTM | R/W | 1 | OT Interrupt Mask<br>0 = the interrupt is not masked<br>1 = the interrupt is masked |
| 0 | nEN_INTM | R/W | 1 | nEN Interrupt Mask<br>0 = the interrupt is not masked<br>1 = the interrupt is masked |

## INTLATCH Interrupt Register

Register Address 0x07

| Bit | Name | Access | Default Reset | Description |
|---|---|---|---|---|
| 7:5 | RSVD | R/C | 0 | RSVD |
| 4 | POS_INT | R/C | 0 | POS Interrupt Latch<br>0 = $V_{OUT}$ has not slewed in positive direction due to DVS ramp-up or soft-start since cleared<br>1 = $V_{OUT}$ was slewed in positive direction due to DVS ramp-up or soft-start since cleared |
| 3 | NEG_INT | R/C | 0 | NEG Interrupt Latch<br>0 = $V_{OUT}$ has not slewed in negative direction due to DVS ramp-down since cleared<br>1 = $V_{OUT}$ was slewed in negative direction due to DVS ramp-down since cleared |
| 2 | RESET_INT | R/C | 0 | Software Reset Interrupt Latch<br>0 = software reset was not performed since this bit was cleared<br>1 = software reset was performed since this bit was cleared<br>The RESET_INT bit is set to 1 when a software reset is written to the RESET bit (B2) in the CONTROL register. The RESET_STAT bit is ***NOT*** reset by the software reset. Instead, it is cleared (reset to 0) after the RESET_INT bit is read or whenever chip power is removed ($V_{IN}$<$V_{POR}$). |
| 1 | OT_INT | R/C | 0 | OT Interrupt Latch<br>0 = the die has not entered thermal shutdown since cleared<br>1 = the die was in thermal shutdown since cleared |
| 0 | nEN_INT | R/C | 0 | nEN (***NOT*** Enabled = Disabled) Interrupt Latch<br>0 = the buck has not been disabled by hardware or software since cleared<br>1 = the buck was disabled by hardware or software since cleared |

# Applications Information

## Recommended Inductors

The KTB8331 is trimmed for inductors with nominal inductance of 330nH or 470nH. Select an inductor with a saturation current rating that is higher than the KTB8331 peak current limit. Also, choose an inductor with sufficient temperature-rise current rating to satisfy the RMS load-current of the application. Consider the inductor's resistance (both DCR and ACR at 2.4MHz), since these will affect the efficiency. (Generally, the ACR vs. frequency characteristic is available upon request from the inductor supplier.) Larger physical case-sizes, good winding designs, and better magnetic materials can increase efficiency. Typically, metric 2012 and 2016 case-sizes are suitable. Table 1 is a list of recommended inductors from two leading suppliers.

**Table 1. Recommended Inductors**

| Maker | Part # | L (typ) | DCR (typ) | $I_{SAT}$ (min) | $I_{\Delta T+40C}$ (min) | Size (typ/typ/max) |
|---|---|---|---|---|---|---|
| Murata | DFE201210U-R33M<br>DFE201210U-R47M | 330nH<br>470nH | 25mΩ<br>34mΩ | 5.2A<br>4.4A | 3.4A<br>3.0A | 2.0 x 1.2 x 1.0mm |
| Murata | DFE201610E-R33M<br>DFE201610E-R47M | 330nH<br>470nH | 21mΩ<br>26mΩ | 5.5A<br>4.8A | 4.0A<br>3.6A | 2.0 x 1.6 x 1.0mm |
| Murata | DFE201612E-R33M<br>DFE201612E-R47M | 330nH<br>470nH | 15mΩ<br>20mΩ | 6.3A<br>5.5A | 4.8A<br>4.5A | 2.0 x 1.6 x 1.2mm |
| Samsung E-M | CIGT201208EHR47MNE | 470nH | 31mΩ | 4.1A | 3.7A | 2.0 x 1.25 x 0.8mm |
| Samsung E-M | CIGT201210UHR33MNE<br>CIGT201210UHR47MNE | 330nH<br>470nH | 21mΩ<br>25mΩ | 5.4A<br>4.9A | 4.0A<br>3.6A | 2.0 x 1.25 x 1.0mm |
| Samsung E-M | CIGT201608EHR47MNE | 470nH | 24mΩ | 4.3A | 4.3A | 2.0 x 1.6 x 0.8mm |
| Samsung E-M | CIGW201610GHR33MLE<br>CIGW201610GLR47MLE<br>CIGT201610EHR47MNE | 330nH<br>470nH<br>470nH | 18mΩ<br>21mΩ<br>18mΩ | 5.5A<br>5.0A<br>5.5A | 4.0A<br>4.7A<br>4.8A | 2.0 x 1.6 x 1.0mm |

## Recommended Capacitors

Ceramic input and output capacitors with X5R or X6S are recommended due to their low ESR, low ESL, low temperature coefficients, and small physical sizes. Consider the voltage rating, size, and DC bias derating characteristic of the capacitor. Table 2 is a list of recommended capacitors from two leading suppliers.

**Table 2. Recommended Capacitors**

| Maker | Part # | C (typ) | $C_{EFF(3V)}$ | $V_{RATING}$ | $T_{CHAR}$ | Size |
|---|---|---|---|---|---|---|
| Murata | GRM155R60J106ME<br>GRM155R60J156ME<br>GRM155R60G226ME<br>GRM155R60J226ME | 10µF<br>15µF<br>22µF<br>22µF | 3.5µF<br>5µF<br>7µF<br>7µF | 6.3V<br>6.3V<br>4.0V<br>6.3V | X5R | (0402) 1.0 x 0.5mm |
| Murata | GRM188R60G226ME<br>GRM188R60J226ME | 22µF<br>22µF | 9µF<br>9µF | 4.0V<br>6.3V | X5R | (0603) 1.6 x 0.8mm |
| Samsung E-M | CL05A106MQ5<br>CL05A156MQ5 | 10µF<br>15µF | 4µF<br>6µF | 6.3V<br>6.3V | X5R | (0402) 1.0 x 0.5mm |
| Samsung E-M | CL10A226MQ8<br>CL10A476MQ8 | 22µF<br>47µF | 11µF<br>14µF | 6.3V<br>6.3V | X5R | (0603) 1.6 x 0.8mm |

### Input Capacitor

Choose an input capacitor with voltage rating of 6.3V or more, 10uF total nominal capacitance or more, and 1005M (0402) case-size or larger. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor. If the application's input voltage is supplied through a connector or a cable, add additional bypass/bulk capacitance where $V_{IN}$ first arrives to the PCB.

### Output Capacitors

Choose output capacitors with voltage rating of 4.0V or more, 20uF total nominal capacitance or more, and 1005M (0402) case-size or larger. Consider the $V_{OUT}$ setting of the regulator and how case size has a significant

impact on DC bias derating. At high $V_{OUT}$ settings, more total nominal capacitance is needed to achieve the same effective capacitance compared to lower $V_{OUT}$ settings.

For the very best possible load transient response, use multiple capacitors in parallel to achieve sufficient total effective output capacitance:

$$C_{OUT_{EFFECTIVE}} \geq \frac{L \times I_{STEP}}{33m\Omega \times (V_{IN} - V_{OUT})}$$

where $I_{STEP}$ is the largest load transient step in the application. Please note that the above formula is already guard-banded by a margin of 2x to accommodate capacitor and inductor tolerances and the variability of a transient arrival time with respect to the switching cycle of the regulator.

If needed, the total effective output capacitance can be distributed by placing additional capacitors remotely at the point of load. In applications where transient performance is less critical, especially when $V_{IN}$ minus $V_{OUT}$ is small, it is acceptable to reduce the total effective output capacitance to save board space and cost at the expense of load transient droop and soar.

As a design example, consider a system with $V_{IN}$ = 3.2V (min), $V_{OUT}$ = 1.8V, and $I_{STEP}$ = 2A (max):

$$C_{OUT_{EFFECTIVE}} \geq \frac{330nH \times 2A}{33m\Omega \times (3.2V - 1.8V)} \cong 14\mu F$$

In this example, choose output capacitors with total effective capacitance of 14µF or more at a DC bias of 1.8V. A single 15µF capacitor will not be enough when considering its DC bias characteristic, per Figure 5. At 1.8V bias, it retains only about 8µF; therefore, for best transient response, use two of these capacitors in parallel for a total effective capacitance of 16µF.

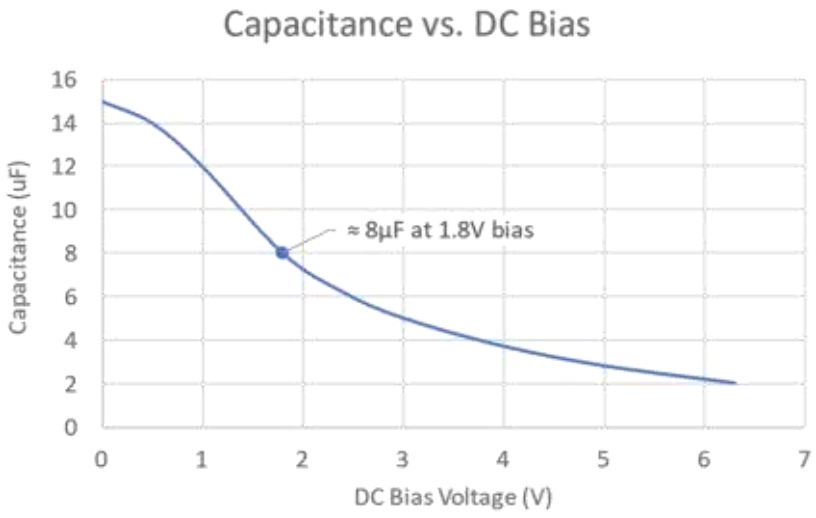



**Figure 5. Typical DC bias derating characteristic for example 15µF ceramic capacitor.**

When operating near dropout with high $V_{OUT}$ and low $V_{IN}$ (for example 3.3$V_{OUT}$ and 3.6$V_{IN}$), add additional bulk capacitance to $C_{OUT}$ to reduce $V_{OUT}$ droop and ringing during load transient events that is inherent in buck regulators operating at high duty-cycle.

## Recommended PCB Layout

Refer to Figure 6 for two example PCB layouts optimized for small footprint, low EMI, and good performance. One example fits in a narrow rectangular area, while the other example is nearly square. Both examples follow the below PCB layout recommendations:

1. Connect the input capacitor $C_{IN}$ as close as possible to the VIN and PGND pins using top-side thick metal traces.
2. Connect the ground terminals of output capacitors $C_{OUT}$ as close as possible to the ground terminal of $C_{IN}$ and the PGND pins using top-side metal.
3. Connect the local top-side PGND island to the PCB ground plane using multiple parallel vias.
4. Do not connect the AGND pins directly to the top-side PGND. Instead, connect the AGND pins to the PCB ground plane using their own vias.
5. Connect the inductor to the LX pins with a wide trace. For smallest $C_{IN}$, the LX trace will not fit between the top-side landing pads of a 1005M (0402) size capacitor. Therefore, the LX trace is normally routed on PCB layer 2 or layer 3 using multiple parallel vias.
    a. The added inductance of vias in series with the actual inductor have minimal effect on performance. However, it is important to use enough parallel vias to handle the peak inductor current in the application.
    b. If using a larger $C_{IN}$ of 1608M (0603) size or more, it is possible to squeeze the LX route on the top-side between the $C_{IN}$ landing pads. If pinched, make sure to widen the LX trace as much as possible before and after the pinched area.
6. Connect the $V_{OUT}$ terminals of the inductor to the output capacitors with a wide and short trace.
7. Route the $V_{OUT}$ sense trace from $C_{OUT}$ to the VOUT pin with care to keep it away from noisy traces, especially the LX trace. Additionally, use ground fill to shield noise from coupling into the $V_{OUT}$ sense.
8. Depending upon PCB design rules, it may be possible to place filled micro-vias directly under WLCSP bumps. If not, route short traces to nearby vias.

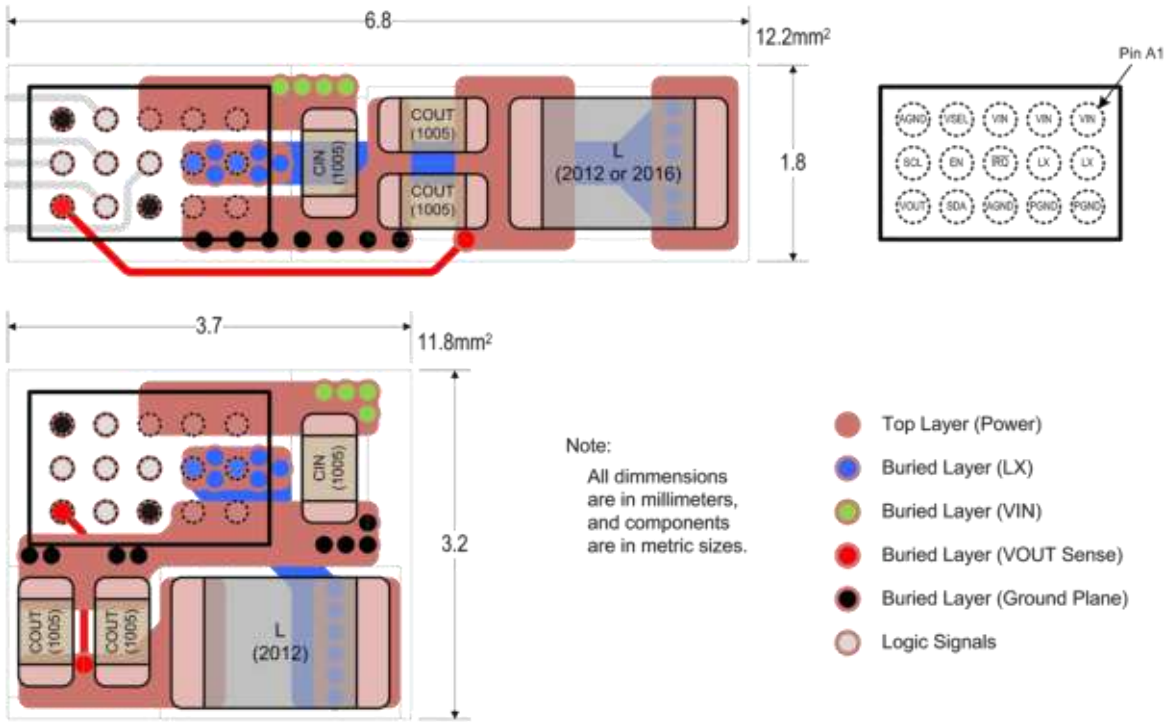
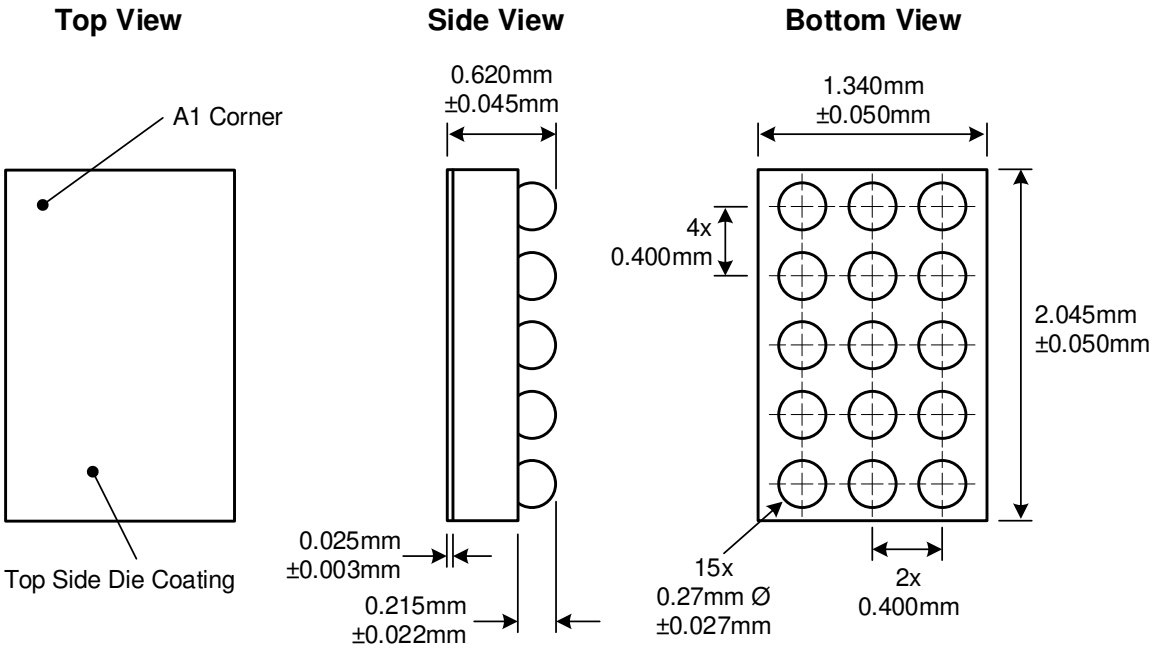


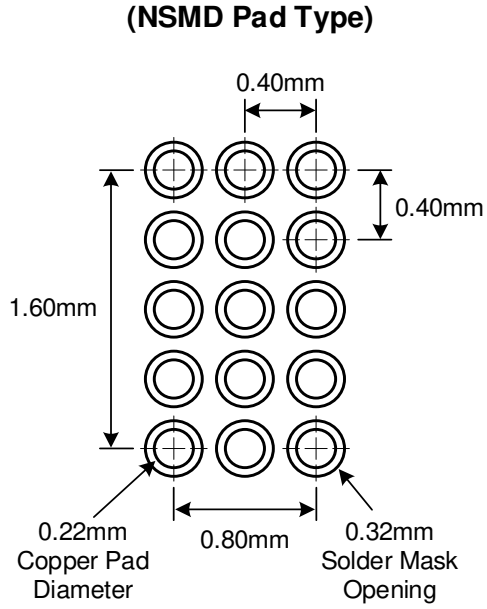

**Figure 6. Two recommended PCB layouts**

## Packaging Information

### WLCSP35-15 (1.340mm x 2.045mm x 0.620mm)




### Recommended Footprint

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