LA-LatticeECP3 Automotive Family Data Sheet

Data Sheet

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Contents

1. Features 9
2. Introduction 10
3. Architecture 11
3.1. Architecture Overview 11
3.2. PFU Blocks 12
3.2.1. Slice 13
3.2.2. Modes of Operation 15
3.3. Routing 16
3.4. sysCLOCK PLLs and DLLs 16
3.4.1. General Purpose PLL 16
3.4.2. Delay Locked Loops (DLL) 17
3.4.3. PLL/DLL Cascading 19
3.4.4. PLL/DLL PIO Input Pin Connections 19
3.5. Clock Dividers 20
3.6. Clock Distribution Network 20
3.6.1. Primary Clock Sources 20
3.6.2. Dynamic Clock Control (DCC) 22
3.6.3. Dynamic Clock Select (DCS) 22
3.6.4. Secondary Clock/Control Sources 22
3.6.5. Secondary Clock/Control Routing 23
3.6.6. Slice Clock Selection 25
3.6.7. Edge Clock Sources 25
3.6.8. Edge Clock Routing 26
3.7. sysMEM Memory 28
3.7.1. sysMEM Memory Block 28
3.7.2. Bus Size Matching 28
3.7.3. RAM Initialization and ROM Operation 28
3.7.4. Memory Cascading 28
3.7.5. Single, Dual and Pseudo-Dual Port Modes 29
3.7.6. Memory Core Reset 29
3.8. sysDSP™ Slice 29
3.8.1. sysDSP Slice Approach Compared to General DSP 29
3.9. sysDSP Slice Architecture Features 30
3.9.1. MULT DSP Element 32
3.9.2. MAC DSP Element 33
3.9.3. MMAC DSP Element 33
3.9.4. MULTADDSUB DSP Element 34
3.9.5. MULTADDSUBSUM DSP Element 35
3.10. Advanced sysDSP Slice Features 36
3.10.1. Cascading 36
3.10.2. Addition 37
3.10.3. Rounding 37
3.10.4. ALU Flags 37
3.10.5. Clock, Clock Enable and Reset Resources 37
3.10.6. Resources Available in the LA-LatticeECP3 Family 37
3.11. Programmable I/O Cells (PIC) 37
3.12. PIO 39
3.12.1. Input Register Block 39
3.12.2. Output Register Block 40
3.12.3. Tristate Register Block 41
3.12.4. ISI Calibration 42
3.12.5. Control Logic Block 42

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3.13. DDR Memory Support 42
3.13.1. Left and Right Edges 42
3.13.2. Bottom Edge 42
3.13.3. Top Edge 42
3.13.4. DLL Calibrated DQS Delay Block 43
3.13.5. Polarity Control Logic 45
3.13.6. DDR3 Memory Support 45
3.14. sysI/O Buffer 46
3.14.1. sysI/O Buffer Banks 46
3.14.2. Typical sysI/O I/O Behavior During Power-up 48
3.14.3. Supported sysI/O Standards 48
3.14.4. On-Chip Programmable Termination 48
3.14.5. Equalization Filter 49
3.14.6. Hot Socketing 50
3.15. SERDES and PCS (Physical Coding Sublayer) 50
3.15.1. PCS 52
3.15.2. SCI (SERDES Client Interface) Bus 52
3.16. Flexible Quad SERDES Architecture 52
3.17. IEEE 1149.1-Compliant Boundary Scan Testability 53
3.18. Device Configuration 53
3.18.1. Enhanced Configuration Options 54
3.18.2. Soft Error Detect (SED) Support 54
3.18.3. External Resistor 54
3.18.4. On-Chip Oscillator 54
3.19. Density Shifting 55
4. DC and Switching Characteristics 55
4.1. Absolute Maximum Ratings[1, 2, 3] 55
4.2. Recommended Operating Conditions[1] 56
4.3. Hot Socketing Specifications[1, 2, 3] 57
4.4. Hot Socketing Requirements[1, 2] 57
4.5. ESD Performance 57
4.6. DC Electrical Characteristics 57
4.7. LA-LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6] 58
4.8. SERDES Power Supply Requirements1, 2, 3 58
4.9. sysI/O Recommended Operating Conditions 59
4.10. sysI/O Single-Ended DC Electrical Characteristics[2] 60
4.11. sysI/O Differential Electrical Characteristics 61
4.11.1. LVDS25 61
4.11.2. Differential HSTL and SSTL 61
4.11.3. LVDS25E 61
4.11.4. LVCMOS33D 62
4.11.5. BLVDS25 62
4.11.6. LVPECL33 63
4.11.7. RSDS25E 64
4.11.8. MLVDS25 65
4.12. Typical Building Block Function Performance 66
4.12.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)[1] 66
4.13. Register-to-Register Performance[1] 67
4.14. Derating Timing Tables 67
4.15. LA-LatticeECP3 External Switching Characteristics[1, 2] 68
4.16. LA-LatticeECP3 Internal Switching Characteristics[1] 74
LA-LatticeECP3 Internal Switching Characteristics[1] 75
4.17. Timing Diagrams 76
4.18. LA-LatticeECP3 Family Timing Adders [1, 2, 3, 4, 5] 78

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4.19. LA-LatticeECP3 Maximum I/O Buffer Speed [1, 2, 3, 4, 5, 6] 80
4.20. Oscillator Output Frequency 81
4.21. sysCLOCK PLL Timing 82
4.22. DLL Timing 83
4.23. SERDES High-Speed Data Transmitter[1] 84
4.24. SERDES/PCS Block Latency 85
4.25. SERDES High Speed Data Receiver 86
4.25.1. Input Data Jitter Tolerance 86
4.25.2. SERDES External Reference Clock 87
4.26. PCI Express Electrical and Timing Characteristics 90
4.26.1. AC and DC Characteristics 90
4.27. XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics 91
4.27.1. AC and DC Characteristics 91
4.28. Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics 92
4.28.1. AC and DC Characteristics 92
4.29. Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics 93
4.29.1. AC and DC Characteristics 93
4.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics 94
4.30.1. AC and DC Characteristics 94
4.31. HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics 95
4.31.1. AC and DC Characteristics 95
4.32. LA-LatticeECP3 sysCONFIG Port Timing Specifications 97
4.33. JTAG Port Timing Specifications 102
4.34. Switching Test Conditions 103
4.35. sysI/O Differential Electrical Characteristics 103
4.35.1. Transition Reduced LVDS (TRLVDS DC Specification) 103
4.35.2. Mini LVDS 104
4.35.3. Point-to-Point LVDS (PPLVDS) 104
4.35.4. RSDS 105
4.36. Signal Descriptions 105
4.37. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin 107
4.38. Pin Information Summary 108
4.39. Package Pinout Information 109
4.40. Thermal Management 110
4.40.1. For Further Information 110
5. Ordering Information 110
5.1. LA-LatticeECP3 Part Number Description 110
5.1.1. Ordering Information 110
6. Supplemental Information 112
6.1. For Further Information 112
Technical Support Assistance 113
Revision History 114

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Figures

Figure 3.1. Simplified Block Diagram, LA-LatticeECP3-35 Device (Top Level) 12
Figure 3.2. PFU Diagram 13
Figure 3.3. Slice Diagram 14
Figure 3.4. General Purpose PLL Diagram 17
Figure 3.5. Delay Locked Loop Diagram (DLL) 18
Figure 3.6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line 19
Figure 3.7. Sharing of PIO Pins by PLLs and DLLs in LA-LatticeECP3 Devices 19
Figure 3.8. Clock Divider Connections 20
Figure 3.9. Primary Clock Sources for LA-LatticeECP3-17 21
Figure 3.10. Primary Clock Sources for LA-LatticeECP3-35 21
Figure 3.11. Per Quadrant Primary Clock Selection 22
Figure 3.12. DCS Waveforms 22
Figure 3.13. Secondary Clock Sources 23
Figure 3.14. LA-LatticeECP3-17 and LA-LatticeECP3-35 Secondary Clock Regions 24
Figure 3.15. Per Region Secondary Clock Selection 24
Figure 3.16. Slice0 through Slice2 Clock Selection 25
Figure 3.17. Slice0 through Slice2 Control Selection 25
Figure 3.18. Edge Clock Sources 26
Figure 3.19. Sources of Edge Clock (Left and Right Edges) 27
Figure 3.20. Sources of Edge Clock (Top Edge) 27
Figure 3.21. Memory Core Reset 29
Figure 3.22. Comparison of General DSP and LA-LatticeECP3 Approaches 30
Figure 3.23. Simplified sysDSP Slice Block Diagram 31
Figure 3.24. Detailed sysDSP Slice Diagram 31
Figure 3.25. MULT sysDSP Element 32
Figure 3.26. MAC DSP Element 33
Figure 3.27. MMAC sysDSP Element 34
Figure 3.28. MULTADDSUB 35
Figure 3.29. MULTADDSUBSUM Slice 0 36
Figure 3.30. MULTADDSUBSUM Slice 1 36
Figure 3.31. PIC Diagram 38
Figure 3.32. Input Register Block for Left, Right and Top Edges 40
Figure 3.33. Output and Tristate Block for Left and Right Edges 41
Figure 3.34. DQS Grouping on the Left, Right and Top Edges 43
Figure 3.35. Edge Clock, DLL Calibration and DQS Local Bus Distribution 44
Figure 3.36. DQS Local Bus 45
Figure 3.37. LA-LatticeECP3 Banks 47
Figure 3.38. On-Chip Termination 49
Figure 3.39. SERDES/PCS Quads (LA-LatticeECP3-35) 50
Figure 3.40. Simplified Channel Block Diagram for SERDES/PCS Block 52
Figure 4.1. LVDS25E Output Termination Example 62
Figure 4.2. BLVDS25 Multi-point Output Example 63
Figure 4.3. Differential LVPECL33 64
Figure 4.4. RSDS25E (Reduced Swing Differential Signaling) 65
Figure 4.5. MLVDS25 (Multipoint Low Voltage Differential Signaling) 66
Figure 4.6. Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned) 73
Figure 4.7. DDR/DDR2/DDR3 Parameters 73
Figure 4.8. Generic DDRX1/DDRX2 (With Clock Center on Data Window) 74
Figure 4.9. Read/Write Mode (Normal) 76
Figure 4.10. Read/Write Mode with Input and Output Registers 77
Figure 4.11. Write Through (SP Read/Write on Port A, Input Registers Only) 77
Figure 4.12. Transmitter and Receiver Latency Block Diagram 86

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Figure 4.13. SERDES External Reference Clock Waveforms 88
Figure 4.14. Jitter Transfer – 3.125 Gbps 88
Figure 4.15. Jitter Transfer – 2.5 Gbps 89
Figure 4.16. Jitter Transfer – 1.25 Gbps 89
Figure 4.17. Jitter Transfer – 622 Mbps 89
Figure 4.18. XAUI Sinusoidal Jitter Tolerance Mask 92
Figure 4.19. Test Loads 96
Figure 4.20. sysCONFIG Parallel Port Read Cycle 98
Figure 4.21. sysCONFIG Parallel Port Write Cycle 99
Figure 4.22. sysCONFIG Master Serial Port Timing 99
Figure 4.23. sysCONFIG Slave Serial Port Timing 99
Figure 4.24. Power-On-Reset (POR) Timing 100
Figure 4.25. sysCONFIG Port Timing 100
Figure 4.26. Configuration from PROGRAMN Timing 101
Figure 4.27. Wake-Up Timing 101
Figure 4.28. Master SPI Configuration Waveforms 101
Figure 4.29. JTAG Port Timing Waveforms 102
Figure 4.30. Output Test Load, LVTTL and LVCMOS Standards 103

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Tables

Table 1.1. LA-LatticeECP3 Family Selection Guide 9
Table 3.1. Resources and Modes Available per Slice 13
Table 3.2. Slice Signal Descriptions 14
Table 3.3. Number of Slices Required to Implement Distributed RAM 15
Table 3.4. PLL Blocks Signal Descriptions 17
Table 3.5. DLL Signals 18
Table 3.6. Secondary Clock Regions 23
Table 3.7. sysMEM Block Configurations 28
Table 3.8. Maximum Number of Elements in a Slice 32
Table 3.9. Maximum Number of DSP Slices in the LA-LatticeECP3 Family 37
Table 3.10. Embedded SRAM in the LA-LatticeECP3 Family 37
Table 3.11. PIO Signal List 39
Table 3.12. On-Chip Termination Options for Input Modes 49
Table 3.13. LA-LatticeECP3 SERDES Standard Support 51
Table 3.14. LA-LatticeECP3 SERDES Standard Support 51
Table 3.15. LatticeECP3 Primary and Secondary Protocol Support 53
Table 3.16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal) 55
Table 4.1. Electrostatic Discharge-Human Body Model[1] 57
Table 4.2. Electrostatic Discharge-Charged Device Model[1] 57
Table 4.3. LVDS25E DC Conditions 62
Table 4.4. BLVDS25 DC Conditions[1] 63
Table 4.5. LVPECL33 DC Conditions[1] 64
Table 4.6. RSDS25E DC Conditions[1] 65
Table 4.7. MLVDS25 DC Conditions[1] 66
Table 4.8. Output Timing and Levels 84
Table 4.9. Channel Output Jitter 84
Table 4.10. SERDES/PCS Latency Breakdown 85
Table 4.11. Serial Input Data Specifications 86
Table 4.12. Receiver Total Jitter Tolerance Specification 87
Table 4.13. Periodic Receiver Jitter Tolerance Specification 87
Table 4.14. External Reference Clock Specification (refclkp/refclkn) 87
Table 4.15. Transmit 91
Table 4.16. Receive and Jitter Tolerance 91
Table 4.17. Transmit 92
Table 4.18. Receive and Jitter Tolerance 92
Table 4.19. Transmit 93
Table 4.20. Receive and Jitter Tolerance 93
Table 4.21. Transmit 94
Table 4.22. Receive 94
Table 4.23. Reference Clock 94
Table 4.24. Transmit and Receive[1, 2] 95
Table 4.25. Test Fixture Required Components, Non-Terminated Interfaces 103

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1. Features

- **AEC-Q100 Tested and Qualified**
- **Higher Logic Density for Increased System Integration**
  - Up to 35 K LUTs
  - 116 to 310 I/O
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 4 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 32 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 1.33 Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36 K to 68 K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to four PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/O
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2 V core power supply

Table 1.1. LA-LatticeECP3 Family Selection Guide

Device	**LA-ECP3-17**	**LA-ECP3-35**
LUTs (K)	17	33
sysMEM Blocks (18 Kbits)	38	72
Embedded Memory (Kbits)	700	1327
Distributed RAM Bits (Kbits)	36	68
18 x 18 Multipliers	24	64
SERDES (Quad)	1	1
PLLs/DLLs	2/2	4/2
Packages and SERDES Channels/ I/O Combinations		
Package	**LA-ECP3-17**	**LA-ECP3-35**
328 csBGA (10 mm x 10 mm)	2/116	—
256 ftBGA (17mm x 17 mm)	4/133	4/133
484 fpBGA (23 mm x 23 mm)	4/222	4/295
672 fpBGA (27 mm x 27 mm)	—	4/310

2. Introduction

The LA-LatticeECP3 automotive FPGA devices are optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65 nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LA-LatticeECP3 device family expands look-up-table (LUT) capacity to 35 K logic elements and supports up to 310 user I/O. The LA-LatticeECP3 device family also offers up to 64 18 x 18 multipliers and a wide range of parallel I/O standards.

The LA-LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LA-LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LA-LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LA-LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LA-LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bitstream encryption, and TransFR field upgrade features.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LA-LatticeECP3 FPGA family. Synthesis library support for LA-LatticeECP3 is available for popular logic synthesis tools. Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LA-LatticeECP3 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LA-LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

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3. Architecture

3.1. Architecture Overview

Each LA-LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 3.1. The LA-LatticeECP3 devices have two rows of DSP slices. In addition, the LA-LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LA-LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LA-LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LA-LatticeECP3 devices feature up to 4 embedded 3.2 Gbps SERDES (Serializer/Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in the quad can be programmed via the SERDES Client Interface (SCI). This quad is located at the bottom of the devices.

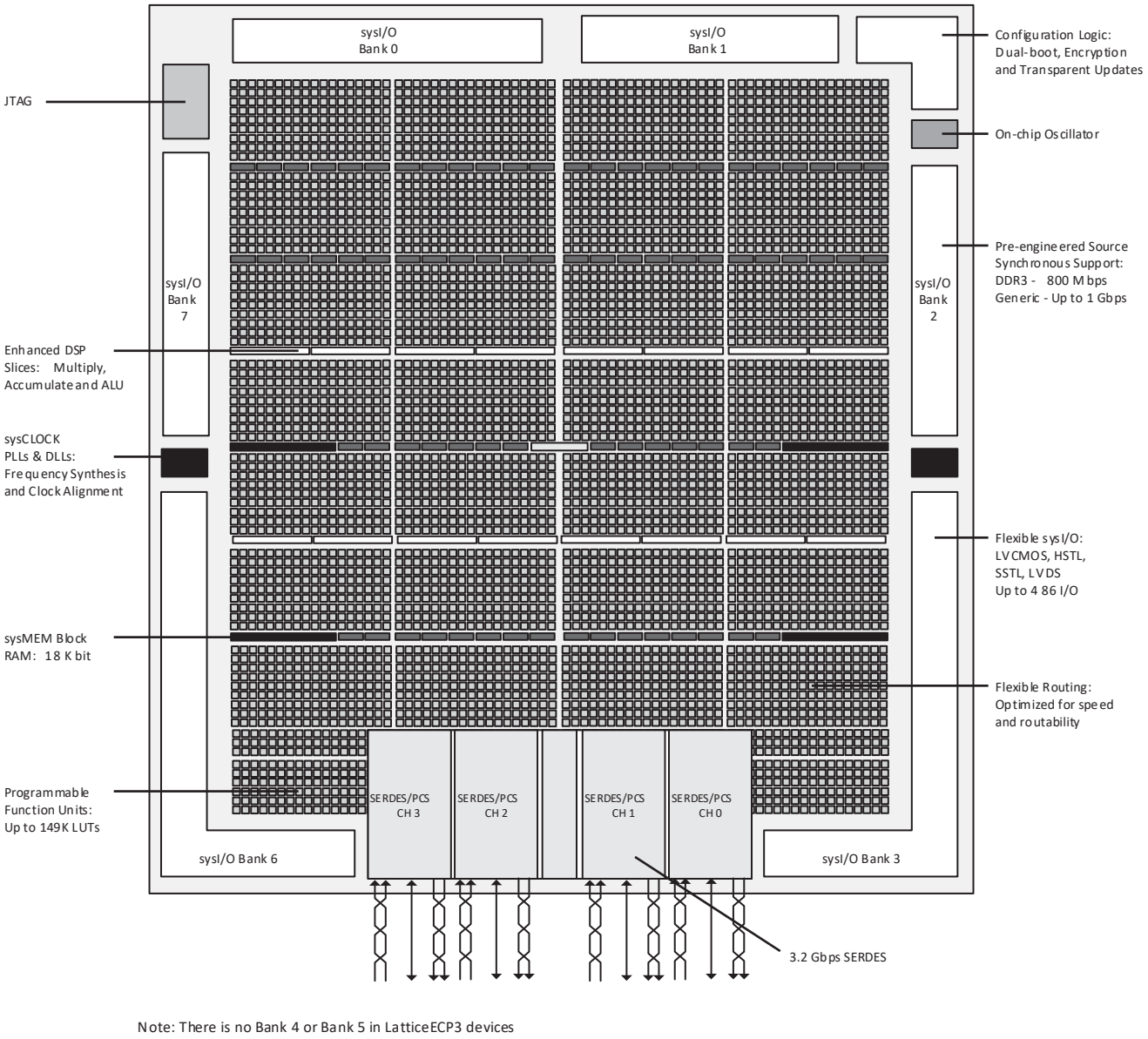
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LA-LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

Other blocks provided include PLLs, DLLs and configuration functions. The LA-LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to four Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LA-LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LA-LatticeECP3 devices use 1.2 V as their core voltage.

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Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices

Figure 3.1. Simplified Block Diagram, LA-LatticeECP3-35 Device (Top Level)

3.2. PFU Blocks

The core of the LA-LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 3.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

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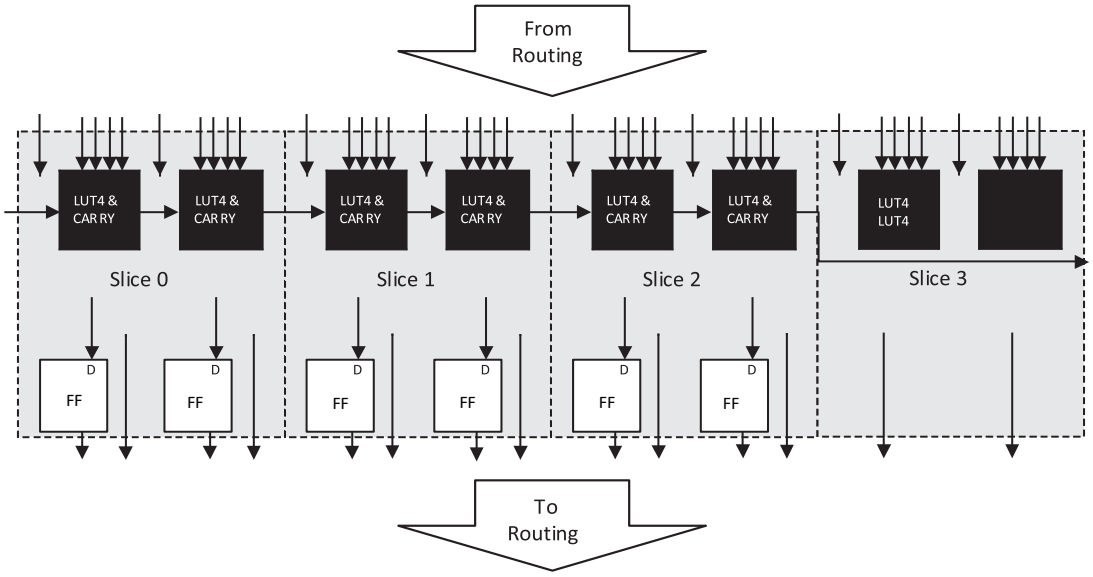


Figure 3.2. PFU Diagram

3.2.1. Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 3.1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

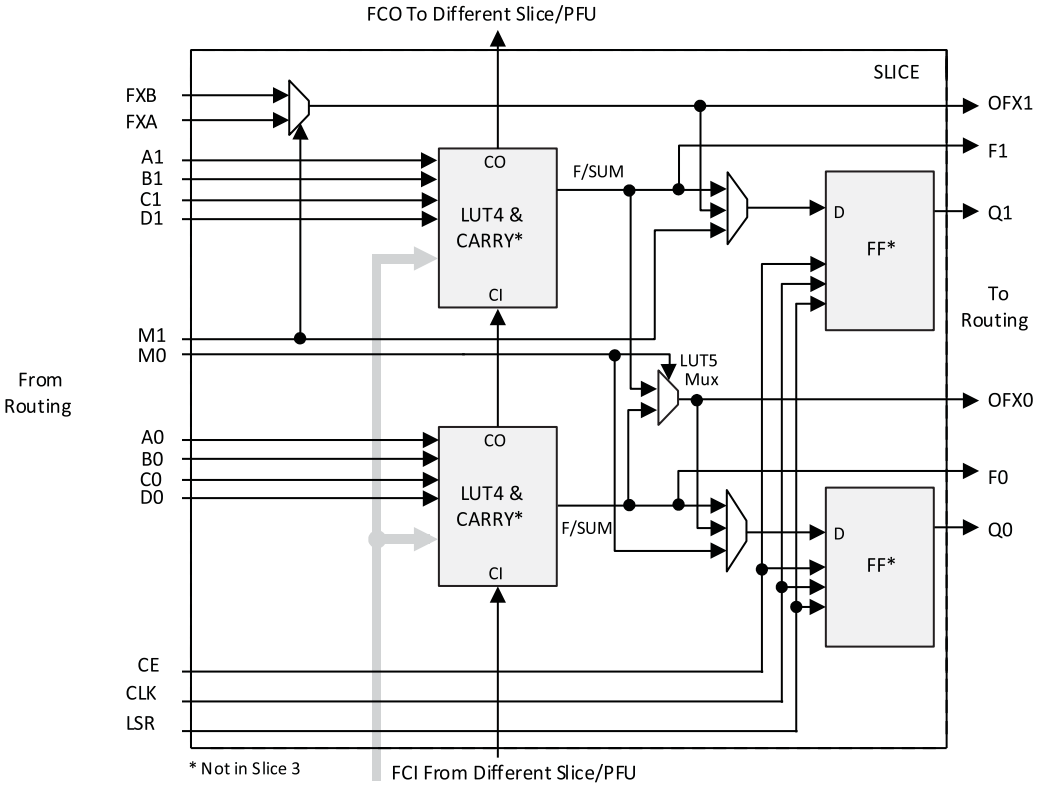
Table 3.1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 3.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 3.2 lists the signals associated with Slice 0 to Slice 2.

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For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 3.3. Slice Diagram

Table 3.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

Notes:

1. See Figure 3.2 for connection details.
2. Requires two PFUs.

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3.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16 x 4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16 x 1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LA-LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 3.3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LA-LatticeECP3 devices, please see LatticeECP3 Memory Usage Guide (FPGA-TN-02188).

Table 3.3. Number of Slices Required to Implement Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to LatticeECP3 Memory Usage Guide (FPGA-TN-02188).

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3.3. Routing

There are many resources provided in the LA-LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LA-LatticeECP3 family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

3.4. sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the LA-LatticeECP3 family support two to ten full-featured General Purpose PLLs.

3.4.1. General Purpose PLL

The architecture of the PLL is shown in Figure 3.4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Phase Frequency Detect Block (PFD) which detects first for the frequency, and then the phase, of the CLKI and CLKFB are the same which then drives the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the tLOCK parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Cycle/Duty Trim block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125 ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

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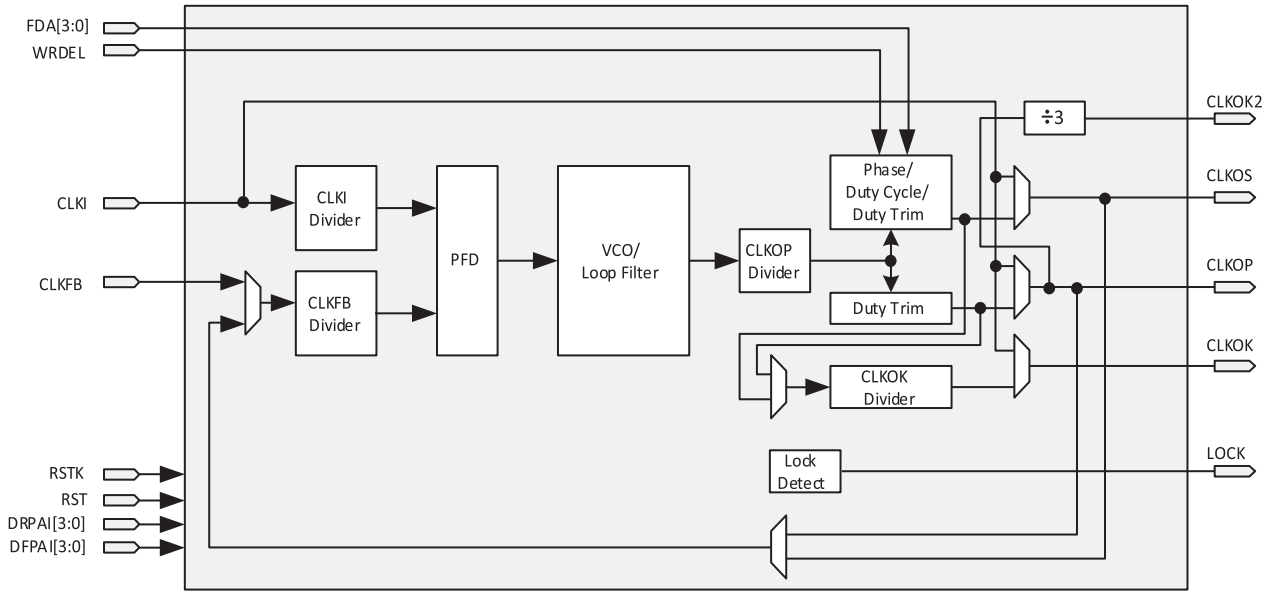


Figure 3.4. General Purpose PLL Diagram

Table 3.4 provides a description of the signals in the PLL blocks.

Table 3.4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

3.4.2. Delay Locked Loops (DLL)

In addition to PLLs, the LA-LatticeECP3 family of devices has two DLLs per device.

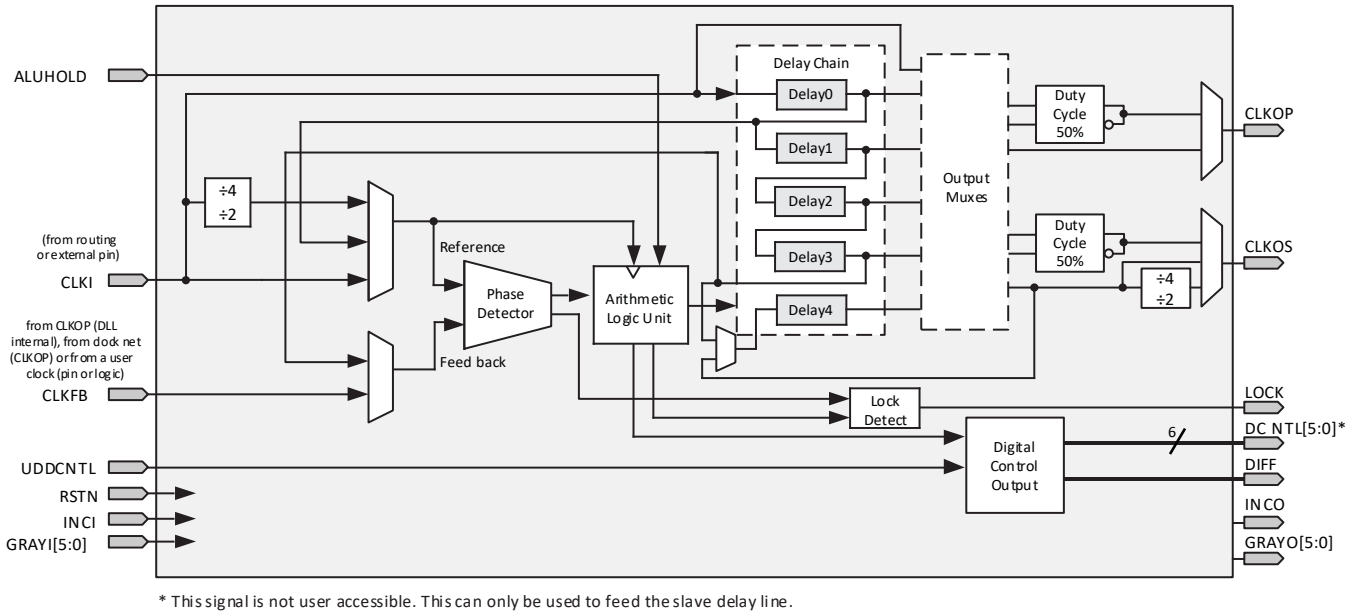
CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

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The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 3.5 shows the DLL block diagram and Table 3.5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.



* This signal is not user accessible. This can only be used to feed the slave delay line.

Figure 3.5. Delay Locked Loop Diagram (DLL)

Table 3.5. DLL Signals

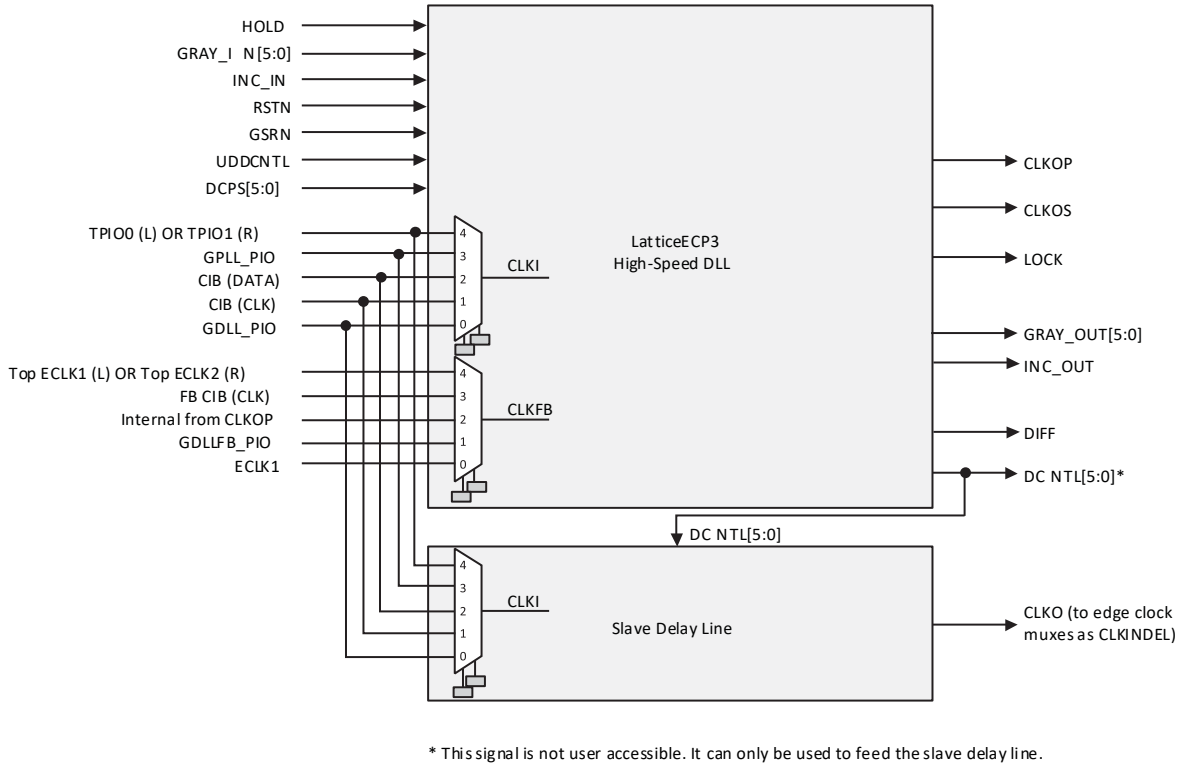
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LA-LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 3.6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

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For more information, please see LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02191).



* This signal is not user accessible. It can only be used to feed the slave delay line.

Figure 3.6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line

3.4.3. PLL/DLL Cascading

LA-LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

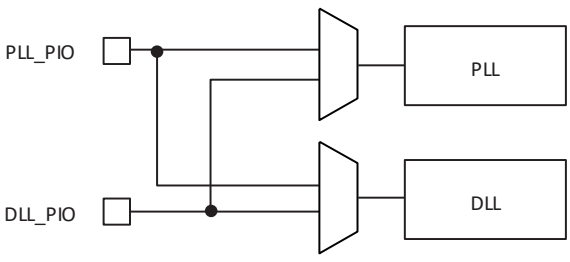
- PLL to PLL supported
- PLL to DLL supported

The DLLs in the LA-LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

3.4.4. PLL/DLL PIO Input Pin Connections

All LA-LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 3.7.



Note: Not every PLL has an associated DLL.

Figure 3.7. Sharing of PIO Pins by PLLs and DLLs in LA-LatticeECP3 Devices

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3.5. Clock Dividers

LA-LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02191). Figure 3.8 shows the clock divider connections.

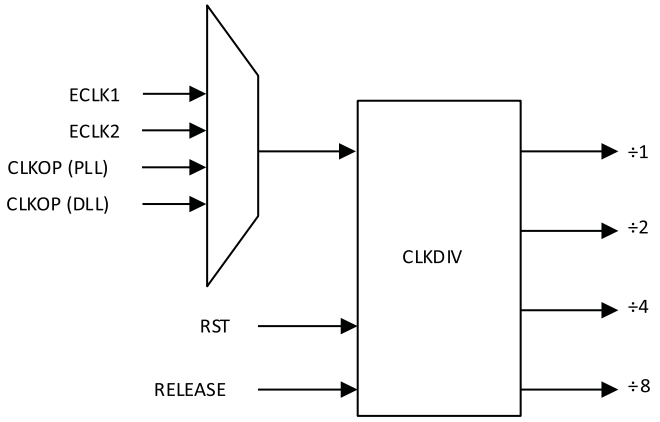


Figure 3.8. Clock Divider Connections

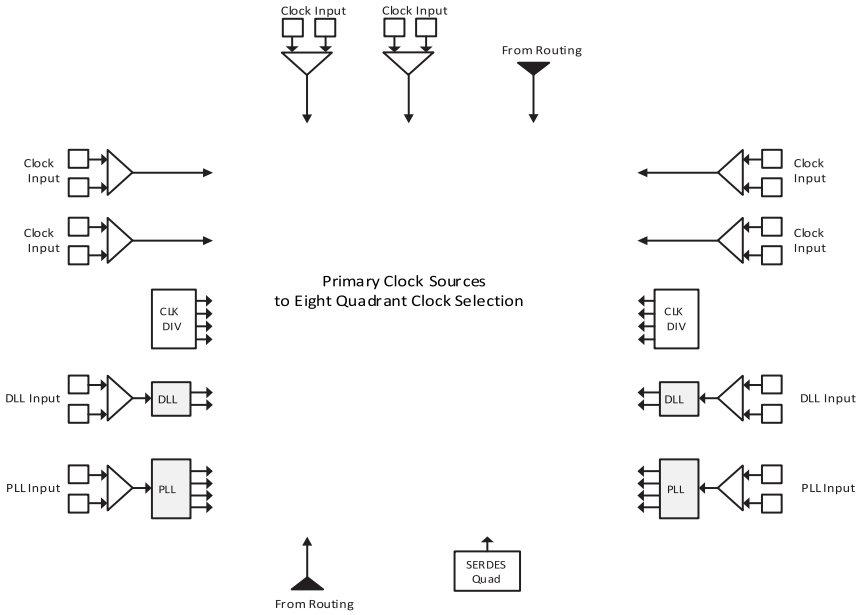
3.6. Clock Distribution Network

LA-LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/O, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

3.6.1. Primary Clock Sources

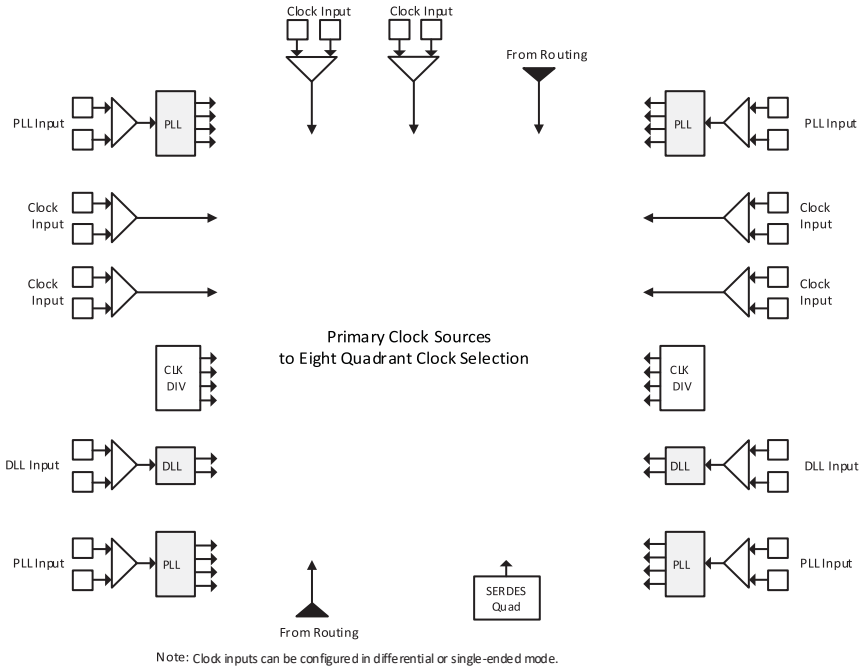
LA-LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quad. LA-LatticeECP3 devices have two to four sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figure 3.9 and Figure 3.10 and show the primary clock sources for LA-LatticeECP3 devices.

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Note: Clock inputs can be configured in differential or single-ended mode.

Figure 3.9. Primary Clock Sources for LA-LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 3.10. Primary Clock Sources for LA-LatticeECP3-35

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LA-LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 3.11 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

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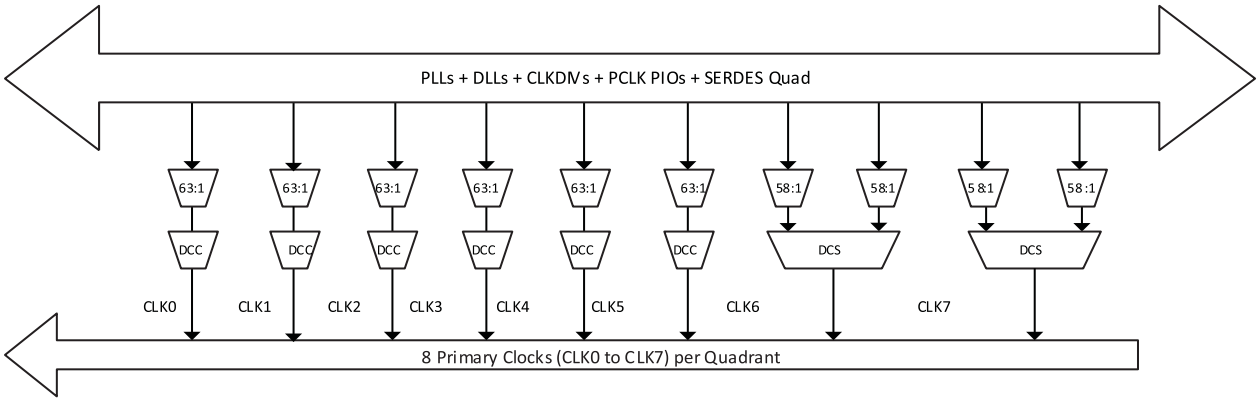


Figure 3.11. Per Quadrant Primary Clock Selection

3.6.2. Dynamic Clock Control (DCC)

The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

3.6.3. Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 3.11).

Figure 3.12 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

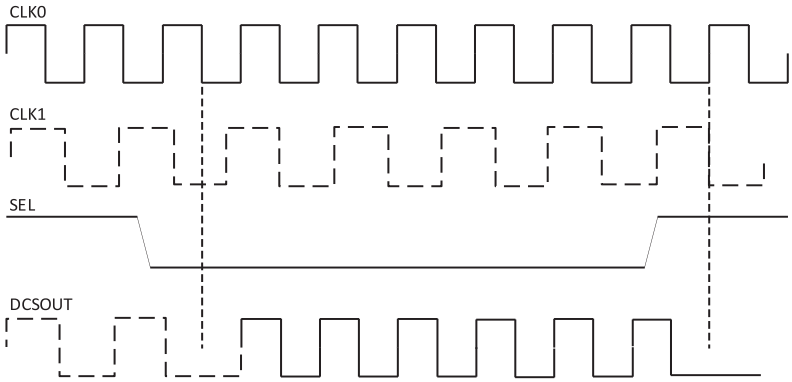


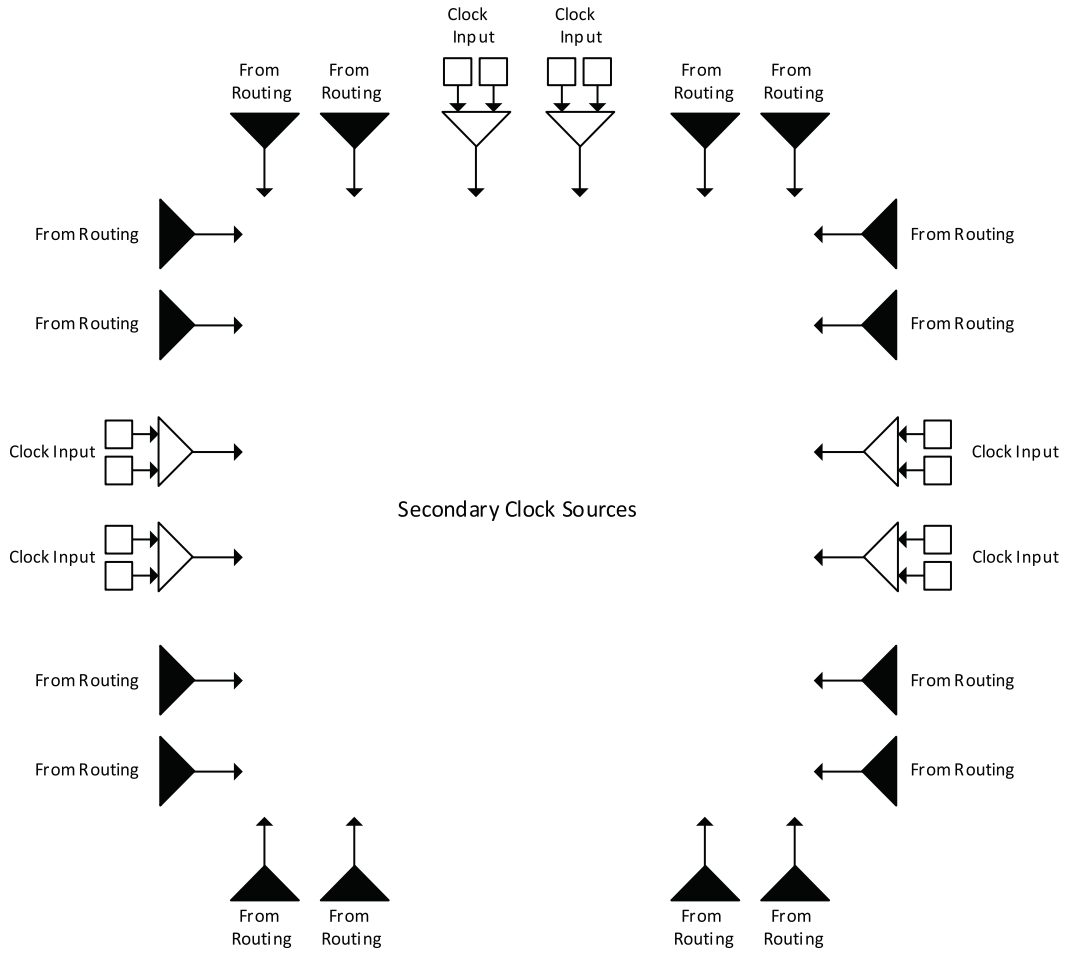
Figure 3.12. DCS Waveforms

3.6.4. Secondary Clock/Control Sources

LA-LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 3.13 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

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Note: Clock inputs can be configured in differential or single-ended mode.

Figure 3.13. Secondary Clock Sources

3.6.5. Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LA- LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 3.14 shows this special vertical routing channel and the 20 secondary clock regions for the LA-LatticeECP3 family of devices. All devices in the LA-LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Table 3.6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
LAE3-17	16
LAE3-35	16

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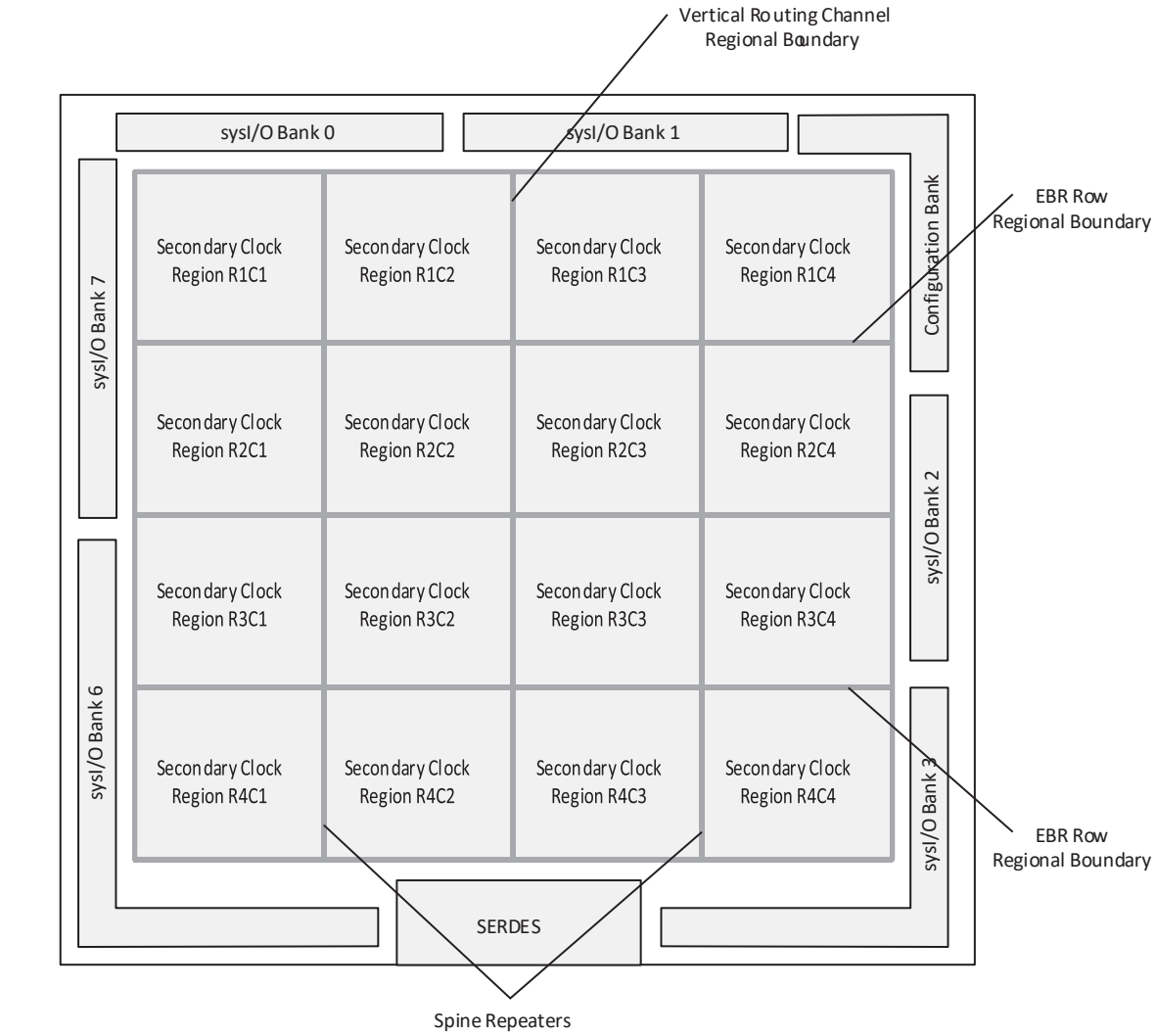


Figure 3.14. LA-LatticeECP3-17 and LA-LatticeECP3-35 Secondary Clock Regions

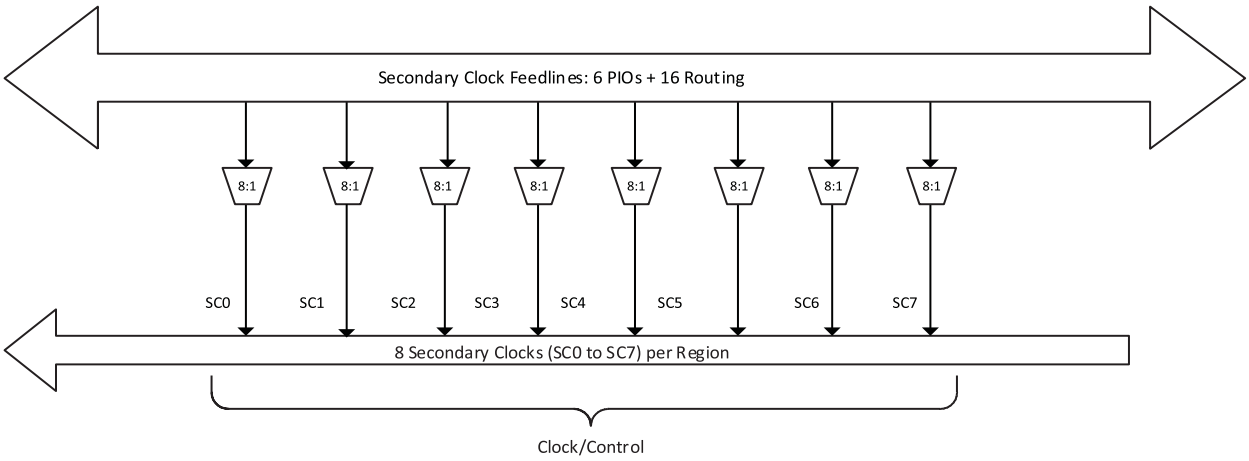


Figure 3.15. Per Region Secondary Clock Selection

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3.6.6. Slice Clock Selection

Figure 3.16 shows the clock selections and Figure 3.17 shows the control selections for Slice 0 through Slice 2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

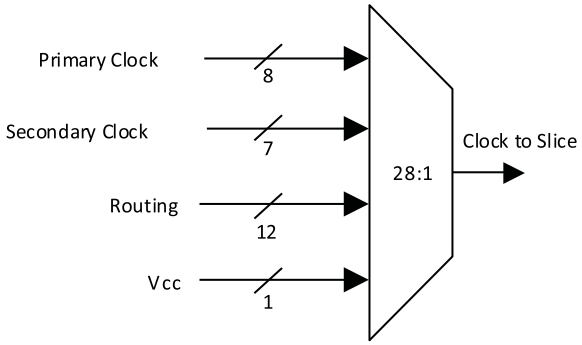


Figure 3.16. Slice 0 through Slice 2 Clock Selection

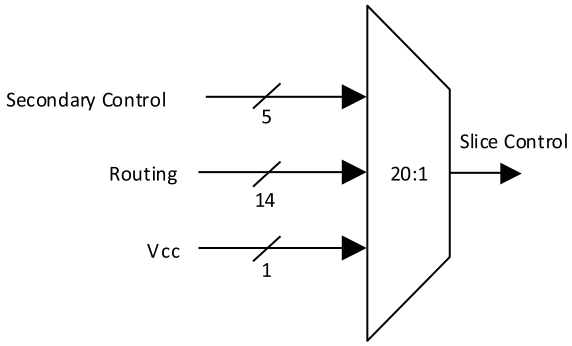
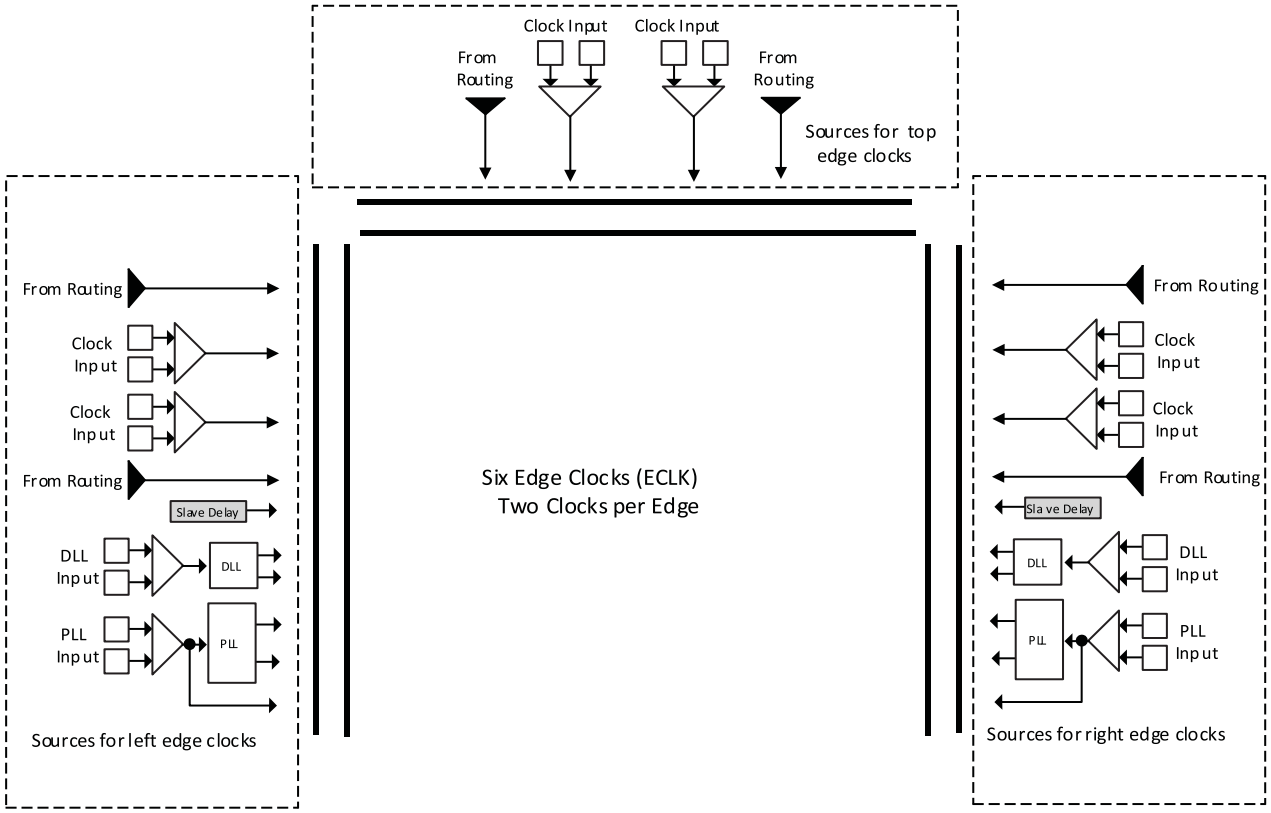


Figure 3.17. Slice 0 through Slice 2 Control Selection

3.6.7. Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 3.18.

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Notes:
1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

Figure 3.18. Edge Clock Sources

3.6.8. Edge Clock Routing

LA-LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 3.19 shows the selection muxes for these clocks.

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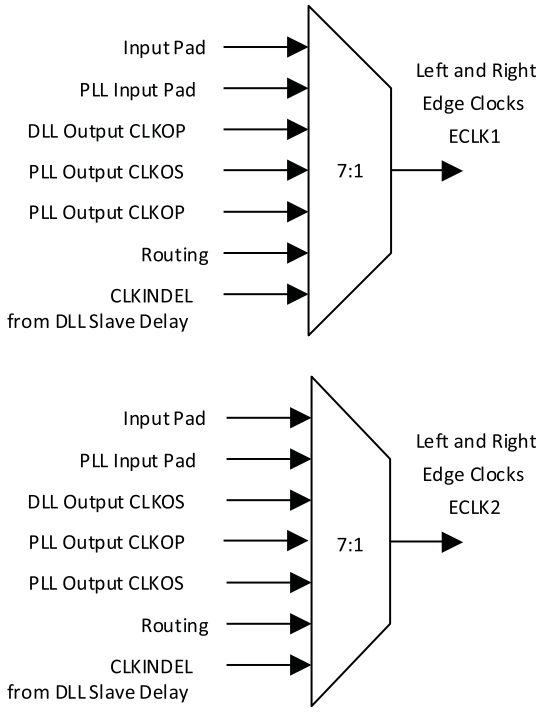


Figure 3.19. Sources of Edge Clock (Left and Right Edges)

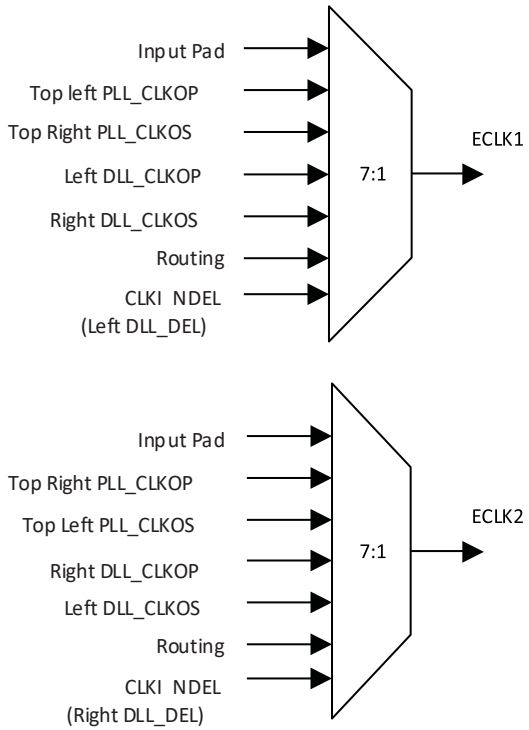


Figure 3.20. Sources of Edge Clock (Top Edge)

The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

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The edge clocks on the top, left, and right sides of the device can drive the secondary clocks or general routing resources of the device. The left and right side edge clocks also can drive the primary clock network through the clock dividers (CLKDIV).

3.7. sysMEM Memory

LA-LatticeECP3 devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers (via external PFUs).

3.7.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 3.7. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths. For more information, please see LatticeECP3 Memory Usage Guide (FPGA-TN-02188).

Table 3.7. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36 16,384 x 1 8,192 x 2
True Dual Port	4,096 x 4 2,048 x 9 1,024 x 18 16,384 x 1 8,192 x 2
Pseudo Dual Port	4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

3.7.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

3.7.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

3.7.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

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3.7.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

3.7.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 3.21.

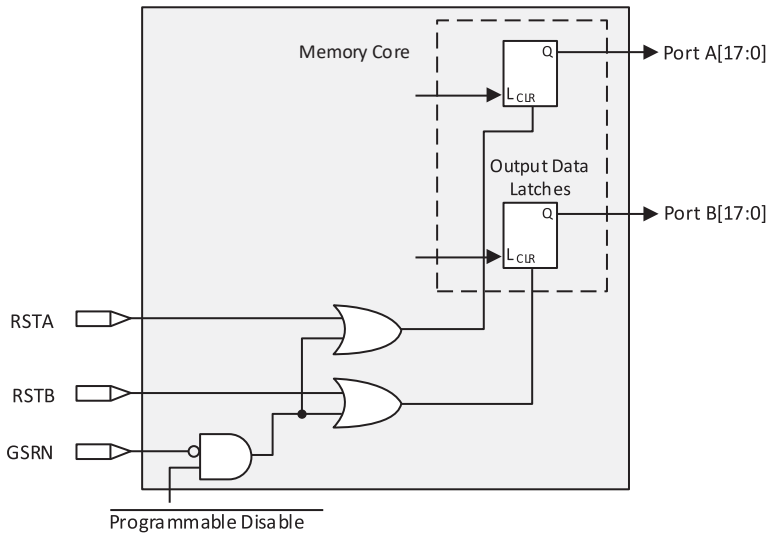


Figure 3.21. Memory Core Reset

For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

3.8. sysDSP™ Slice

The LA-LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, highperformance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

3.8.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LA-LatticeECP3, on the other hand, has many DSP slices that support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs.

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area by choosing appropriate levels of parallelism. Figure 3.22 compares the fully serial implementation to the mixed parallel and serial implementation.

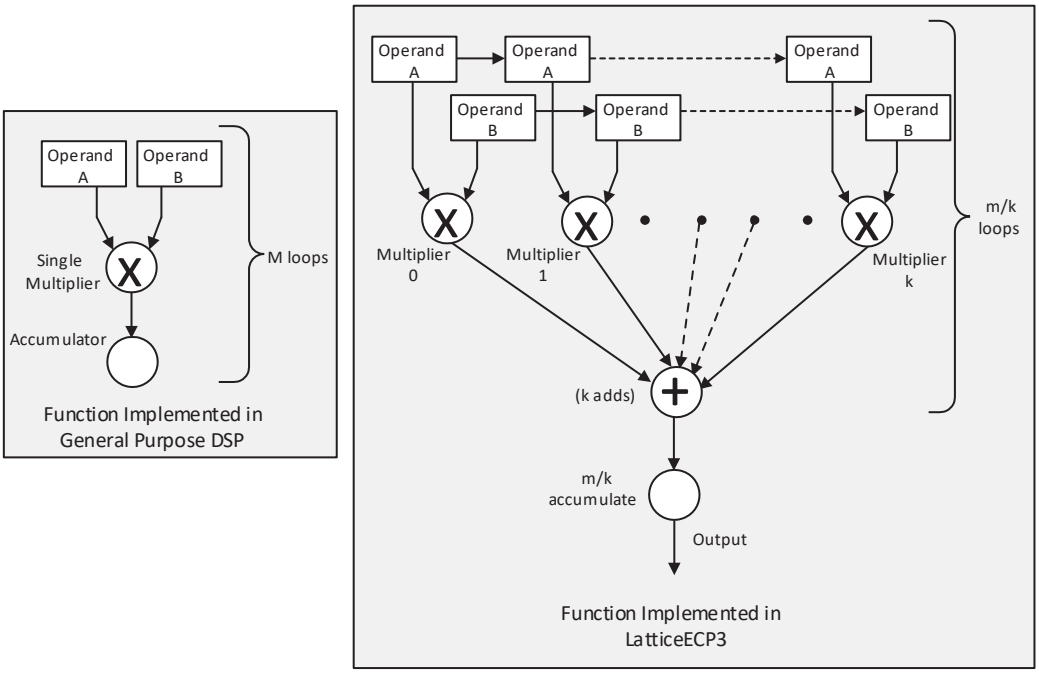


Figure 3.22. Comparison of General DSP and LA-LatticeECP3 Approaches

3.9. sysDSP Slice Architecture Features

The LA-LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The LA-LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18 x 36, two 18 x 18 or four 9 x 9 Multiplies per Slice).
- Multiply (36 x 36 by cascading across two sysDSP slices).
- Multiply Accumulate (up to 18 x 36 Multipliers feeding an Accumulator that can have up to 54-bit resolution).
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18 x 18 Multiplies feed into an accumulator that can accumulate up to 52 bits).
- Flexible saturation and rounding options to satisfy a diverse set of applications situations.
- Flexible cascading across DSP slices.
  - Minimizes fabric use for common DSP and ALU functions.
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only.
  - Provides matching pipeline registers.
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains.
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE.
  - Ternary arithmetic (addition/subtraction of three inputs).
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR).
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as, overflow, underflow and convergent rounding, and others.
  - Flexible cascading across slices to get larger functions.
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users.
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle.

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For most cases, as shown in Figure 3.23, the LA-LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2™ sysDSP block, such that, legacy applications can be targeted to the LA-LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LA-LatticeECP3 sysDSP slices, as shown in Figure 3.24.

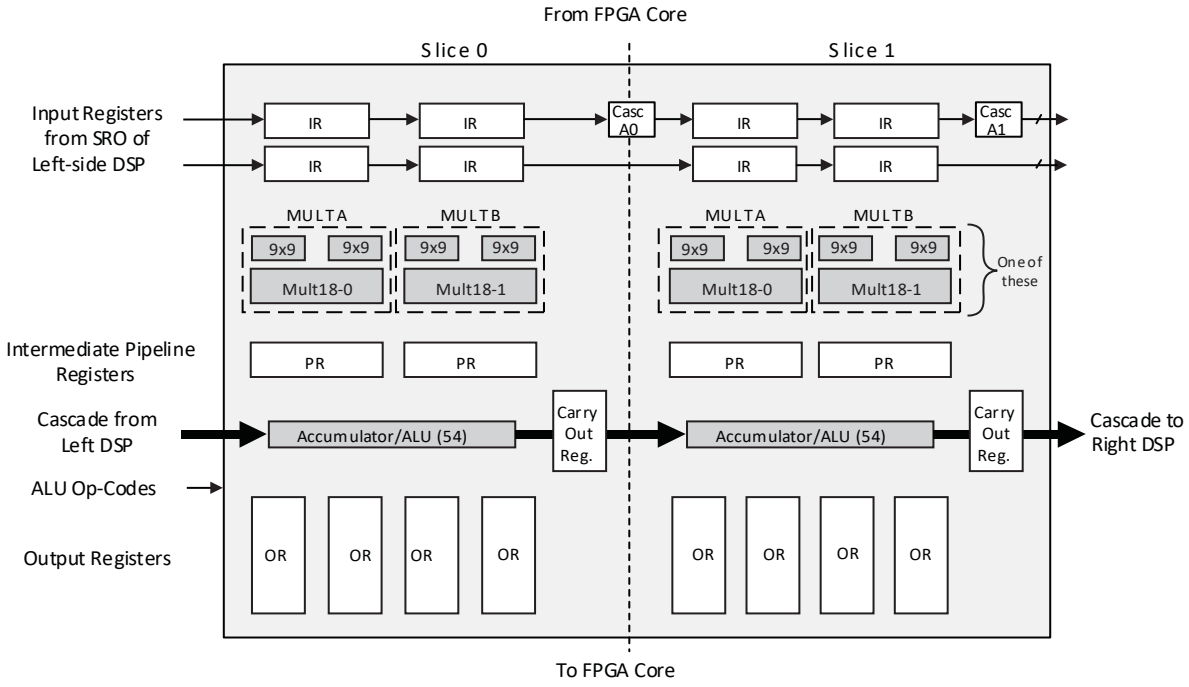
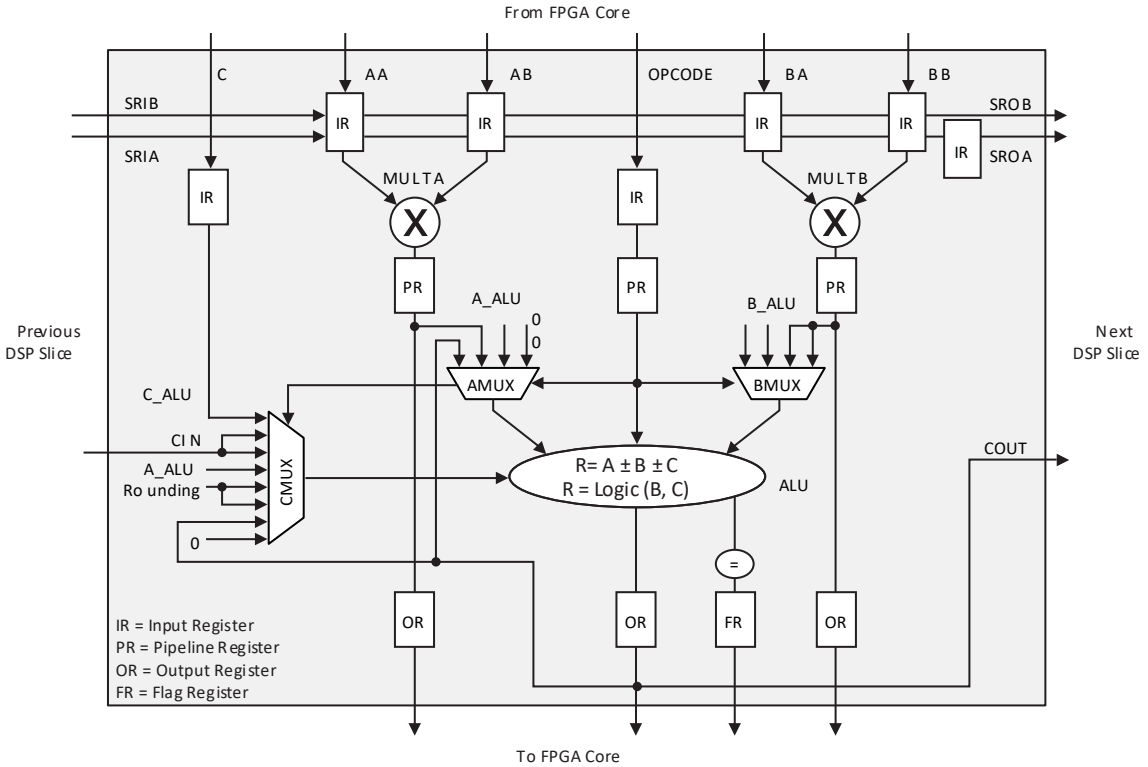


Figure 3.23. Simplified sysDSP Slice Block Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See LatticeECP3 sysDSP Usage Guide (FPGA-TN-02193), for further information.

Figure 3.24. Detailed sysDSP Slice Diagram

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The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 3.8 shows the capabilities of each of the LA-LatticeECP3 slices versus the above functions.

Table 3.8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1[1]	1/2	—

Note:

1. One slice can implement 1/2 9 x 9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, please refer to LatticeECP3 sysDSP Usage Guide (FPGA-TN-02193).

3.9.1. MULT DSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, AA and AB, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 3.25 shows the MULT sysDSP element.

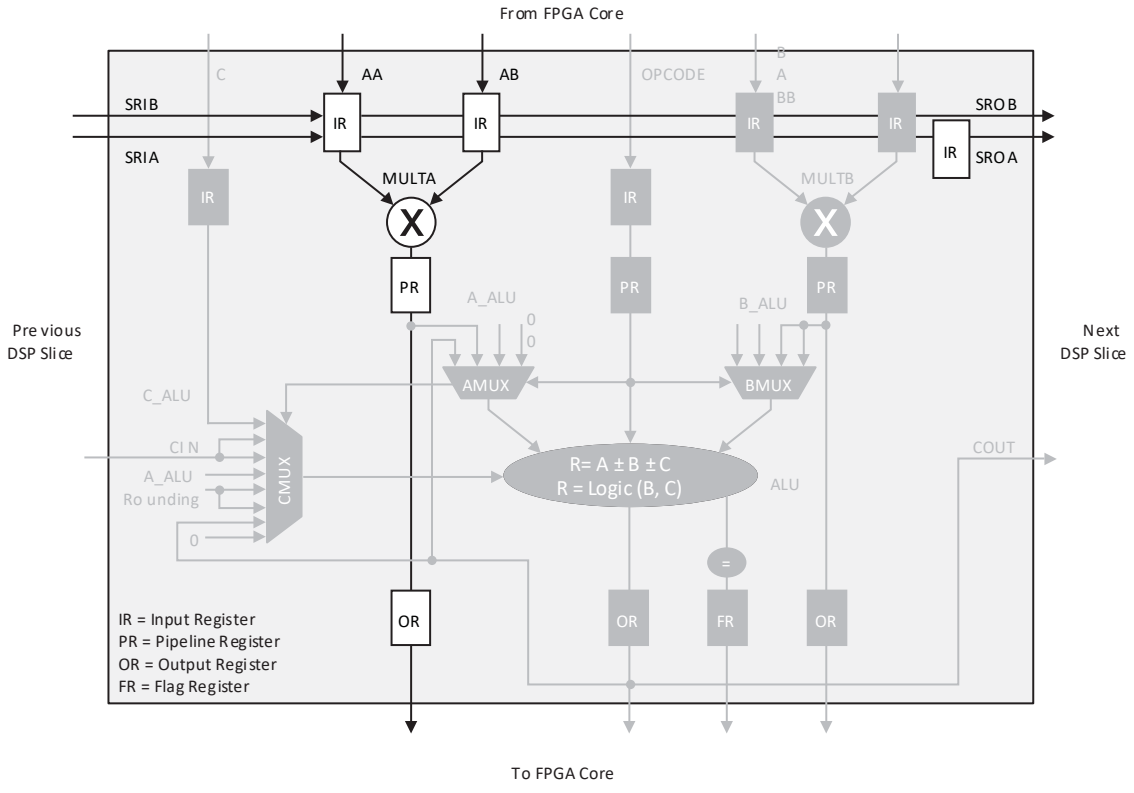


Figure 3.25. MULT sysDSP Element

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3.9.2. MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LA-LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 3.26 shows the MAC sysDSP element.

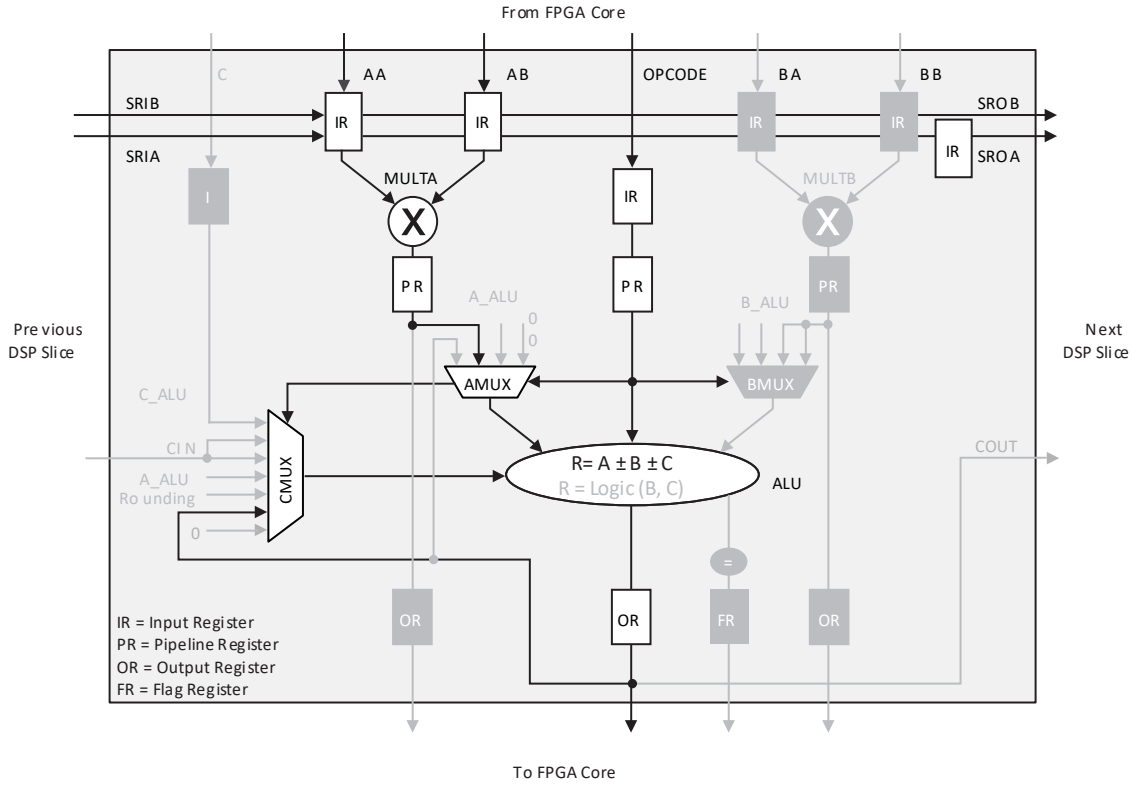


Figure 3.26. MAC DSP Element

3.9.3. MMAC DSP Element

The LA-LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 3.27 shows the MMAC sysDSP element.

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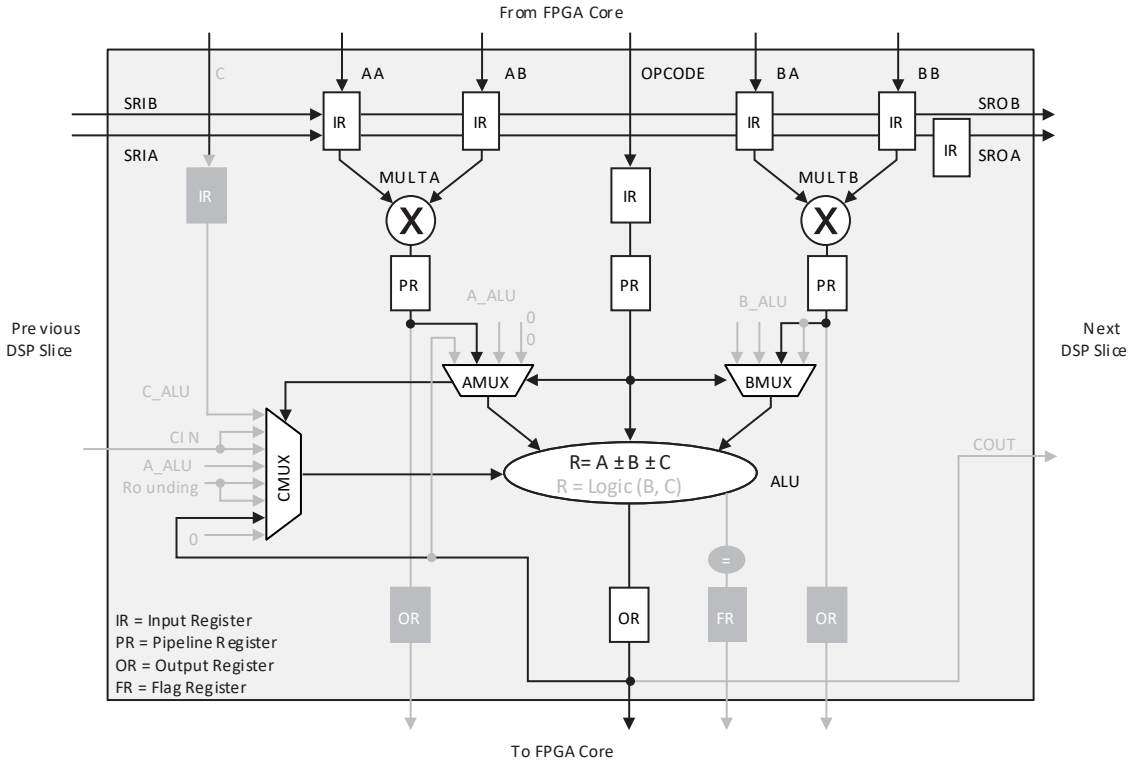


Figure 3.27. MMAC sysDSP Element

3.9.4. MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 3.28 shows the MULTADDSUB sysDSP element.

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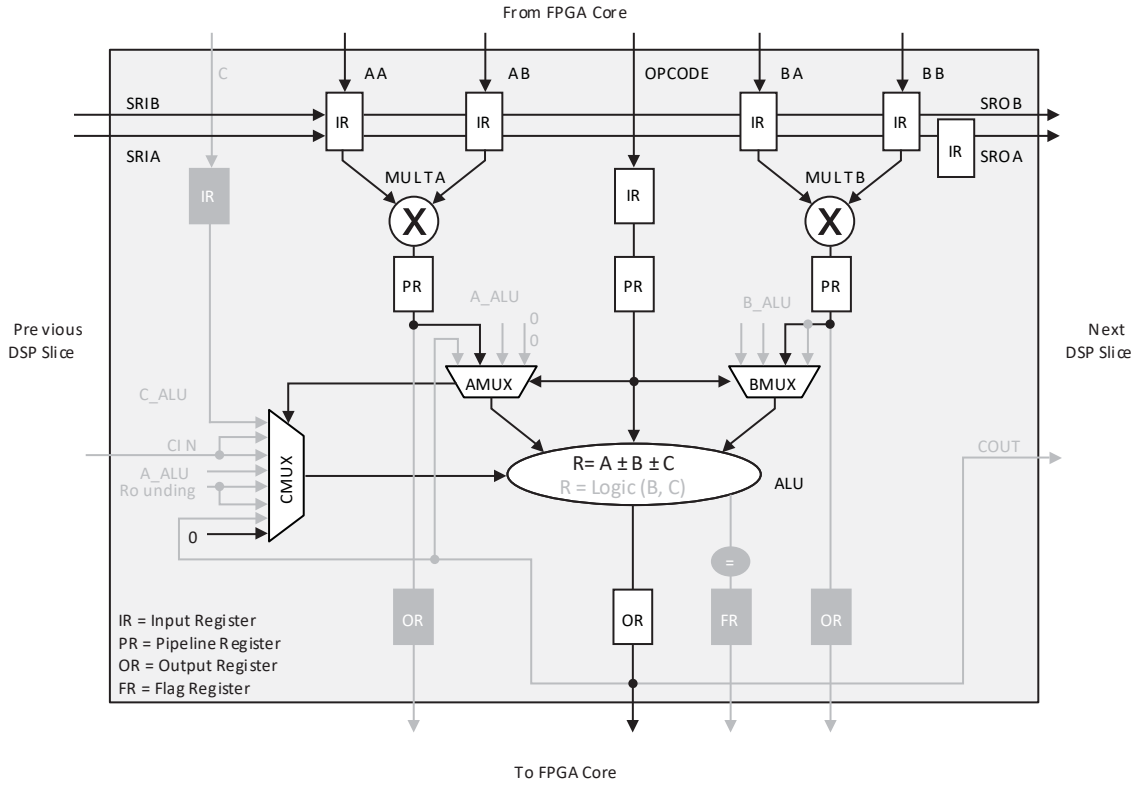


Figure 3.28. MULTADDSUB

3.9.5. MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 3.29 and Figure 3.30 show the MULTADDSUBSUM sysDSP element.

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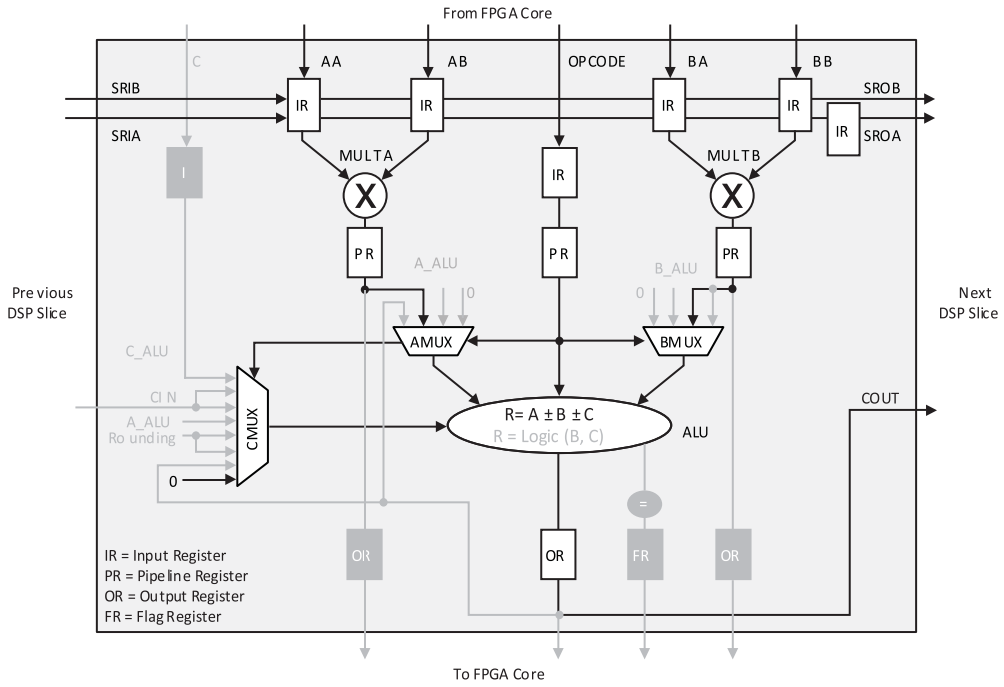


Figure 3.29. MULTADDSUBSUM Slice 0

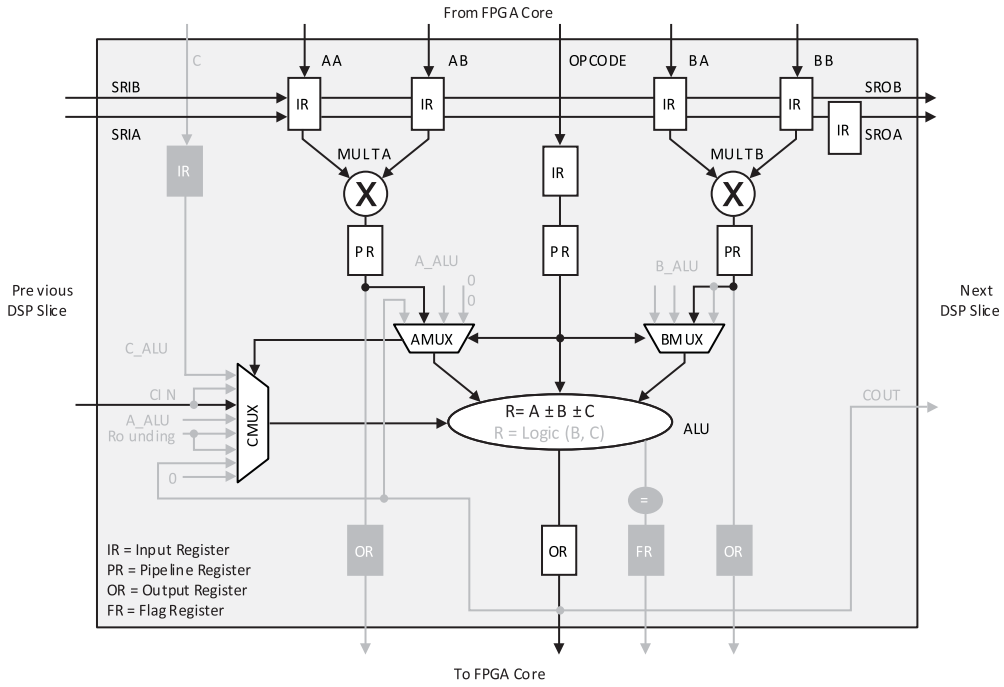


Figure 3.30. MULTADDSUBSUM Slice 1

3.10. Advanced sysDSP Slice Features

3.10.1. Cascading

The LA-LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

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3.10.2. Addition

The LA-LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

3.10.3. Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

3.10.4. ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

3.10.5. Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

3.10.6. Resources Available in the LA-LatticeECP3 Family

Table 3.9 shows the maximum number of multipliers for each member of the LA-LatticeECP3 family. Table 3.10 shows the maximum available EBR RAM Blocks in each LA-LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 3.9. Maximum Number of DSP Slices in the LA-LatticeECP3 Family

Device	DSP Slices	9 x 9 Multiplier	18 x 18 Multiplier	36 x 36 Multiplier
LAE3-17	12	48	24	6
LAE3-35	32	128	64	16

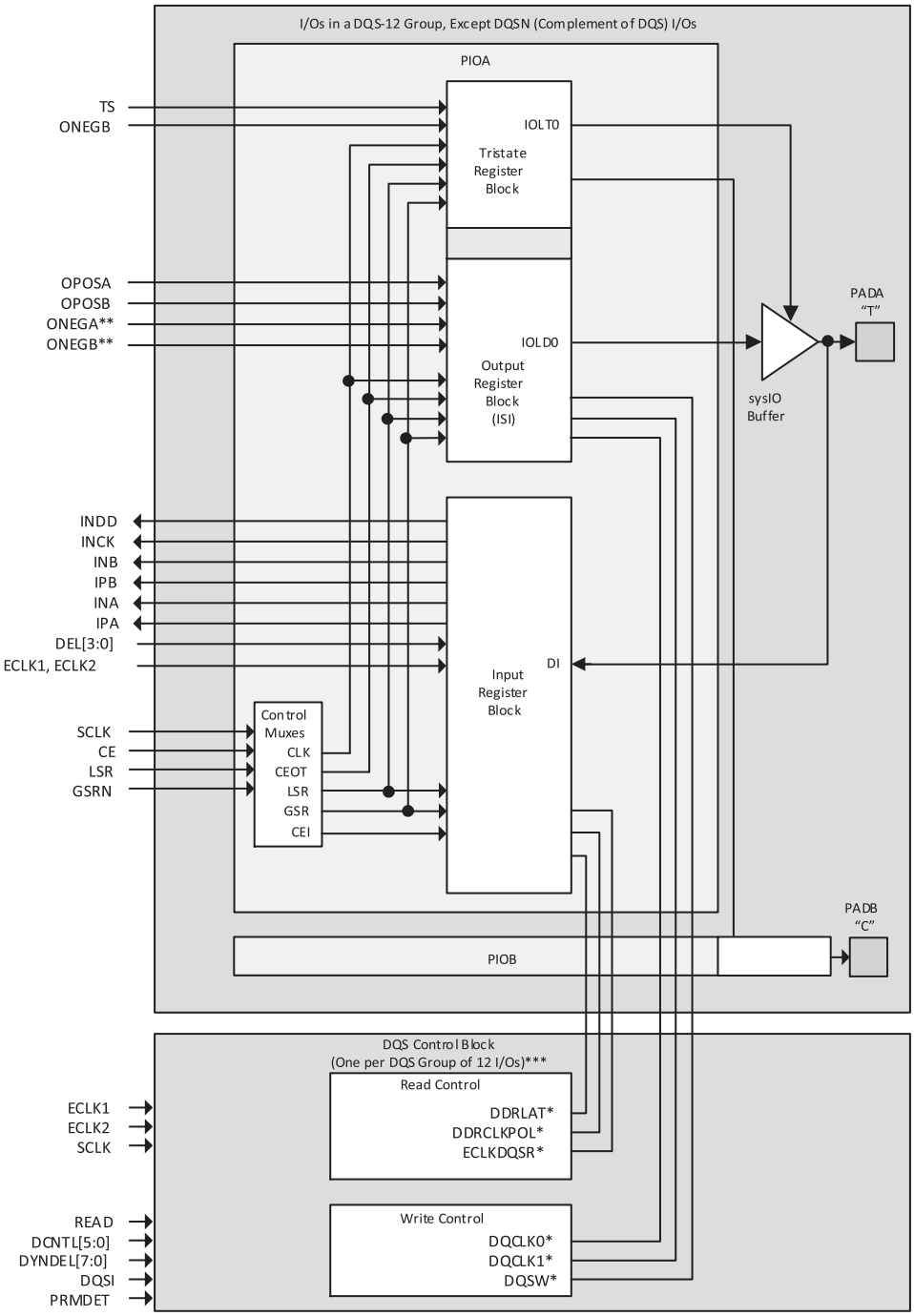
Table 3.10. Embedded SRAM in the LA-LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
LAE3-17	38	700

3.11. Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 3.31. The PIO Block supplies the output data (DO) and the tristate control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 3.11 provides the PIO signal list.

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* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

Figure 3.31. PIC Diagram

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as T and C) as shown in Figure 3.31. The PAD Labels T and C distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as LVDS inputs.

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Table 3.11. PIO Signal List

Name	Type	Description
INDD	Input Data	Register bypassed input. This is not the same port as INCK.
IPA, INA, IPB, INB	Input Data	Ports to core for input data
OPOSA, ONEGA[1], OPOSB, ONEGB[1]	Output Data	Output signals from core. An exception is the ONEGB port, used for tristate logic at the DQS pad.
CE	PIO Control	Clock enables for input and output block flip-flops.
SCLK	PIO Control	System Clock (PCLK) for input and output/TS blocks. Connected from clock ISB.
LSR	PIO Control	Local Set/Reset
ECLK1, ECLK2	PIO Control	Edge clock sources. Entire PIO selects one of two sources using mux.
ECLKDQSR[1]	Read Control	From DQS_STROBE, shifted strobe for memory interfaces only.
DDRCLKPOL[1]	Read Control	Ensures transfer from DQS domain to SCLK domain.
DDRLAT[1]	Read Control	Used to guarantee INDDRX2 gearing by selectively enabling a D-Flip-Flop in datapath.
DEL[3:0]	Read Control	Dynamic input delay control bits.
INCK	To Clock Distribution and PLL	PIO treated as clock PIO, path to distribute to primary clocks and PLL.
TS	Tristate Data	Tristate signal from core (SDR)
DQCLK0[1], DQCLK1[1]	Write Control	Two clocks edges, 90 degrees out of phase, used in output gearing.
DQSW[2]	Write Control	Used for output and tristate logic at DQS only.
DYNDEL[7:0]	Write Control	Shifting of write clocks for specific DQS group, using 6:0 each step is approximately 25 ps, 128 steps. Bit 7 is an invert (timing depends on input frequency). There is also a static control for this 8-bit setting, enabled with a memory cell.
DCNTL[6:0]	PIO Control	Original delay code from DDR DLL
DATAVALID[1]	Output Data	Status flag from DATAVALID logic, used to indicate when input data is captured in IOLOGIC and valid to core.
READ	For DQS_Strobe	Read signal for DDR memory interface
DQSI	For DQS_Strobe	Unshifted DQS strobe from input pad
PRMBDET	For DQS_Strobe	DQSI biased to go high when DQSI is tristate, goes to input logic block as well as core logic.
GSRN	Control from routing	Global Set/Reset

Notes:
1. Signals available on left/right/top edges only.
2. Selected PIO.

3.12. PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

3.12.1. Input Register Block

The input register blocks for the PIOs, in the left, right and top edges, contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 3.32 shows the input register block for the left, right and top edges. The input register block for the bottom edge contains one element to register the input signal and no DDR registers. The following description applies to the input register block for PIOs in the left, right and top edges only.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay

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or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

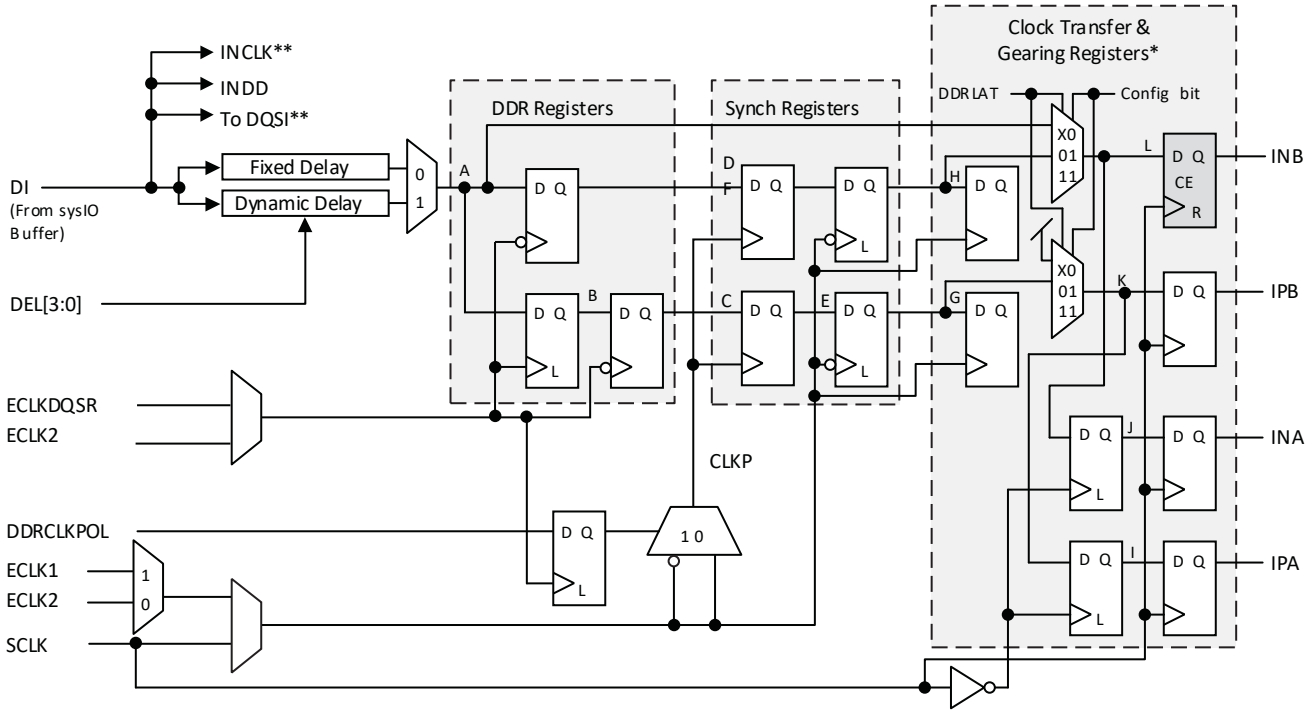
A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 3.29 provides further information on the use of the gearbox function.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 3.36 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184) Interface for more information on this topic.



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

Figure 3.32. Input Register Block for Left, Right and Top Edges

3.12.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as

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the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers but do not support generic DDR.

Figure 3.33 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 3.36 for an overview of the DQS write control logic.

Please see LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184) Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

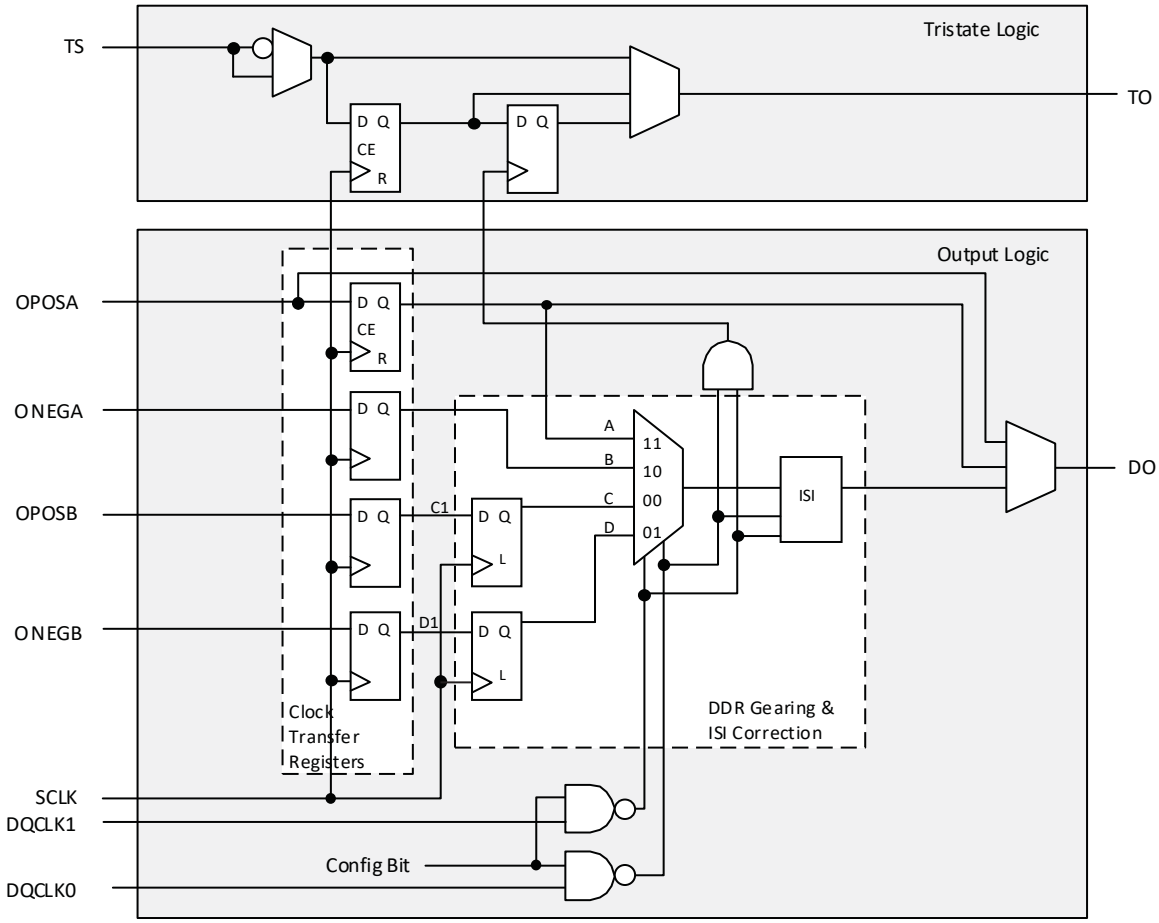


Figure 3.33. Output and Tristate Block for Left and Right Edges

3.12.3. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

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In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

3.12.4. ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS- 12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.

3.12.5. Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

3.13. DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

3.13.1. Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 3.34 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

3.13.2. Bottom Edge

PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

3.13.3. Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

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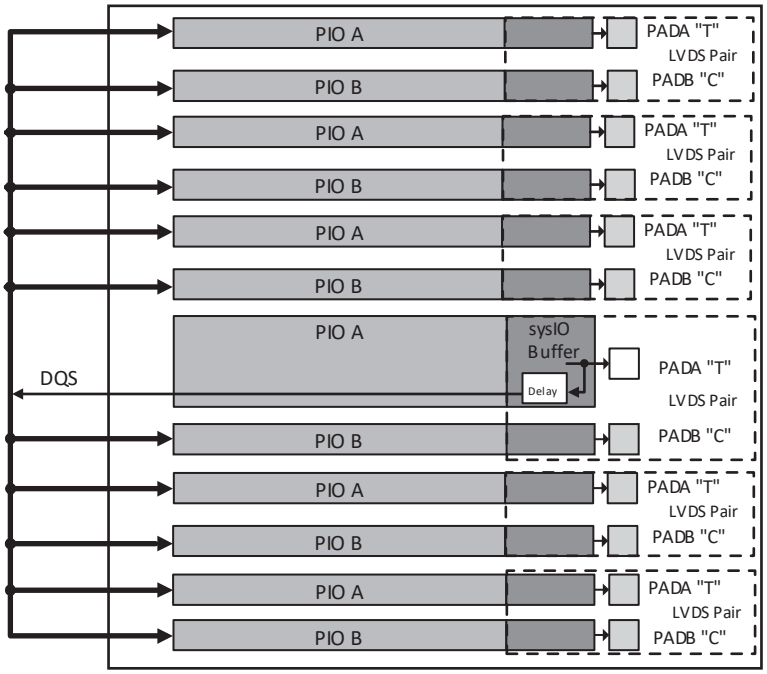


Figure 3.34. DQS Grouping on the Left, Right and Top Edges

3.13.4. DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 3.36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 3.34) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 3.35, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

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Figure 3.35 and Figure 3.36 show how the DQS transition signals that are routed to the PIOs. Please see LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184) for more information on this topic.

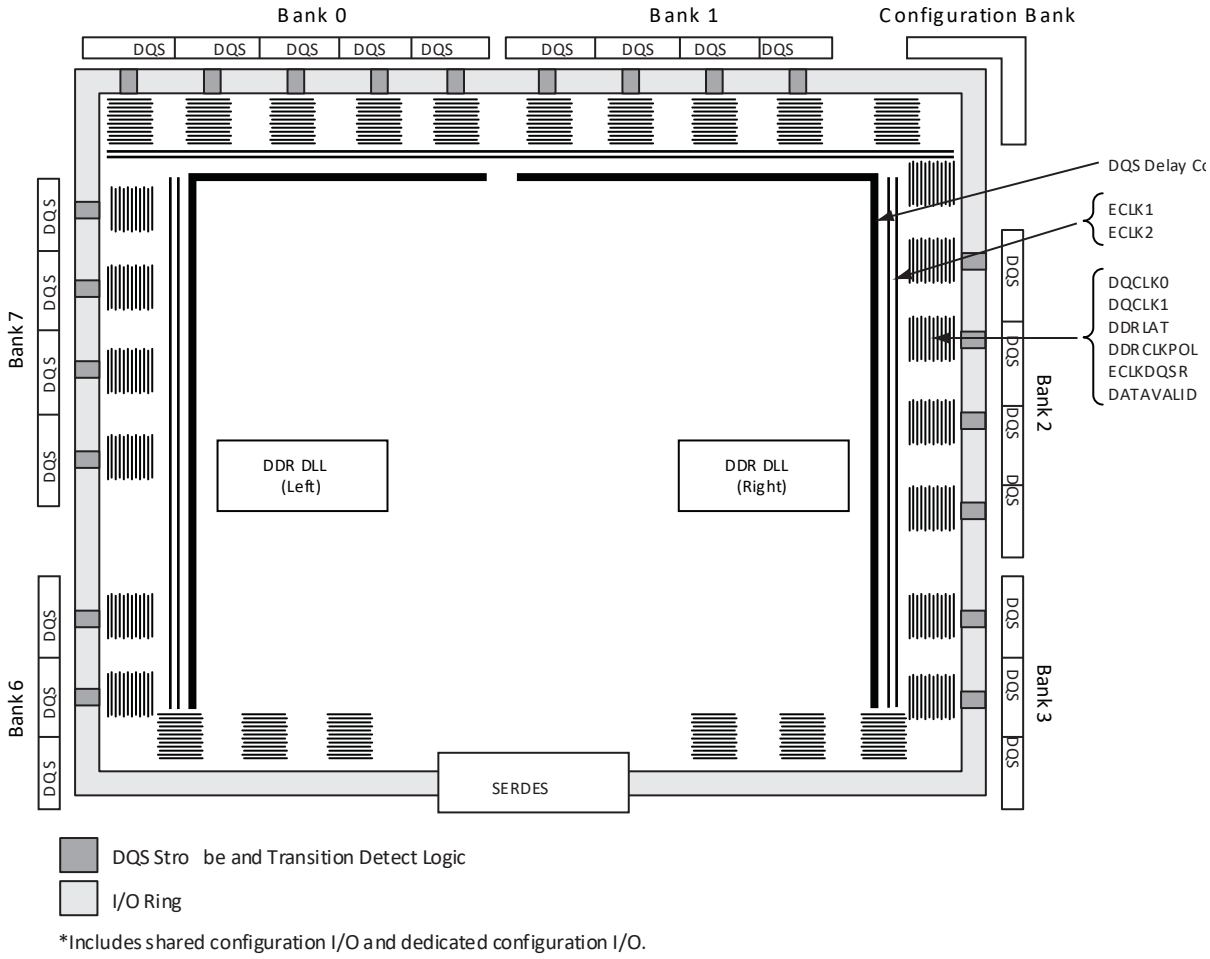


Figure 3.35. Edge Clock, DLL Calibration and DQS Local Bus Distribution

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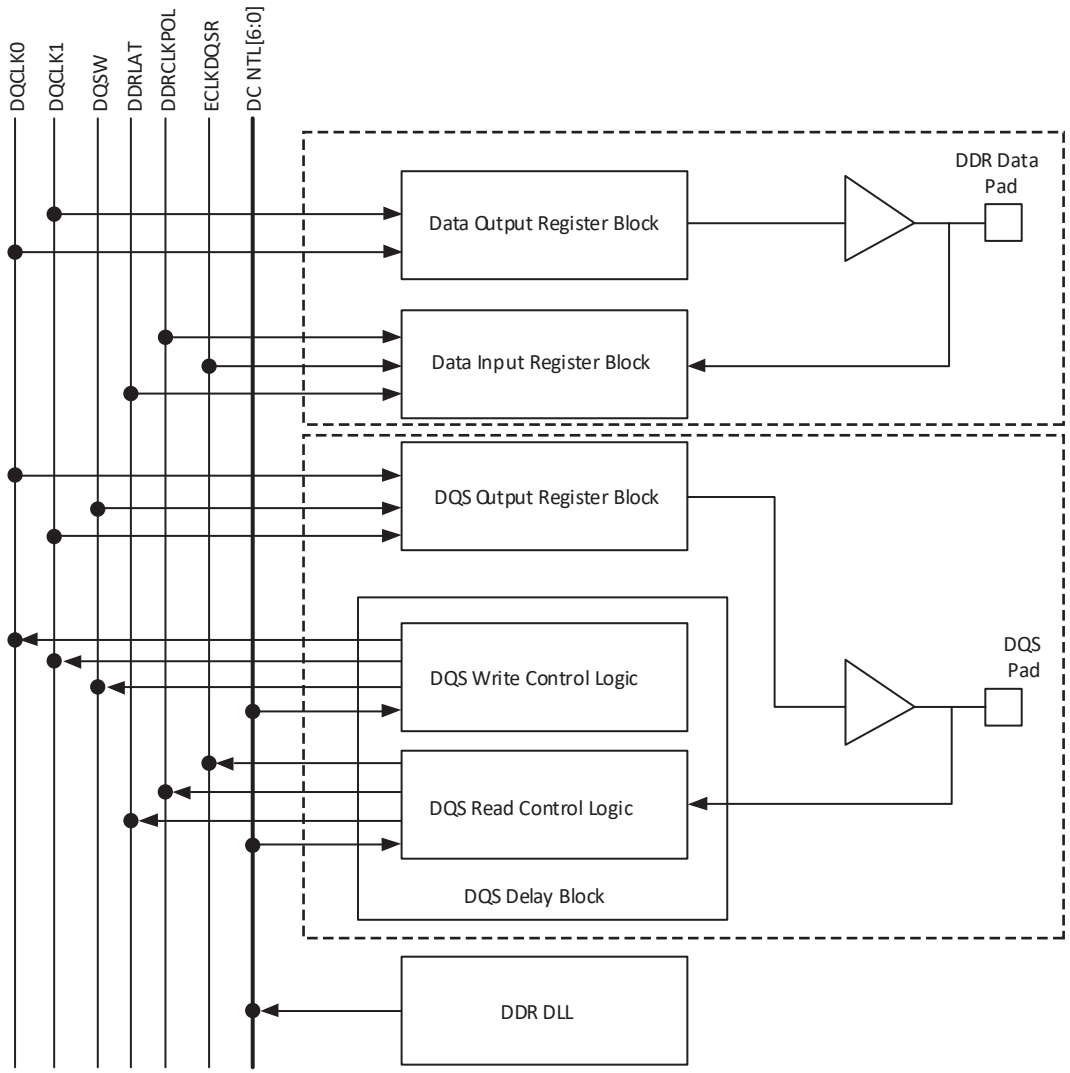


Figure 3.36. DQS Local Bus

3.13.5. Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LA-LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

3.13.6. DDR3 Memory Support

LA-LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

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To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LA-LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LA-LatticeECP3 supports the 1.5 V SSTL I/O standard required for the DDR3 memory interface. For more information, refer to the sysI/O section of this data sheet.

Please see LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184) Interface for more information on DDR Memory interface implementation in LA-LatticeECP3.

3.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

3.14.1. sysI/O Buffer Banks

LA-LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/O arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/O for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (VCCIO). In addition, each bank, except the Configuration Bank, has voltage references, VREF1 and VREF2, which allow it to be completely independent from the others. Figure 3.37 shows the seven banks and their associated supplies.

In LA-LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using VCCIO. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of VCCIO.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

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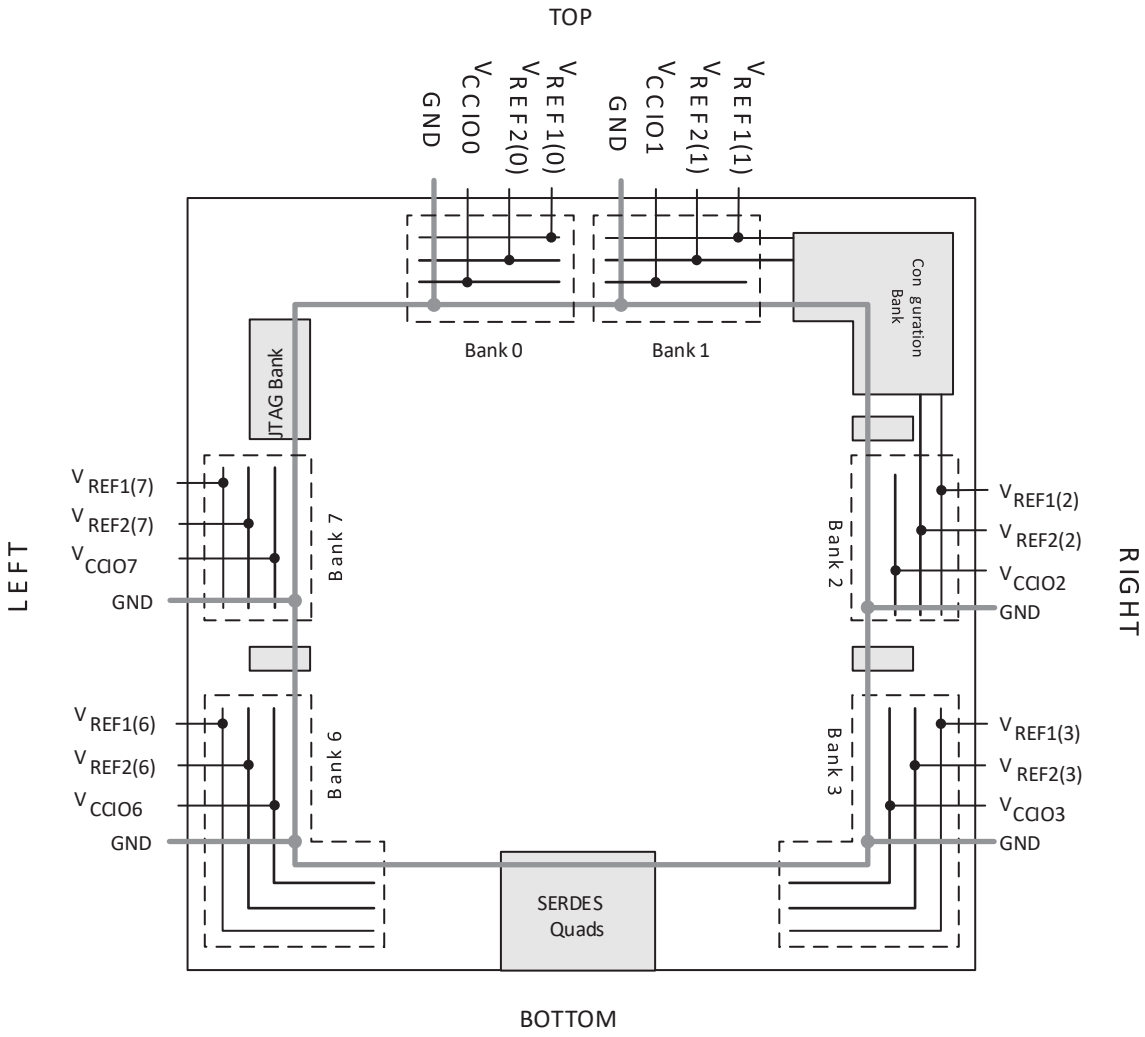


Figure 3.37. LA-LatticeECP3 Banks

LA-LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)**

   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

   The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**

   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are

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described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**

   The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

3.14.2. Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LA-LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

3.14.3. Supported sysI/O Standards

The LA-LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS

1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see LatticeECP3 sysIO Usage Guide (FPGA-TN-02194).

3.14.4. On-Chip Programmable Termination

The LA-LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 40, 50, or 60 Ω. External termination to Vtt should be used for DDR2 and DDR3 memory controller implementation.
- Common mode termination of 80, 100, 120 Ω for differential inputs

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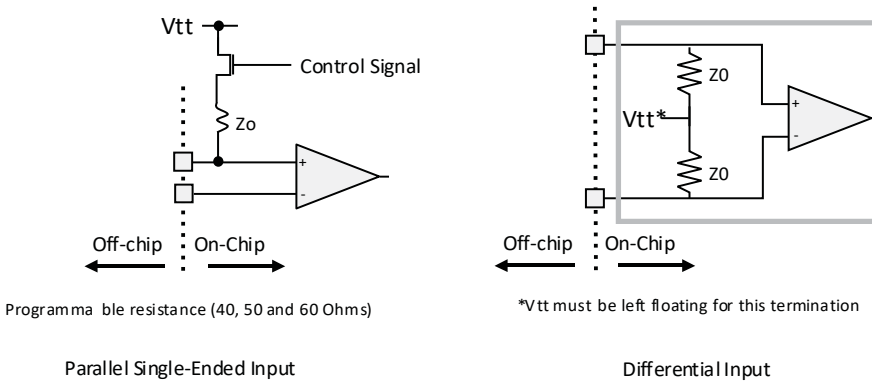


Figure 3.38. On-Chip Termination

See Table 3.12 for termination options for input modes.

Table 3.12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT[1, 2]	DIFFERENTIAL TERMINATION RESISTOR[1]
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

Notes:

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature. Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 and DDR3 memory controller.

Please see LatticeECP3 sysIO Usage Guide (FPGA-TN-02194) for on-chip termination usage and value ranges.

3.14.5. Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/O, and for differential inputs on the true I/O on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LA-LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input I/OLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

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3.14.6. Hot Socketing

LA-LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/O remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications1, 2, 3 section in this data sheet.

3.15. SERDES and PCS (Physical Coding Sublayer)

LA-LatticeECP3 devices feature up to 4 channels of embedded SERDES/PCS arranged as quad at the bottom of the devices supporting up to 3.2 Gbps data rate. Figure 3.39 shows the position of the quad block for the LA-LatticeECP3-35 devices. Table 3.14 shows the location of available SERDES Quad for both devices.

The LA-LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

The quad contains four dedicated SERDES for high speed, full duplex serial data transfer. The quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged as quad, multiple baud rates can be supported within a quad with the use of dedicated, per channel ÷1, ÷2 and ÷11 rate dividers.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190).

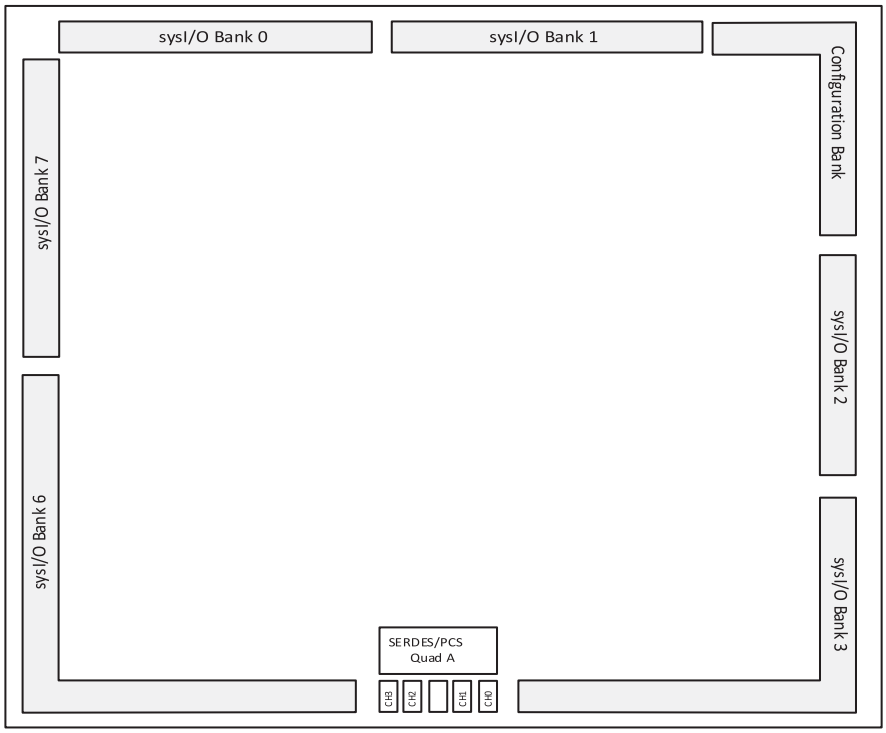


Figure 3.39. SERDES/PCS Quads (LA-LatticeECP3-35)

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Table 3.13. LA-LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143[1], 177[1], 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3[2]	155.52	x1	N/A
SONET-STS-12[2]	622.08	x1	N/A
SONET-STS-48[2]	2488	x1	N/A

Notes:

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.
2. The SONET protocol is supported in 8-bit SERDES mode. See LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190) for more information.

Table 3.14. LA-LatticeECP3 SERDES Standard Support

Package	LAE3-17	LAE3-35
256 ftBGA	1	1
328 csBGA	2 channels	—
484 fpBGA	1	1
672 fpBGA	—	1

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and deserialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 3.40 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

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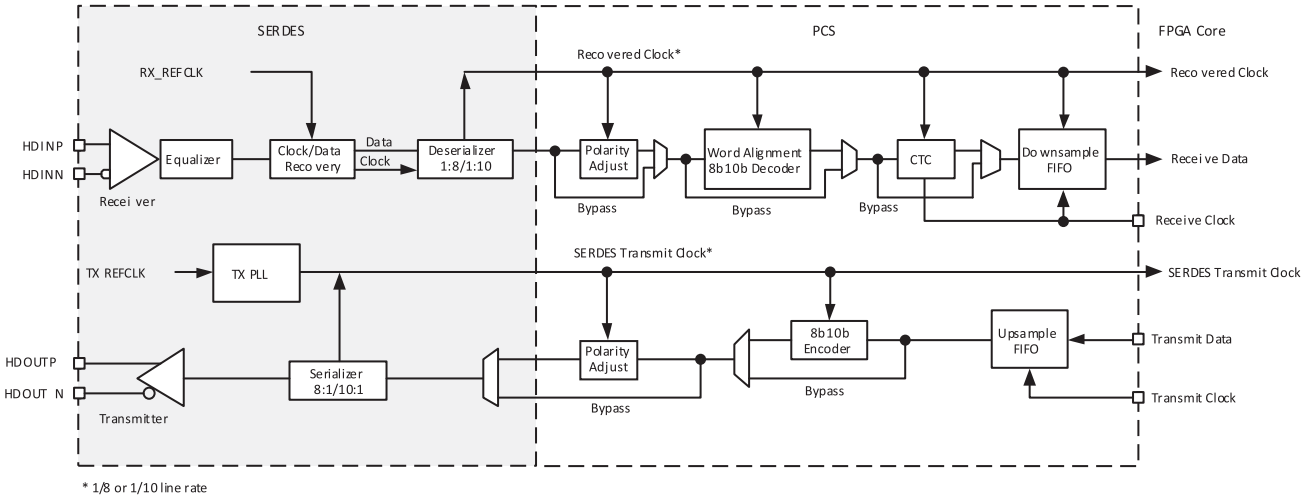


Figure 3.40. Simplified Channel Block Diagram for SERDES/PCS Block

3.15.1. PCS

As shown in Figure 3.40, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

3.15.2. SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tool supports all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LA-LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LA-LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 3.15 lists the allowable combination of primary and secondary protocol combinations.

3.16. Flexible Quad SERDES Architecture

The LA-LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LA-LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 3.15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 3.15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

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Furthermore, Table 3.15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 3.15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

There are some restrictions to be aware of when using spread spectrum. When a quad shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the quad is compatible with all protocols within the quad. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LA-LatticeECP3 architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, Serial RapidIO or SGMII channel within the same quad, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190).

3.17. IEEE 1149.1-Compliant Boundary Scan Testability

All LA-LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK and TMS. The test access port has its own supply voltage VCCJ and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see LatticeECP3 sysCONFIG Usage Guide (FPGA-TN-02192).

3.18. Device Configuration

All LA-LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/O used as dedicated pins with the remaining pins used as dual-use pins. See LatticeECP3 sysCONFIG Usage Guide (FPGA-TN-02192) for more information about using the dual-use pins as general purpose I/O.

There are various ways to configure a LA-LatticeECP3 device:

1. JTAG
2. Standard Serial Peripheral Interface (SPI and SPIm modes) - interface to boot PROM memory
3. System microprocessor to drive a x8 CPU port (PCM mode)
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Generic byte wide flash with a MachXO™ device, providing control and addressing

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On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LA-LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

3.18.1. Enhanced Configuration Options

LA-LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**

   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02198) for details.

2. **Dual-Boot Image Support**

   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LA-LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LA-LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see LatticeECP3 sysCONFIG Usage Guide (FPGA-TN-02192).

3.18.2. Soft Error Detect (SED) Support

LA-LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LA-LatticeECP3 device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see LatticeECP3 Soft Error Detection (SED) Usage Guide (FPGA-TN-02207).

3.18.3. External Resistor

LA-LatticeECP3 devices require a single external, 10K Ω ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

3.18.4. On-Chip Oscillator

Every LA-LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCCLK) for configuration. The oscillator and the MCCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCCLK is nominally 2.5 MHz. Table 3.16 lists all the available MCCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCCLK frequency of 2.5 MHz.

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This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see LatticeECP3 sysCONFIG Usage Guide (FPGA-TN-02192).

Table 3.16. Selectable Master Clock (MCCLK) Frequencies During Configuration (Nominal)

MCCLK (MHz)	MCCLK (MHz)
	10
2.5[1]	13
4.3	15[2]
5.4	20
6.9	26
8.1	33[3]
9.2	

Notes:

1. Software default MCCLK frequency. Hardware default is 3.1 MHz.
2. Maximum MCCLK with encryption enabled.
3. Maximum MCCLK without encryption.

3.19. Density Shifting

The LA-LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/O may become No Connects in smaller devices in the same package. Refer to the LatticeECP3 Pin Migration Tables and Diamond software for specific restrictions and limitations.

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings[1, 2, 3]

Supply Voltage VCC	–0.5 V to 1.32 V
Supply Voltage VCCAUX	–0.5 V to 3.75 V
Supply Voltage VCCJ	–0.5 V to 3.75 V
Output Supply Voltage VCCIO	–0.5 V to 3.75 V
Input or I/O Tristate Voltage Applied4	–0.5 tV o 3.75 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (TJ)	+125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.

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4.2. Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[2]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[2,4]	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2,3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}[5]	Termination Voltage	0.5	1.3125	V
t_{AUTO}	Junction Temperature, Automotive Operation	–40	125	°C
SERDES External Power Supply[6]				
V_{CCIB}	Input Buffer Power Supply (1.2 V)	1.14	1.26	V
	Input Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2 V)	1.14	1.26	V
	Output Buffer Power Supply (1.5 V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

Notes:

1. For correct operation, all supplies except VREF and VTT must be held in their valid operation range. This is true independent of feature usage.
2. If VCCIO or VCCJ is set to 1.2 V, they must be connected to the same power supply as VCC. If VCCIO or VCCJ is set to 3.3 V, they must be connected to the same power supply as VCCAUX.
3. See recommended voltages by I/O standard in subsequent table.
4. VCCAUX ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3.3 V.
5. If not used, VTT should be left floating.
6. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

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4.3. Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS[4]	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (Max.)	—	—	+/-1	mA
IDK[5]	Input or I/O Leakage Current	$0 \le V_{IN} < V_{CCIO}$	—	—	+/-1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO}$ + 0.5 V	—	18	—	mA

Notes:

1. VCC, VCCAUX and VCCIO should rise/fall monotonically.
2. IDK is additive to IPU, IPW or IBH.
3. LVCMOS and LVTTL only.
4. Applicable to general purpose I/O pins located on the top and bottom sides of the device.
5. Applicable to general purpose I/O pins located on the left and right sides of the device.

4.4. Hot Socketing Requirements[1, 2]

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

Notes:

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575 V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 4-channel device, the total input current would be 8 mA*4 channels *2 input pins per channel = 64 mA.

4.5. ESD Performance

Table 4.1. Electrostatic Discharge-Human Body Model[1]

Product	AEC-Q100-002 Component Classification
LAE3-17EA	H1C
LAE3-35EA	H1C

Note:

1. HBM Classification for Automotive products per AEC_Q100-002D

Table 4.2. Electrostatic Discharge-Charged Device Model[1]

Product	AEC-Q100-011 Component Classification
LAE3-17EA	C3A
LAE3-35EA	C3A

Note:

1. CDM Classification for Automotive products per AEC_Q100-011B

4.6. DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Low Leakage	$0 \le V_{IN} \le (V_{CCIO}$ - 0.2 V)	—	—	10	µA
I_{IH}[1, 3]	Input or I/O High Leakage	(V_{CCIO} - 0.2 V) < $V_{IN} \le$ 3.6 V	—	—	150	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	–30	—	–210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{CCIO}$	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	210	µA

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–210	µA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	5	8	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	5	7	pf

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0 MHz.
3. Applicable to general purpose I/O in top and bottom banks.
4. When used as VREF, maximum leakage= 25µA.

4.7. LA-LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical –6 Current	Typical –6L Current	Units
ICC	Core Power Supply Current	LAE3-17EA	49.4	29.8	mA
		LAE3-35EA	89.4	53.7	mA
ICCAUX	Auxiliary Power Supply Current	LAE3-17EA	19.4	18.3	mA
		LAE3-35EA	23.1	19.6	mA
ICCPLL	PLL Power Supply Current (Per PLL)	LAE3-17EA	0	0	mA
		LAE3-35EA	0.1	0.1	mA
ICCIO	Bank Power Supply Current (Per Bank)	LAE3-17EA	1.4	1.4	mA
		LAE3-35EA	1.4	1.4	mA
ICCJ	JTAG Power Supply Current	All Devices	2.5	2.5	mA
ICCA	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	LAE3-17EA	6.1	6.1	mA
		LAE3-35EA	6.1	6.1	mA

Notes:

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the VCCIO or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. TJ = 85 °C, power supplies at nominal voltage.
6. To determine the LA-LatticeECP3 peak start-up current data, use the Power Calculator tool.

4.8. SERDES Power Supply Requirements1, 2, 3

Over Recommended Operating Conditions

Symbol	Description	Typ.	Max.	Units
Standby (Power Down)				
I_{CCA-SB}	V_{CCA} current (per channel)	3	5	mA
$I_{CCIB-SB}$	Input buffer current (per channel)	—	—	mA
$I_{CCOB-SB}$	Output buffer current (per channel)	—	—	mA
Operating (Data Rate = 3.2 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	68	77	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	5	7	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	19	25	mA

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Symbol	Description	Typ.	Max.	Units
Operating (Data Rate = 2.5 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	66	76	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 1.25 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	62	72	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 250 Mbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	55	65	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	14	17	mA
Operating (Data Rate = 150 Mbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	55	65	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	14	17	mA

Notes:

1. Equalization enabled, pre-emphasis disabled.
2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
3. Pre-emphasis adds 20 mA to ICCA-OP data.

4.9. sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS33D	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15[3]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
LVDS25E	2.375	2.5	2.625	—	—	—
MLVDS[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
Mini LVDS	2.375	2.5	2.625	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—

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Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
RSDS[2]	2.375	2.5	2.625	—	—	—
RSDSE[1, 2]	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D[3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[2, 3], II[2, 3]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

Notes:

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. For input voltage compatibility, see LatticeECP3 sysIO Usage Guide (FPGA-TN-02194).
3. VREF is required when using Differential SSTL to interface to DDR memory.

4.10. sysI/O Single-Ended DC Electrical Characteristics[2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS33	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	–20, –16, –12, –8,–4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	–20, –16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	–16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS15	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	–8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS12	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	–6, –2
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVTTL33	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	–20, –16, –12, –8, –4
					0.2	V_{CCIO} - 0.2	0.1	–0.1
PCI33	–0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	–0.5
SSTL18_I	–0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	–6.7
SSTL18_II (DDR2 Memory)	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	–8
							11	–11
SSTL2_I	–0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	–7.6
							12	–12
SSTL2_II (DDR Memory)	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	–15.2
							20	–20
SSTL3_I	–0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	–8

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Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
SSTL3_II	–0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	–16
SSTL15 (DDR3 Memory)	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.3	V_{CCIO} - 0.3	7.5	–7.5
						V_{CCIO} * 0.8	9	–9
HSTL15_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
HSTL18_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	–8
							12	–12
HSTL18_II	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	–16

Note:

1. For electromigration, the average DC current drawn by I/O between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8 mA, where n is the number of I/O between bank GND connections or between the last VCCIO and GND in a bank and the end of a bank.
2. For I/Os with mixed voltage support, V_{OH} follows respective sysI/O bank V_{CCIO} supply voltage, and V_{IL} / V_{IH} follows the I/O signaling standard.

4.11. sysI/O Differential Electrical Characteristics

4.11.1. LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}[1], V_{INM}[1]	Input Voltage	—	0	—	2.4	V
V_{CM}[1]	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/– 100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/–10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver Outputs Shorted to Each Other	—	—	12	mA

Note:

1. On the left and right sides of the device, this specification is valid only for VCCIO = 2.5 V or 3.3 V

4.11.2. Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

4.11.3. LVDS25E

The top and bottom sides of LA-LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 4.1 is one possible solution for point-to-point signals.

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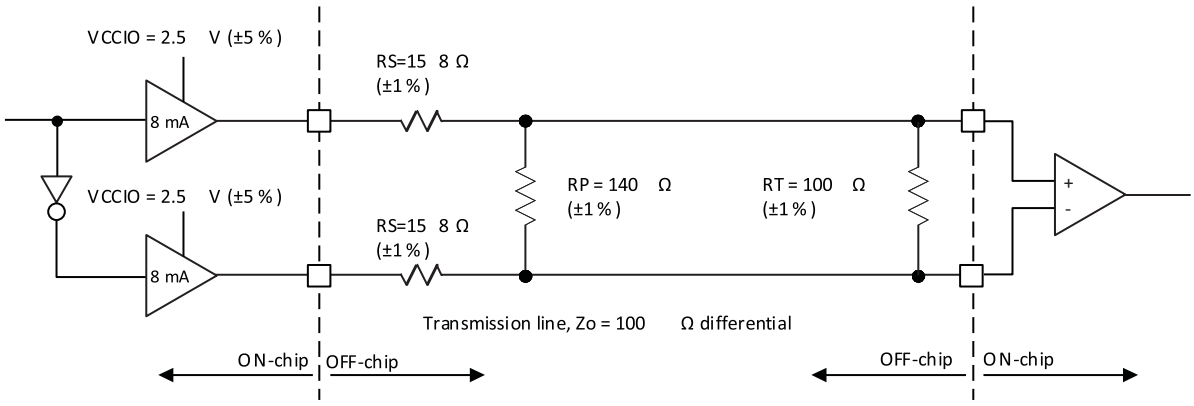


Figure 4.1. LVDS25E Output Termination Example

Table 4.3. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	158	Ω
R_P	Driver Parallel Resistor (+/–1%)	140	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

4.11.4. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

4.11.5. BLVDS25

The LA-LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 4.2 is one possible solution for bi-directional multi-point differential signals.

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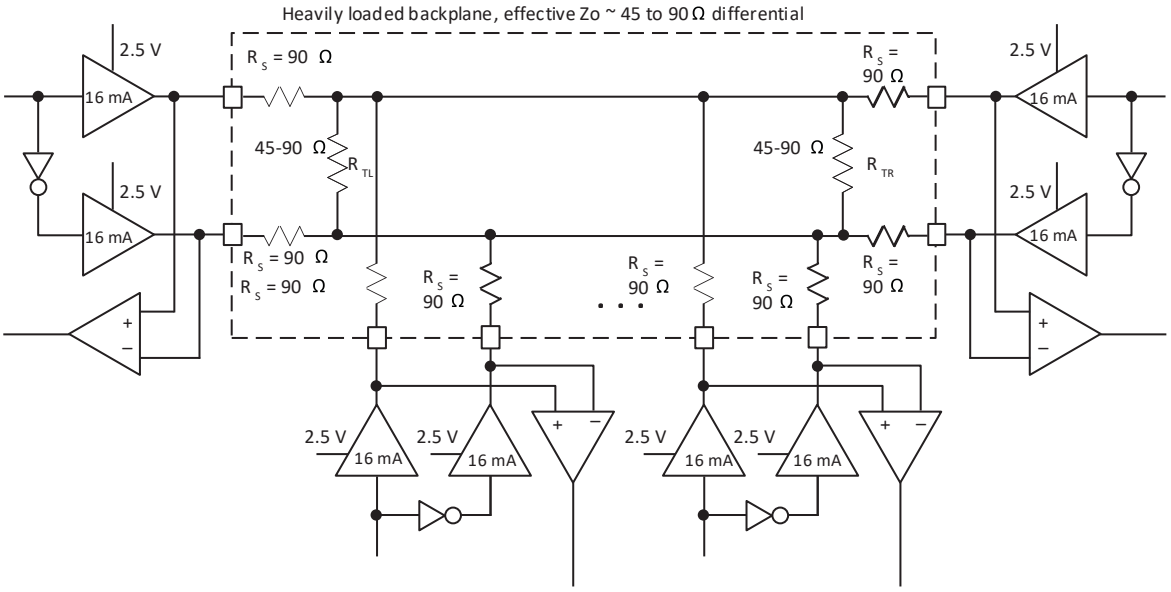


Figure 4.2. BLVDS25 Multi-point Output Example

Table 4.4. BLVDS25 DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45 Ω	Zo = 90 Ω	
V_{CCIO}	Output Driver Supply (+/– 5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/– 1%)	90.00	90.00	Ω
R_{TL}	Driver Parallel Resistor (+/– 1%)	45.00	90.00	Ω
R_{TR}	Receiver Termination (+/– 1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage	1.38	1.48	V
V_{OL}	Output Low Voltage	1.12	1.02	V
V_{OD}	Output Differential Voltage	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

Note:

1. For input buffer, see LVDS table.

4.11.6. LVPECL33

The LA-LatticeECP3 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 4.3 is one possible solution for point-to-point signals.

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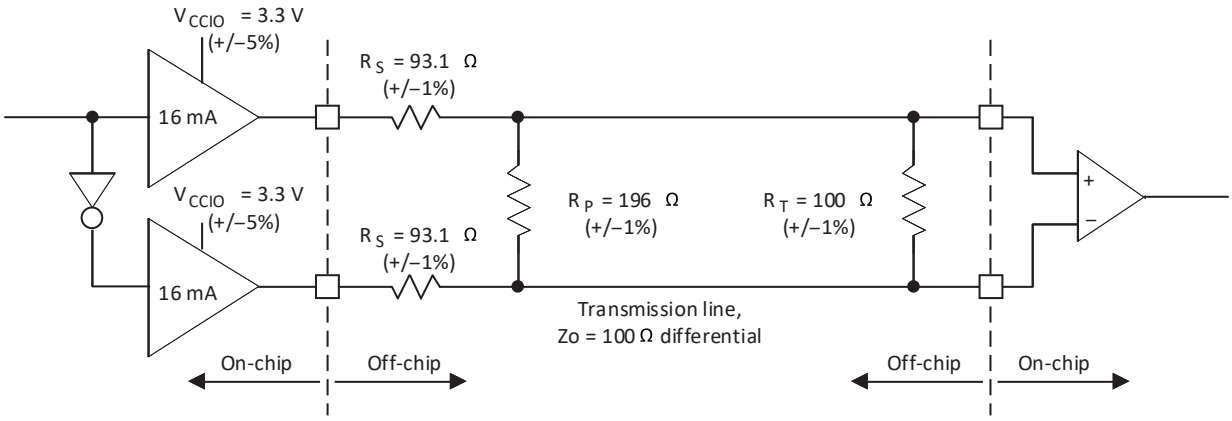


Figure 4.3. Differential LVPECL33

Table 4.5. LVPECL33 DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/–1%)	93	Ω
R_P	Driver Parallel Resistor (+/–1%)	196	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

Notes:

1. For input buffer, see LVDS table.

4.11.7. RSDS25E

The LA-LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 4.4 is one possible solution for RSDS standard implementation. Resistor values in Figure 4.4 are industry standard values for 1% resistors.

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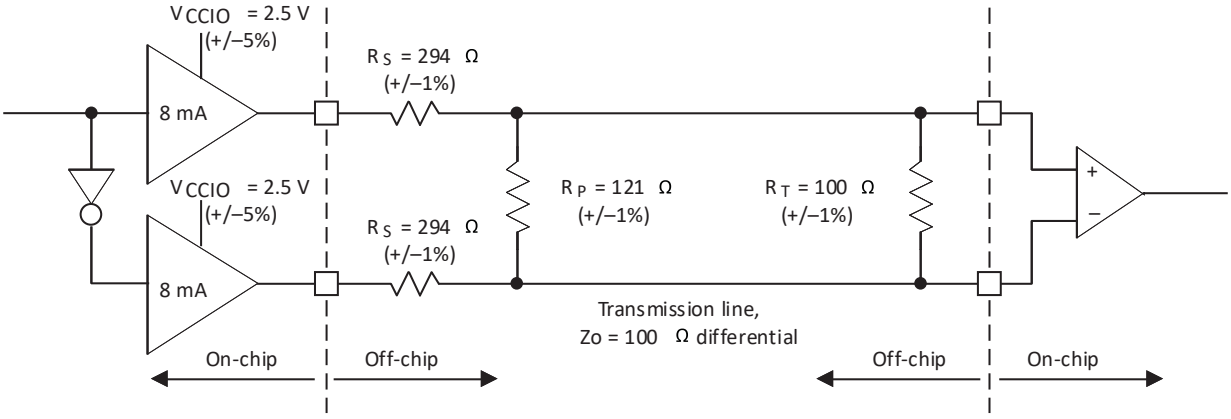


Figure 4.4. RSDS25E (Reduced Swing Differential Signaling)

Table 4.6. RSDS25E DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/–1%)	294	Ω
R_P	Driver Parallel Resistor (+/–1%)	121	Ω
R_T	Receiver Termination (+/–1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

Note:

1. For input buffer, see LVDS table.

4.11.8. MLVDS25

The LA-LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 4.5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 4.5 are industry standard values for 1% resistors.

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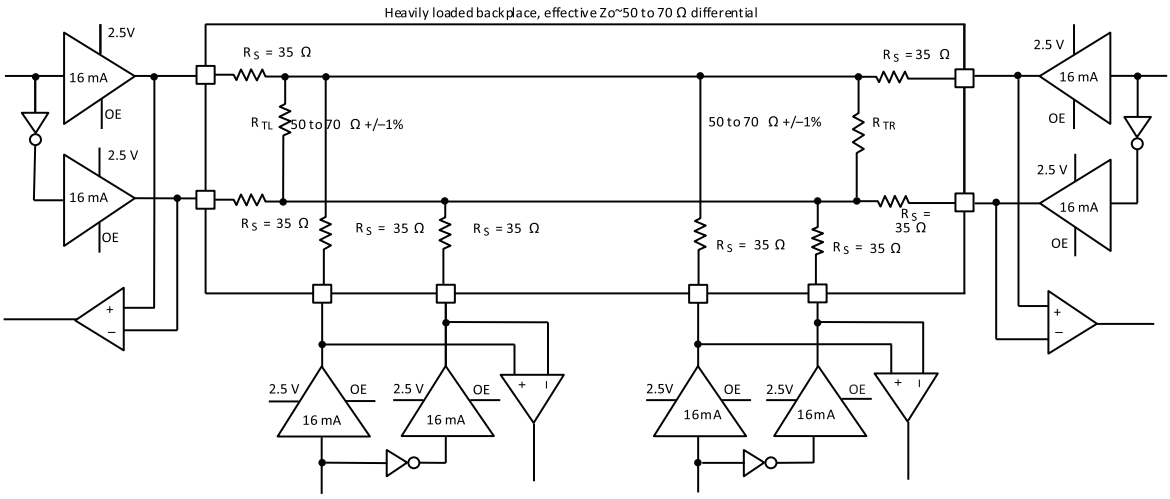


Figure 4.5. MLVDS25 (Multipoint Low Voltage Differential Signaling)

Table 4.7. MLVDS25 DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50 Ω	Zo=70 Ω	
V_{CCIO}	Output Driver Supply (+/–5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/–1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/–1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/–1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

Note:

1. For input buffer, see LVDS table.

4.12. Typical Building Block Function Performance

4.12.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)[1]

Function	–6 / –6L Timing	Units
Basic Functions		
16-bit Decoder	4.9	ns
32-bit Decoder	5.3	ns
64-bit Decoder	7.0	ns
4:1 MUX	4.9	ns
8:1 MUX	5.2	ns
16:1 MUX	5.7	ns
32:1 MUX	5.8	ns

Note:

1. Automotive timing numbers are shown.

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4.13. Register-to-Register Performance[1]

Function	–6 / –6L Timing	Units
Basic Functions		
16-bit Decoder	368	MHz
32-bit Decoder	368	MHz
64-bit Decoder	247	MHz
4:1 MUX	368	MHz
8:1 MUX	368	MHz
16:1 MUX	368	MHz
32:1 MUX	358	MHz
8-bit Adder	368	MHz
16-bit Adder	368	MHz
64-bit Adder	252	MHz
16-bit Counter	368	MHz
32-bit Counter	368	MHz
64-bit Counter	262	MHz
64-bit Accumulator	251	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers	103	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	222	MHz
Distributed Memory Functions		
16 x 4 Pseudo-Dual Port RAM (One PFU)	368	MHz
32 x 4 Pseudo-Dual Port RAM	368	MHz
64 x 8 Pseudo-Dual Port RAM	324	MHz
DSP Function		
18 x 18 Multiplier (All Registers)	331	MHz
9 x 9 Multiplier (All Registers)	331	MHz
36 x 36 Multiply (All Registers)	212	MHz
18 x 18 Multiply/Accumulate (Input & Output Registers)	176	MHz
18 x 18 Multiply-Add/Sub (All Registers)	331	MHz

Note:

1. Automotive timing numbers are shown.

4.14. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

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4.15. LA-LatticeECP3 External Switching Characteristics[1, 2]

Over Recommended Operating Ranges

Parameter	Description	Device	–6 / –6L		Units
			Min.	Max.	
Clocks					
Primary Clock [6]					
f_{MAX_PRI}	Frequency for Primary Clock Tree	LAE3-35EA	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	LAE3-35EA	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LAE3-35EA	—	360	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	LAE3-35EA	—	300	ps
f_{MAX_PRI}	Frequency for Primary Clock Tree	LAE3-17EA	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	LAE3-17EA	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LAE3-17EA	—	370	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	LAE3-17EA	—	240	ps
Edge Clock [6]					
f_{MAX_EDGE}	Frequency for Edge Clock	LAE3-35EA	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	LAE3-35EA	1.2	—	ns
$t_{SKEW_EDGE_DQS}$	Edge Clock Skew Within an Edge of the Device	LAE3-35EA	—	220	ps
f_{MAX_EDGE}	Frequency for Edge Clock	LAE3-17EA	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	LAE3-17EA	1.2	—	ns
$t_{SKEW_EDGE_DQS}$	Edge Clock Skew Within an Edge of the Device	LAE3-17EA	—	220	ps
Generic SDR					
General I/O Pin Parameters (using dedicated clock input Primary Clock without PLL) [2]					
t_{CO}	Clock to Output - PIO Output Register	LAE3-35EA	—	4.54	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LAE3-35EA	0.00	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LAE3-35EA	1.62	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-35EA	1.48	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-35EA	0.00	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LAE3-35EA	—	375	MHz
t_{CO}	Clock to Output - PIO Output Register	LAE3-17EA	—	4.34	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LAE3-17EA	0.00	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LAE3-17EA	1.62	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-17EA	1.48	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-17EA	0.00	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LAE3-17EA	—	375	MHz
General I/O Pin Parameters (using dedicated clock input Primary Clock with PLL with clock injection removal setting) [2]					
t_{COPLL}	Clock to Output - PIO Output Register	LAE3-35EA	—	2.72	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LAE3-35EA	0.81	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LAE3-35EA	0.37	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register	LAE3-35EA	1.82	—	ns

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Parameter	Description	Device	–6 / –6L		Units
			Min.	Max.	
	with Data Input Delay				
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-35EA	0.00	—	ns
t_{COPLL}	Clock to Output - PIO Output Register	LAE3-17EA	—	2.49	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LAE3-17EA	0.81	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LAE3-17EA	0.37	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-17EA	1.82	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-17EA	0.00	—	ns
Generic DDR[12]					
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input					
t_{SUGDDR}	Data Setup Before CLK	All Devices	480	—	ps
t_{HOGDDR}	Data Hold After CLK	All Devices	480	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.PLL.Aligned) Using PLLCLKIN Pin for Clock Input					
Data Left, Right, and Top Sides and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using DLL - CLKIN Pin for Clock Input					
Data Left, Right and Top Sides and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
GenericDDRX1 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_RX.DQS.Centered) Using DQS Pin for Clock Input					
t_{SUGDDR}	Data Setup After CLK	All Devices	535	—	ps
t_{HOGDDR}	Data Hold After CLK	All Devices	535	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
GenericDDRX1 Inputs with Clock and Data (<10bits wide) Aligned at Pin (GDDRX1_RX.DQS.Aligned) Using DQS Pin for Clock Input					
Data and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
GenericDDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock Input					
Left and Right Sides					
t_{SUGDDR}	Data Setup Before CLK	LAE3-35EA	535	—	ps
t_{HOGDDR}	Data Hold After CLK	LAE3-35EA	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	—	250	MHz

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Parameter	Description	Device	–6 / –6L		Units
			Min.	Max.	
t_{SUGDDR}	Data Setup Before CLK	LAE3-17EA	535	—	ps
t_{HOGDDR}	Data Hold After CLK	LAE3-17EA	535	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	—	250	MHz
GenericDDRX2 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_RX.ECLK.Aligned)					
Left and Right Side Using DLLCLKIN Pin for Clock Input					
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-35EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-35EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-17EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-17EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	—	311	MHz
Top Side Using PCLK Pin for Clock Input					
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-35EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-35EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-17EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-17EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	—	130	MHz
GenericDDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDRX2_RX.ECLK.Aligned) (No CLKDIV)					
Left and Right Sides Using DLLCLKPIN for Clock Input					
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-35EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-35EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	—	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Sides)	LAE3-17EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-17EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	—	311	MHz
Top Side Using PCLK Pin for Clock Input					
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-35EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-35EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	—	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-17EA	—	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-17EA	0.79	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	—	130	MHz
GenericDDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX2_RX.DQS.Centered) Using DQS Pin for Clock Input					
Left and Right Sides					
t_{SUGDDR}	Data Setup Before CLK	All Devices	352	—	ps
t_{HOGDDR}	Data Hold After CLK	All Devices	352	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	—	375	MHz
GenericDDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDRX2_RX.DQS.Aligned) Using DQS Pin for Clock Input					
Left and Right Sides					

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Parameter	Description	Device	–6 / –6L		Units
			Min.	Max.	
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775 -	—	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	—	375	MHz
GenericDDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_TX.SCLK.Centered)10					
$t_{DVBGDDR}$	Data Valid Before CLK	LAE3-35EA	690	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	LAE3-35EA	690	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-35EA	—	250	MHz
$t_{DVBGDDR}$	Data Valid Before CLK	LAE3-17EA	690	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	LAE3-17EA	690	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-17EA	—	250	MHz
GenericDDRX1 Output with Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned)[10]					
$t_{DIBGDDR}$	Data Invalid Before Clock Data Invalid After Clock	LAE3-35EA	—	321	ps
$t_{DIAGDDR}$		LAE3-35EA	—	321	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-35EA	—	250	MHz
$t_{DIBGDDR}$	Data Invalid Before Clock	LAE3-17EA	—	321	ps
$t_{DIAGDDR}$	Data Invalid After Clock	LAE3-17EA	—	321	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-17EA	—	250	MHz
GenericDDRX1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_TX.DQS.Centered)10					
Left and Right Sides					
$t_{DVBGDDR}$	Data Valid Before CLK	LAE3-35EA	676	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	LAE3-35EA	676	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-35EA	—	250	MHz
$t_{DVBGDDR}$	Data Valid Before CLK	LAE3-17EA	670	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	LAE3-17EA	670	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-17EA	—	250	MHz
GenericDDRX2 Output with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_TX.Aligned)					
Left and Right Sides					
$t_{DIBGDDR}$	Data Invalid Before Clock	All Devices	—	220	ps
$t_{DIAGDDR}$	Data Invalid After Clock	All Devices	—	220	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	—	375	MHz
GenericDDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQS- DLL.Centered)[11]					
Left and Right Sides					
$t_{DVBGDDR}$	Data Valid Before CLK	All Devices	431	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	All Devices	432	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	—	375	MHz
GenericDDRX2 Output with Clock and Data (>10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)10					
Left and Right Sides					
$t_{DVBGDDR}$	Data Valid Before CLK	All Devices	431	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	All Devices	432	—	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	—	375	MHz
Memory Interface					
DDR/DDR2 I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]					

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Parameter	Description	Device	–6 / –6L		Units
			Min.	Max.	
t_{DVADQ}	Data Valid After DQS (DDR Read)	All Devices	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All Devices	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All Devices	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All Devices	0.25	—	UI
f_{MAX_GDDR}	DDR Clock Frequency	All Devices	95	166	MHz
f_{MAX_GDDR2}	DDR2 Clock Frequency	All Devices	125	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters					
t_{DVADQ}	Data Valid After DQS (DDR Read)	All Devices	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	All Devices	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	All Devices	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	All Devices	0.25	—	UI
f_{MAX_DDR3}	DDR3 Clock Frequency	All Devices	266	300	MHz
DDR3 Clock Timing					
t_{CH}	Average High Pulse Width	All Devices	0.47	0.53	UI
t_{CL}	Average Low Pulse Width	All Devices	0.47	0.53	UI
t_{JIT}	Output Clock Period Jitter During DLL Locking Period	All Devices	–90	90	ps
t_{JIT}	Output Cycle-to-Cycle Period Jitter During DLL Locking Period	All Devices	—	180	ps

Notes:

1. Automotive timing numbers are shown.
2. General I/O timing numbers based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
8. Using settings generated by IPexpress.
9. These numbers are generated using best case PLL located in the center of the device.
10. Uses SSTL25 Class II Differential I/O Standard.
11. All numbers are generated with Diamond 2.x software.

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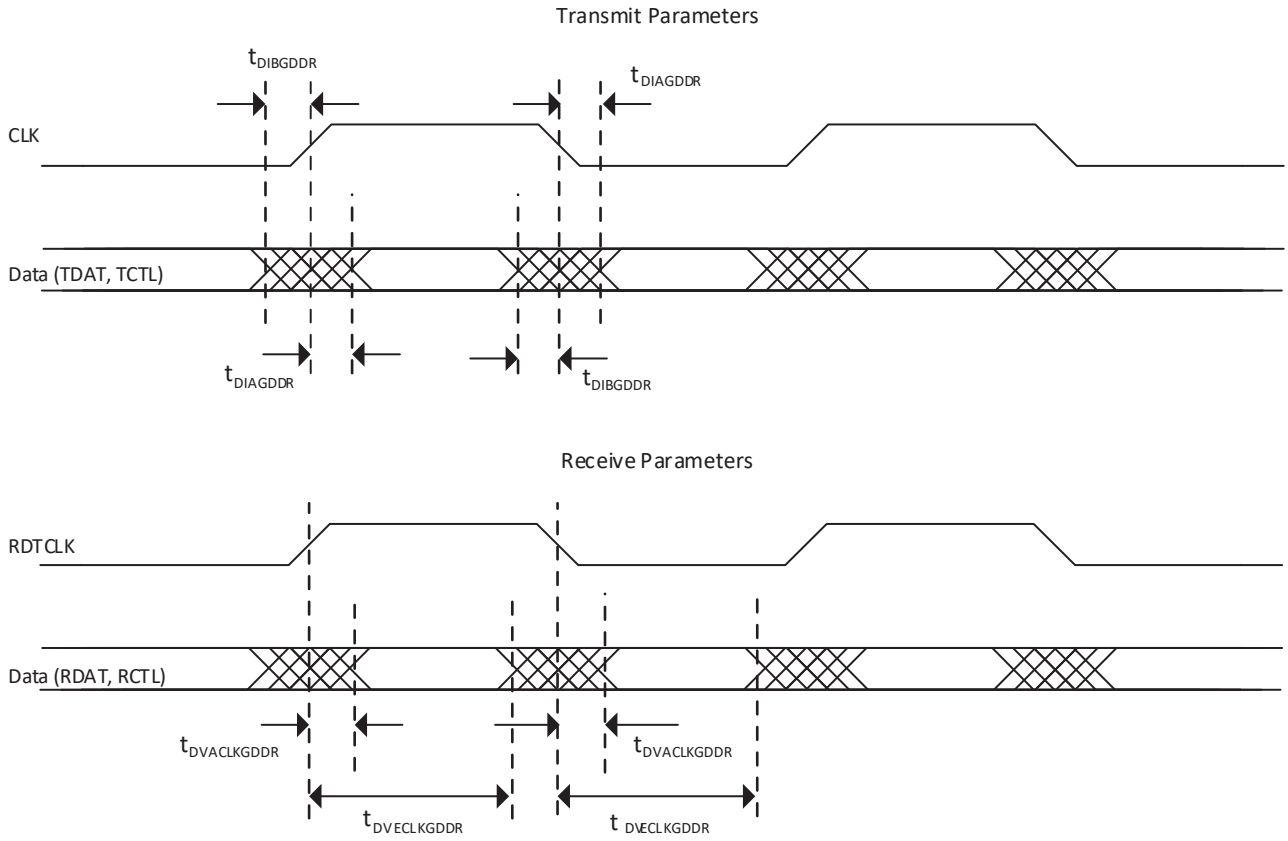


Figure 4.6. Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)

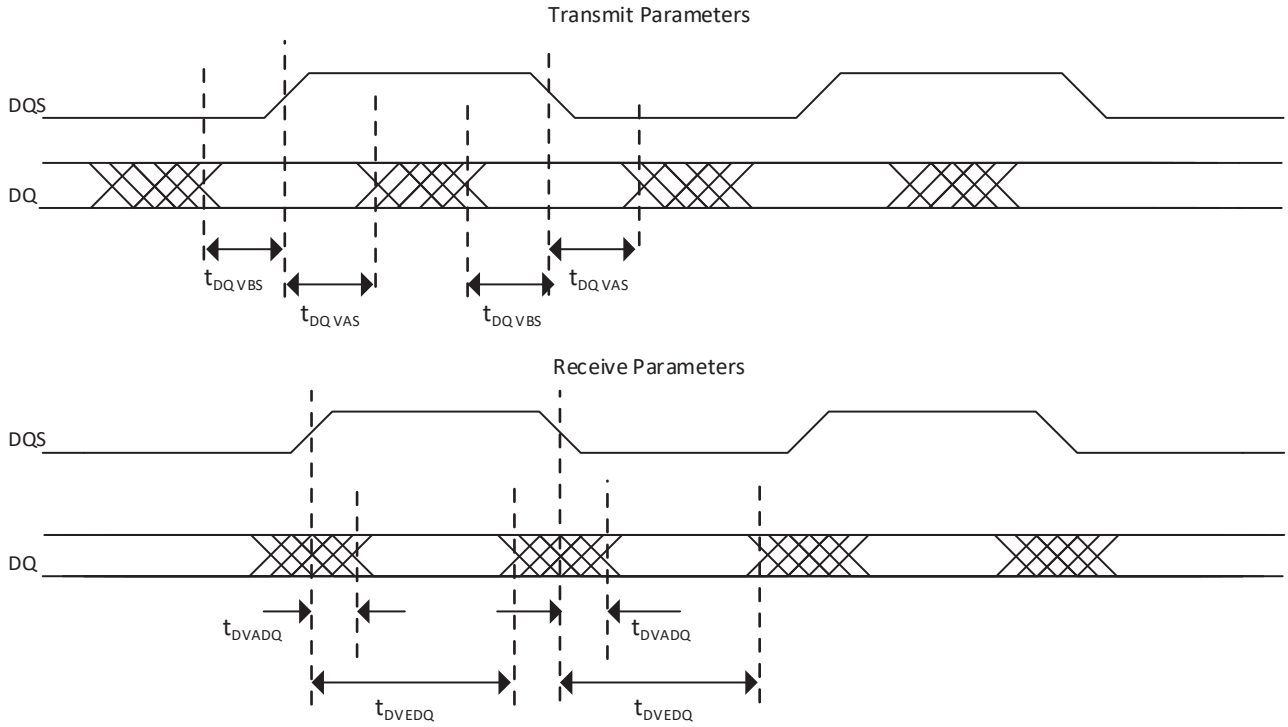


Figure 4.7. DDR/DDR2/DDR3 Parameters

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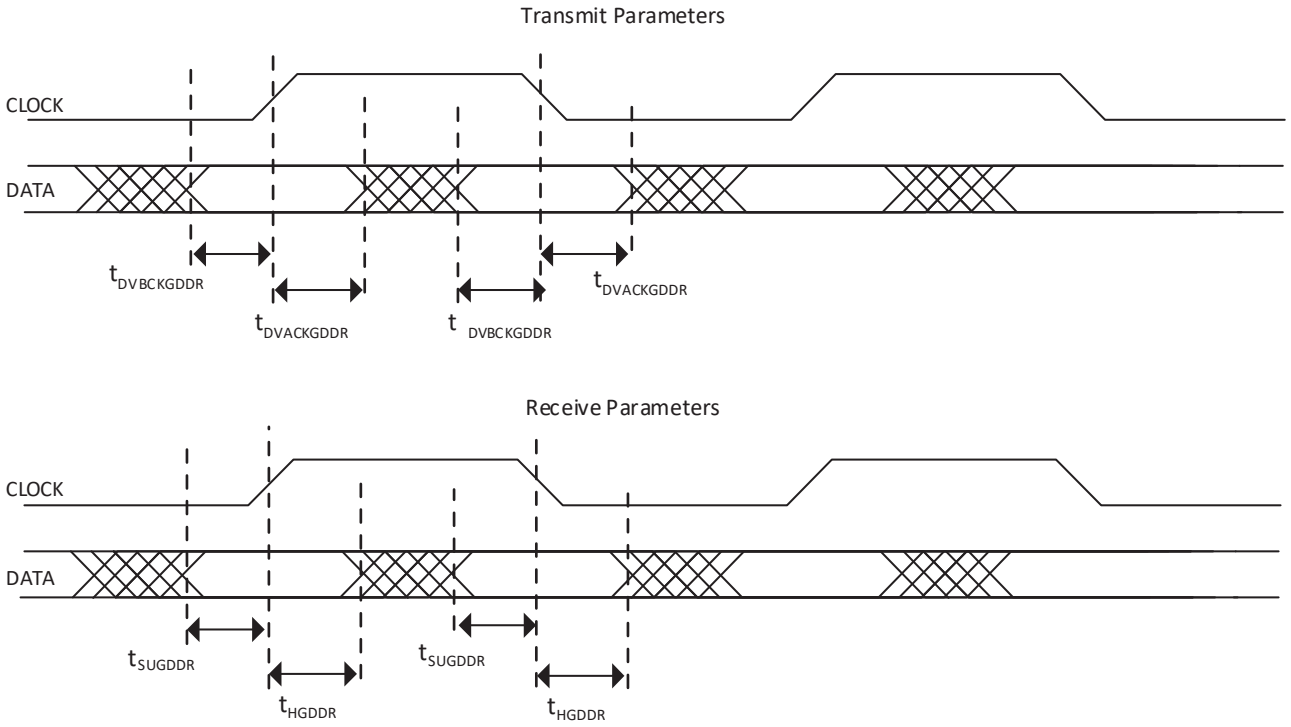


Figure 4.8. Generic DDRX1/DDRX2 (With Clock Center on Data Window)

4.16. LA-LatticeECP3 Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	–6 / –6L		Units
		Min.	Max.	
PFU/PFF Logic Mode Timing				
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.181	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.383	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronus)	—	0.764	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.155	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	–0.110	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.076	—	ns
t_{HD_PFU}	Clock to D input hold time	0.015	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.306	ns
PFU Dual Port Memory Mode Timing				
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.906	ns
t_{SUDATA_PFU}	Data Setup Time	–0.176	—	ns
t_{HDATA_PFU}	Data Hold Time	0.248	—	ns
t_{SUADDR_PFU}	Address Setup Time	–0.289	—	ns
t_{HADDR_PFU}	Address Hold Time	0.313	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	–0.064	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.072	—	ns
PIC Timing				
PIO Input/Output Buffer Timing				

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Parameter	Description	–6 / –6L		Units
		Min.	Max.	
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.53	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.42	ns
IOLOGIC Input/Output Timing				
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	1.306	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	1.306	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	1.31	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.152	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	–0.059	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.089	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	–0.082	—	ns
EBR Timing				
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	3.10	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.34	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	–0.246	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.275	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memroy	–0.071	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.080	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	–0.110	—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.155	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.108	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	–0.097	—	ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	–0.071	—	ns

LA-LatticeECP3 Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	–6 / –6L		Units
		Min.	Max.	
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.080	-	ns
PLL Parameters				
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	ns
DSP Block Timing[2, 3]				
t_{SUI_DSP}	Input Register Setup Time	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	–0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.39	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	–1.16	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.37	—	ns
t_{HO_DSP}	Output Register Hold Time	–1.86	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.77	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.66	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.63	ns

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Parameter	Description	–6 / –6L		Units
		Min.	Max.	
t_{SUOPT_DSP}	Opcode Register Setup Time	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	–0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	2.16	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	–0.98	—	ns

Note:

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LA-LatticeECP3 devices only.
3. DSP Block is configured in Multiply Add/Sub 18 x 18 Mode.

4.17. Timing Diagrams

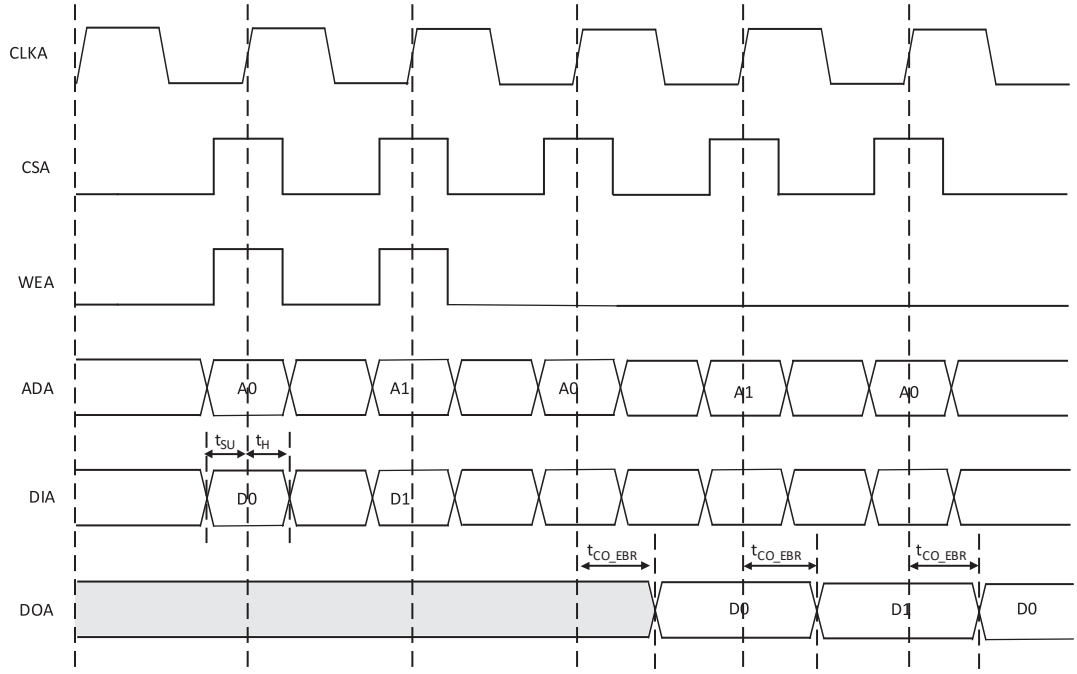


Figure 4.9. Read/Write Mode (Normal)

Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

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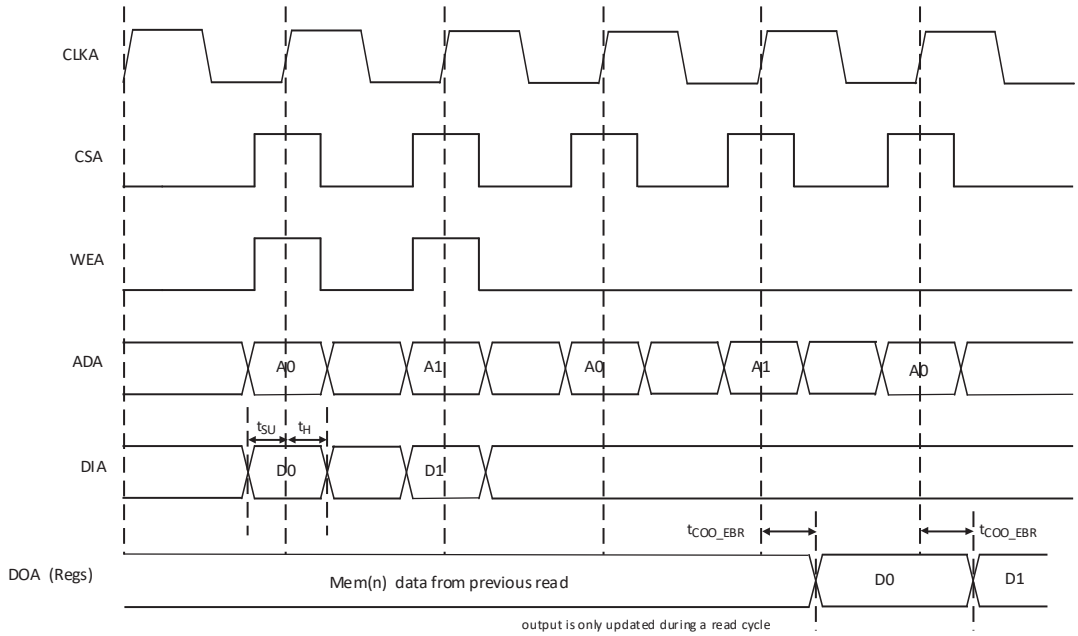


Figure 4.10. Read/Write Mode with Input and Output Registers

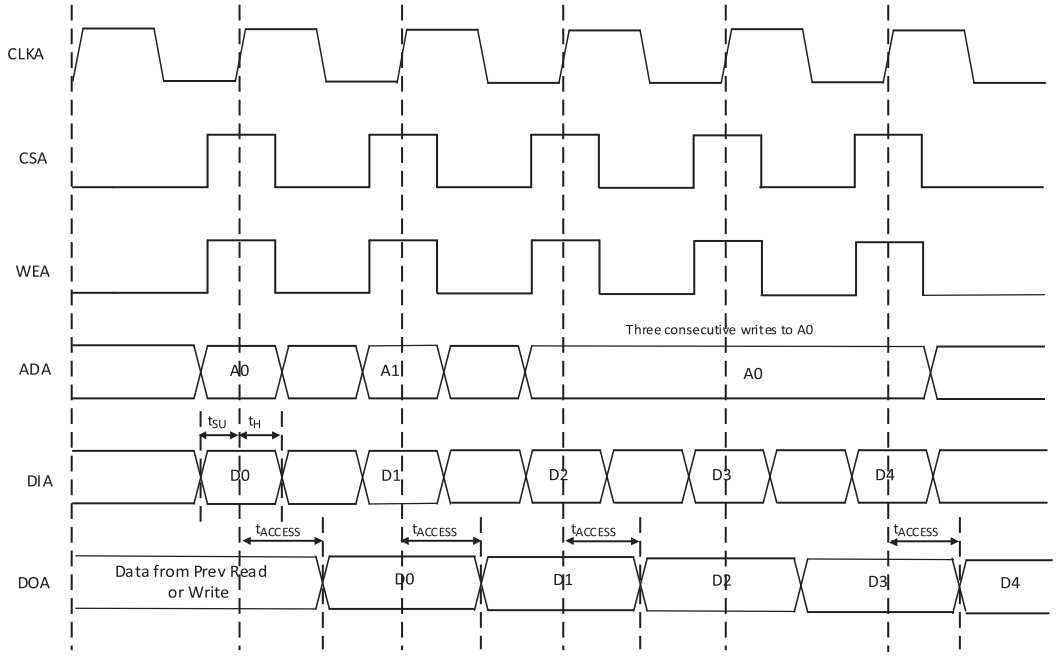


Figure 4.11. Write Through (SP Read/Write on Port A, Input Registers Only)

Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

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4.18. LA-LatticeECP3 Family Timing Adders [1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Buffer Type	Description	–6 / –6L	Units
Input Adjusters			
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	–0.04	ns
LVDS25	LVDS, VCCIO = 2.5 V	–0.04	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	–0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	–0.04	ns
RSDS25	RSDS, VCCIO = 2.5 V	–0.04	ns
PPLVDS	Point-to-Point LVDS	–0.04	ns
TRLVDS	Transition-Reduced LVDS	–0.04	ns
HYPT	HyperTransport	–0.04	ns
Mini MLVDS	Mini LVDS	–0.04	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.0 V	–0.04	ns
HSTL18_I	HSTL_18 class I, VCCIO = 1.8 V	0.14	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	0.14	ns
HSTL18D_I	Differential HSTL 18 class I	0.14	ns
HSTL18D_II	Differential HSTL 18 class II	0.14	ns
HSTL15_I	HSTL_15 class I, VCCIO = 1.5 V	0.14	ns
HSTL15D_I	Differential HSTL 15 class I	0.14	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.0 V	0.30	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.0 V	0.30	ns
SSTL33D_I	Differential SSTL_3 class I	0.30	ns
SSTL33D_II	Differential SSTL_3 class II	0.30	ns
SSTL25_I	SSTL_2 class I, VCCIO = 2.5 V	0.17	ns
SSTL25_II	SSTL_2 class II, VCCIO = 2.5 V	0.17	ns
SSTL25D_I	Differential SSTL_2 class I	0.17	ns
SSTL25D_II	Differential SSTL_2 class II	0.17	ns
SSTL18_I	SSTL_18 class I, VCCIO = 1.8 V	0.04	ns
SSTL18_II	SSTL_18 class II, VCCIO = 1.8 V	0.04	ns
SSTL18D_I	Differential SSTL_18 class I	0.04	ns
SSTL18D_II	Differential SSTL_18 class II	0.04	ns
SSTL15	SSTL_15, VCCIO = 1.5 V	0.03	ns
SSTL15D	Differential SSTL_15	–0.04	ns
LVTTL33	LVTTL, VCCIO = 3.0 V	0.05	ns
LVCMOS33	LVCMOS, VCCIO = 3.0 V	0.05	ns
LVCMOS25	LVCMOS, VCCIO = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, VCCIO = 1.8 V	0.11	ns
LVCMOS15	LVCMOS, VCCIO = 1.5 V	0.26	ns
LVCMOS12	LVCMOS, VCCIO = 1.2 V	0.09	ns
PCI33	PCI, VCCIO = 3.0 V	0.05	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, VCCIO = 2.5 V	0.16	ns
LVDS25	LVDS, VCCIO = 2.5 V	0.01	ns
BLVDS25	BLVDS, Emulated, VCCIO = 2.5 V	–0.04	ns
MLVDS25	MLVDS, Emulated, VCCIO = 2.5 V	–0.03	ns
RSDS25	RSDS, VCCIO = 2.5 V	0.16	ns
PPLVDS	Point-to-Point LVDS, Emulated, VCCIO = 2.5 V	0.01	ns

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Buffer Type	Description	–6 / –6L	Units
HYPT	HyperTransport	0.01	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.0 V	–0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8 V	–0.13	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8 V	–0.26	ns
HSTL18D_I	Differential HSTL 18 class I 8 mA drive	–0.13	ns
HSTL18D_II	Differential HSTL 18 class II	–0.26	ns
HSTL15_I	HSTL_15 class I 4 mA drive, VCCIO = 1.5 V	–0.16	ns
HSTL15D_I	Differential HSTL 15 class I 4 mA drive	–0.16	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.0 V	0.20	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.0 V	–0.15	ns
SSTL33D_I	Differential SSTL_3 class I	0.20	ns
SSTL33D_II	Differential SSTL_3 class II	–0.15	ns
SSTL25_I	SSTL_2 class I 8 mA drive, VCCIO = 2.5 V	0.02	ns
SSTL25_II	SSTL_2 class II 16 mA drive, VCCIO = 2.5 V	–0.13	ns
SSTL25D_I	Differential SSTL_2 class I 8 mA drive	0.02	ns
SSTL25D_II	Differential SSTL_2 class II 16 mA drive	–0.13	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8 V	–0.07	ns
SSTL18_II	SSTL_1.8 class II 8mA drive, VCCIO = 1.8 V	–0.15	ns
SSTL18D_I	Differential SSTL_1.8 class I	–0.07	ns
SSTL18D_II	Differential SSTL_1.8 class II 8 mA drive	–0.15	ns
SSTL15	SSTL_1.5, VCCIO = 1.5 V	1.55	ns
SSTL15D	Differential SSTL_15	1.55	ns
LVTTL33_4mA	LVTTL 4 mA drive, VCCIO = 3.0 V	0.24	ns
LVTTL33_8mA	LVTTL 8 mA drive, VCCIO = 3.0 V	–0.07	ns
LVTTL33_12mA	LVTTL 12 mA drive, VCCIO = 3.0 V	–0.02	ns
LVTTL33_16mA	LVTTL 16 mA drive, VCCIO = 3.0 V	–0.09	ns
LVTTL33_20mA	LVTTL 20 mA drive, VCCIO = 3.0 V	–0.15	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, fast slew rate	0.24	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, fast slew rate	–0.07	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, fast slew rate	–0.02	ns
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, fast slew rate	–0.09	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, fast slew rate	–0.15	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, fast slew rate	0.10	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, fast slew rate	–0.07	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, fast slew rate	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, fast slew rate	–0.15	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, fast slew rate	–0.15	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, fast slew rate	0.14	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, fast slew rate	0.14	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, fast slew rate	–0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, fast slew rate	–0.03	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, fast slew rate	0.30	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, fast slew rate	0.09	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, fast slew rate	0.61	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, fast slew rate	0.35	ns
LVCMOS33_4mA	LVCMOS 3.3 4 mA drive, slow slew rate	1.79	ns
LVCMOS33_8mA	LVCMOS 3.3 8 mA drive, slow slew rate	1.27	ns
LVCMOS33_12mA	LVCMOS 3.3 12 mA drive, slow slew rate	0.90	ns

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Buffer Type	Description	–6 / –6L	Units
LVCMOS33_16mA	LVCMOS 3.3 16 mA drive, slow slew rate	1.26	ns
LVCMOS33_20mA	LVCMOS 3.3 20 mA drive, slow slew rate	0.89	ns
LVCMOS25_4mA	LVCMOS 2.5 4 mA drive, slow slew rate	1.86	ns
LVCMOS25_8mA	LVCMOS 2.5 8 mA drive, slow slew rate	1.32	ns
LVCMOS25_12mA	LVCMOS 2.5 12 mA drive, slow slew rate	0.98	ns
LVCMOS25_16mA	LVCMOS 2.5 16 mA drive, slow slew rate	1.32	ns
LVCMOS25_20mA	LVCMOS 2.5 20 mA drive, slow slew rate	0.97	ns
LVCMOS18_4mA	LVCMOS 1.8 4 mA drive, slow slew rate	2.02	ns
LVCMOS18_8mA	LVCMOS 1.8 8 mA drive, slow slew rate	1.44	ns
LVCMOS18_12mA	LVCMOS 1.8 12 mA drive, slow slew rate	1.14	ns
LVCMOS18_16mA	LVCMOS 1.8 16 mA drive, slow slew rate	1.12	ns
LVCMOS15_4mA	LVCMOS 1.5 4 mA drive, slow slew rate	2.17	ns
LVCMOS15_8mA	LVCMOS 1.5 8 mA drive, slow slew rate	1.55	ns
LVCMOS12_2mA	LVCMOS 1.2 2 mA drive, slow slew rate	1.82	ns
LVCMOS12_6mA	LVCMOS 1.2 6 mA drive, slow slew rate	1.50	ns
PCI33	PCI, VCCIO = 3.0 V	–0.15	ns

Notes:

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Conditions on page 103.
3. All other standards tested according to the appropriate specifications.
4. These timing adders are measured with the recommended resistor values.
5. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.

4.19. LA-LatticeECP3 Maximum I/O Buffer Speed [1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
PPLVDS	Point-to-Point LVDS	400	MHz
TRLVDS	Transition-Reduced LVDS	612	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.0 V	400	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
HSTL15	HSTL_15 class I, V_{CCIO} = 1.5 V	400	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, V_{CCIO} = 3.0 V	400	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, V_{CCIO} = 2.5 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.0 V	166	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.0 V	166	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	166	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	166	MHz
LVCMOS15	LVCMOS 1.5, V_{CCIO} = 1.5 V	166	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	166	MHz
PCI33	PCI, V_{CCIO} = 3.3 V	66	MHz

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Buffer	Description	Max.	Units
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	300	MHz
LVDS25	LVDS, V_{CCIO} = 2.5V	612	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	300	MHz
RSDS25	RSDS, Emulated, V_{CCIO} = 2.5 V	612	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	300	MHz
PPLVDS	Point-to-point LVDS	612	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.0 V	612	MHz
Mini-LVDS	Mini LVDS	612	MHz
HSTL18 (all supported classes)	HSTL_18 class I, II, V_{CCIO} = 1.8 V	200	MHz
HSTL15 (all supported classes)	HSTL_15 class I, V_{CCIO} = 1.5 V	200	MHz
SSTL33 (all supported classes)	SSTL_3 class I, II, V_{CCIO} = 3.0 V	233	MHz
SSTL25 (all supported classes)	SSTL_2 class I, II, V_{CCIO} = 2.5 V	233	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	266	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.0 V	166	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	166	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	166	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	166	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	166	MHz
LVCMOS12 (For all drives except 2 mA)	LVCMOS, V_{CCIO} = 1.2 V	166	MHz
LVCMOS12 (2 mA drive)	LVCMOS, V_{CCIO} = 1.2 V	100	MHz
PCI33	PCI, V_{CCIO} = 3.3 V	66	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

4.20. Oscillator Output Frequency

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{MAX}	Oscillator Output Frequency (Automotive Grade Devices, –40° to 125 °C)	110.5	130	149.5	MHz

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4.21. sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f_{IN}	Input clock frequency (CLKI, CLKFB)	—	Edge clock	2	—	500	MHz
			Primary clock[4]	2	—	420	MHz
f_{OUT}	Output clock frequency (CLKOP, CLKOS)	—	Edge clock	4	—	500	MHz
			Primary clock[4]	4	—	420	MHz
f_{OUT1}	K-Divider output frequency	CLKOK	—	0.03125	—	250	MHz
f_{OUT2}	K2-Divider output frequency	CLKOK2	—	0.667	—	166	MHz
f_{VCO}	PLL VCO frequency	—	—	500	—	1000	MHz
f_{PFD}[3]	Phase detector input frequency	—	Edge clock	2	—	500	MHz
		—	Primary clock[4]	2	—	420	MHz
AC Characteristics							
t_{PA}	Programmable delay unit	—	—	65	130	260	ps
t_{DT}	Output clock duty cycle (CLKOS, at 50% setting)	—	Edge clock	45	50	55	%
		$f_{OUT} \leq 250$ MHz	Primary clock	45	50	55	%
		$f_{OUT} > 250$MHz	Primary clock	30	50	70	%
t_{CPA}	Coarse phase shift error (CLKOS, at all settings)	—	—	-5	0	+5	% of period
t_{OPW}	Output clock pulse width high or low (CLKOS)	—	—	1.8	—	—	ns
t_{OPJIT}	Output clock period jitter	$f_{OUT} \geq 420$ MHz	—	—	—	200	ps
		420 MHz > $f_{OUT} \geq 100$ MHz	—	—	—	250	ps
		$f_{OUT} < 100$ MHz	—	—	—	0.025	UIPP
t_{SK}	Input clock to output clock skew when N/M = integer		—	—	—	500	ps
t_{LOCK}[2]	Lock time	2 to 25 MHz	—	—	—	200	us
		25 to 500 MHz	—	—	—	50	us
t_{UNLOCK}	Reset to PLL unlock time to ensure fast reset		—	—	—	50	ns
t_{HI}	Input clock high time	90% to 90%	—	0.5	—	—	ns
t_{LO}	Input clock low time	10% to 10%	—	0.5	—	—	ns
t_{IPJIT}	Input clock period jitter	—	—	—	—	400	ps
t_{RST}	Reset signal pulse width high, RSTK	—	—	10	—	—	ns
	Reset signal pulse width high, RST	—	—	500	—	—	ns

Notes:

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$ MHz. For $f_{PFD} < 4$ MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for fPFD < 4MHz.
4. When using internal feedback, maximum can be up to 500 MHz.

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4.22. DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)	—	133	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)	—	133	—	500	MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP	—	133	—	500	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS	—	33.3	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)	—		—	200	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	Edge Clock	40		60	%
		Primary Clock	30		70	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	Primary Clock < 250 MHz	45		55	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading	Primary Clock < 250 MHz	40		60	%
		Primary Clock ≥ 250 MHz	30		70	%
		Edge Clock	45		55	%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting	—	—	—	100	ps
t_{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks	—	—	—	+/- 400	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)	—	550	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)	—	550	—	—	ps
t_{INSTB}	Input clock period jitter	—	—	—	500	ps
t_{LOCK}	DLL lock time	—	8	—	8200	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)	—	3	—	—	ns
t_{DEL}	Delay step size	—	27	45	70	ps
t_{RANGE1}	Max. delay setting for single delay block (64 taps)	—	1.9	3.1	4.4	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks	—	7.6	12.4	17.6	ns

Notes:

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

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4.23. SERDES High-Speed Data Transmitter[1]

Table 4.8. Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44 V setting)[1, 2]	0.15 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35 V setting)[1, 2]	0.15 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26 V setting)[1, 2]	0.15 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13 V setting)[1, 2]	0.15 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04 V setting)[1, 2]	0.15 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92 V setting)[1, 2]	0.15 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87 V setting)[1, 2]	0.15 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78 V setting)[1, 2]	0.15 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64 V setting)[1, 2]	0.15 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} –0.75	V_{CCOB} –0.60	V_{CCOB} –0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ω (single ended)	—	–20%	50/75/ Hi Z	+20%	Ω
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps

Notes:

1. All measurements are with 50 Ω impedance.
2. See LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190) for actual binary settings and the min-max range.

Table 4.9. Channel Output Jitter

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5Gbps	—	—	0.17	UI, p-p
Random	2.5Gbps	—	—	0.20	UI, p-p
Total	2.5Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p

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Description	Frequency	Min.	Typ.	Max.	Units
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p
Deterministic	150 Mbps	—	—	0.10	UI, p-p
Random	150 Mbps	—	—	0.18	UI, p-p
Total	150 Mbps	—	—	0.24	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/O around SERDES pins quiet, reference clock @ 10X mode.

4.24. SERDES/PCS Block Latency

Table 4.10 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 4.12 shows the location of each block.

Table 4.10. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

Notes:

1. Δ1 = -245ps, Δ2 = +88ps, Δ3 = +112ps.
2. Δ1 = +118ps, Δ2 = +132ps, Δ3 = +700ps.

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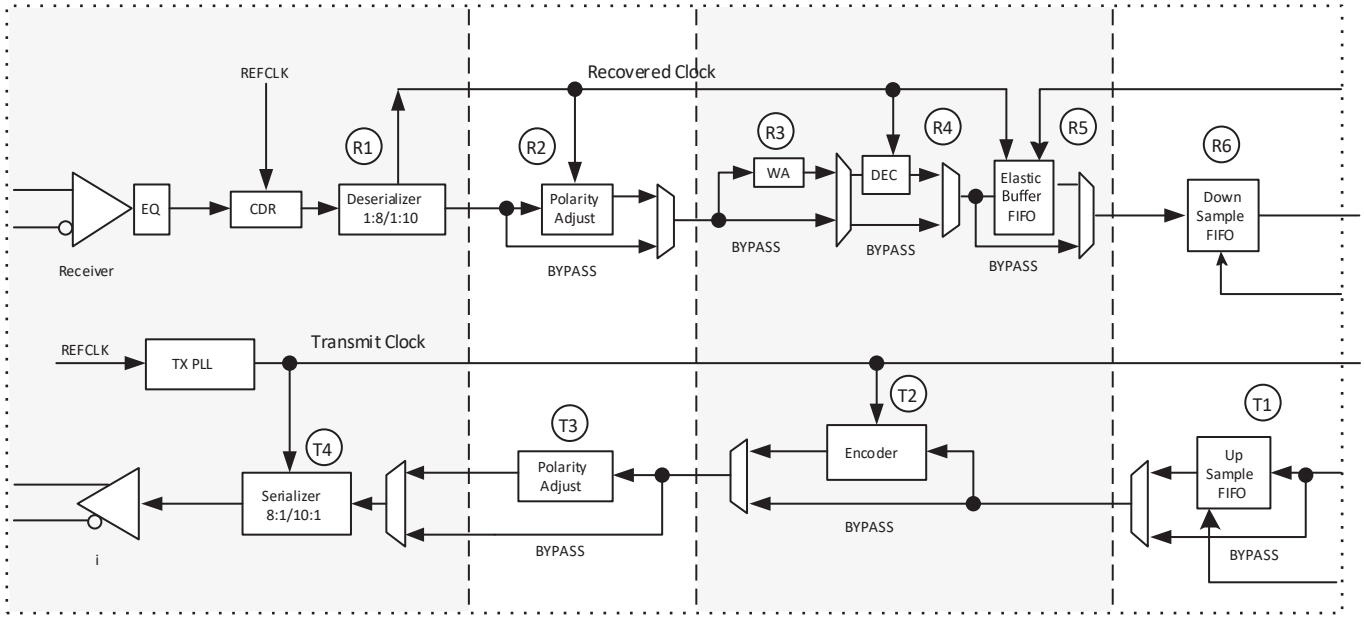


Figure 4.12. Transmitter and Receiver Latency Block Diagram

4.25. SERDES High Speed Data Receiver

Table 4.11. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125 G	—	—	136	Bits
		2.5 G	—	—	144	
		1.485 G	—	—	160	
		622 M	—	—	204	
		270 M	—	—	228	
		150 M	—	—	296	
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity		150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ω/High Z		-20%	50/75/HiZ	+20%	Ω
$RL_{RX\text{-}RL}$	Return loss (without package)		10	—	—	dB

Notes:

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76 V.

4.25.1. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

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Table 4.12. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/O around SERDES pins quiet, voltages are nominal, room temperature.

Table 4.13. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	150 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 27-1, all channels operating, FPGA Logic active, I/O around SERDES pins quiet, voltages are nominal, room temperature.

4.25.2. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 4.14 specifies reference clock requirements, over the full range of operating conditions.

Table 4.14. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–20%	100/2K	+20%	Ω
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

Notes:

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190).
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.

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3. Measured at 50% amplitude.

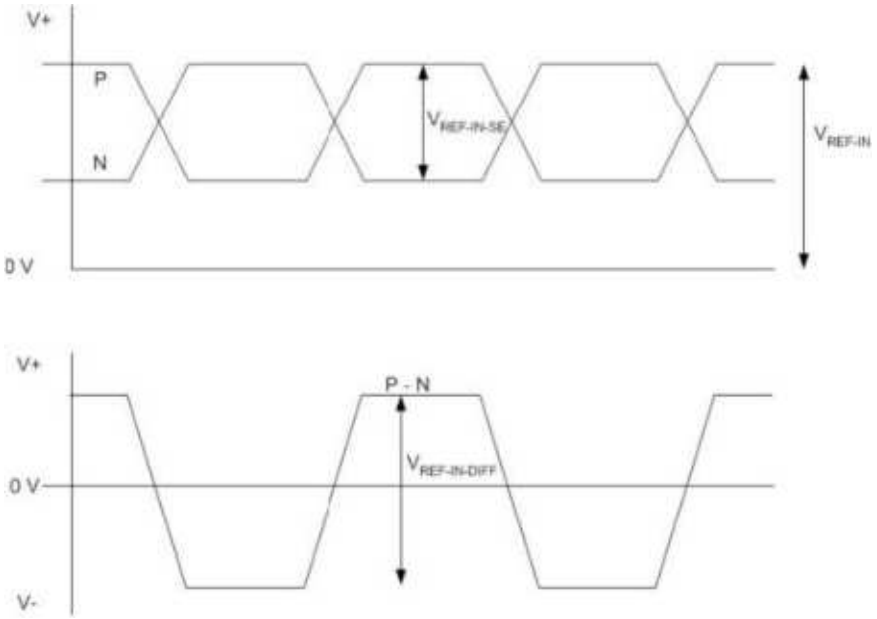


Figure 4.13. SERDES External Reference Clock Waveforms

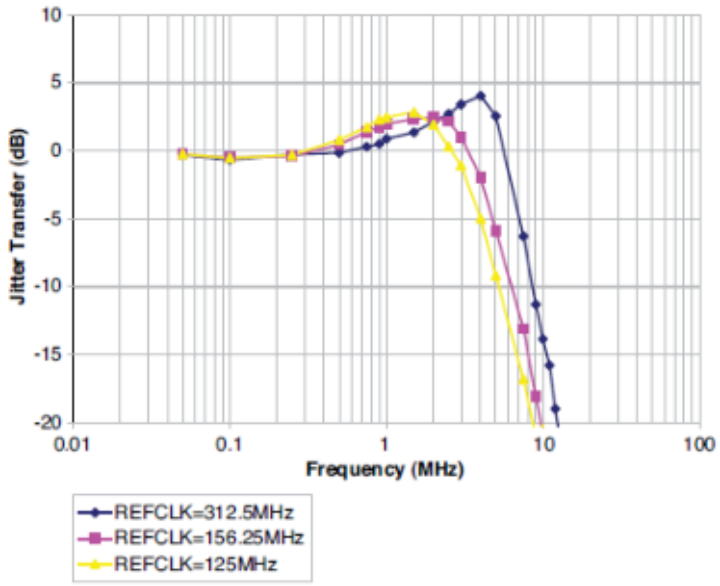


Figure 4.14. Jitter Transfer – 3.125 Gbps

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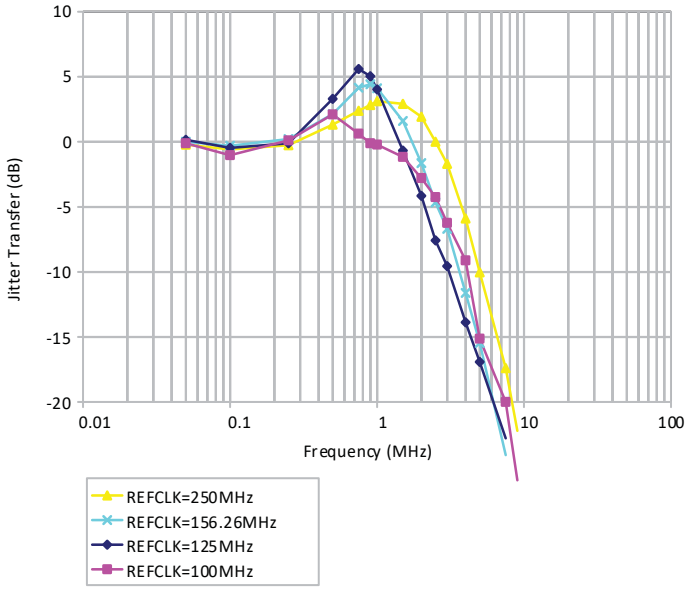


Figure 4.15. Jitter Transfer – 2.5 Gbps

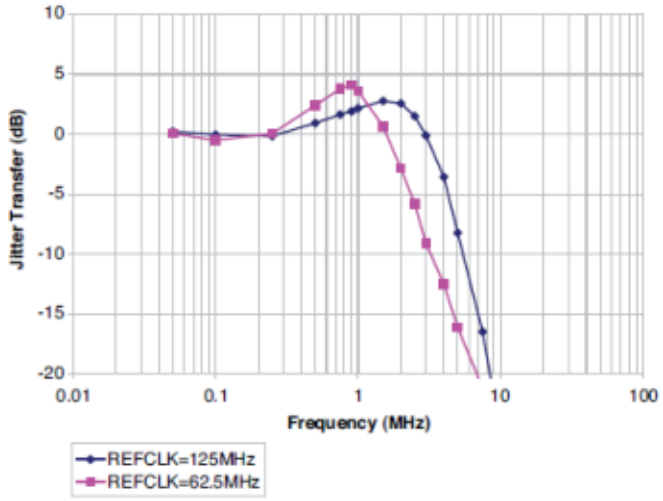


Figure 4.16. Jitter Transfer – 1.25 Gbps

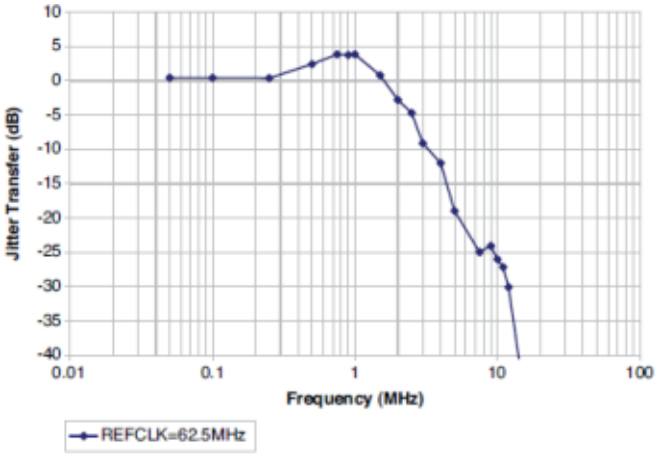


Figure 4.17. Jitter Transfer – 622 Mbps

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4.26. PCI Express Electrical and Timing Characteristics

4.26.1. AC and DC Characteristics

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min	Typ	Max	Units
Transmit[1]						
UI	Unit interval	—	399.88	400	400.12	ps
$V_{TX-DIFF_P-P}$	Differential peak-to-peak output voltage	—	0.8	1.0	1.2	V
$V_{TX-DE-RATIO}$	De-emphasis differential output voltage ratio	—	-3	-3.5	-4	dB
$V_{TX-CM-AC_P}$	RMS AC peak common-mode output voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection	—	—	—	600	mV
$V_{TX-DC-CM}$	Tx DC common mode voltage	—	0	—	V_{CCOB} + 5%	V
$I_{TX-SHORT}$	Output short circuit current	V_{TX-D+}=0.0 V V_{TX-D-}=0.0 V	—	—	90	mA
$Z_{TX-DIFF-DC}$	Differential output impedance	—	80	100	120	Ω
$RL_{TX-DIFF}$	Differential return loss	—	10	—	—	dB
RL_{TX-CM}	Common mode return loss	—	6.0	—	—	dB
$T_{TX-RISE}$	Tx output rise time	20 to 80%	0.125	—	—	UI
$T_{TX-FALL}$	Tx output fall time	20 to 80%	0.125	—	—	UI
$L_{TX-SKEW}$	Lane-to-lane static output skew for all lanes in port/link	—	—	—	1.3	ns
T_{TX-EYE}	Transmitter eye width	—	0.75	—	—	UI
$T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median	—	—	—	0.125	UI
Receive[1, 2]						
UI	Unit Interval	—	399.88	400	400.12	ps
$V_{RX-DIFF_P-P}$	Differential peak-to-peak input voltage	—	0.34[3]	—	1.2	V
$V_{RX-IDLE-DET-DIFF_P-P}$	Idle detect threshold voltage	—	65	—	340[3]	mV
$V_{RX-CM-AC_P}$	Receiver common mode voltage for AC coupling	—	—	—	150	mV
$Z_{RX-DIFF-DC}$	DC differential input impedance	—	80	100	120	Ω
Z_{RX-DC}	DC input impedance	—	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Power-down DC input impedance	—	200K	—	—	Ω
$RL_{RX-DIFF}$	Differential return loss	—	10	—	—	dB
RL_{RX-CM}	Common mode return loss	—	6.0	—	—	dB
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Maximum time required for receiver to recognize and signal an unexpected idle on link	—	—	—	—	ms

Notes:

1. Values are measured at 2.5 Gbps.
2. Measured with external AC-coupling on the receiver.
3. Not in compliance with PCI Express 1.1 standard.

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4.27. XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

4.27.1. AC and DC Characteristics

Table 4.15. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential impedance		80	100	120	Ω
J_{TX_DDJ}[2,3,4]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[1,2,3,4]	Total output data jitter		—	—	0.35	UI

Notes:

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-Ω impedance (100-Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 4.16. Receive and Jitter Tolerance

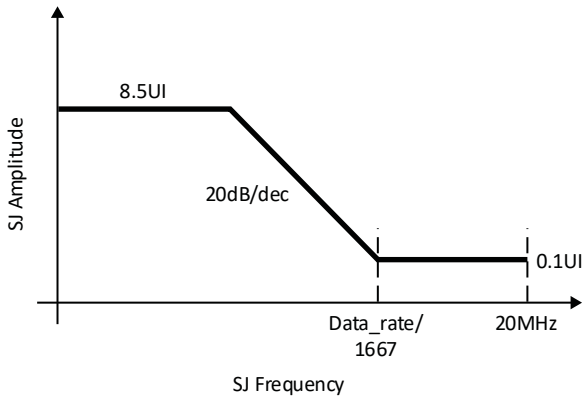
Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance	—	80	100	120	Ω
J_{RX_DJ}[1,2,3]	Deterministic jitter tolerance (peak-to-peak)	—	—	—	0.37	UI
J_{RX_RJ}[1,2,3]	Random jitter tolerance (peak-to-peak)	—	—	—	0.18	UI
J_{RX_SJ}[1,2,3]	Sinusoidal jitter tolerance (peak-to-peak)	—	—	—	0.10	UI
J_{RX_TJ}[1,2,3]	Total jitter tolerance (peak-to-peak)	—	—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening	—	0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 4.18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

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Note: The sinusoidal jitter tolerance is measured with at least 0.37UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

Figure 4.18. XAUI Sinusoidal Jitter Tolerance Mask

4.28. Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

4.28.1. AC and DC Characteristics

Table 4.17. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}[1]	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential impedance		80	100	120	Ω
J_{TX_DDJ}[3,4,5]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[2, 3, 4, 5]	Total output data jitter		—	—	0.35	UI

Notes:

1. Rise and Fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ω impedance (100-Ω differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

Table 4.18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ω
J_{RX_DJ}[2,3,4,5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[2,3,4,5]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[2,3,4,5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1,2,3,4,5]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

Notes:

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 4.18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ω impedance.

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3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

4.29. Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

4.29.1. AC and DC Characteristics

Table 4.19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX_DIFF_DC}$	Differential impedance		80	100	120	Ω
J_{TX_DDJ}[3,4,5]	Output data deterministic jitter		—	—	0.10	UI
J_{TX_TJ}[2, 3, 4, 5]	Total output data jitter		—	—	0.24	UI

Notes:
1. Rise and fall times measured with board trace, connector and approximately 2.5 pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-Ω impedance (100-Ω differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

Table 4.20. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ω
J_{RX_DJ}[1,2,3,4,5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.34	UI
J_{RX_RJ}[1,2,3,4,5]	Random jitter tolerance (peak-to-peak)		—	—	0.26	UI
J_{RX_SJ}[1,2,3,4,5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.11	UI
J_{RX_TJ}[1,2,3,4,5]	Total jitter tolerance (peak-to-peak)		—	—	0.71	UI
T_{RX_EYE}	Receiver eye opening		0.29	—	—	UI

Notes:
1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 4.18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.

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4.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

4.30.1. AC and DC Characteristics

Table 4.21. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDO}	Serial data rate		270	—	2975	Mbps
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$[2]	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$[1,2]	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission stan- dard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of fSCLK is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50-Ω impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75 kΩ 1%.

Table 4.22. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 4.23. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F_{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC_V	Duty cycle, video clock		45	50	55	%

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4.31. HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

4.31.1. AC and DC Characteristics

Table 4.24. Transmit and Receive[1, 2]

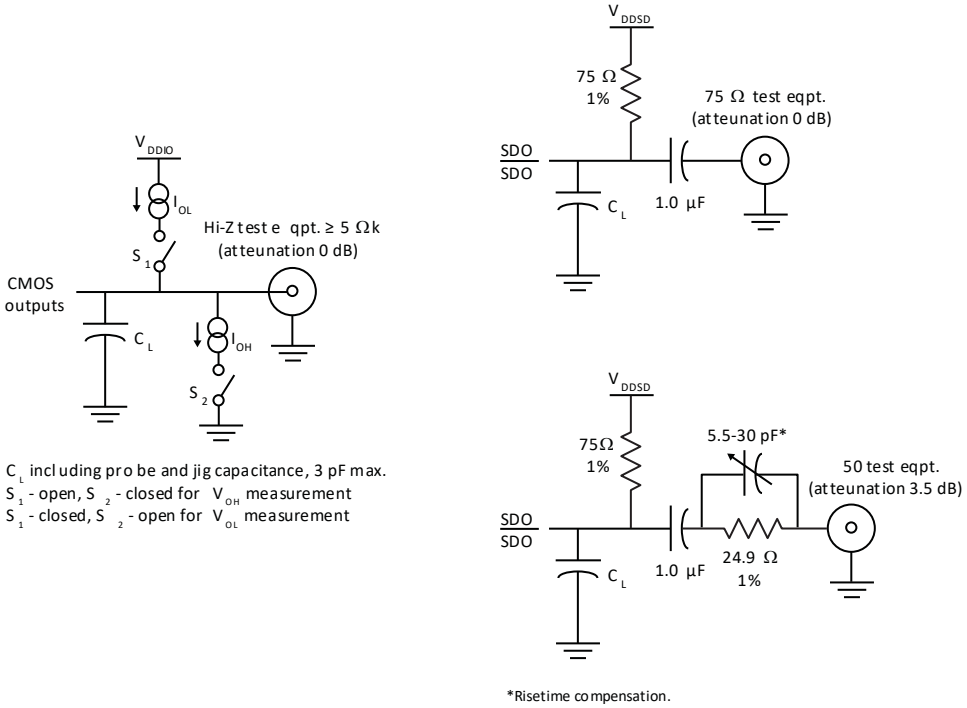
Symbol	Description	Spec. Compliance		Units
		Min. Spec.	Max. Spec.	
Transmit				
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive				
R_T	Termination Resistance	40	60	Ω
V_{ICM}	Input AC Common Mode Voltage (50-Ω Setting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

Notes:

1. Output buffers must drive a translation device. Max. speed is 2 Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5 Gbps.
2. Input buffers must be AC coupled in order to support the 3.3 V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LA-LatticeECP3 device.

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Test Loads



Timing Jitter Bandpass

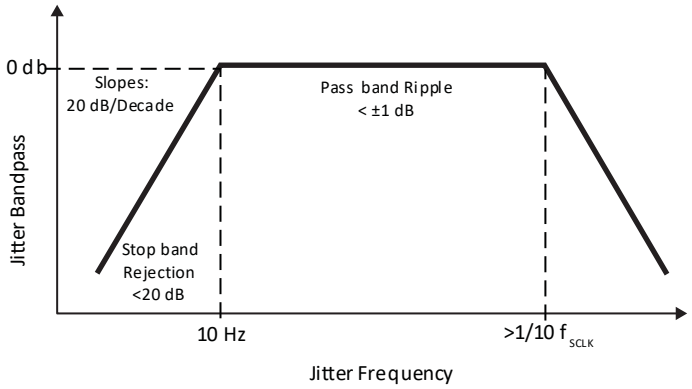


Figure 4.19. Test Loads

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4.32. LA-LatticeECP3 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description		Min.	Max.	Units
POR, Configuration Initialization, and Wakeup					
t_{ICFG}	Time from the Application of V_{CC}, V_{CCAUX} or V_{CCIO8}* (Whichever is the Last to Cross the POR Trip Point) to the Rising Edge of INITN	Master mode	—	23	ms
		Slave mode	—	6	ms
t_{VMC}	Time from t_{ICFG} to the Valid Master MCLK		—	5	µs
t_{PRGM}	PROGRAMN Low Time to Start Configuration		25	—	ns
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection		—	10	ns
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low		—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low		—	37	ns
t_{DINIT}[1]	PROGRAMN High to INITN High Delay		—	1	ms
t_{MWC}	Additional Wake Master Clock Signals After DONE Pin is High		100	500	cycles
t_{CZ}	MCLK From Active To Low To High-Z		—	300	ns
All Configuration Modes					
t_{SUCDI}	Data Setup Time to CCLK/MCLK		5	—	ns
t_{HCDI}	Data Hold Time to CCLK/MCLK		1	—	ns
t_{CODO}	CCLK/MCLK to DOUT in Flowthrough Mode		-0.2	12	ns
Slave Serial					
t_{SSCH}	CCLK Minimum High Pulse		5	—	ns
t_{SSCL}	CCLK Minimum Low Pulse		5	—	ns
f_{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave Parallel					
t_{SUCS}	CSN[1:0] Setup Time to CCLK/MCLK		7	—	ns
t_{HCS}	CSN[1:0] Hold Time to CCLK/MCLK		1	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK/MCLK		7	—	ns
t_{HWD}	WRITEN Hold Time to CCLK/MCLK		1	—	ns
t_{DCB}	CCLK/MCLK to BUSY Delay Time		—	12	ns
t_{CORD}	CCLK to Out for Read Data		—	12	ns
t_{BSCH}	CCLK Minimum High Pulse		6	—	ns
t_{BSCL}	CCLK Minimum Low Pulse		6	—	ns
t_{BSCYC}	Byte Slave Cycle Time		30	—	ns
f_{CCLK}	CCLK/MCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
Master and Slave SPI					
t_{CFGX}	INITN High to MCLK Low		—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low		0.2	2	µs
t_{SOCDO}	MCLK Low to Output Valid		—	15	ns
t_{CSPID}	CSSPIN[0:1] Low to First MCLK Edge Setup Time		0.3		µs
f_{CCLK}	CCLK Frequency	Without encryption	—	33	MHz
		With encryption	—	20	MHz
t_{SSCH}	CCLK Minimum High Pulse		5	—	ns
t_{SSCL}	CCLK Minimum Low Pulse		5	—	ns

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Parameter	Description	Min.	Max.	Units
t_{HLCH}	HOLDN Low Setup Time (Relative to CCLK)	5	—	ns
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

Note:

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

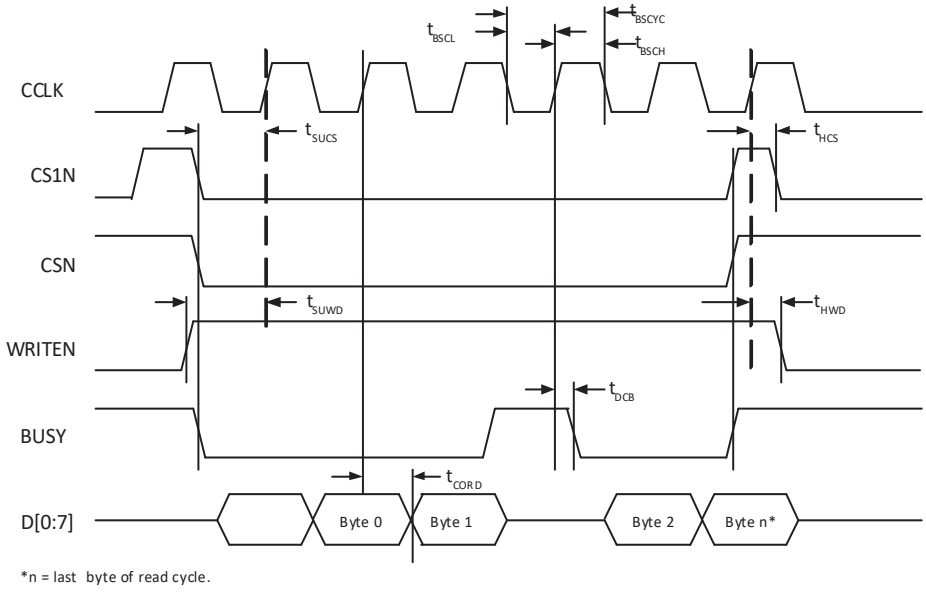
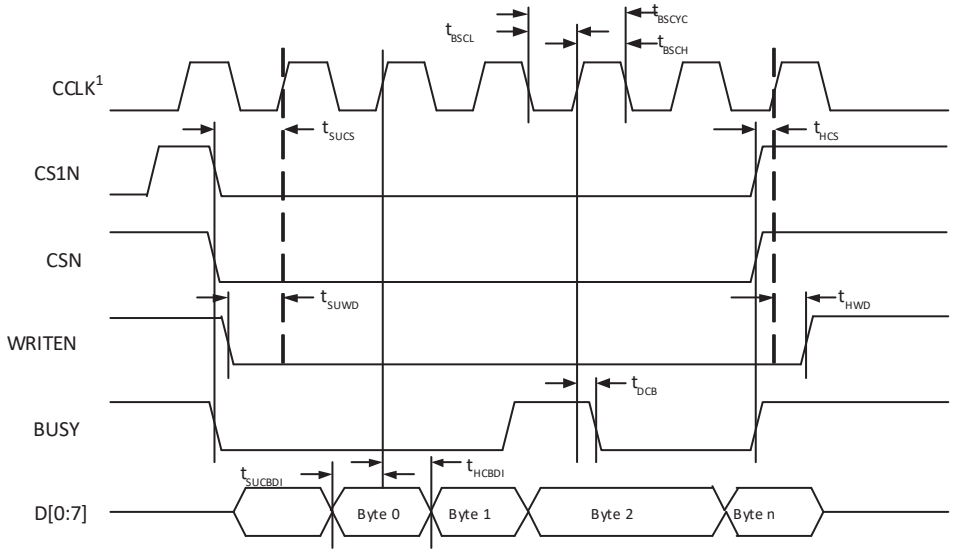


Figure 4.20. sysCONFIG Parallel Port Read Cycle

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1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 4.21. sysCONFIG Parallel Port Write Cycle

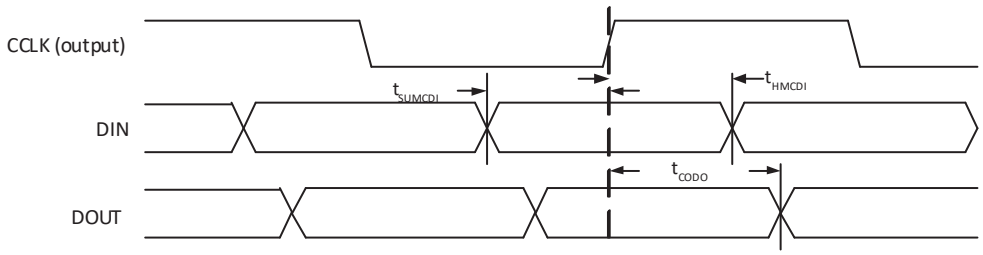


Figure 4.22. sysCONFIG Master Serial Port Timing

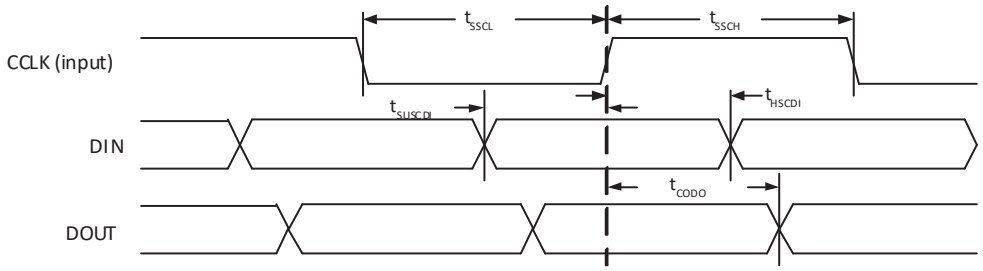
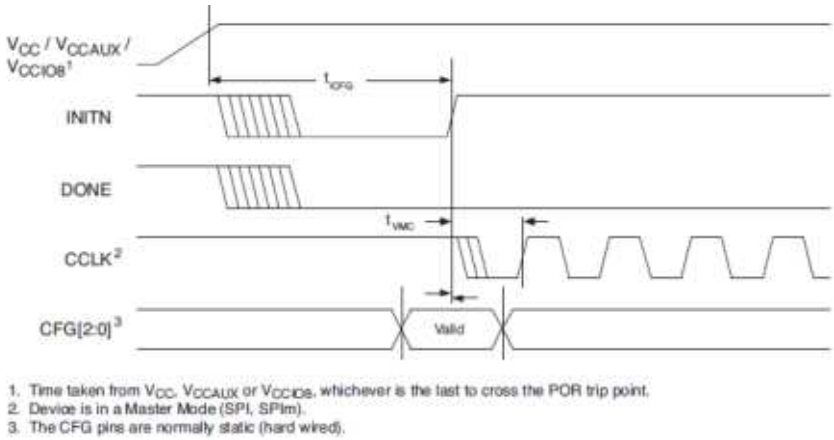


Figure 4.23. sysCONFIG Slave Serial Port Timing

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1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hard wired).

Figure 4.24. Power-On-Reset (POR) Timing

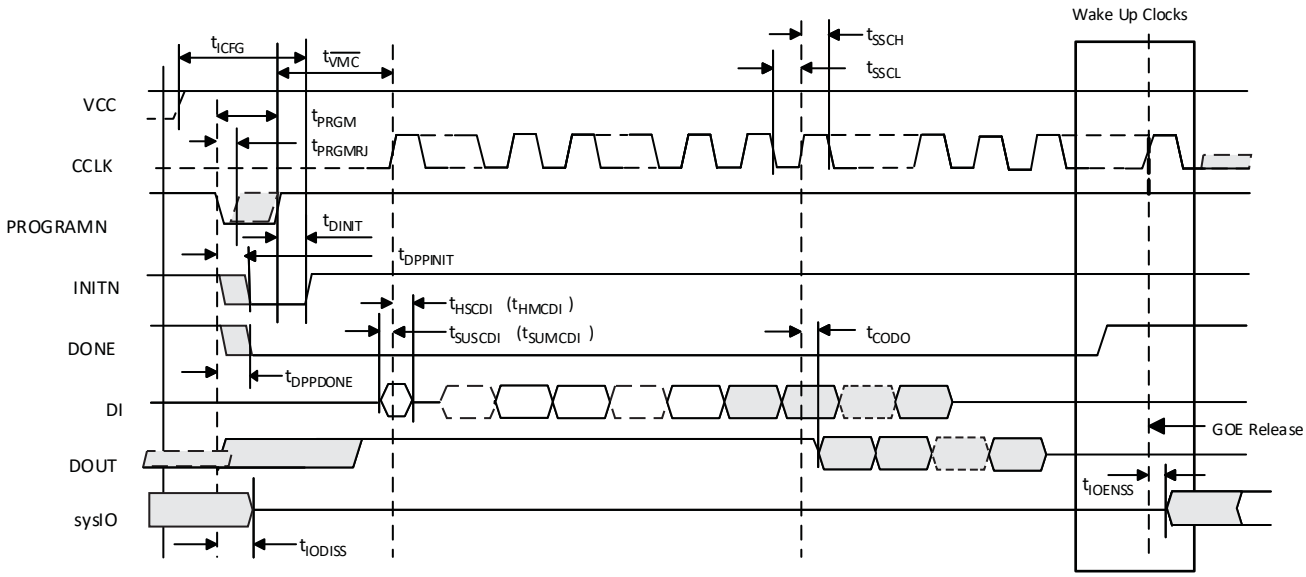
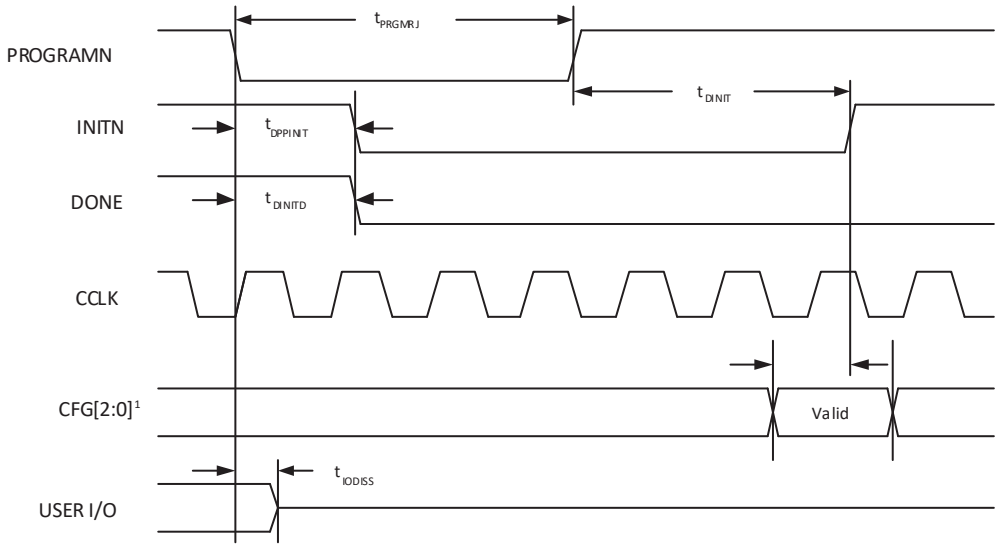


Figure 4.25. sysCONFIG Port Timing

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1. The CFG pins are normally static (hard wired)

Figure 4.26. Configuration from PROGRAMN Timing

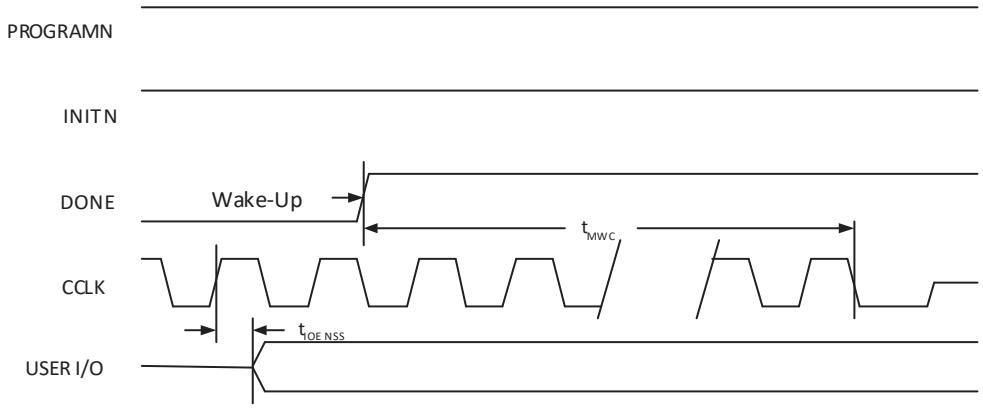


Figure 4.27. Wake-Up Timing

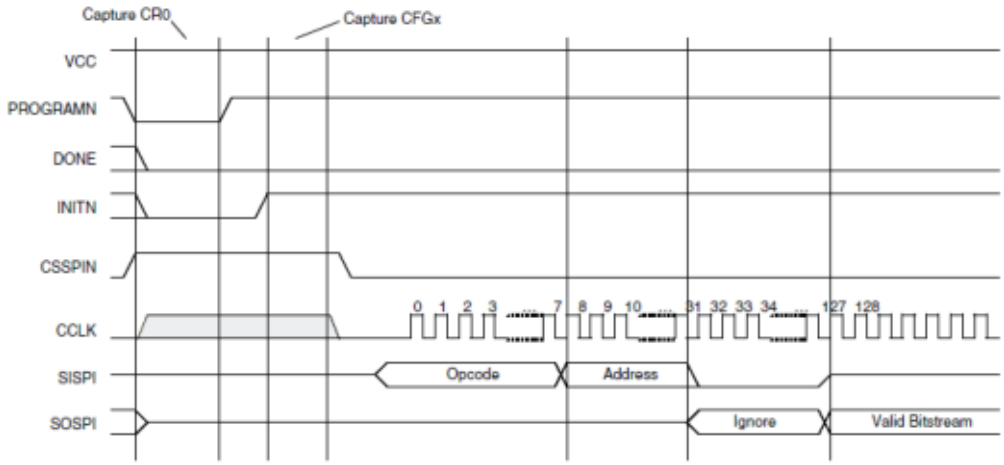


Figure 4.28. Master SPI Configuration Waveforms

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4.33. JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

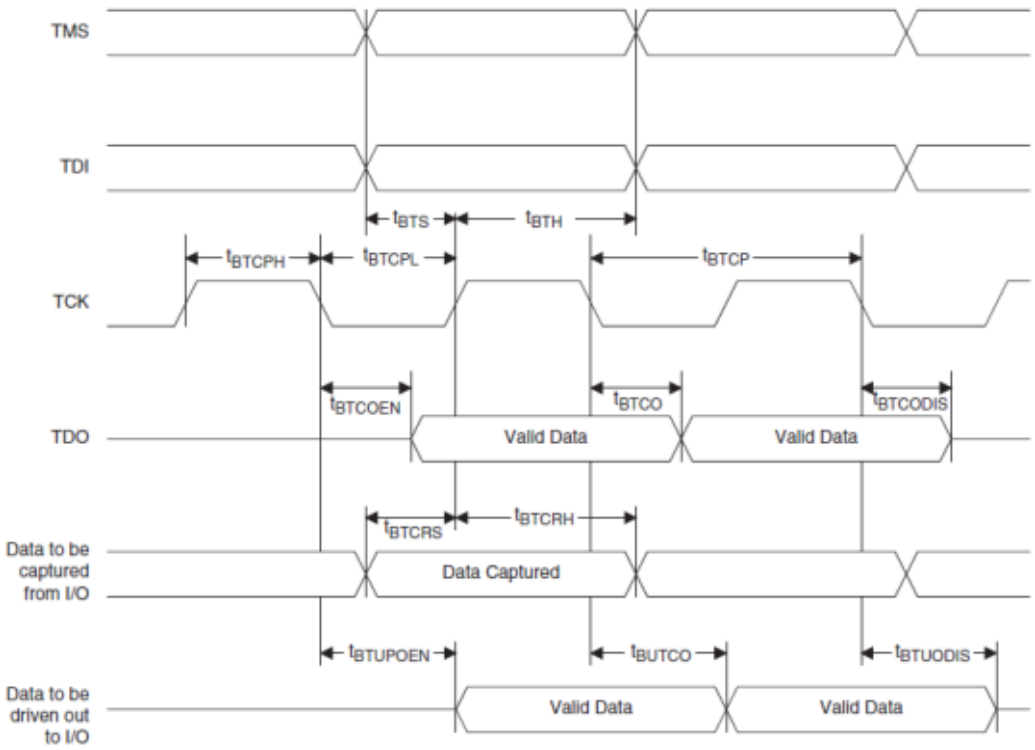
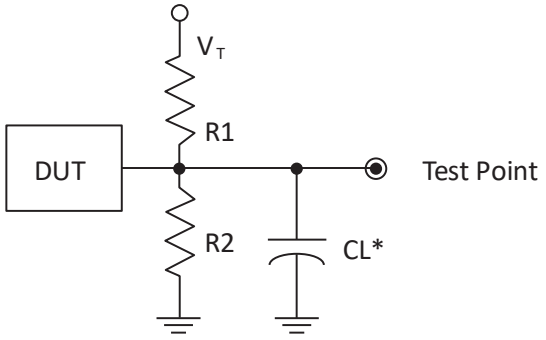


Figure 4.29. JTAG Port Timing Waveforms

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4.34. Switching Test Conditions

Figure 4.30 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 4.25.



*CL Includes Test Fixture and Probe Capacitance

Figure 4.30. Output Test Load, LVTTL and LVCMOS Standards

Table 4.25. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞	0pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0pF	V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

4.35. sysI/O Differential Electrical Characteristics

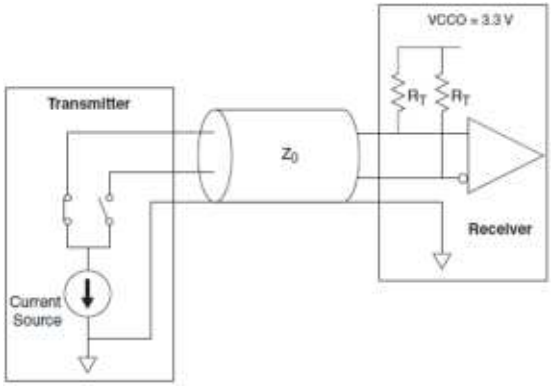
4.35.1. Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/– 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150	—	1200	mV
V_{ICM}	Input common mode voltage	3	—	3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ω

Note: LA-LatticeECP3 only supports the TRLVDS receiver.

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4.35.2. Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	Ω
R_T	Differential termination resistance	50	100	150	Ω
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6 mA differential current drive. Other differential driver current options are available.

4.35.3. Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Typ.	Max.	Units
Output driver supply (+/- 5%)	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100	—	400	mV
Input common mode voltage	0.2	—	2.3	V
Output differential voltage	130	—	400	mV
Output common mode voltage	0.5	0.8	1.4	V

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4.35.4. RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, R_T = 100 Ω	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2 mA drive. Other differential driver current options are available.

4.36. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Column Number. When Edge is L (Left) or R (Right), only need to specify Row Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/O for user logic. During configuration the user-programmable I/O are tristated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tristated with an internal pull-up resistor enabled after configuration.
P[Edge][Row Number]E_[A/B/C/D]	I	These general purpose signals are input-only pins and are located near the PLLs.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{CCA}	—	SERDES, transmit, receive, PLL and reference clock buffer power supply. All V_{CCA} supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect V_{CCA} to V_{CC}.
$V_{CCPLL_[LOC]}$	—	General purpose PLL supply pins where LOC=L (left) or R (right).
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
VTTx	—	Power supply for on-chip termination of I/O.
XRES[1]	—	10K Ω +/-1% resistor must be connected between this pad and ground.
PLL, DLL and Clock Functions		
[LOC][num]_GPLL[T, C]_IN_[index]	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from

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Signal Name	I/O	Description
		center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_[index]	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC]0_GDLLT_IN_[index][2]	I/O	General Purpose DLL (GDLL) input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
[LOC]0_GDLLT_FB_[index][2]	I/O	Optional feedback GDLL input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
PCLK[T, C][n:0]_[3:0][2]	I/O	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank.
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSON/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration.
		sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.

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Signal Name	I/O	Description
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals[3]		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	O	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	O	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm	—	Output buffer power supply, channel m (1.2 V/1.5)
PCS[Index]_VCCIBm	—	Input buffer power supply, channel m (1.2 V/1.5V)

Notes:

1. When placing switching I/O around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

4.37. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
For Top Edge of the Device		
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ

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PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ

Note: "n" is a row PIC number.

4.38. Pin Information Summary

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		**256 ftBGA**	**328 csBGA**	**484 fpBGA**	**256 ftBGA**	**484 fpBGA**	**672 fpBGA**
General Purpose Inputs/Outputs per Bank	Bank 0	26	20	36	26	42	48
	Bank 1	14	10	24	14	36	36
	Bank 2	6	7	12	6	24	24
	Bank 3	18	12	44	16	54	59
	Bank 6	20	11	44	18	63	61
	Bank 7	19	26	32	19	36	42
	Bank 8	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4
	Bank 3	0	0	0	2	4	4
	Bank 6	0	0	0	2	4	4
	Bank 7	4	4	4	4	4	4
	Bank 8	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0
Total Single-Ended User I/O		133	116	222	133	295	310
VCC		6	16	16	6	16	32
VCCAUX		4	5	8	4	8	12
VTT		4	7	4	4	4	4
VCCA		4	6	4	4	4	8
VCCPLL		2	2	4	2	4	4
VCCIO	Bank 0	2	3	2	2	2	4
	Bank 1	2	3	2	2	2	4
	Bank 2	2	2	2	2	2	4
	Bank 3	2	3	2	2	2	4
	Bank 6	2	3	2	2	2	4
	Bank 7	2	3	2	2	2	4
	Bank 8	1	2	2	1	2	2
VCCJ		1	1	1	1	1	1
TAP		4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139
NC		0	0	73	0	0	96

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Pin Information Summary		ECP3-17EA			ECP3-35EA		
Reserved[1]		0	0	2	0	2	2
SERDES		26	18	26	26	26	26
Miscellaneous Pins		8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672
Pin Type		**256 ftBGA**	**328 csBGA**	**484 fpBGA**	**256 ftBGA**	**484 fpBGA**	**672 fpBGA**
Emulated Differential I/O per Bank	Bank 0	13	10	18	13	21	24
	Bank 1	7	5	12	7	18	18
	Bank 2	2	2	4	1	8	8
	Bank 3	4	2	13	5	20	19
	Bank 6	5	1	13	6	22	20
	Bank 7	6	9	10	6	11	13
	Bank 8	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	3	3	6	6
	Bank 3	5	4	9	4	9	12
	Bank 6	5	4	9	4	11	12
	Bank 7	5	6	8	5	9	10
	Bank 8	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	20/10	36/18	26/13	42/21	48/24
	Bank 1	14/7	10/5	24/12	14/7	36/18	36/18
	Bank 2	8/4	9/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	12/6	44/22	18/9	58/29	63/31
	Bank 6	20/10	11/5	44/22	20/10	67/33	65/32
	Bank 7	23/11	30/15	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank[2]	Bank 0	2	1	3	2	3	4
	Bank 1	1	0	2	1	3	3
	Bank 2	0	0	1	0	2	2
	Bank 3	1	0	3	1	3	4
	Bank 6	1	0	3	1	4	4
	Bank 7	1	2	2	1	3	3
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	1	1	1	1	1

Notes:

1. These pins must remain floating on the board.
2. Some DQS groups may not support DQS-12. Refer to the device pinout (.csv) file.

4.39. Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at www.latticesemi.com/products/fpga/ecp3 and in the Diamond software tool. To create a pin information file from within Diamond select **Tools > Spreadsheet View or Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond Help for more information.

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4.40. Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

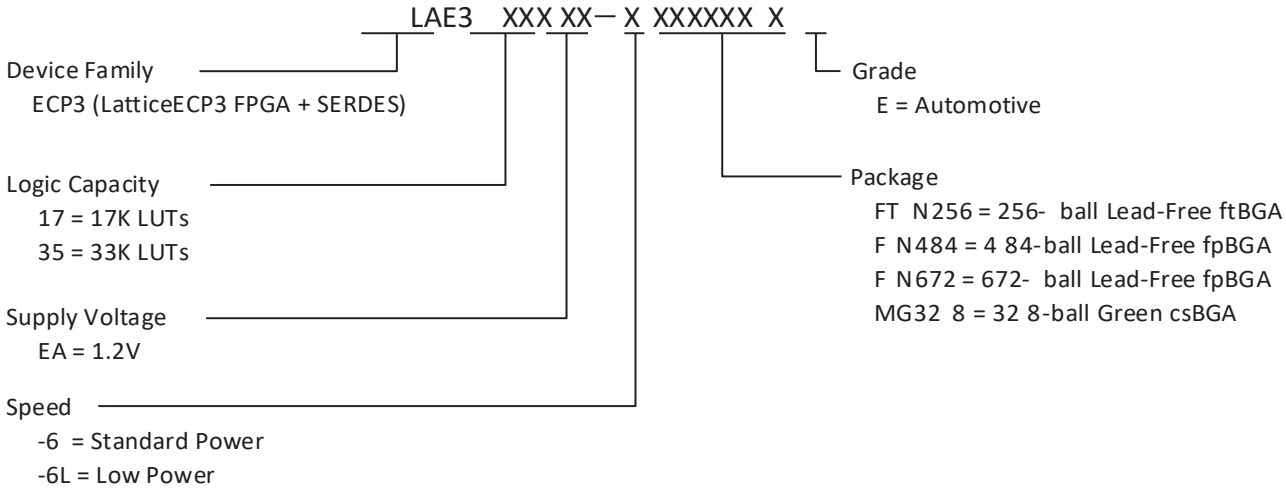
4.40.1. For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- Power Consumption and Management for LatticeECP3 Devices (FPGA-TN-02189)
- Power Calculator tool included with the Diamond design tool, or as a standalone download from www.latticesemi.com/software

5. Ordering Information

5.1. LA-LatticeECP3 Part Number Description



5.1.1. Ordering Information

LA-LatticeECP3 devices have top-side markings, for automotive grades, as shown below:



Note: See PCN 05A-12 for information regarding a change to the top-side mark logo.

Products are not designed, intended or warranted to be fail-safe and are not designed, intended or warranted for use in applications related to deployment of airbags. Further, products are not intended to be used, designed, or warranted for use in applications that affect the control of the vehicle unless there is a fail-safe or redundancy feature and also a warning signal to the operator of the vehicle upon failure. Use of products in such applications is fully at the risk of the customer, subject to applicable laws and regulations governing limitations on product liability.

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5.1.1.1. LA-LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUT (Ks)
LAE3-17EA-6FTN256E	1.2	6	Lead-Free ftBGA	256	Auto	17
LAE3-17EA-6LFTN256E	1.2	6L	Lead-Free ftBGA	256	Auto	17
LAE3-17EA-6MG328E	1.2	6	Green csBGA	328	Auto	17
LAE3-17EA-6LMG328E	1.2	6L	Green csBGA	328	Auto	17
LAE3-17EA-6FN484E	1.2	6	Lead-Free fpBGA	484	Auto	17
LAE3-17EA-6LFN484E	1.2	6L	Lead-Free fpBGA	484	Auto	17
LAE3-35EA-6LFTN256E	1.2	6L	Lead-Free ftBGA	256	Auto	35
LAE3-35EA-6FN484E	1.2	6	Lead-Free fpBGA	484	Auto	35
LAE3-35EA-6LFN484E	1.2	6L	Lead-Free fpBGA	484	Auto	35
LAE3-35EA-6FN672E	1.2	6	Lead-Free fpBGA	672	Auto	35
LAE3-35EA-6LFN672E	1.2	6L	Lead-Free fpBGA	672	Auto	35

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6. Supplemental Information

6.1. For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website.

- LatticeECP3 sysCONFIG Usage Guide (FPGA-TN-02192)
- LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190)
- LatticeECP3 sysIO Usage Guide (FPGA-TN-02194)
- LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02191)
- LatticeECP3 Memory Usage Guide (FPGA-TN-02188)
- LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184)
- Power Consumption and Management for LatticeECP3 Devices (FPGA-TN-02189)
- LatticeECP3 sysDSP Usage Guide (FPGA-TN-02193)
- LatticeECP3 Soft Error Detection (SED) Usage Guide (FPGA-TN-02207)
- LatticeECP3 Hardware Checklist (FPGA-TN-02183)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

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Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

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Revision History

Revision 1.3, July 2021

Section	Change Summary
All	Updated document template.
Disclaimers	Added this section.
DC and Switching Characteristics	Added Note 2 in section 4.10 sysI/O Single-Ended DC Electrical Characteristics.

Revision 1.2, March 2019

Section	Change Summary
All	• Changed document status from Advance to Final. • Updated document number from DS1041 to FPGA-DS-02052. • Applied minor style and formatting changes. • Updated document template.
Ordering Information	Specified Standard Power (-6) and Low Power (-6L) for Speed.

Revision 1.1, April 2014

Section	Change Summary
Introduction	Added AEC-Q100 Tested and Qualified feature.

Revision 1.0, June 2013

Section	Change Summary
All	Initial release.

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