LA-ispMACH 4000V/Z® Automotive Family

3.3 V/1.8 V In-System Programmable SuperFAST High Density PLDs

Data Sheet

FPGA-DS-02021 Version 2.6

September 2017

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AEC	Automotive Electronic Council
GLB	Generic Logic Blocks
GRP	Global Routing Pool
IOB	I/O Blocks
ISP	In-System Programming
ORP	Output Routing Pool
TQFP	Thin Quad Flat Pack
UES	User Electronic Signature

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1. Features

- High Performance
  - f_{MAX} = 168 MHz maximum operating frequency
  - t_{PD} = 7.5 ns propagation delay
  - Up to four global clock pins with programmable clock polarity control
  - Up to 80 PTs per output
- Ease of Design
  - Enhanced macrocells with individual clock, reset, preset and clock enable controls
  - Up to four global OE controls
  - Individual local OE control per I/O pin
  - Excellent First-Time-Fit™ and refit
  - Fast path, SpeedLocking™ Path, and wide-PT path
  - Wide input gating (36 input logic blocks) for fast counters, state machines and address decoders
- Zero Power (LA-ispMACH 4000Z)
  - Typical static current 10 µA (4032Z)
  - 1.8 V core low dynamic power
  - LA-ispMACH 4000Z operational down to 1.6 V
- AEC-Q100 Tested and Qualified
  - Automotive: -40 to 125 °C ambient (T_A)
- Easy System Integration
  - Superior solution for power sensitive consumer applications
  - Operation with 3.3 V, 2.5 V or 1.8 V LVCMOS I/O
  - Operation with 3.3 V (4000V) or 1.8 V (4000Z) supplies
  - 5 V tolerant I/O for LVCMOS 3.3, LVTTL, and PCI interfaces
  - Hot-socketing
  - Open-drain capability
  - Input pull-up, pull-down or bus-keeper
  - Programmable output slew rate
  - 3.3 V PCI compatible
  - IEEE 1149.1 boundary scan testable
  - 3.3 V/2.5 V/1.8 V In-System Programmable (ISP™) using IEEE 1532 compliant interface
  - I/O pins with fast setup path
  - Lead-free (RoHS) package

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2. Introduction

The high performance LA-ispMACH 4000V/Z automotive family from Lattice offers a SuperFAST CPLD solution that is tested and qualified to the AEC-Q100 standard. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the LA-ispMACH 4000V/Z architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The LA-ispMACH 4000V/Z automotive family combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pinout retention and density migration.

Table 2.1. LA-ispMACH 4000V Automotive Family Selection Guide

	LA-ispMACH 4032V	LA-ispMACH 4064V	LA-ispMACH 4128V
Macrocells	32	64	128
I/O + Dedicated Inputs	30+2/32+4	30+2/32+4/64+10	64+10/92+4/96+4
t_{PD} (ns)	7.5	7.5	7.5
t_S (ns)	4.5	4.5	4.5
t_{CO} (ns)	4.5	4.5	4.5
f_{MAX} (MHz)	168	168	168
Supply Voltage (V)	3.3 V	3.3 V	3.3 V
Pins/Package	44-pin Lead-Free TQFP 48-pin Lead-Free TQFP	44-pin Lead-Free TQFP 48-pin Lead-Free TQFP 100-pin Lead-Free TQFP	100-pin Lead-Free TQFP 128-pin Lead-Free TQFP 144-pin Lead-Free TQFP

Table 2.2. LA-ispMACH 4000Z Automotive Family Selection Guide

	LA-ispMACH 4032Z	LA-ispMACH 4064Z	LA-ispMACH 4128Z
Macrocells	32	64	128
I/O + Dedicated Inputs	32+4	32+4/64+10	64+10
t_{PD} (ns)	7.5	7.5	7.5
t_S (ns)	4.5	4.5	4.5
t_{CO} (ns)	4.5	4.5	4.5
f_{MAX} (MHz)	168	168	168
Supply Voltage (V)	1.8 V	1.8 V	1.8 V
Pins/Package	48-pin Lead-Free TQFP	48-pin Lead-Free TQFP 100-pin Lead-Free TQFP	100-pin Lead-Free TQFP

The LA-ispMACH 4000V/Z automotive family offers densities ranging from 32 to 128 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) packages ranging from 44 to 144 pins. Table 2.1 and Table 2.2 show the macrocell, package and I/O options, along with other key parameters.

The LA-ispMACH 4000V/Z automotive family has enhanced system integration capabilities. It supports 3.3 V (4000V and 1.8 V (4000Z) supply voltages and 3.3 V, 2.5 V and 1.8 V interface voltages. Additionally, inputs can be safely driven up to 5.5 V when an I/O bank is configured for 3.3 V operation, making this family 5 V tolerant. The LA-ispMACH 4000V/Z also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The LA-ispMACH 4000V/Z automotive family is in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to VCC (logic core).

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3. Overview

The LA-ispMACH 4000V/Z automotive devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 3.1.

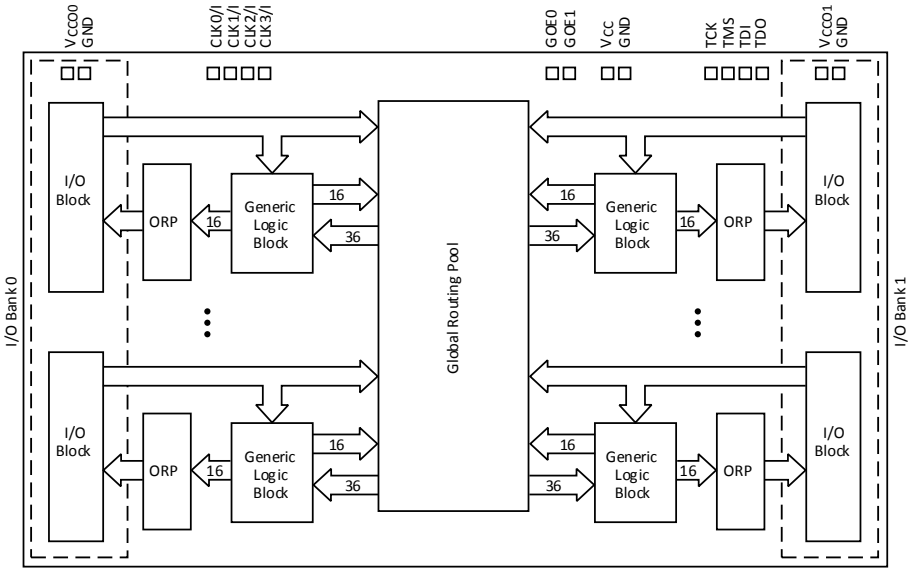


Figure 3.1. Functional Block Diagram

The I/Os in the LA-ispMACH 4000V/Z automotive devices are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5 V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0 V to 3.6 V for LVCMOS 3.3, LVTTL and PCI interfaces.

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4. Architecture

There are a total of two GLBs in the LA-ispMACH 4032V/Z, increasing to 8 GLBs in the LA-ispMACH 4128V/Z. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

4.1. Generic Logic Block

The LA-ispMACH 4000V/Z Automotive GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 4.1 illustrates the GLB.

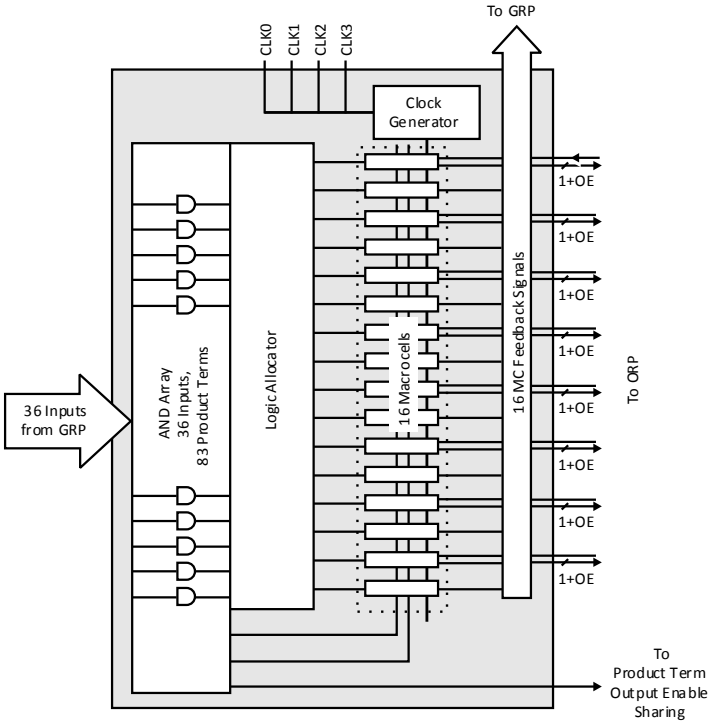


Figure 4.1. Generic Logic Block

4.2. AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 4.2 is a graphical representation of the AND Array.

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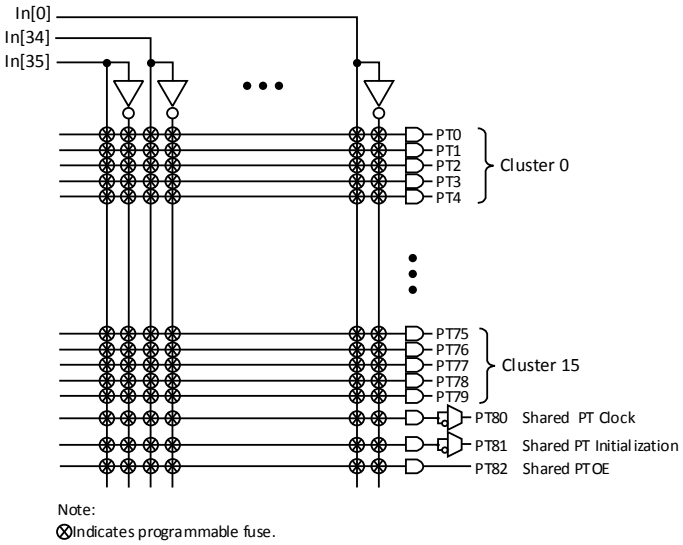


Figure 4.2. AND Array

4.3. Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the LA-ispMACH 4000V/Z automotive family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the LA-ispMACH 4000V/Z automotive family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4.3 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

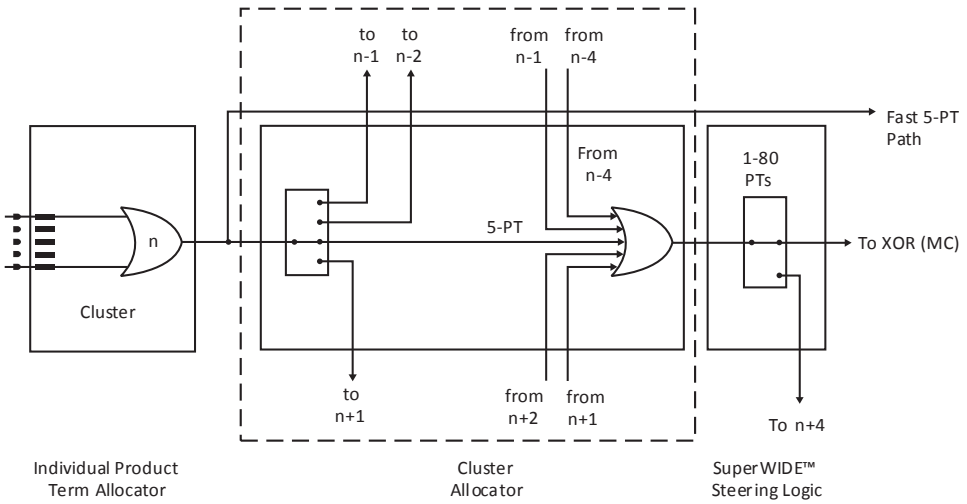


Figure 4.3. Macrocell Slice

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4.4. Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 4.1 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 4.1. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

4.5. Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 4.2 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 4.2. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

4.6. Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4.3 shows the product term chains.

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Table 4.3. Product Term Expansion Capability

Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 → M4 → M8 → M12 → M0	75
Chain-1	M1 → M5 → M9 → M13 → M1	80
Chain-2	M2 → M6 → M10 → M14 → M2	75
Chain-3	M3 → M7 → M11 → M15 → M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

4.7. Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 4.4 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

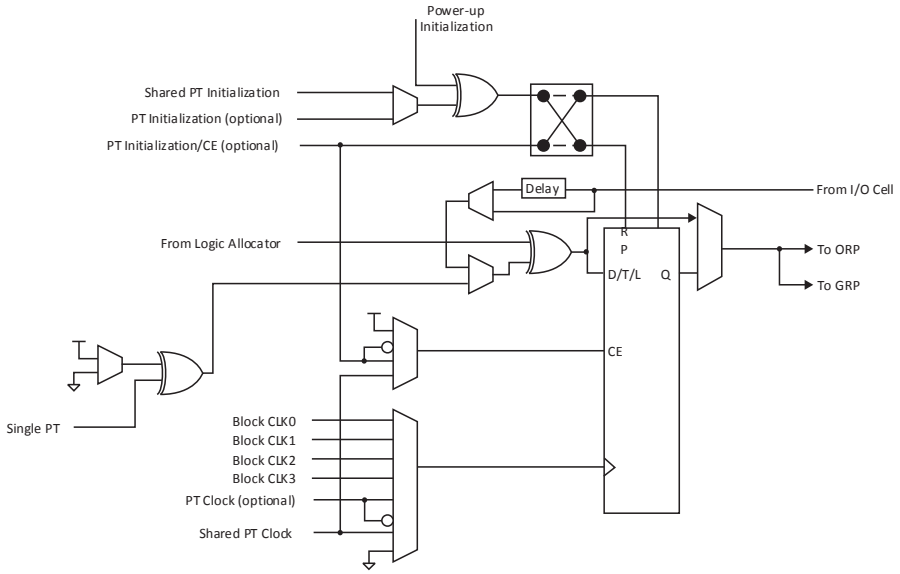


Figure 4.4. Macrocell

4.8. Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1
- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

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4.9. Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

4.10. Initialization Control

The LA-ispMACH 4000V/Z automotive family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power- up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

4.11. GLB Clock Generator

Each LA-ispMACH 4000V/Z automotive device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 4.5. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

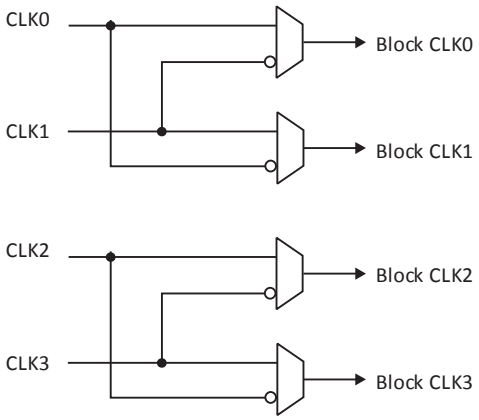


Figure 4.5. GLB Clock Generator

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4.12. Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multiplexers and feed the I/O cell directly. The enhanced ORP of the LA-ispMACH 4000V/Z family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 4.6 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

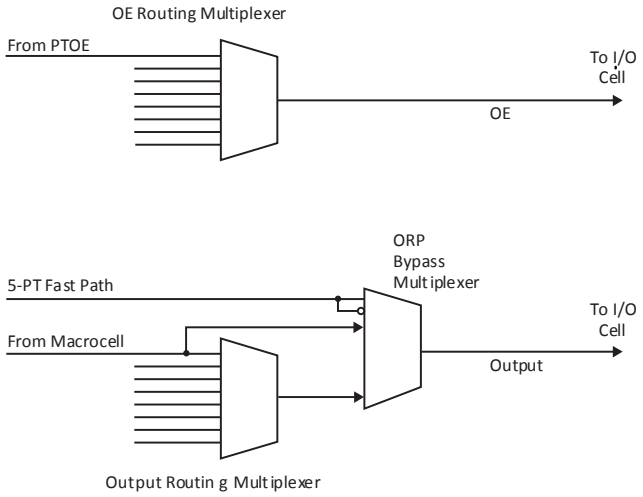


Figure 4.6. ORP Slice

4.13. Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Table 4.4 to Table 4.6 provide the connection details.

Table 4.4. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

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Table 4.5. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M13
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 4.6. ORP Combinations for I/O Blocks with 12 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M4, M5, M6, M7, M8, M9, M10, M11
I/O 4	M5, M6, M7, M8, M9, M10, M11, M12
I/O 5	M6, M7, M8, M9, M10, M11, M12, M13
I/O 6	M8, M9, M10, M11, M12, M13, M14, M15
I/O 7	M9, M10, M11, M12, M13, M14, M15, M0
I/O 8	M10, M11, M12, M13, M14, M15, M0, M1
I/O 9	M12, M13, M14, M15, M0, M1, M2, M3
I/O 10	M13, M14, M15, M0, M1, M2, M3, M4
I/O 11	M14, M15, M0, M1, M2, M3, M4, M5

4.14. ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

4.15. Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

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5. I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 5.1 details the I/O cell.

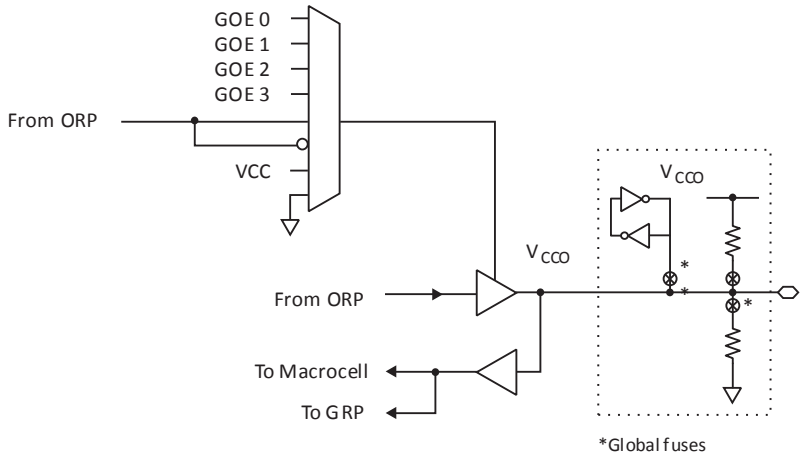


Figure 5.1. I/O Cell

Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 1.8
- LVCMOS 3.3
- 3.3 V PCI Compatible
- LVCMOS 2.5

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each LA-ispMACH 4000V/Z automotive device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

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6. Global OE Generation

Most LA-ispMACH 4000V/Z automotive family devices have a 4-bit wide Global OE Bus, except the LA-ispMACH 4032V and LA-ispMACH4032Z devices that have a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 128-macrocell device (with 16 blocks), each line of the bus is driven from 8 OE product terms. Figure 6.1 and Figure 6.2 show a graphical representation of the global OE generation.

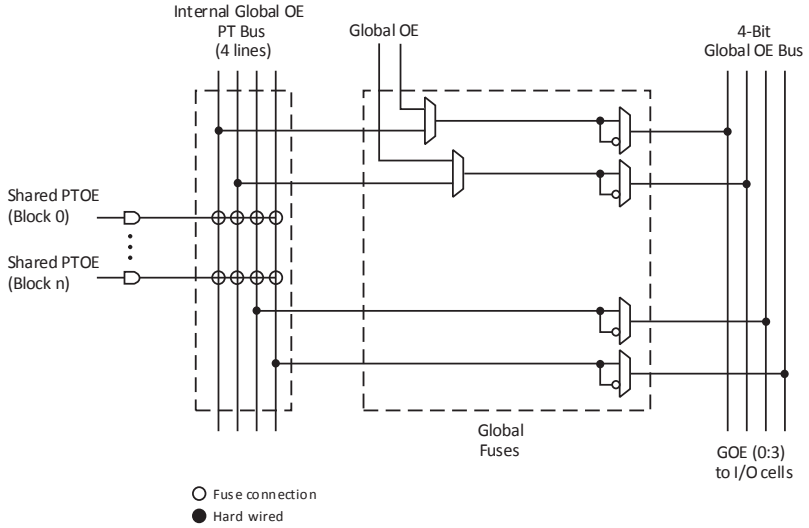


Figure 6.1. Global OE Generation for All Devices Except LA-ispMACH 4032V/Z

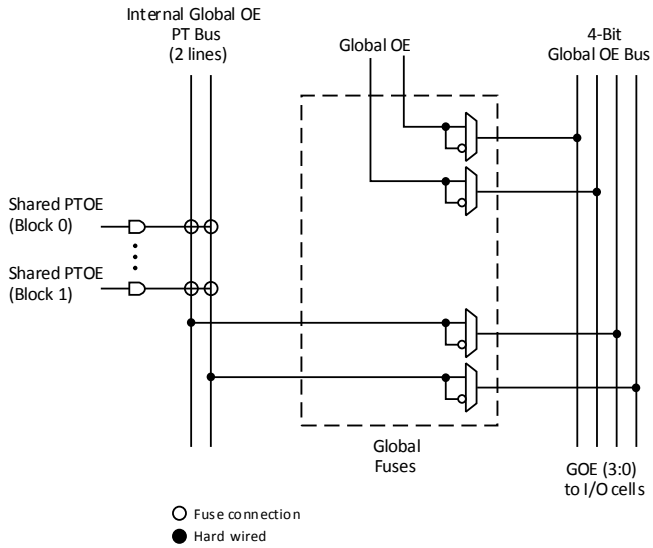


Figure 6.2. Global OE Generation for LA-ispMACH 4032V/Z

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7. Zero Power/Low Power and Power Management

The LA-ispMACH 4000V/Z automotive family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E2 low power cell and nonsense-amplifier design approach (full CMOS logic approach), the LA-ispMACH 4000V/Z automotive family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power LA-ispMACH 4000Z is based on the 1.8 V ispMACH 4000C family. With innovative circuit design changes, the LA-ispMACH 4000Z family is able to achieve the industry’s “lowest static power”.

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8. IEEE 1149.1-Compliant Boundary Scan Testability

All LA-ispMACH 4000V/Z automotive devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

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9. I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The LA-ispMACH 4000V/Z automotive family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

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10. IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. The LA-ispMACH 4000V/Z automotive devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All LA-ispMACH 4000V/Z automotive devices are also compliant with the IEEE 1532 standard.

The LA-ispMACH 4000V/Z automotive devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of LA-ispMACH 4000V/Z automotive devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program LA- ispMACH 4000V/Z automotive devices during the testing of a circuit board.

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11. User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E2CMOS memory. The LA-ispMACH 4000V/Z automotive device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

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12. Security Bit

A programmable security bit is provided on the LA-ispMACH 4000V/Z automotive devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

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13. Hot Socketing

The LA-ispMACH 4000V/Z automotive devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The LA-ispMACH 4000V/Z automotive devices provide this capability for input voltages in the range 0 V to 3.0 V.

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14. Density Migration

The LA-ispMACH 4000V/Z automotive family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

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15. AEC-Q100 Tested and Qualified

The Automotive Electronics Council (AEC) consists of two committees: the Quality Systems Committee and the Component Technical Committee. These committees are composed of representatives from sustaining and other associate members. The AEC Component Technical Committee is the standardization body for establishing standards for reliable, high quality electronic components. In particular, the AEC-Q100 specification “Stress Test for Qualification for Integrated Circuits” defines qualification and re-qualification requirements for electronic components. Components meeting these specifications are suitable for use in the harsh automotive environment without additional component-level qualification testing. Lattice's LA-ispMACH 4000V/Z and LA-MachXO devices completed and passed the requirements of the AEC-Q100 specification.

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16. Absolute Maximum Ratings[1, 2, 3]

Table 16.1. Absolute Maximum Ratings

Parameter	Min	Max
Supply Voltage (V_{CC})	–0.5 V to 5.5 V	–0.5 V to 2.5V
Output Supply Voltage (V_{CCO})	–0.5 V to 4.5 V	–0.5 V to 4.5 V
Input or I/O Tristate Voltage Applied[4, 5]	–0.5 V to 5.5 V	–0.5 V to 5.5 V
Storage Temperature	–65 °C to 150 °C	–65 °C to 150 °C
Junction Temperature (T_j) with Power Applied	–55 °C to 150 °C	–55 °C to 150 °C

Notes:

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Semiconductor Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot of –2 V and overshoot of (VIH (MAX) + 2 V), up to a total pin voltage of 6.0 V, is permitted for a duration of < 20 ns.
5. Maximum of 64 I/Os per device with VIN > 3.6 V is allowed.

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17. Recommended Operating Conditions

Table 17.1. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	LA-ispMACH 4000V Supply Voltage	3.0	3.6	V
	LA-ispMACH 4000Z Supply Voltage	1.7	1.9	V
	LA-ispMACH 4000Z, Extended Functional Voltage	1.6*	1.9	V
t_A	Ambient Temperature (Automotive)	–40	125	°C

***Note**: Devices operating at 1.6 V can expect performance degradation up to 35%.

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18. Erase Reprogram Specifications

Table 18.1. Erase Reprogram Specifications

Parameter	Min	Max	Unit
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

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19. Hot Socketing Characteristics[1, 2, 3]

Table 19.1. Hot Socketing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DK}	Input or I/O Leakage Current	0 ≤ VIN ≤ 3.0 V, Tj = 105 °C	—	±30	±150	µA
		0 ≤ VIN ≤ 3.0 V, Tj = 130 °C	—	±30	±200	µA

Notes:

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6 V.
2. 0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

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20. I/O Recommended Operating Conditions

Table 20.1. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)[1]	
	Min	Max
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3[2]	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

Notes:

1. Typical values for V_{CCO} are the average of the min. and max. values.
2. LA-ispMACH 4000Z only.

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21. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 21.1. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4]	Input Leakage Current (LA-ispMACH 4000Z)	$0 \le V_{IN} \le V_{CCO}$	—	0.5	1	µA
I_{IH}[1, 2]	Input High Leakage Current (LA-ispMACH 4000V)	3.6 V < V_{IN} ≤ 5.5 V, Tj = 105 °C 3.0 V ≤ V_{CCO} ≤ 3.6 V	—	—	20	µA
		3.6 V < V_{IN} ≤ 5.5 V, Tj = 130 °C 3.0 V ≤ V_{CCO} ≤ 3.6 V	—	—	50	µA
	Input High Leakage Current (LA-ispMACH 4000Z)	$V_{CCO} < V_{IN} \le 5.5$ V	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000V)	$0 \le V_{IN} \le 0.7\ V_{CCO}$	–30	—	–200	µA
	I/O Weak Pull-up Resistor Current (LA-ispMACH 4000Z)	$0 \le V_{IN} \le 0.7\ V_{CCO}$	–30		–150	
I_{PD}	I/O Weak Pull-down Resistor	V_{IL} (MAX) ≤ V_{IN} ≤ V_{IH} (MIN)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	–30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	–150	µA
V_{BHT}	Bus Hold Trip Points	—	VCCO * 0.35	—	VCCO * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3 V, 2.5 V, 1.8 V	—	8	—	pf
		V_{CC} = 1.8 V, V_{IO} = 0 to V_{IH}	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3 V, 2. 5 V, 1.8 V	—	6	—	pf
		V_{CC} = 1.8 V, V_{IO} = 0 to V_{IH}	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3 V, 2.5 V, 1.8 V	—	6	—	pf
		V_{CC} = 1.8 V, V_{IO} = 0 to V_{IH}	—		—	

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 2. 5 V tolerant inputs and I/O should only be placed in banks where 3.0 V ≤ V_{CCO} ≤ 3.6 V.
3. T_A = 25 °C, f = 1.0 MHz.
4. I_{IH} excursions of up to 1.5 µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.

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22. Supply Current, LA-ispMACH 4000V

Over recommended operating conditions.

Table 22.1. Supply Current, LA-ispMACH 4000V

Symbol	Parameter	Condition	Min.	Typical		Unit
LA-ispMACH 4032V						
ICC	Operating Power Supply Current	V_{CC} = 3.3 V	—	11.8	—	mA
	Standby Power Supply Current	V_{CC} = 3.3 V	—	11.3	—	mA
LA-ispMACH 4064V						
ICC	Operating Power Supply Current	V_{CC} = 3.3 V	—	12	—	mA
	Standby Power Supply Current	V_{CC} = 3.3 V	—	11.5	—	mA
LA-ispMACH 4128V						
ICC	Operating Power Supply Current	V_{CC} = 3.3 V	—	12	—	mA
	Standby Power Supply Current	V_{CC} = 3.3 V	—	11.5	—	mA

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23. Supply Current, LA-ispMACH 4000Z

Over recommended operating conditions.

Table 23.1. Supply Current, LA-ispMACH 4000Z

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
LA-ispMACH 4032Z						
$ICC^{1, 2, 3, 5}$	Operating Power Supply Current	V_{CC} = 1.8 V, T_A = 25 °C	—	50	—	µA
		V_{CC} = 1.9 V, T_A = 70 °C	—	58	—	µA
		V_{CC} = 1.9 V, T_A = 85 °C	—	60	—	µA
		V_{CC} = 1.9 V, T_A = 125 °C	—	70	—	µA
$ICC^{4, 5}$	Standby Power Supply Current	V_{CC} = 1.8 V, T_A = 25 °C	—	10	—	µA
		V_{CC} = 1.9 V, T_A = 70 °C	—	13	20	µA
		V_{CC} = 1.9 V, T_A = 85 °C	—	15	25	µA
		V_{CC} = 1.9 V, T_A = 125 °C	—	22		µA
LA-ispMACH 4064Z						
$ICC^{1, 2, 3, 5}$	Operating Power Supply Current	V_{CC} = 1.8 V, T_A = 25 °C	—	80	—	µA
		V_{CC} = 1.9 V, T_A = 70 °C	—	89	—	µA
		V_{CC} = 1.9 V, T_A = 85 °C	—	92	—	µA
		V_{CC} = 1.9 V, T_A = 125 °C	—	109	—	µA
$ICC^{4, 5}$	Standby Power Supply Current	V_{CC} = 1.8 V, T_A = 25 °C	—	11	—	µA
		V_{CC} = 1.9 V, T_A = 70 °C	—	15	25	µA
		V_{CC} = 1.9 V, T_A = 85 °C	—	18	35	µA
		V_{CC} = 1. 9V, T_A = 125 °C	—	37		µA
LA-ispMACH 4128Z						
$ICC^{1, 2, 3, 5}$	Operating Power Supply Current	V_{CC} = 1.8 V, T_A = 25 °C	—	168	—	µA
		V_{CC} = 1.9 V, T_A = 70 °C	—	190	—	µA
		V_{CC} = 1.9 V, T_A = 85 °C	—	195	—	µA
		V_{CC} = 1.9 V, T_A = 125 °C	—	212	—	µA
$ICC^{4, 5}$	Standby Power Supply Current	V_{CC} = 1.8 V, T_A = 25 °C	—	12	—	µA
		V_{CC} = 1.9 V, T_A = 70 °C	—	16	35	µA
		V_{CC} = 1.9 V, T_A = 85 °C	—	19	50	µA
		V_{CC} = 1.9 V, T_A = 125 °C	—	42	—	µA

Notes:

1. T_A = 25 °C, frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. ICC varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6 V, V_{IN} = 0 V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby ICC.
5. Includes V_{CCO} current without output loading.

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24. I/O DC Electrical Characteristics

Over recommended operating conditions.

Table 24.1. I/O DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}* (mA)	I_{OH}* (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	–0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	–4.0
					0.20	V_{CCO} - 0.20	0.1	–0.1
LVCMOS 3.3	–0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	–4.0
					0.20	V_{CCO} - 0.20	0.1	–0.1
LVCMOS 2.5	–0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	–4.0
					0.20	V_{CCO} - 0.20	0.1	–0.1
LVCMOS 1.8 (4000V)	–0.3	0.63	1.17	3.6	0.40	V_{CCO} - 0.45	2.0	–2.0
					0.20	V_{CCO} - 0.20	0.1	–0.1
LVCMOS 1.8 (4000Z)	–0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	–2.0
					0.20	V_{CCO} - 0.20	0.1	–0.1
PCI 3.3 (4000V)	–0.3	1.08	1.5	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	–0.5
PCI 3.3 (4000Z)	–0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	–0.5

***Note**:

The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8 mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

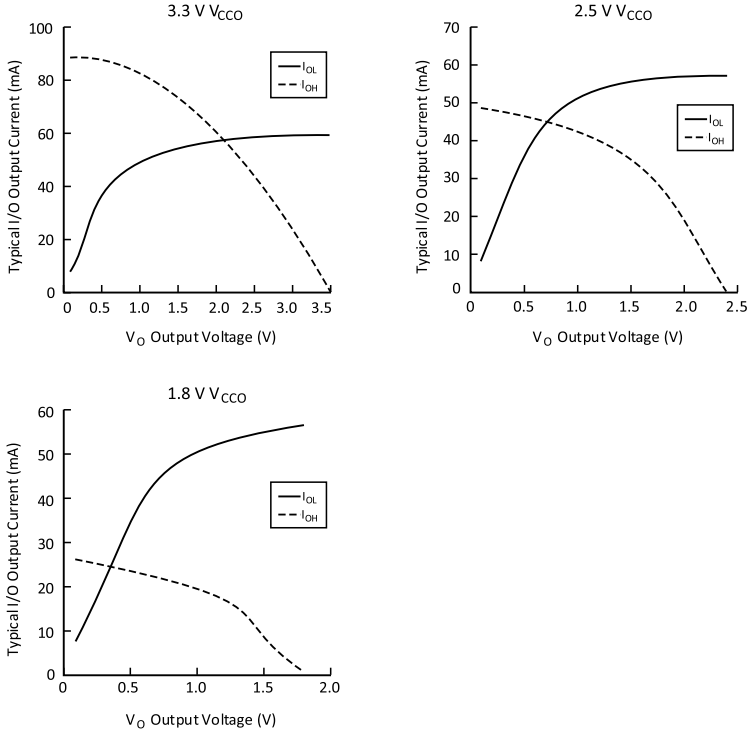


Figure 24.1. I/O DC Electrical Characteristics

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25. LA-ispMACH 4000V/Z External Switching Characteristics

Over recommended operating conditions.

Table 25.1. LA-ispMACH 4000V/Z External Switching Characteristics

Parameter	Description[1, 2, 3]	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	5-PT bypass combinatorial propagation delay	—	7.5	—	7.5	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	8.0	—	8.0	ns
t_S	GLB register setup time before clock	4.5	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	4.7	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.7	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.7	—	2.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.5	—	4.5	ns
t_R	External reset pin to output delay	—	9.0	—	9.0	ns
t_{RW}	External reset pulse duration	4.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term	—	9.0	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	10.3	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	7.0	—	7.0	ns
t_{CW}	Global clock width, high or low	2.8	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	2.8	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	2.8	—	2.8	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	168	—	168	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/(t_S + t_{CO})]$	—	111	—	111	MHz

Timing v.3.2

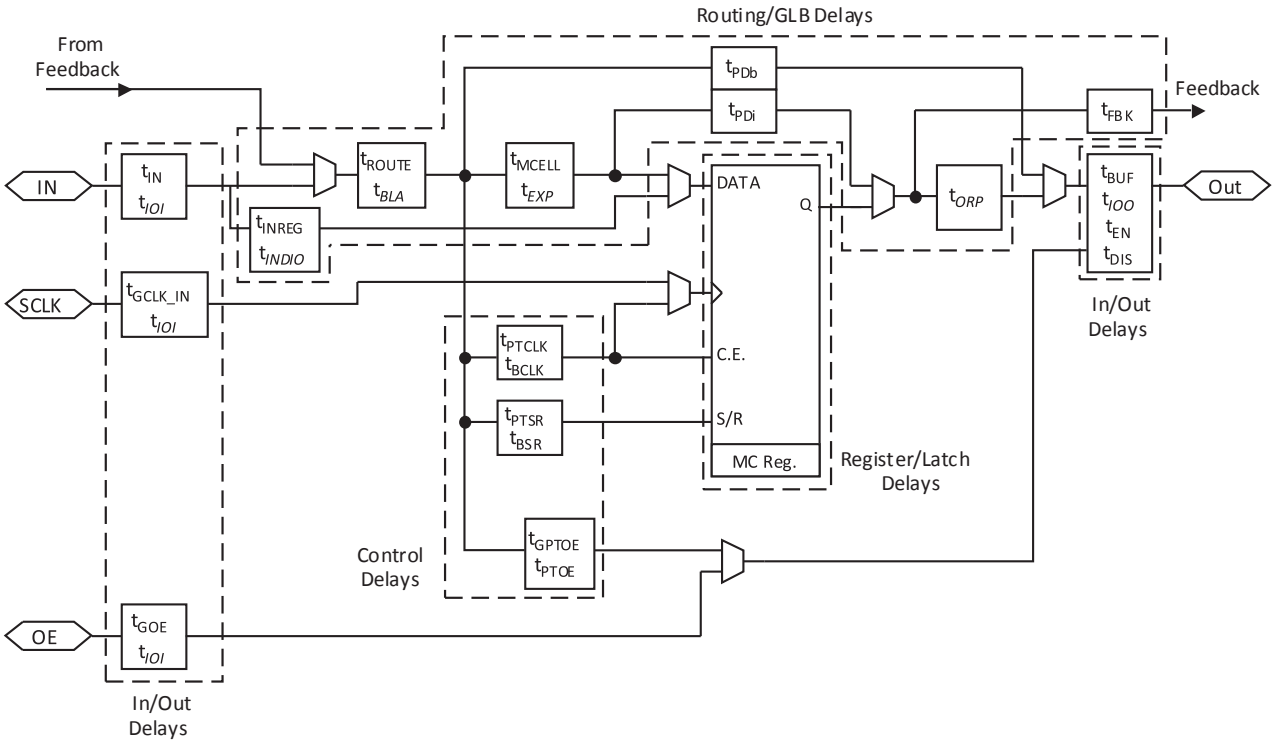
Notes:

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback

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26. Timing Model

The task of determining the timing through the LA-ispMACH 4000V/Z automotive family, like any CPLD, is relatively simple. The timing model provided in Figure 26.1 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines.



Note: Italicized items are optional delay adders.

Figure 26.1. LA-ispMACH 4000V/Z Automotive Timing Model

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27. LA-ispMACH 4000V/Z Internal Timing Parameters

Over recommended operating conditions.

Table 27.1. LA-ispMACH 4000V/Z Internal Timing Parameters

Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
In/Out Delays						
t_{IN}	Input Buffer Delay	—	1.50	—	1.80	ns
t_{GOE}	Global OE Pin Delay	—	6.04	—	4.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	2.28	—	2.15	ns
t_{BUF}	Delay through Output Buffer	—	1.50	—	1.30	ns
t_{EN}	Output Enable Time	—	0.96	—	2.70	ns
t_{DIS}	Output Disable Time	—	0.96	—	2.70	ns
Routing/GLB Delays						
t_{ROUTE}	Delay through GRP	—	2.26	—	2.50	ns
t_{MCELL}	Macrocell Delay	—	1.45	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.96	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.05	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	2.24	—	1.90	ns
t_{PDi}	Macrocell Propagation Delay	—	1.24	—	1.00	ns
Register/Latch Delays						
t_S	D-Register Setup Time (Global Clock)	1.57	—	1.35	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.32	—	2.45	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.77	—	1.55	—	ns
t_{ST_PT}	T-Register Setup Time (Product Term Clock)	1.32	—	2.75	—	ns
t_H	D-Register Hold Time	2.93	—	3.15	—	ns
t_{HT}	T-Register Hold Time	2.93	—	3.15	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.57	—	0.75	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.18	—	1.95	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.18	—	1.18	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.67	—	1.05	ns
t_{CES}	Clock Enable Setup Time	2.25	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	1.88	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	1.57	—	1.65	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.32	—	2.15	—	ns
t_{HL}	Latch Hold Time	1.17	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.33	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	ns

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Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
		Min.	Max.	Min.	Max.	
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	0.28	—	—	0.28	ns
t_{SRR}	Asynchronous Reset or Set Recovery Time	1.67	—	—	1.67	ns
Control Delays						
t_{BCLK}	GLB PT Clock Delay	—	1.12	—	1.25	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	0.87	—	1.25	ns
t_{BSR}	GLB PT Set/Reset Delay	—	1.83	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	3.41	—	2.72	ns
t_{GPTOE}	Global PT OE Delay	—	5.58	—	3.50	ns
t_{PTOE}	Macrocell PT OE Delay	—	4.28	—	2.00	ns

Timing v.3.2

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the Timing Model in this data sheet for further details.

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28. LA-ispMACH 4000V/Z Timing Adders

Table 28.1. LA-ispMACH 4000V/Z Timing Adders*

Parameter	Base Parameter	Description	LA-ispMACH 4000V -75		LA-ispMACH 4000Z -75		Units
			Min.	Max.	Min.	Max.	
Open Delay Adders							
t_{INDIO}	t_{INREG}	Input register delay	—	1.00	—	1.30	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.50	ns
t_{ORP}	—	Output routing pool delay	—	0.05	—	0.40	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.05	ns
t_{IOI} Input Adjusters							
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	ns
T_{IOO} Output Adjusters							
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3 V buffer	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5 V buffer	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8 V buffer	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00		1.00	ns

***Note:**
Open drain timing is the same as corresponding LVCMOS timing.
Refer to TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines for information regarding use of these adders.

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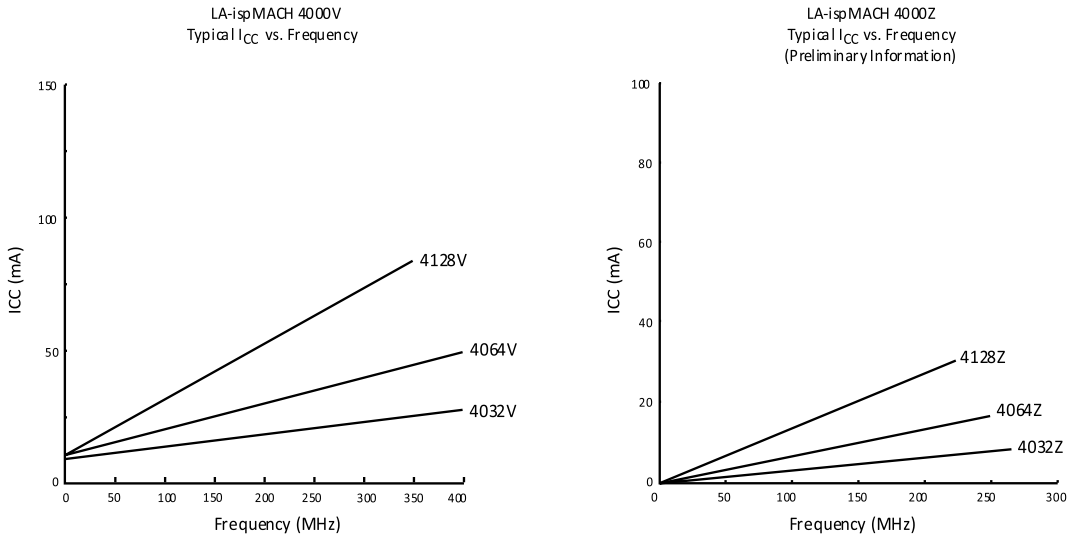
29. Boundary Scan Waveforms and Timing Specifications

Table 29.1. Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

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30. Power Consumption



Note: The devices are configured with the maximum number of 16-bit counters, typical current at 3.3 V, 2.5 V, 25 °C.

Note: The devices are configured with the maximum number of 16-bit counters, typical current at 1.8 V, 25 °C.

Figure 30.1. Power Consumption

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31. Power Estimation Coefficients*

Table 31.1. Power Estimation Coefficients

Device	A	B
LA-ispMACH 4032V	11.3	0.010
LA-ispMACH 4064V	11.5	0.010
LA-ispMACH 4128V	11.5	0.011
LA-ispMACH 4032Z	0.010	0.010
LA-ispMACH 4064Z	0.011	0.010
LA-ispMACH 4128Z	0.012	0.010

***Note:** For further information about the use of these coefficients, refer to TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices.

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32. Switching Test Conditions

Figure 32.1 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 32.1.

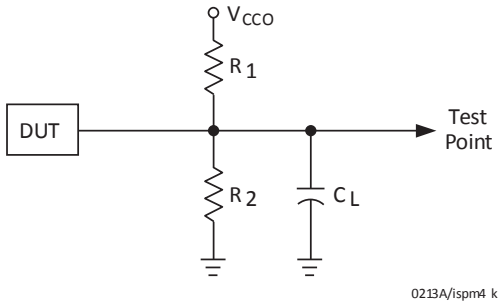


Figure 32.1. Output Test Load, LVTTL and LVCMOS Standards

Table 32.1. Test Fixture Required Components

Test Condition	R_1	R_2	C_L^*	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106 Ω	106 Ω	35 pF	LVCMOS 3.3 = 1.5 V	LVCMOS 3.3 = 3.0 V
				LVCMOS 2.5 = VCCO/2	LVCMOS 2.5 = 2.3 V
				LVCMOS 1.8 = VCCO/2	LVCMOS 1.8 = 1.65 V
LVCMOS I/O (Z -> H)	∞	106 Ω	35 pF	1.5 V	3.0 V
LVCMOS I/O (Z -> L)	106 Ω	∞	35 pF	1.5 V	3.0 V
LVCMOS I/O (H -> Z)	∞	106 Ω	5 pF	V_{OH} - 0.3	3.0 V
LVCMOS I/O (L -> Z)	106 Ω	∞	5 pF	V_{OL} + 0.3	3.0 V

***Note**: C_L includes test fixtures and probe capacitance.

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33. Signal Descriptions

Table 33.1. Signal Descriptions

Parameter	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for the logic core and JTAG port	
CLK0/I, CLK1/I, CLK2/I,	These pins are configured to be either CLK input or as an input	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank	
yzz	Input/Output1 – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15	
	LA-ispMACH 4032V/Z	y: A-B
	LA-ispMACH 4064V/Z	y: A-D
	LA-ispMACH 4128V/Z	y: A-H

***Note**: In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

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34. LA-ispMACH 4000V ORP Reference Table

Table 34.1. LA-ispMACH 4000V ORP Reference Table

Parameter	4032V		4064V			4128V		
Number of I/Os	30[1]	32	30[2]	32	64	64	92[3]	96
Number of GLBs	2	2	4	4	4	8	8	8
Number of I/Os /GLB	16	16	8	8	16	8	12	12
Reference ORP Table	16 I/Os / GLB		8 I/Os / GLB		16 I/Os / GLB	8 I/Os / GLB	12 I/Os /GLB	

Notes:

1. 32-macrocell device, 44 TQFP: 2 GLBs have 15 out of 16 I/Os bonded out.
2. 64-macrocells device, 44 TQFP: 2 GLBs have 7 out of 8 I/Os bonded out.
3. 128-macrocell device, 128 TQFP: 4 GLBs have 11 out of 12 I/Os.

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35. LA-ispMACH 4000Z ORP Reference Table

Table 35.1. LA-ispMACH 4000V ORP Reference Table

Parameter	4032Z	4064Z		4128Z
Number of I/Os	32	32	64	64
Number of GLBs	2	4	4	8
Number of I/Os /GLB	16	8	16	8
Reference ORP Table	16 I/Os / GLB	8 I/Os / GLB	16 I/Os / GLB	8 I/Os / GLB

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36. LA-ispMACH 4000V/Z Power Supply and NC Connections[1]

Table 36.1. LA-ispMACH 4000V ORP Reference Table

Signal	44 TQFP[2]	48 TQFP[2]	100 TQFP[2]	128 TQFP[2]	144 TQFP[2]
VCC	11, 33	12, 36	25, 40, 75, 90	32, 51, 96, 115	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	6	6	13, 33, 95	3, 17, 30, 41, 122	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	28	30	45, 63, 83	58, 67, 81, 94, 105	64, 75, 91, 106, 119
GND	12, 34	13, 37	1, 26, 51, 76	1, 33, 65, 97	1, 37, 73, 109
GND (Bank 0)	5	5	7, 18, 32, 96	10, 24, 40, 113, 123	10, 18[6], 27, 46, 127, 137
GND (Bank 1)	27	29	46, 57, 68, 82	49, 59, 74, 88, 104	55, 65, 82, 90[6], 99, 118
NC	None	None	None	None	17, 20, 38, 45, 72, 89, 92, 110, 117, 144

Notes:

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.

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37. LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Table 37.1. LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	—	TDI	—	TDI	—
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	—	GND (Bank 0)	—
6	0	VCCO (Bank 0)	—	VCCO (Bank 0)	—
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	—	TCK	—	TCK	—
11	—	VCC	—	VCC	—
12	—	GND	—	GND	—
13	0	A12	A^12	B8	B^4
14	0	A13	A^13	B10	B^5
15	0	A14	A^14	B12	B^6
16	0	A15	A^15	B14	B^7
17	1	CLK2/I	—	CLK2/I	—
18	1	B0	B^0	C0	C^0
19	1	B1	B^1	C2	C^1
20	1	B2	B^2	C4	C^2
21	1	B3	B^3	C6	C^3
22	1	B4	B^4	C8	C^4
23	—	TMS	—	TMS	—
24	1	B5	B^5	C10	C^5
25	1	B6	B^6	C12	C^6
26	1	B7	B^7	C14	C^7
27	1	GND (Bank 1)	—	GND (Bank 1)	—
28	1	VCCO (Bank 1)	—	VCCO (Bank 1)	—
29	1	B8	B^8	D0	D^0
30	1	B9	B^9	D2	D^1
31	1	B10	B^10	D4	D^2
32	—	TDO	—	TDO	—
33	—	VCC	—	VCC	—
34	—	GND	—	GND	—
35	1	B12	B^12	D8	D^4
36	1	B13	B^13	D10	D^5
37	1	B14	B^14	D12	D^6
38	1	B15/GOE1	B^15	D14/GOE1	D^7
39	0	CLK0/I	—	CLK0/I	—
40	0	A0/GOE0	A^0	A0/GOE0	A^0
41	0	A1	A^1	A2	A^1

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Table 37.1. LA-ispMACH 4032V and 4064V Logic Signal Connections: 44-Pin TQFP *(Continued)*

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	0	A2	A^2	A4	A^2
43	0	A3	A^3	A6	A^3
44	0	A4	A^4	A8	A^4

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38. LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Table 38.1. LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	—	TDI	—	TDI	—
2	0	A5	A^5	A10	A^5
3	0	A6	A^6	A12	A^6
4	0	A7	A^7	A14	A^7
5	0	GND (Bank 0)	—	GND (Bank 0)	—
6	0	VCCO (Bank 0)	—	VCCO (Bank 0)	—
7	0	A8	A^8	B0	B^0
8	0	A9	A^9	B2	B^1
9	0	A10	A^10	B4	B^2
10	0	A11	A^11	B6	B^3
11	—	TCK	—	TCK	—
12	—	VCC	—	VCC	—
13	—	GND	—	GND	—
14	0	A12	A^12	B8	B^4
15	0	A13	A^13	B10	B^5
16	0	A14	A^14	B12	B^6
17	0	A15	A^15	B14	B^7
18	0	CLK1/I	—	CLK1/I	—
19	1	CLK2/I	—	CLK2/I	—
20	1	B0	B^0	C0	C^0
21	1	B1	B^1	C2	C^1
22	1	B2	B^2	C4	C^2
23	1	B3	B^3	C6	C^3
24	1	B4	B^4	C8	C^4
25	—	TMS	—	TMS	—
26	1	B5	B^5	C10	C^5
27	1	B6	B^6	C12	C^6
28	1	B7	B^7	C14	C^7
29	1	GND (Bank 1)	—	GND (Bank 1)	—
30	1	VCCO (Bank 1)	—	VCCO (Bank 1)	—
31	1	B8	B^8	D0	D^0
32	1	B9	B^9	D2	D^1
33	1	B10	B^10	D4	D^2
34	1	B11	B^11	D6	D^3
35	—	TDO	—	TDO	—
36	—	VCC	—	VCC	—
37	—	GND	—	GND	—
38	1	B12	B^12	D8	D^4
39	1	B13	B^13	D10	D^5
40	1	B14	B^14	D12	D^6
41	1	B15/GOE1	B^15	D14/GOE1	D^7

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Table 38.1. LA-ispMACH 4032V/Z and 4064V/Z Logic Signal Connections: 48-Pin TQFP *(Continued)*

Pin Number	Bank Number	LA-ispMACH 4032V		LA-ispMACH 4064V	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	CLK3/I	—	CLK3/I	—
43	0	CLK0/I	—	CLK0/I	—
44	0	A0/GOE0	A^0	A0/GOE0	A^0
45	0	A1	A^1	A2	A^1
46	0	A2	A^2	A4	A^2
47	0	A3	A^3	A6	A^3
48	0	A4	A^4	A8	A^4

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39. LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Table 39.1. LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
1	—	GND	—	GND	—
2	—	TDI	—	TDI	—
3	0	A8	A^8	B0	B^0
4	0	A9	A^9	B2	B^1
5	0	A10	A^10	B4	B^2
6	0	A11	A^11	B6	B^3
7	0	GND (Bank 0)	—	GND (Bank 0)	—
8	0	A12	A^12	B8	B^4
9	0	A13	A^13	B10	B^5
10	0	A14	A^14	B12	B^6
11	0	A15	A^15	B13	B^7
12*	0	I	—	I	—
13	0	VCCO (Bank 0)	—	VCCO (Bank 0)	—
14	0	B15	B^15	C14	C^7
15	0	B14	B^14	C12	C^6
16	0	B13	B^13	C10	C^5
17	0	B12	B^12	C8	C^4
18	0	GND (Bank 0)	—	GND (Bank 0)	—
19	0	B11	B^11	C6	C^3
20	0	B10	B^10	C5	C^2
21	0	B9	B^9	C4	C^1
22	0	B8	B^8	C2	C^0
23*	0	I	—	I	—
24	—	TCK	—	TCK	—
25	—	VCC	—	VCC	—
26	—	GND	—	GND	—
27*	0	I	—	I	—
28	0	B7	B^7	D13	D^7
29	0	B6	B^6	D12	D^6
30	0	B5	B^5	D10	D^5
31	0	B4	B^4	D8	D^4
32	0	GND (Bank 0)	—	GND (Bank 0)	—
33	0	VCCO (Bank 0)	—	VCCO (Bank 0)	—
34	0	B3	B^3	D6	D^3
35	0	B2	B^2	D4	D^2
36	0	B1	B^1	D2	D^1
37	0	B0	B^0	D0	D^0
38	0	CLK1/I	—	CLK1/I	—
39	1	CLK2/I	—	CLK2/I	—
40	—	VCC	—	VCC	—
41	1	C0	C^0	E0	E^0

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Table 39.1. LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP *(Continued)*

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
42	1	C1	C^1	E2	E^1
43	1	C2	C^2	E4	E^2
44	1	C3	C^3	E6	E^3
45	1	VCCO (Bank 1)	—	VCCO (Bank 1)	—
46	1	GND (Bank 1)	—	GND (Bank 1)	—
47	1	C4	C^4	E8	E^4
48	1	C5	C^5	E10	E^5
49	1	C6	C^6	E12	E^6
50	1	C7	C^7	E14	E^7
51	—	GND	—	GND	—
52	—	TMS	—	TMS	—
53	1	C8	C^8	F0	F^0
54	1	C9	C^9	F2	F^1
55	1	C10	C^10	F4	F^2
56	1	C11	C^11	F6	F^3
57	1	GND (Bank 1)	—	GND (Bank 1)	—
58	1	C12	C^12	F8	F^4
59	1	C13	C^13	F10	F^5
60	1	C14	C^14	F12	F^6
61	1	C15	C^15	F13	F^7
62*	1	I	—	I	—
63	1	VCCO (Bank 1)	—	VCCO (Bank 1)	—
64	1	D15	D^15	G14	G^7
65	1	D14	D^14	G12	G^6
66	1	D13	D^13	G10	G^5
67	1	D12	D^12	G8	G^4
68	1	GND (Bank 1)	—	GND (Bank 1)	—
69	1	D11	D^11	G6	G^3
70	1	D10	D^10	G5	G^2
71	1	D9	D^9	G4	G^1
72	1	D8	D^8	G2	G^0
73*	1	I	—	I	—
74	—	TDO	—	TDO	—
75	—	VCC	—	VCC	—
76	—	GND	—	GND	—
77*	1	I	—	I	—
78	1	D7	D^7	H13	H^7
79	1	D6	D^6	H12	H^6
80	1	D5	D^5	H10	H^5
81	1	D4	D^4	H8	H^4
82	1	GND (Bank 1)	—	GND (Bank 1)	—
83	1	VCCO (Bank 1)	—	VCCO (Bank 1)	—
84	1	D3	D^3	H6	H^3
85	1	D2	D^2	H4	H^2
86	1	D1	D^1	H2	H^1

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Table 39.1. LA-ispMACH 4064V/Z and 4128V/Z Logic Signal Connections: 100-Pin TQFP *(Continued)*

Pin Number	Bank Number	LA-ispMACH 4064V/Z		LA-ispMACH 4128V/Z	
		GLB/MC/Pad	ORP	GLB/MC/Pad	ORP
87	1	D0/GOE1	D^0	H0/GOE1	H^0
88	1	CLK3/I	—	CLK3/I	—
89	0	CLK0/I	—	CLK0/I	—
90	—	VCC	—	VCC	—
91	0	A0/GOE0	A^0	A0/GOE0	A^0
92	0	A1	A^1	A2	A^1
93	0	A2	A^2	A4	A^2
94	0	A3	A^3	A6	A^3
95	0	VCCO (Bank 0)	—	VCCO (Bank 0)	—
96	0	GND (Bank 0)	—	GND (Bank 0)	—
97	0	A4	A^4	A8	A^4
98	0	A5	A^5	A10	A^5
99	0	A6	A^6	A12	A^6
100	0	A7	A^7	A14	A^7

***Note:** This pin is input only.

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40. LA-ispMACH 4128V Signal Connections: 128-Pin TQFP

Table 40.1. LA-ispMACH 4128V Signal Connections: 100-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
1	0	GND	—
2	0	TDI	—
3	0	VCCO (Bank 0)	—
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	—
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	0	VCCO (Bank 0)	—
18	0	C14	C^11
19	0	C13	C^10
20	0	C12	C^9
21	0	C10	C^8
22	0	C9	C^7
23	0	C8	C^6
24	0	GND (Bank 0)	—
25	0	C6	C^5
26	0	C5	C^4
27	0	C4	C^3
28	0	C2	C^2
29	0	C0	C^0
30	0	VCCO (Bank 0)	—
31	0	TCK	—
32	0	VCC	—
33	0	GND	—
34	0	D14	D^11
35	0	D13	D^10
36	0	D12	D^9
37	0	D10	D^8
38	0	D9	D^7
39	0	D8	D^6
40	0	GND (Bank 0)	—
41	0	VCCO (Bank 0)	—
42	0	D6	D^5
43	0	D5	D^4

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Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
44	0	D4	D^3
45	0	D2	D^2
46	0	D1	D^1
47	0	D0	D^0
48	0	CLK1/I	—
49	1	GND (Bank 1)	—
50	1	CLK2/I	—
51	1	VCC	—
52	1	E0	E^0
53	1	E1	E^1
54	1	E2	E^2
55	1	E4	E^3
56	1	E5	E^4
57	1	E6	E^5
58	1	VCCO (Bank 1)	—
59	1	GND (Bank 1)	—
60	1	E8	E^6
61	1	E9	E^7
62	1	E10	E^8
63	1	E12	E^9
64	1	E14	E^11
65	1	GND	—
66	1	TMS	—
67	1	VCCO (Bank 1)	—
68	1	F0	F^0
69	1	F1	F^1
70	1	F2	F^2
71	1	F4	F^3
72	1	F5	F^4
73	1	F6	F^5
74	1	GND (Bank 1)	—
75	1	F8	F^6
76	1	F9	F^7
77	1	F10	F^8
78	1	F12	F^9
79	1	F13	F^10
80	1	F14	F^11
81	1	VCCO (Bank 1)	—
82	1	G14	G^11
83	1	G13	G^10
84	1	G12	G^9
85	1	G10	G^8
86	1	G9	G^7
87	1	G8	G^6
88	1	GND (Bank 1)	—
89	1	G6	G^5

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Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
90	1	G5	G^4
91	1	G4	G^3
92	1	G2	G^2
93	1	G0	G^0
94	1	VCCO (Bank 1)	—
95	1	TDO	—
96	1	VCC	—
97	1	GND	—
98	1	H14	H^11
99	1	H13	H^10
100	1	H12	H^9
101	1	H10	H^8
102	1	H9	H^7
103	1	H8	H^6
104	1	GND (Bank 1)	—
105	1	VCCO (Bank 1)	—
106	1	H6	H^5
107	1	H5	H^4
108	1	H4	H^3
109	1	H2	H^2
110	1	H1	H^1
111	1	H0/GOE1	H^0
112	1	CLK3/I	—
113	0	GND (Bank 0)	—
114	0	CLK0/I	—
115	0	VCC	—
116	0	A0/GOE0	A^0
117	0	A1	A^1
118	0	A2	A^2
119	0	A4	A^3
120	0	A5	A^4
121	0	A6	A^5
122	0	VCCO (Bank 0)	—
123	0	GND (Bank 0)	—
124	0	A8	A^6
125	0	A9	A^7
126	0	A10	A^8
127	0	A12	A^9
128	0	A14	A^11

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41. LA-ispMACH 4128V Signal Connections: 144-Pin TQFP

Table 41.1. LA-ispMACH 4128V Signal Connections: 144-Pin TQFP

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
1	—	GND	—
2	—	TDI	—
3	0	VCCO (Bank 0)	—
4	0	B0	B^0
5	0	B1	B^1
6	0	B2	B^2
7	0	B4	B^3
8	0	B5	B^4
9	0	B6	B^5
10	0	GND (Bank 0)	—
11	0	B8	B^6
12	0	B9	B^7
13	0	B10	B^8
14	0	B12	B^9
15	0	B13	B^10
16	0	B14	B^11
17	—	NC	—
18	0	GND (Bank 0)[1]	—
19	0	VCCO (Bank 0)	—
20	0	NC	—
21	0	C14	C^11
22	0	C13	C^10
23	0	C12	C^9
24	0	C10	C^8
25	0	C9	C^7
26	0	C8	C^6
27	0	GND (Bank 0)	—
28	0	C6	C^5
29	0	C5	C^4
30	0	C4	C^3
31	0	C2	C^2
32	0	C1	C^1
33	0	C0	C^0
34	0	VCCO (Bank 0)	—
35	—	TCK	—
36	—	VCC	—
37	—	GND	—
38	0	NC	—
39	0	D14	D^11
40	0	D13	D^10
41	0	D12	D^9
42	0	D10	D^8
43	0	D9	D^7

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Table 41.1. LA-ispMACH 4128V Signal Connections: 144-Pin TQFP *(Continued)*

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
44	0	D8	D^6
45	0	NC	—
46	0	GND (Bank 0)	—
47	0	VCCO (Bank 0)	—
48	0	D6	D^5
49	0	D5	D^4
50	0	D4	D^3
51	0	D2	D^2
52	0	D1	D^1
53	0	D0	D^0
54	0	CLK1/I	—
55	1	GND (Bank 1)	—
56	1	CLK2/I	—
57	—	VCC	—
58	1	E0	E^0
59	1	E1	E^1
60	1	E2	E^2
61	1	E4	E^3
62	1	E5	E^4
63	1	E6	E^5
64	1	VCCO (Bank 1)	—
65	1	GND (Bank 1)	—
66	1	E8	E^6
67	1	E9	E^7
68	1	E10	E^8
69	1	E12	E^9
70	1	E13	E^10
71	1	E14	E^11
72	1	NC	—
73	—	GND	—
74	—	TMS	—
75	1	VCCO (Bank 1)	—
76	1	F0	F^0
77	1	F1	F^1
78	1	F2	F^2
79	1	F4	F^3
80	1	F5	F^4
81	1	F6	F^5
82	1	GND (Bank 1)	—
83	1	F8	F^6
84	1	F9	F^7
85	1	F10	F^8
86	1	F12	F^9
87	1	F13	F^10
88	1	F14	F^11

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Table 41.1. LA-ispMACH 4128V Signal Connections: 144-Pin TQFP *(Continued)*

Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
89	1	NC	—
90	1	GND (Bank 1)1	—
91	1	VCCO (Bank 1)	—
92	1	NC	—
93	1	G14	G^11
94	1	G13	G^10
95	1	G12	G^9
96	1	G10	G^8
97	1	G9	G^7
98	1	G8	G^6
99	1	GND (Bank 1)	—
100	1	G6	G^5
101	1	G5	G^4
102	1	G4	G^3
103	1	G2	G^2
104	1	G1	G^1
105	1	G0	G^0
106	1	VCCO (Bank 1)	—
107	—	TDO	—
108	—	VCC	—
109	—	GND	—
110	1	NC	—
111	1	H14	H^11
112	1	H13	H^10
113	1	H12	H^9
114	1	H10	H^8
115	1	H9	H^7
116	1	H8	H^6
117	1	NC	—
118	1	GND (Bank 1)	—
119	1	VCCO (Bank 1)	—
120	1	H6	H^5
121	1	H5	H^4
122	1	H4	H^3
123	1	H2	H^2
124	1	H1	H^1
125	1	H0/GOE1	H^0
126	1	CLK3/I	—
127	0	GND (Bank 0)	—
128	0	CLK0/I	—
129	—	VCC	—
130	0	A0/GOE0	A^0
121	1	H5	H^4
122	1	H4	H^3
123	1	H2	H^2

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Table 41.1. LA-ispMACH 4128V Signal Connections: 144-Pin TQFP *(Continued)*

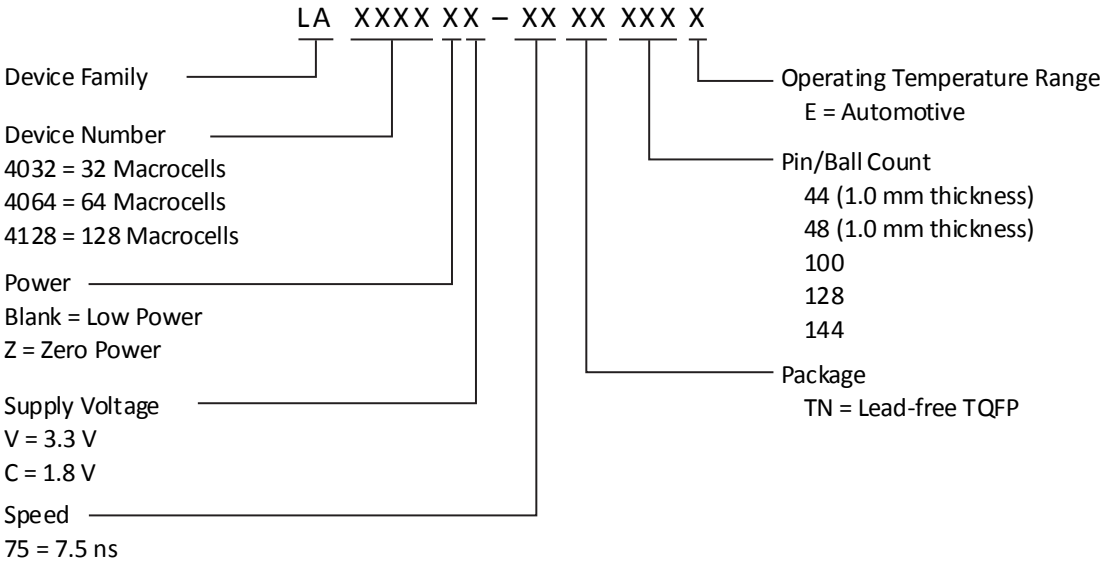
Pin Number	Bank Number	LA-ispMACH 4128V	
		GLB/MC/Pad	ORP
124	1	H1	H^1
125	1	H0/GOE1	H^0
126	1	CLK3/I	—
127	0	GND (Bank 0)	—
128	0	CLK0/I	—
129	—	VCC	—
130	0	A0/GOE0	A^0
131	0	A1	A^1
132	0	A2	A^2
133	0	A4	A^3
134	0	A5	A^4
135	0	A6	A^5
136	0	VCCO (Bank 0)	—
137	0	GND (Bank 0)	—
138	0	A8	A^6
139	0	A9	A^7
140	0	A10	A^8
141	0	A12	A^9
142	0	A13	A^10
143	0	A14	A^11
144	0	NC[2]	—

***Note:** For device migration considerations, these NC pins are GND pins for I/O banks in LA-ispMACH 4128V devices.

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42. Ordering Information

42.1. Part Number Description



42.2. Ordering Part Numbers

Table 42.1. Ordering Information

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LA4032V	LA4032V-75TN48E	32	3.3	7.5	Lead-free TQFP	48	32	E
	LA4032V-75TN44E	32	3.3	7.5	Lead-free TQFP	44	30	E
LA4064V	LA4064V-75TN100E	64	3.3	7.5	Lead-free TQFP	100	64	E
	LA4064V-75TN48E	64	3.3	7.5	Lead-free TQFP	48	32	E
	LA4064V-75TN44E	64	3.3	7.5	Lead-free TQFP	44	30	E
LA4128V	LA4128V-75TN144E	128	3.3	7.5	Lead-free TQFP	144	96	E
	LA4128V-75TN128E	128	3.3	7.5	Lead-free TQFP	128	92	E
	LA4128V-75TN100E	128	3.3	7.5	Lead-free TQFP	100	64	E
LA4032Z	LA4032ZC-75TN48E	32	1.8	7.5	Lead-free TQFP	48	32	E
LA4064Z	LA4064ZC-75TN100E	64	1.8	7.5	Lead-free TQFP	100	64	E
	LA4064ZC-75TN48E	64	1.8	7.5	Lead-free TQFP	48	32	E
LA4128Z	LA4128ZC-75TN100E	128	1.8	7.5	Lead-free TQFP	100	64	E

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Supplemental Information

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the LA-ispMACH 4000V/Z automotive family:

- TN1004, ispMACH 4000 Timing Model Design and Usage Guidelines
- TN1005, Power Estimation in ispMACH 4000V/B/C/Z Devices

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Revision History

Date	Version	Change Summary
September 2017	2.6	Updated document template. Changed document ID from DS1017 to FPGA-DS-02021.
May 2009	02.5	Correction to tCW, tGW, tWIR and fMAX parameters in External Switching Characteristics table.
	02.4	Correction to tCW, tGW, and tWIR parameters in External Switching Characteristics table.
July 2008	02.3	Lowered the maximum supply current at 85 °C to match the commercial product values. Added automotive disclaimer.
September 2007	02.2	DC Electrical Characteristics table, removed duplicate specifications.
March 2007	02.1	Updated ispMACH 4000 Introduction section. Updated Signal Descriptions table.
October 2006	02.0	Added LA-ispMACH 4000Z support information throughout.
April 2006	01.0	Initial release.

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7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com