

LD6805 series

Low-dropout regulators, high PSRR, 150 mA

Rev. 2 — 25 June 2012 Product data sheet

1. Product profile

1.1 General description

The LD6805 series is a small-size Low DropOut regulator (LDO) family with ultra high Power Supply Rejection Ratio (PSRR) of 75 dB. The voltage drop is 250 mV at 150 mA current rating.

Operating voltages can range from 2.3 V to 5.5 V. The devices are available with fixed output voltages between 1.2 V to 3.6 V.

The LD6805K/xxH devices show a high-ohmic state at the output pin when set to disabled mode. The LD6805K/xxP devices contain a pull-down switching transistor to provide a low-ohmic output state (auto discharge function) in disabled mode.

The LD6805 series devices are available in a 1 × 1 mm DFN plastic package making them ideal for use in portable applications requiring component miniaturization. All devices are manufactured in monolithic silicon technology.

1.2 Features and benefits

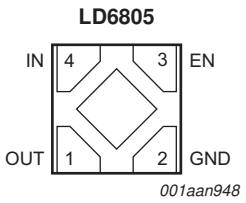
- 150 mA output current rating
- 75 dB PSRR at 1 kHz
- Input voltage range 2.3 V to 5.5 V
- Fixed output voltage between 1.2 V to 3.6 V
- Dropout voltage 250 mV at 150 mA output rating
- Low quiescent current in shutdown mode (typical 0.1 μA)
- 40 μV RMS output noise voltage (typical value) at 10 Hz to 100 kHz
- Turn-on time 150 μs
- LD6805K/xxH: high-ohmic (3-state) output state when disabled
- LD6805K/xxP: low-ohmic output state when disabled (auto discharge function)
- Integrated ESD protection up to 6 kV Human Body Model (HBM)
- DFN1010C-4 (SOT1194-1) plastic package with a size of 1 × 1 × 0.55 mm
- Pb-free, RoHS compliant and free of halogen and antimony (dark green compliant)

1.3 Applications

- Analog and digital interfaces requiring lower than standard supply voltages in mobile appliances such as smart phones, mobile phone handsets and cordless telephones. Other typical applications are digital still cameras, mobile internet devices, personal navigation devices and portable media players.

2. Pinning information

2.1 Pinning



Transparent top view

Fig 1. Pin configuration for DFN1010C-4 (SOT1194-1)

2.2 Pin description

Table 1. Pin description for DFN1010C-4 (SOT1194-1)

Symbol	Pin	Description
OUT	1	regulator output voltage
GND	2	supply ground
EN	3	device enable input; active HIGH
IN	4	regulator input voltage
i.c.	TAB	internal connected[1]

[1] The TAB is GND level (it is placed on the reverse side of the IC).
It is recommended to connect the TAB to GND. Leaving it unconnected is also allowed but it may result in lower thermal performance.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6805 series	DFN1010C-4	plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 × 1 × 0.55 mm	SOT1194-1

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3.1 Ordering options

Further information on output voltage is available on request; see Section 20 “Contact information”.

Table 3. Type number extension of high-ohmic output

Type number	Nominal output voltage	Type number	Nominal output voltage
LD6805K/12H	1.2 V	LD6805K/22H	2.2 V
LD6805K/13H	1.3 V	LD6805K/23H	2.3 V
LD6805K/14H	1.4 V	LD6805K/25H	2.5 V
LD6805K/15H	1.5 V	LD6805K/28H	2.8 V
LD6805K/16H	1.6 V	LD6805K/29H	2.9 V
LD6805K/18H	1.8 V	LD6805K/30H	3.0 V
LD6805K/185H	1.85 V	LD6805K/31H	3.1 V
LD6805K/20H	2.0 V	LD6805K/33H	3.3 V
LD6805K/21H	2.1 V	LD6805K/36H	3.6 V

Table 4. Type number extension of pull-down output

Type number	Nominal output voltage	Type number	Nominal output voltage
LD6805K/12P	1.2 V	LD6805K/23P	2.3 V
LD6805K/13P	1.3 V	LD6805K/25P	2.5 V
LD6805K/14P	1.4 V	LD6805K/28P	2.8 V
LD6805K/15P	1.5 V	LD6805K/29P	2.9 V
LD6805K/16P	1.6 V	LD6805K/30P	3.0 V
LD6805K/18P	1.8 V	LD6805K/31P	3.1 V
LD6805K/20P	2.0 V	LD6805K/33P	3.3 V
LD6805K/21P	2.1 V	LD6805K/36P	3.6 V
LD6805K/22P	2.2 V	-	-

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4. Block diagram

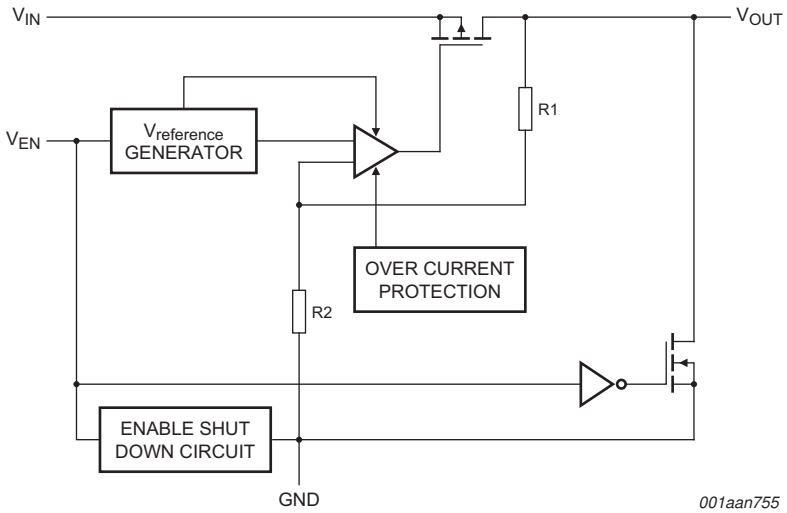


Fig 2. Block diagram of LD6805K/xxP (auto discharge function)

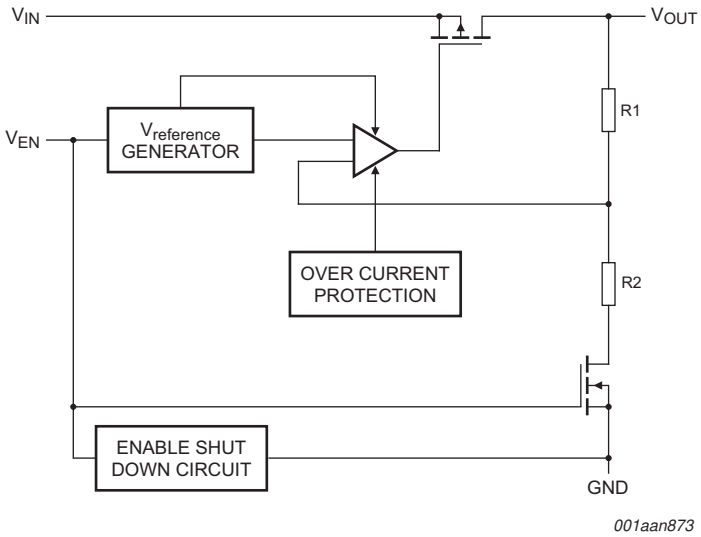


Fig 3. Block diagram of LD6805K/xxH

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5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	voltage on pin IN	4 ms transient		−0.5	+6.0	V
P_{tot}	total power dissipation		[1]	-	400	mW
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+125	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model level 6	[2]	-	±6	kV
		machine model class 3	[3]	-	±400	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

[2] According to IEC 61340-3-1.

[3] According to JESD22-A115C.

6. Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature		−40	-	+85	°C
T_j	junction temperature		-	-	+125	°C
Pin IN						
V_{IN}	voltage on pin IN		2.3	-	5.5	V
Pin EN						
V_{EN}	voltage on pin EN		0	-	V_{IN}	V
Pin OUT						
$C_{L(ext)}$	external load capacitance	[1]	0.7	1.0	-	µF

[1] See Section 10.1 “Output capacitor values”.

7. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	250	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multi-layer PCB applications, the second layer is used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it is connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.

[2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

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8. Characteristics

Table 8. Electrical characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output voltage							
V_{do}	dropout voltage	I_{OUT} = 150 mA; $V_{IN} < V_{O(nom)}$	[1]	-	250	-	mV
ΔV_O	output voltage variation	V_{OUT} < 1.8 V; I_{OUT} = 1 mA					
		T_{amb} = +25 °C		−3	±0.5	+3	%
		−30 °C ≤ T_{amb} ≤ +85 °C		−4	-	+4	%
		V_{OUT} ≥ 1.8 V; I_{OUT} = 1 mA					
		T_{amb} = +25 °C		−2	±0.5	+2	%
		−30 °C ≤ T_{amb} ≤ +85 °C		−3	-	+3	%
Line regulation error							
$\Delta V_O/(V_O x \Delta V_I)$	relative output voltage variation with input voltage	V_{IN} = ($V_{O(nom)}$ + 0.5 V) to 5.5 V	[1]	−0.1	-	+0.1	%/V
Load regulation error							
$\Delta V_O/(V_O x \Delta I_O)$	relative output voltage variation with output current	1 mA ≤ I_{OUT} ≤ 150 mA		-	0.0025	0.01	%/mA
Output current							
I_{OUT}	current on pin OUT			-	-	150	mA
I_{OM}	peak output current	V_{IN} = ($V_{O(nom)}$ + 0.5 V) to 5.5 V	[1]				
		$V_{O(nom)}$ > 1.8 V; V_{OUT} = 0.95 × $V_{O(nom)}$		200	-	-	mA
		$V_{O(nom)}$ < 1.8 V; V_{OUT} = 0.9 × $V_{O(nom)}$		200	-	-	mA
I_{sc}	short-circuit current	pin OUT		-	300	-	mA
Regulator quiescent current							
I_q	quiescent current	V_{EN} = 1.1 V; I_{OUT} = 0 mA		-	35	-	µA
		V_{EN} = 1.1 V; 1 mA ≤ I_{OUT} ≤ 150 mA		-	150	-	µA
		V_{EN} ≤ 0.4 V		-	0.1	1	µA
Ripple rejection and output noise							
PSRR	power supply rejection ratio	V_{IN} = $V_{O(nom)}$ + 1.0 V; I_{OUT} = 50 mA; f_{ripple} = 1 kHz	[1]	-	−75	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	f_{ripple} = 10 Hz to 100 kHz; $C_{L(ext)}$ = 1 µF		-	40	-	µV
Enable input and timing							
V_{IL}	LOW-level input voltage	pin EN		0	-	0.4	V
V_{IH}	HIGH-level input voltage	pin EN		1.1	-	5.5	V
$t_{startup(reg)}$	regulator start-up time	V_{IN} = 5.5 V; V_{OUT} = 0.95 × $V_{O(nom)}$; I_{OUT} = 150 mA; $C_{L(ext)}$ = 1 µF	[1]	-	150	-	µs

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Table 8. Electrical characteristics *...continued*

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LD6805K/xxP; auto discharge function						
$t_{sd(reg)}$	regulator shutdown time	V_{IN} = 5.5 V; V_{OUT} = 0.05 × $V_{O(nom)}$; $C_{L(ext)}$ = 1 µF	-	300	-	µs
R_{pd}	pull-down resistance		-	100	-	Ω

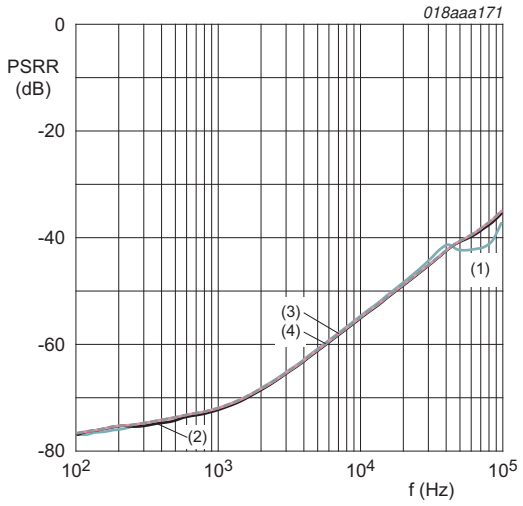
[1] $V_{O(nom)}$ = nominal output voltage (device specific).

9. Dynamic behavior

9.1 Power Supply Rejection Ratio (PSRR)

PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR[dB] = 20log\frac{V_{out(ripple)}}{V_{in(ripple)}}$$ for all frequencies



(1) I_{OUT} = 1 mA
(2) I_{OUT} = 50 mA
(3) I_{OUT} = 100 mA
(4) I_{OUT} = 200 mA

Fig 4. PSRR for LD6805K/18x

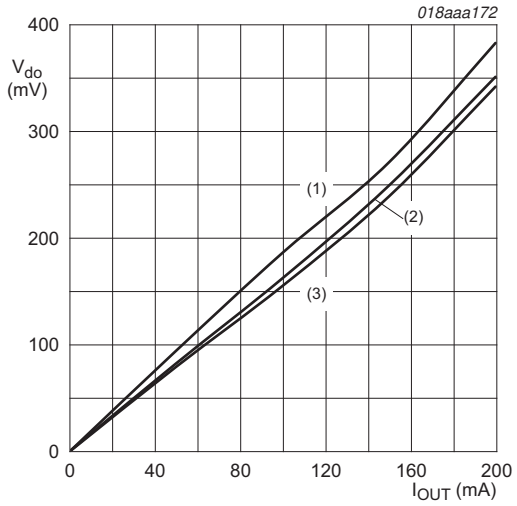
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9.2 Dropout

The dropout voltage is defined as the smallest input to output voltage difference at a specified load current when the regulator operates within its linear region. This means that the input voltage is below the nominal output voltage value and the pass transistor works as a plain resistor.

A small dropout voltage guarantees lower power consumption and efficiency maximization.



(1) T_{amb} = +85 °C
(2) T_{amb} = +25 °C
(3) T_{amb} = −40 °C

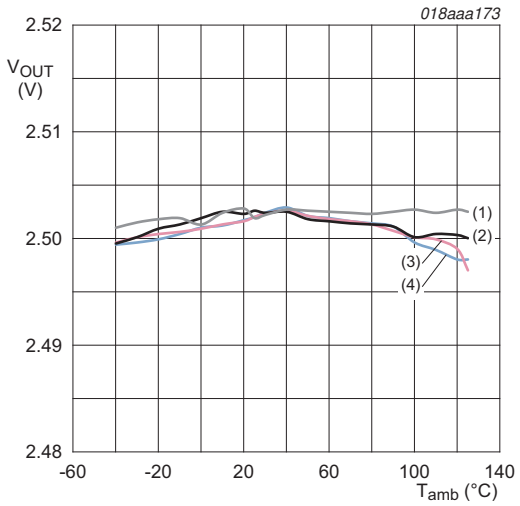
Fig 5. Dropout voltage as a function of output current for LD6805K/25x

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9.3 Accuracy

The LD6805 series guarantees high accuracy of the nominal output voltage.



(1) I_{OUT} = 1 mA
(2) I_{OUT} = 100 mA
(3) I_{OUT} = 150 mA
(4) I_{OUT} = 200 mA

Fig 6. Accuracy for LD6805K/25x

10. Application information

10.1 Output capacitor values

The LD6805 series requires external capacitors at the output to guarantee a stable regulator behavior. Also an input capacitor is recommended to keep the input voltage stable. It is not allowed to under-run the specified minimum Equivalent Series Resistance (ESR).

The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ($t_{sd(reg)}$) of the LD6805 series.

Table 9. External load capacitor

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{L(ext)}$	external load capacitance		[1]	-	1.0	-	µF
ESR	equivalent series resistance			5	-	500	mΩ

[1] The minimum value of capacitance for stability and correct operation is 0.7 µF. The specified capacitor tolerance is ±30 % or better over the temperature and operating conditions range. The recommended capacitor type is X7R to meet the full device temperature specification of −40 °C to +125 °C.

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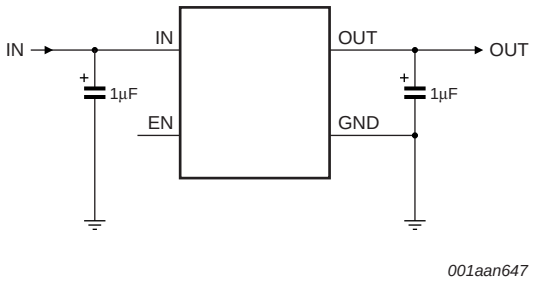


Fig 7. Application diagram

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX2-00001 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

12. Marking

Table 10. Marking of high-ohmic output

Type number	Voltage	Version code	Type number	Voltage	Version code
LD6805K/12H	1.2 V	AH	LD6805K/22H	2.2 V	KH
LD6805K/13H	1.3 V	BH	LD6805K/23H	2.3 V	LH
LD6805K/14H	1.4 V	CH	LD6805K/25H	2.5 V	NH
LD6805K/15H	1.5 V	DH	LD6805K/28H	2.8 V	QH
LD6805K/16H	1.6 V	EH	LD6805K/29H	2.9 V	RH
LD6805K/18H	1.8 V	GH	LD6805K/30H	3.0 V	SH
LD6805K/185H	1.85 V	5H	LD6805K/31H	3.1 V	TH
LD6805K/20H	2.0 V	IH	LD6805K/33H	3.3 V	VH
LD6805K/21H	2.1 V	JH	LD6805K/36H	3.6 V	YH

Table 11. Marking of pull-down output

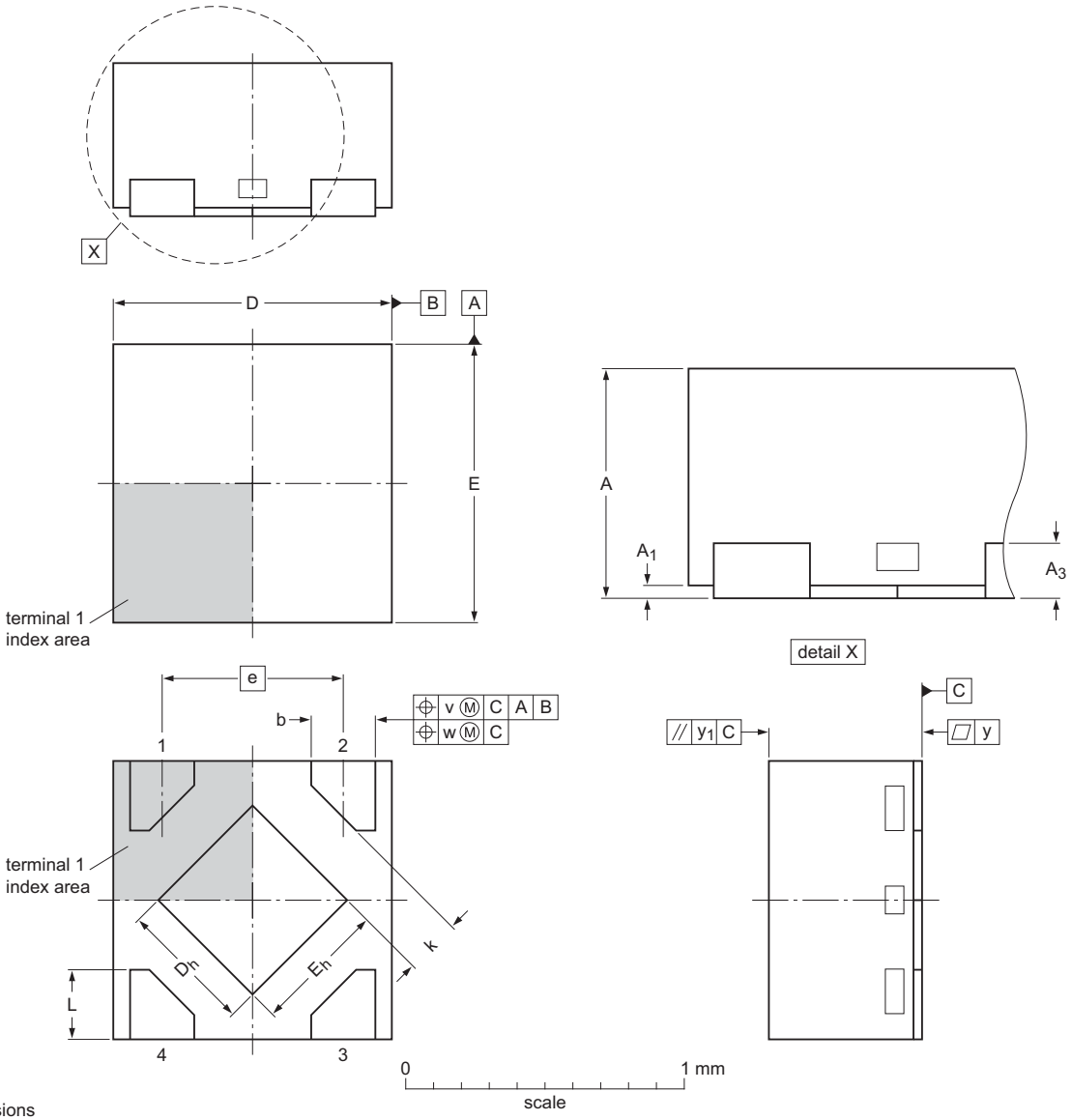
Type number	Voltage	Version code	Type number	Voltage	Version code
LD6805K/12P	1.2 V	AP	LD6805K/23P	2.3 V	LP
LD6805K/13P	1.3 V	BP	LD6805K/25P	2.5 V	NP
LD6805K/14P	1.4 V	CP	LD6805K/28P	2.8 V	QP
LD6805K/15P	1.5 V	DP	LD6805K/29P	2.9 V	RP
LD6805K/16P	1.6 V	EP	LD6805K/30P	3.0 V	SP
LD6805K/18P	1.8 V	GP	LD6805K/31P	3.1 V	TP
LD6805K/20P	2.0 V	IP	LD6805K/33P	3.3 V	VP
LD6805K/21P	2.1 V	JP	LD6805K/36P	3.6 V	YP
LD6805K/22P	2.2 V	KP	-	-	-

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13. Package outline

Plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 x 1 x 0.55 mm **SOT1194-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	D_h	E	E_h	e	k	L	v	w	y	y_1
mm	max	0.55	0.05	0.152	0.30	1.05	0.53	1.05	0.53			0.30				
	nom				0.25	1.00	0.48	1.00	0.48	0.65		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.05	0.20	0.95	0.43	0.95	0.43		0.2	0.20				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1194-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1194-1	- - -	- - -	- - -			~~11-05-30~~ 12-05-22

Fig 8. Package outline DFN1010C-4 (SOT1194-1)

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14. Soldering

Footprint information for reflow soldering of HXSON4 package **SOT1194-1**

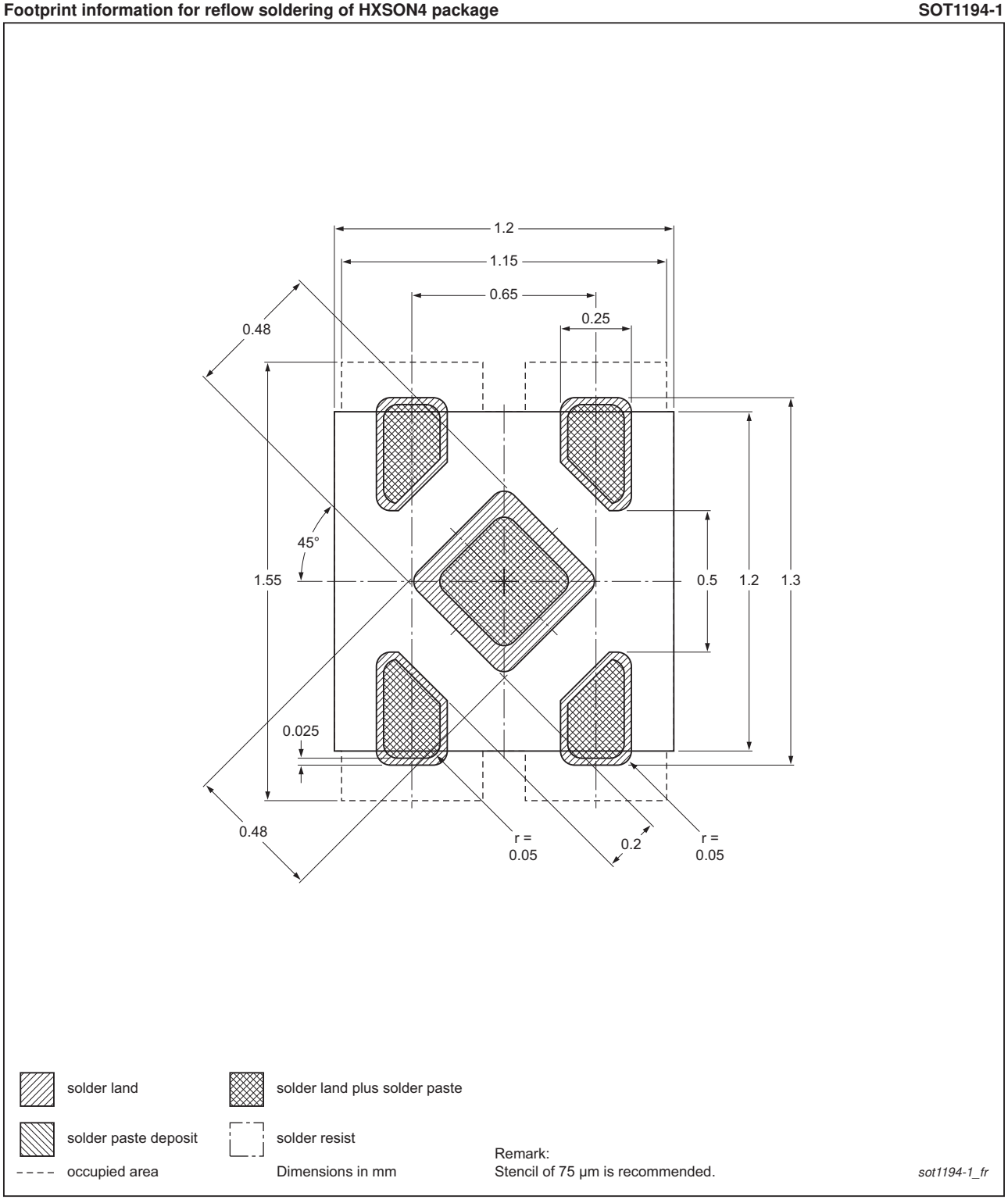


Fig 9. Soldering footprint DFN1010C-4 (SOT1194-1)

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15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

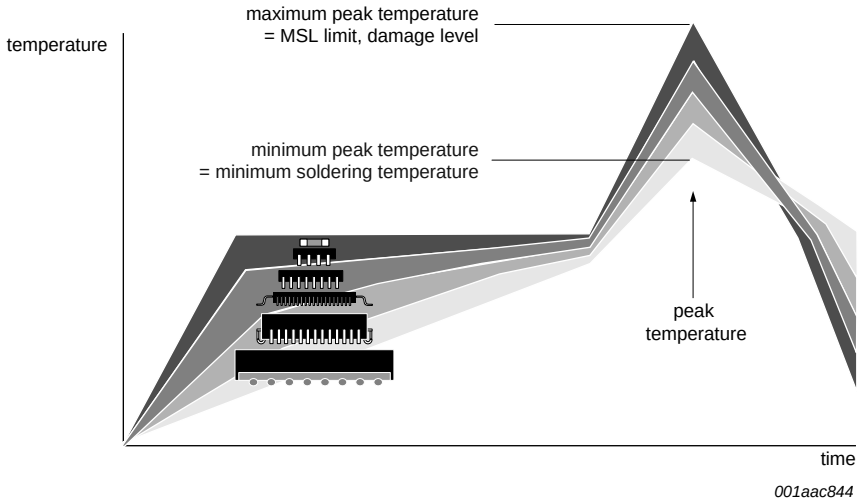
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.

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MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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16. Abbreviations

Table 14. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LDO	Low DropOut
MM	Machine Model
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PSRR	Power Supply Rejection Ratio
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances

17. References

[1] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[2] **IEC 61340-3-1 —** Methods for simulation of electrostatic effects - Human body model (HBM) electrostatic discharge test waveforms

[3] **JESD22-A115C —** Electrostatic discharge (ESD) Sensitivity Testing Machine Model (MM)

[4] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[5] **AN10365 —** Surface mount reflow soldering description

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18. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6805_SER v.2	20120625	Product data sheet	-	LD6805_SER v.1
Modifications:	• Block diagrams updated • Minor text changes			
LD6805_SER v.1	20110922	Objective data sheet	-	-

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19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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21. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
2 Pinning information 2
2.1 Pinning 2
2.2 Pin description 2
3 Ordering information 2
3.1 Ordering options 3
4 Block diagram 4
5 Limiting values 5
6 Recommended operating conditions 5
7 Thermal characteristics 5
8 Characteristics 6
9 Dynamic behavior 7
9.1 Power Supply Rejection Ratio (PSRR) 7
9.2 Dropout 8
9.3 Accuracy 9
10 Application information 9
10.1 Output capacitor values 9
11 Test information 10
11.1 Quality information 10
12 Marking 10
13 Package outline 11
14 Soldering 12
15 Soldering of SMD packages 13
15.1 Introduction to soldering 13
15.2 Wave and reflow soldering 13
15.3 Wave soldering 13
15.4 Reflow soldering 14
16 Abbreviations 16
17 References 16
18 Revision history 17
19 Legal information 18
19.1 Data sheet status 18
19.2 Definitions 18
19.3 Disclaimers 18
19.4 Trademarks 19
20 Contact information 19
21 Contents 20

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