LF411JAN Low Offset, Low Drift JFET Input Operational Amplifier

Check for Samples: LF411JAN

FEATURES

- **Internally Trimmed Offset Voltage: 0.5 mV(Typ)**
- **Input Offset Voltage Drift: 30 μV/°C**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$**
- **Wide Gain Bandwidth: 3 MHz Typ.**
- **High Slew Rate: 7V/μs (Min.)**
- **Low Supply Current: 1.8 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: A_V = 10, R_L = 10KΩ, V_O = 20V_{P-P}, BW = 20Hz - 20kHz <0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 1.5 μs**

DESCRIPTION

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and ensured input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Connection Diagram

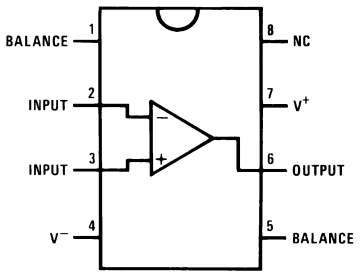
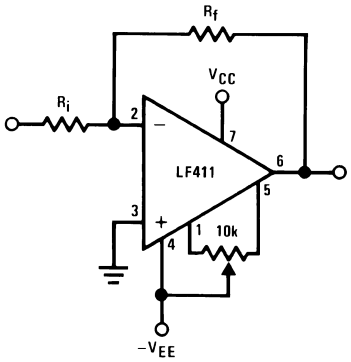


Figure 1. 8LD Ceramic Dual-in Line Package See Package Number NAB0008A (Top View)

Typical Connection



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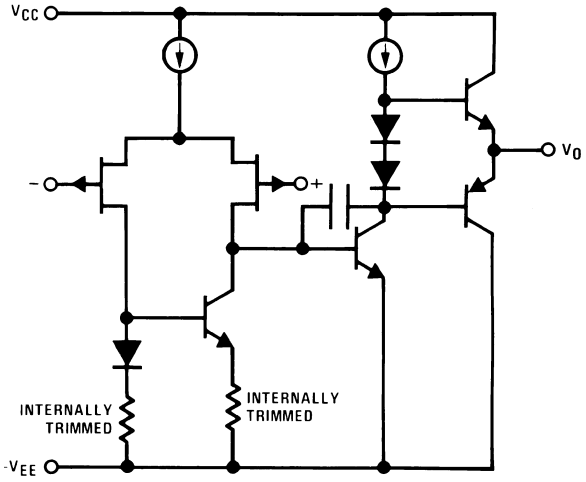
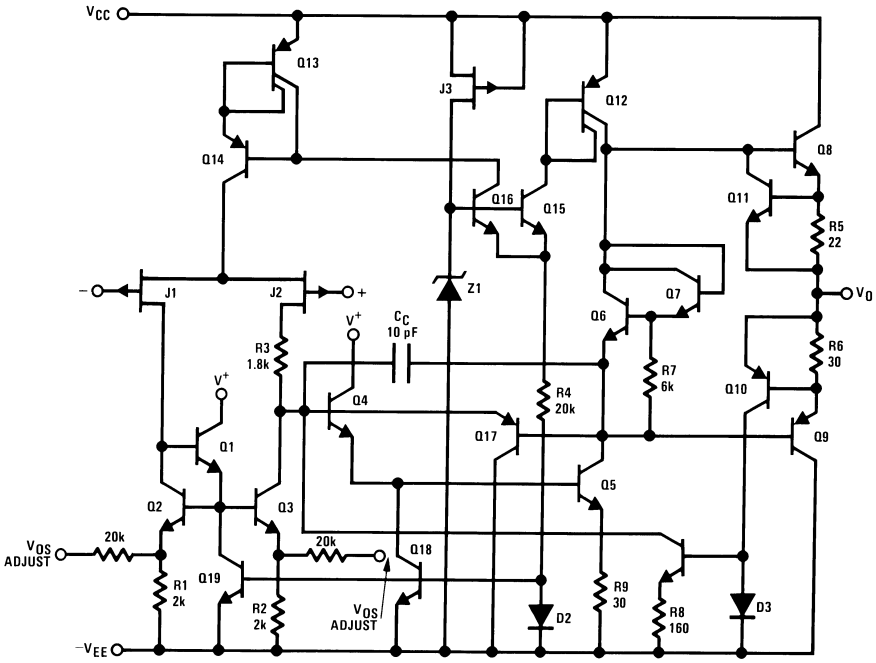
Simplified Schematic



Detailed Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1]

Supply Voltage			±18V
Differential Input Voltage			±30V
Input Voltage Range[2]			±15V
Output Short Circuit Duration			Continuous
Power Dissipation[3][4]			400mW
T_{Jmax}			175°C
Thermal Resistance	θ_{JA}	Still Air	162°C/W
		400LF/Min Air Flow	65°C/W
	θ_{JC}		20°C/W
Operating Temperature Range			−55°C ≤ T_A ≤ 125°C
Storage Temperature Range			−65°C ≤ T_A ≤ 150°C
Lead Temperature (Soldering, 10 seconds)			300°C
Package Weight (Typical)			TBD
ESD Tolerance[5]			750V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(4) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.
(5) Human body model, 100pF discharged through 1.5KΩ.

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

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Electrical Characteristics DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 26V, $-V_{CC}$ = -4V, V_{CM} = -11V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC}$ = 4V, $-V_{CC}$ = -26V, V_{CM} = 11V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
				-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		$\pm V_{CC}$ = ±5V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 26V, $-V_{CC}$ = -4V, V_{CM} = -11V, t ≤ 25mS		-0.4	0.2	nA	1
				-10	50	nA	2
		t ≤ 25mS		-0.2	0.2	nA	1
				-10	50	nA	2
		$+V_{CC}$ = 4V, $-V_{CC}$ = -26V, V_{CM} = 11V, t ≤ 25mS		-0.2	1.2	nA	1
				-10	70	nA	2
I_{IO}	Input Offset Current	t ≤ 25mS		-0.1	0.1	nA	1
				-20	20	nA	2
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 10V to 20V, $-V_{CC}$ = -15V		80		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 15V, $-V_{CC}$ = -10V to -20V		80		dB	1, 2, 3
CMR	Input Voltage Common Mode Rejection	V_{CM} = -11V to +11V		80		dB	1, 2, 3
$V_{IO\ Adj}+$	Adjustment for Input Offset Voltage			8.0		mV	1, 2, 3
$V_{IO\ Adj}-$	Adjustment for Input Offset Voltage				-8.0	mV	1, 2, 3
$I_{OS}+$	Output Short Circuit Current	t ≤ 25mS		-80		mA	1, 2, 3
$I_{OS}-$	Output Short Circuit Current	t ≤ 25mS			80	mA	1, 2, 3
I_{CC}	Supply Current				3.5	mA	1, 2
					4.0	mA	3
$\Delta V_{IO} / \Delta T$	Input Offset Voltage	25°C ≤ T_A ≤ +125°C	See (1)	-30	30	µV/°C	2
		-55°C ≤ T_A ≤ 25°C	See (1)	-30	30	µV/°C	3
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ		12		V	4, 5, 6
		R_L = 2KΩ		10		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ			-12	V	4, 5, 6
		R_L = 2KΩ			-10	V	4, 5, 6
$+A_{VS}$	Open Loop Voltage Gain	R_L = 2KΩ, V_O = 0 to 10V	See (2)	50		K	4
			See (2)	25		K	5, 6
$-A_{VS}$	Open Loop Voltage Gain	R_L = 2KΩ, V_O = 0 to -10V	See (2)	50		K	4
			See (2)	25		K	5, 6
A_{VS}	Open Loop Voltage Gain	R_L = 10KΩ, V_O = ±2V, $\pm V_{CC}$ = ±5V	See (2)	20		K	4, 5, 6

(1) Calculated parameter. For calculation use V_{IO} test at $\pm V_{CC}$ = ±15V
(2) Datalog in K = V/mV.

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Electrical Characteristics AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.
AC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR+	Slew Rate	V_I = -5V to +5V		7.0		V/µS	7
				5.0		V/µS	8A, 8B
SR-	Slew Rate	V_I = +5V to -5V		7.0		V/µS	7
				5.0		V/µS	8A, 8B
TR_{TR}	Transient Response Rise Time	A_V = 1, V_I = 50mV, C_L = 100pF, R_L = 2KΩ			200	nS	7, 8A, 8B
TR_{OS}	Transient Response Overshoot	A_V = 1, V_I = 50mV, C_L = 100pF, R_L = 2KΩ			40	%	7, 8A, 8B
NI_{BB}	Noise Broadband	BW of 10Hz to 15KHz			15	$µV_{RMS}$	7
NI_{PC}	Noise Popcorn	BW of 10Hz to 15KHz, R_S = 100KΩ			80	$µV_{PK}$	7
+tS	Settling Time	A_V = 1			1,500	nS	12
-tS	Settling Time	A_V = 1			1,500	nS	12

Electrical Characteristics DC Drift Parameters

The following conditions apply to all the following parameters, unless otherwise specified.
DC: V_{CC} = ±15V, V_{CM} = 0V
Delta Calculations performed at Group B, subgroup 5, Only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
$±I_{IB}$	Input Bias Current			-0.1	0.1	nA	1

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Typical Performance Characteristics

Input Bias Current

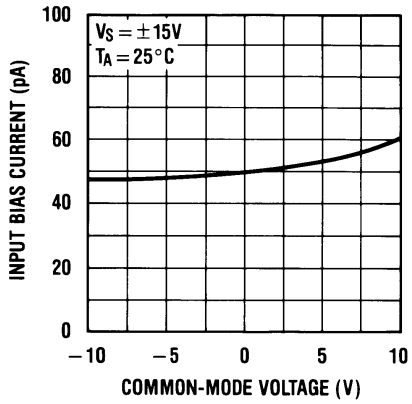

Figure 2.

Input Bias Current

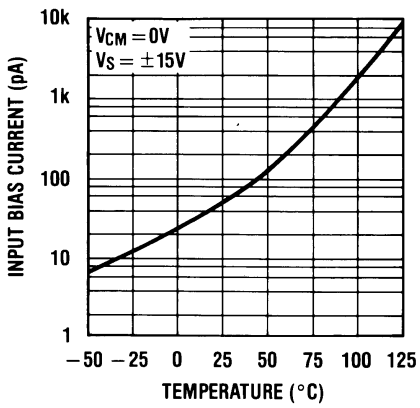

Figure 3.

Supply Current

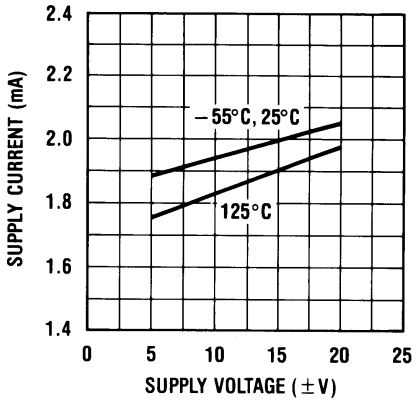

Figure 4.

Positive Common-Mode Input Voltage Limit

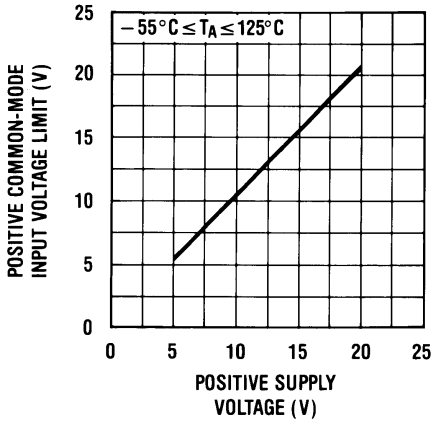

Figure 5.

Negative Common-Mode Input Voltage Limit

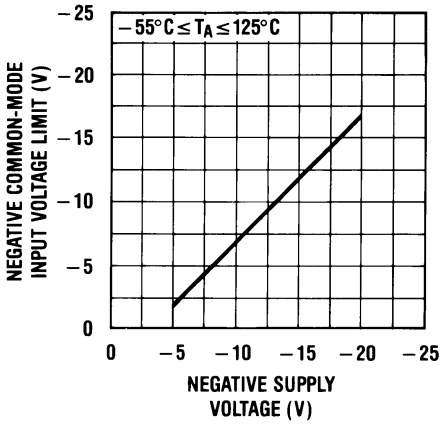

Figure 6.

Positive Current Limit

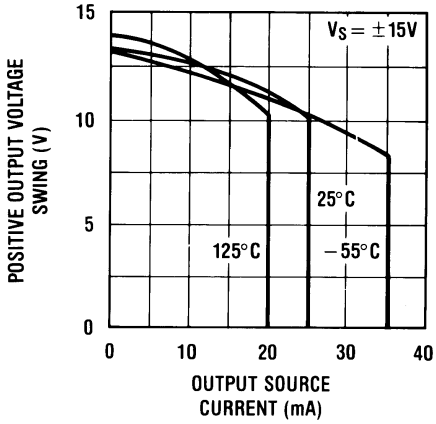

Figure 7.

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Typical Performance Characteristics (continued)

Negative Current Limit

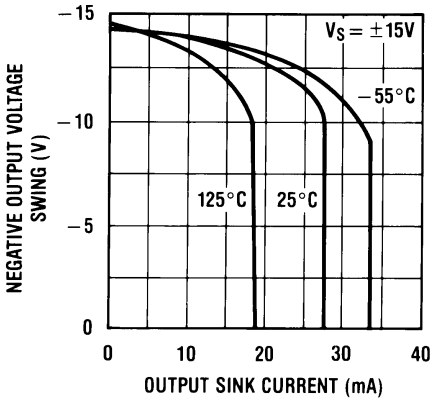

Figure 8.

Output Voltage Swing

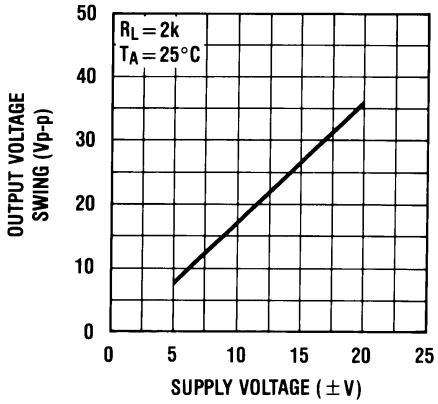

Figure 9.

Output Voltage Swing

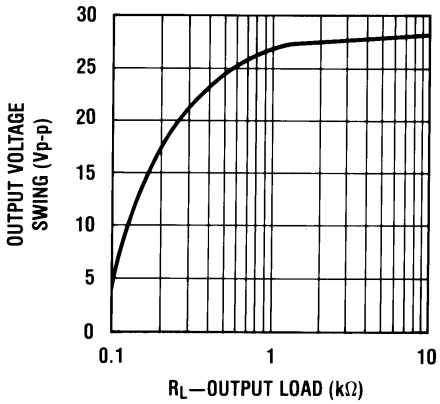

Figure 10.

Gain Bandwidth

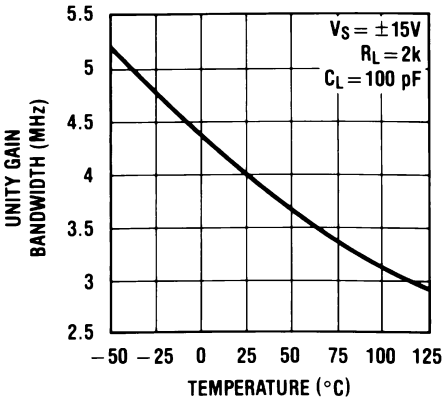

Figure 11.

Bode Plot

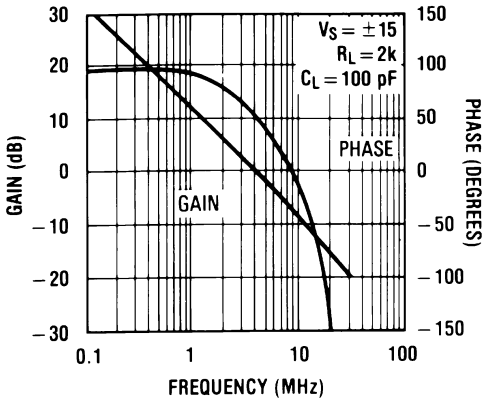

Figure 12.

Slew Rate

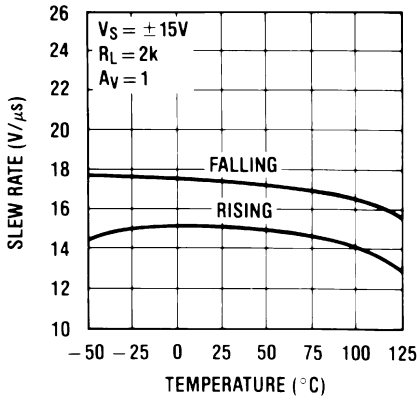

Figure 13.

Typical Performance Characteristics (continued)

Distortion vs Frequency

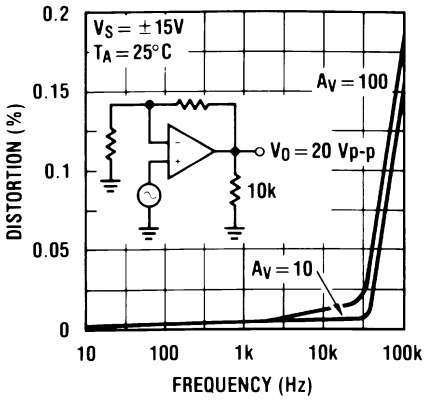

Figure 14.

Undistorted Output Voltage Swing

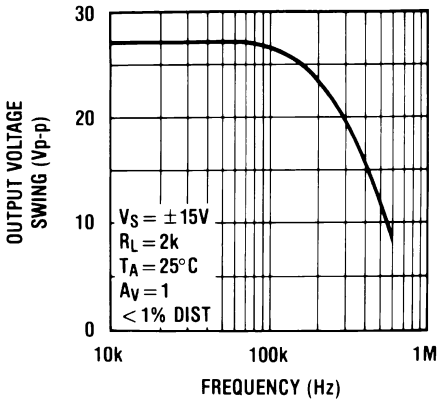

Figure 15.

Open Loop Frequency Response

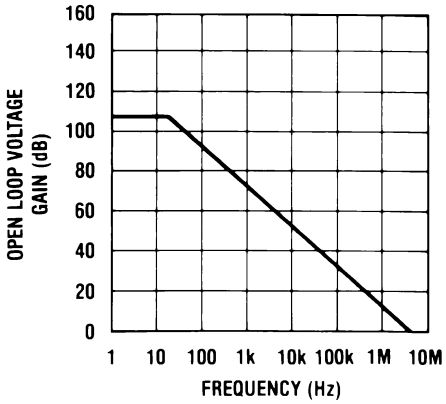

Figure 16.

Common-Mode Rejection Ratio

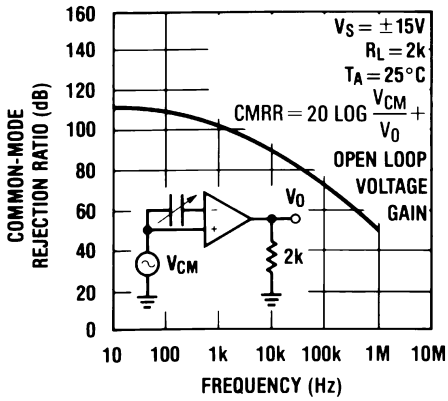

Figure 17.

Power Supply Rejection Ratio

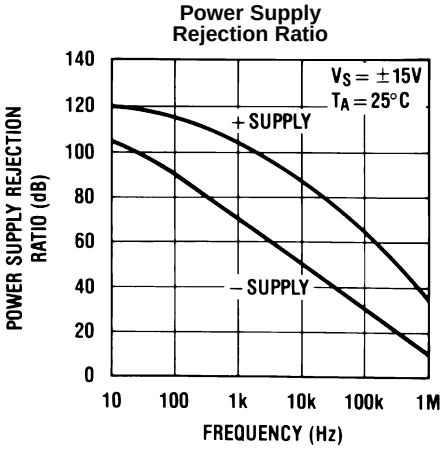

Figure 18.

Equivalent Input Noise Voltage

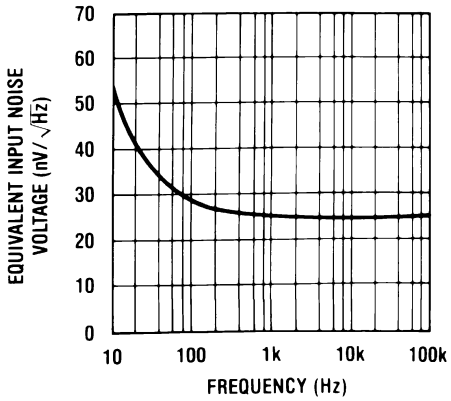

Figure 19.

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Typical Performance Characteristics (continued)

Open Loop Voltage Gain

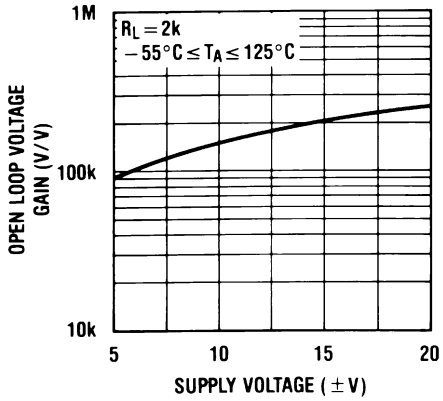

Figure 20.

Output Impedance

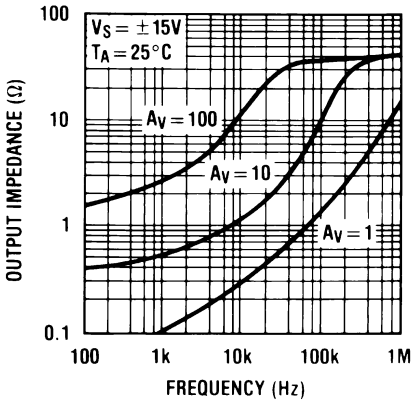

Figure 21.

Inverter Settling Time

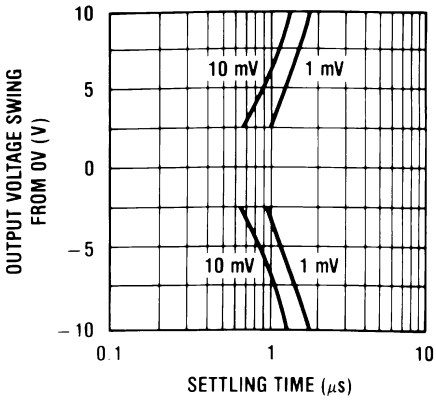

Figure 22.

Pulse Response

R_L=2 kΩ, C_L10 pF

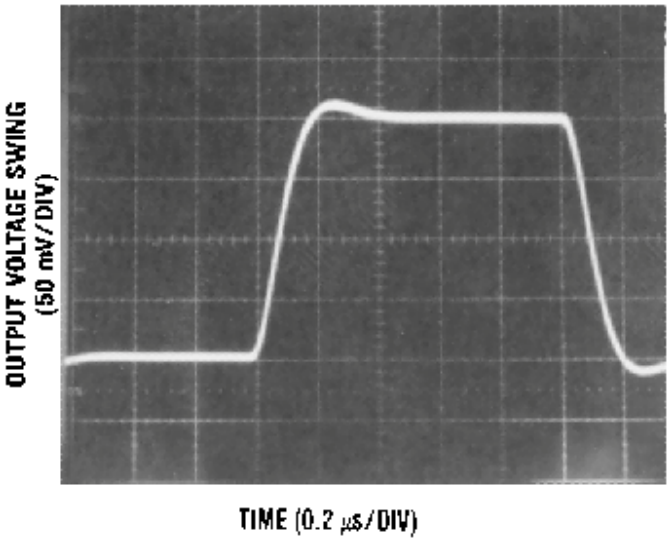

Figure 23. Small Signal Inverting

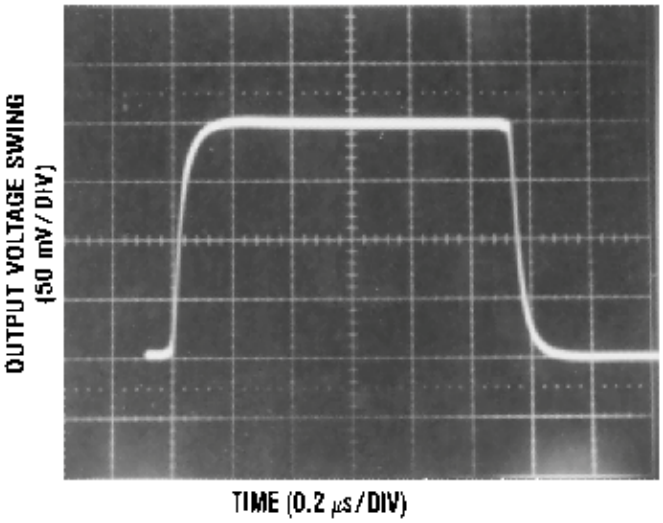

Figure 24. Small Signal Non-Inverting

Pulse Response (continued)

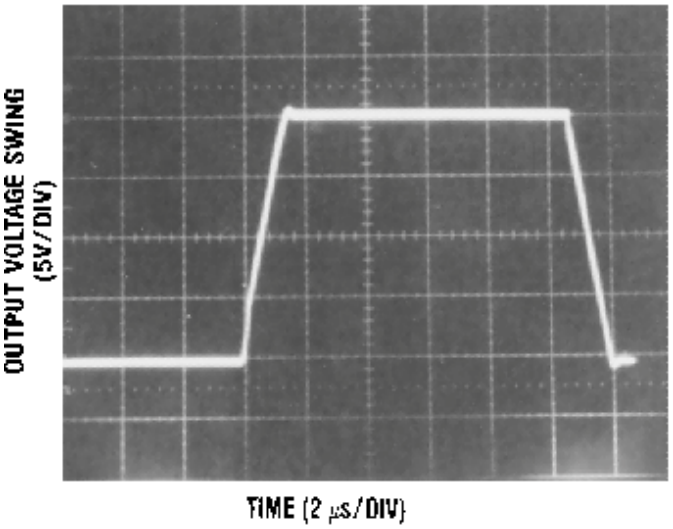

Figure 25. Large Signal Inverting

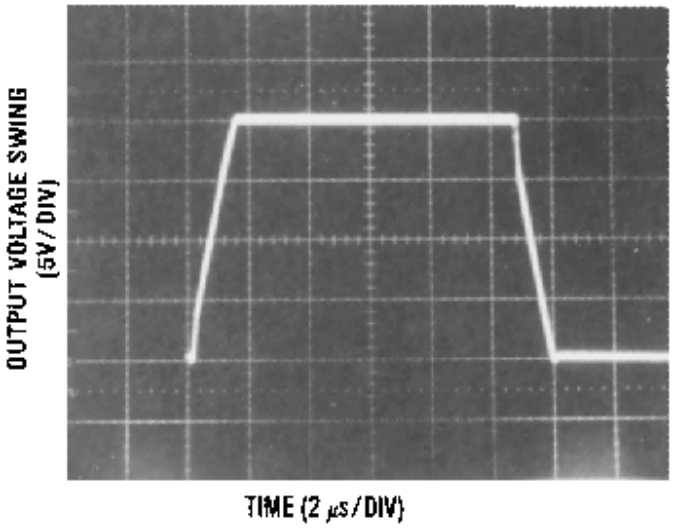

Figure 26. Large Signal Non-Inverting

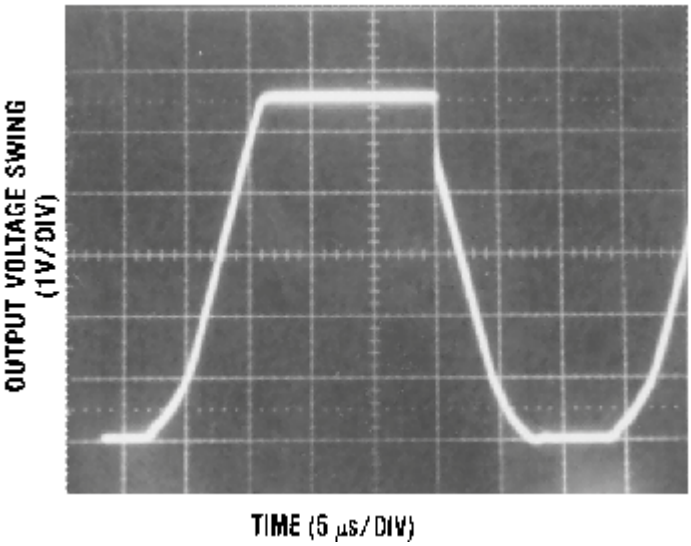

Figure 27. Current Limit (R_L=100Ω)

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APPLICATION HINTS

The LF411JAN series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and ensured input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

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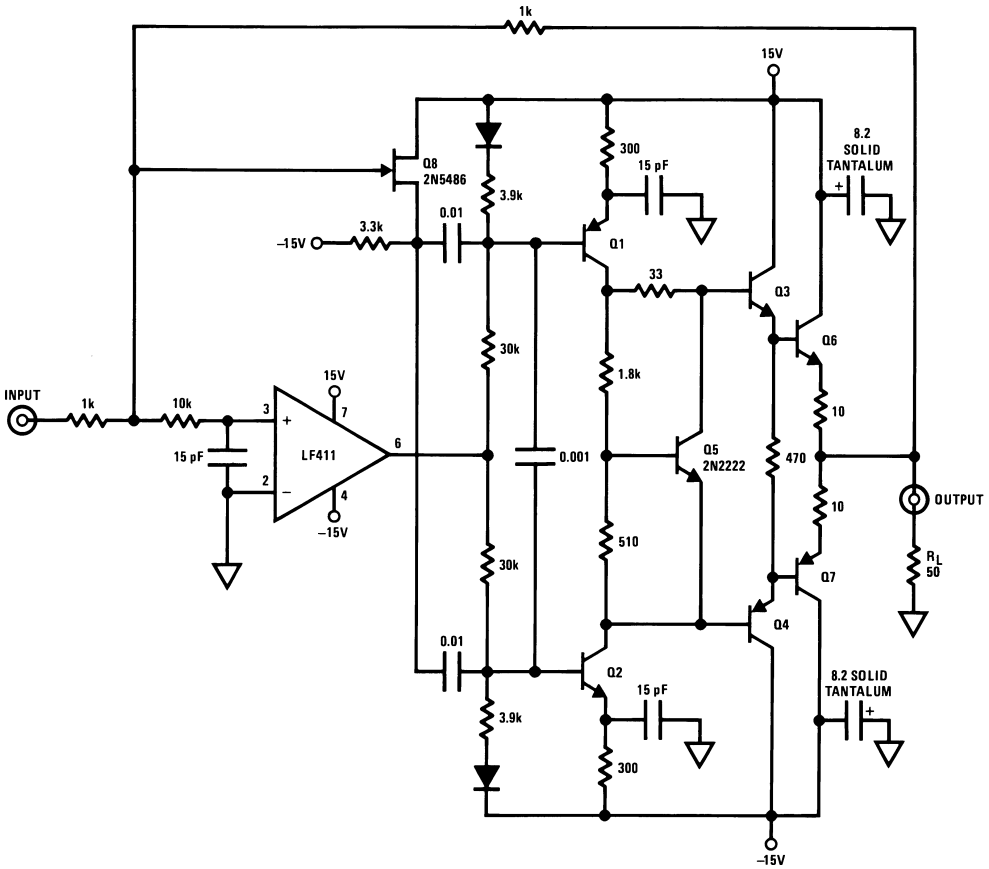
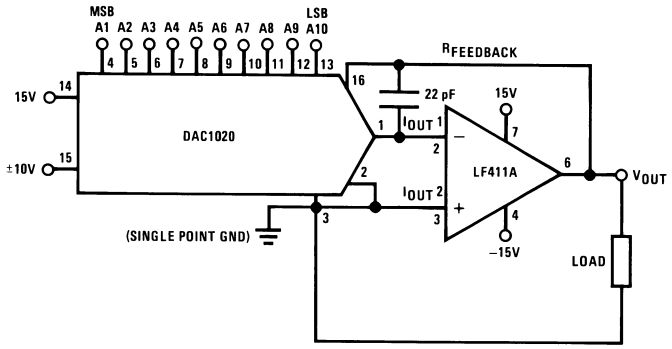
Typical Applications

Figure 28. High Speed Current Booster



PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

Figure 29. 10-Bit Linear DAC with No V_{OS} Adjust



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024}V_{REF}$$

where A_N=1 if the A_N digital input is high
A_N=0 if the A_N digital input is low

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Figure 30. Single Supply Analog Switch with Buffered Output

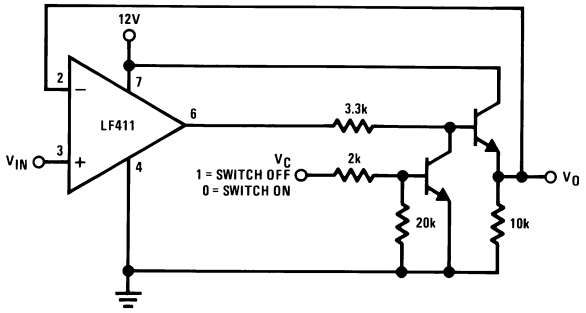

Table 2. Revision History

Date Released	Revision	Section	Originator	Changes
10/11/05	A	New Release to corporate format	L. Lytle	1 MDS data sheet was converted into the corporate data sheet format. MDS MJLF411-X Rev 0C1 will be archived.
3/27/2013	A	All Sections		Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/11904BPA	LIFEBUY	CDIP	NAB	8		TBD	Call TI	Call TI	-55 to 125	JL411BPA Q JM38510/ 11904BPA ACO 11904BPA >T	
M38510/11904BPA	LIFEBUY	CDIP	NAB	8		TBD	Call TI	Call TI	-55 to 125	JL411BPA Q JM38510/ 11904BPA ACO 11904BPA >T	
M38510/11904BPX	LIFEBUY	CDIP	NAB	8		TBD	Call TI	Call TI	-55 to 125	JL411BPA Q JM38510/ 11904BPA ACO 11904BPA >T	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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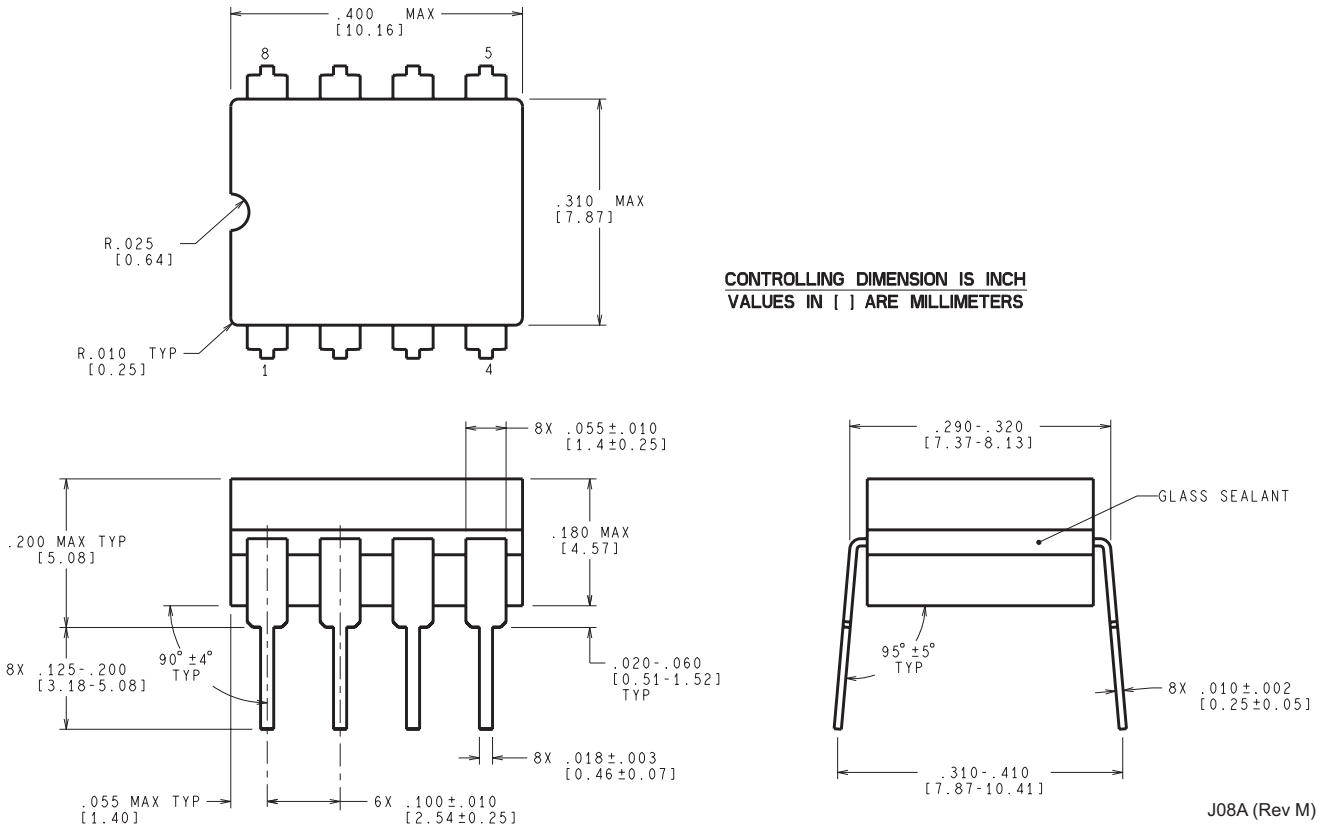
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5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
90° ±4°
TYP
8X .125-.200
[3.18-5.08]
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

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