Addressable 2-Wire Bus Buffers

FEATURES

- **Bidirectional Buffer for SDA and SCL Lines Increases Fanout**
- **Connect SDA and SCL Lines with 2-Wire Bus Commands**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane**
- **Compatible with I²C™ Standard Mode, I²C Fast Mode and SMBus Standards**
- Rise Time Accelerators on SDA, SCL Lines
- 1V Precharge on SDA and SCL Lines
- 32 Unique Addresses from a Single ADDRESS Pin
- Two General Purpose Inputs-Outputs (LTC4302-1)
- Translates Between 5V and 3.3V Systems (LTC4302-2)
- Small 10-Pin MSOP Package

APPLICATIONS

- Live Board Insertion
- 5V/3.3V Level Translator
- Servers
- Capacitance Buffer/Bus Extender
- Nested Addressing

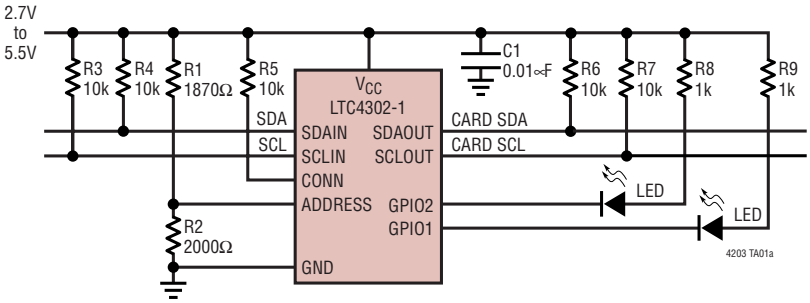
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*U.S. Patent No. 6,650,174

DESCRIPTION

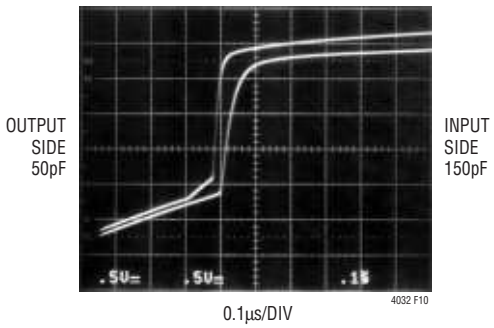
The LTC®4302-1/LTC4302-2 addressable I²C bus and SMBus compatible bus buffers allow a peripheral board to be inserted and removed from a live backplane without corruption of the bus. The LTC4302-1/LTC4302-2 maintain electrical isolation between the backplane and peripheral board until their V_{CC} supply is valid and a master device on the backplane side addresses the LTC4302-1/LTC4302-2 and commands them to connect. The LTC4302-1/LTC4302-2's ADDRESS pin provides 32 possible addresses set by an external resistive divider between V_{CC} and GND. The LTC4302-1/LTC4302-2 work with supply voltages ranging from 2.7V to 5.5V. The SDA and SCL inputs and outputs do not load the bus lines when V_{CC} is low.

Rise time accelerator circuitry* allows for heavier capacitive bus loading while still meeting system timing requirements. During insertion, the SDA and SCL lines are precharged to 1V to minimize bus disturbances. Two general purpose input/output pins (GPIOs) on the LTC4302-1 can be configured as inputs, open-drain outputs or push-pull outputs. The LTC4302-2 option replaces one GPIO pin with a second supply voltage pin V_{CC2}, providing level shifting between systems with different supply voltages. The LTC4302-1/LTC4302-2 are available in a 10-pin MSOP package.

TYPICAL APPLICATION



Input-Output Connection t_{PLH}

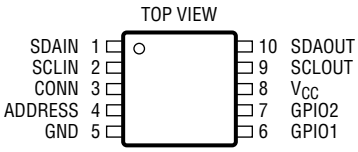


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND ..... –0.3V to 7V
SDAIN, SCLIN, SDAOUT, SCLOUT,
GPIO1, CONN, GPIO2 (LTC4302-1),
V_{CC2} (LTC4302-2) ..... –0.3V to 7V
ADDRESS ..... –0.3V to V_{CC} + 0.3V

Operating Temperature Range
LTC4302C-1/LTC4302C-2 ..... 0°C to 70°C
LTC4302I-1/LTC4302I-2 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

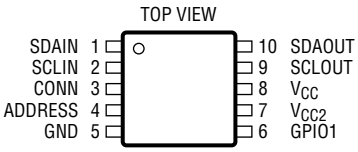
PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC4302CMS-1 LTC4302IMS-1
MS PART MARKING
LTYF LTYG



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC4302CMS-2 LTC4302IMS-2
MS PART MARKING
LTABY LTABZ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V (LTC4302-1), V_{CC} = V_{CC2} = 2.7V to 5.5V (LTC4302-2) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply/Start-Up							
V_{CC}	Positive Supply Voltage	LTC4302-1	●	2.7		5.5	V
V_{CC2}	Card Side Supply Voltage	LTC4302-2	●	2.7		5.5	V
I_{CC}	Supply Current	V_{SDAIN} = 0V, V_{CC} = 5.5V (Note 2) LTC4302-1	●		5.9	8	mA
I_{VCC}	V_{CC} Supply Current	V_{SDAIN} = 0V, V_{CC} = V_{CC2} = 5.5V (Note 2) LTC4302-2	●		3.4	5	mA
I_{VCC2}	V_{CC2} Supply Current	V_{SDAIN} = 0V, V_{CC} = V_{CC2} = 5.5V (Note 2) LTC4302-2	●		2.3	4	mA
V_{UVLOU}	UVLO Upper Threshold	V_{CC} Rising	●		2.5	2.7	V
V_{UVLOL}	UVLO Lower Threshold	V_{CC} Falling			2.35		V
V_{UVLO2U}	V_{CC2} UVLO Upper Threshold	LTC4302-2	●		2.5	2.7	V
V_{UVLO2L}	V_{CC2} UVLO Lower Threshold	LTC4302-2			2.35		V
V_{PRE}	Precharge Voltage	SDA, SCL Floating	●	0.8	1	1.2	V
V_{THCONN}	CONN Threshold Voltage		●	0.8	1.5	2.2	V
t_{PHL}	CONN Delay, On-Off				60		ns
t_{PLH}	CONN Delay, Off-On				20		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V (LTC4302-1), V_{CC} = V_{CC2} = 2.7V to 5.5V (LTC4302-2) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
General Purpose I/Os							
V_{LOW}	I/O Logic Low Voltage	I_{SINK} = 10mA, V_{CC} = 2.7V	●		0.36	0.8	V
V_{HIGH}	I/O Logic High Voltage	I_{SOURCE} = 200µA, V_{CC} = 2.7V	●	2.4			V
I_{LEAK}	I/O Leakage Current	$V_{I/O}$ = 0V to 5.5V (Note 3)	●			±5	µA
V_{THRESH}	Input Threshold Voltage	Input Mode	●	0.8	1.5	2.2	V
Rise Time Accelerators							
$I_{PULLUP,AC}$	Transient Boosted Pull-Up Current	Positive Transition on SDA, SCL, Slew Rate = 0.8V/µs, V_{CC} = 2.7V (Note 4)	●	1	2		mA
Input-Output Connection							
V_{OS}	Output-Input Offset Voltage	10k to V_{CC} on SDA, SCL Pins (Note 5),	●	0	100	175	mV
C_{IN}	Digital Input Capacitance	(Note 9)				10	pF
V_{OL}	Output Low Voltage	SDA, SCL Pins, I_{SINK} = 3mA	●	0		0.4	V
I_{LEAK}	Input Leakage Current	SDA, SCL Pins, V_{CC} = 0V to 5.5V Connection Circuits Inactive	●			±5	µA
2-Wire Digital Interface Voltage Characteristics							
V_{LTH}	Logic Threshold Voltage		●	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
I_{LEAK}	Digital Input Leakage	V_{CC} = 0V to 5.5V	●			±5	µA
V_{OL}	Digital Output Low Voltage	I_{PULLUP} = 3mA Into SDAIN Pin	●			0.4	V
2-Wire Digital Interface Timing Characteristics (Note 6)							
$f_{I2C,MAX}$	I^2C Operating Frequency	(Note 9)		400	600		kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition	(Note 9)			0.75	1.3	µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition	(Note 9)			45	100	ns
$t_{SU,STA}$	Repeated Start Condition Setup Time	(Note 9)			–30	0	ns
$t_{SU,STO}$	Stop Condition Setup Time	(Note 9)			–30	0	ns
$t_{HD,DATI}$	Data Hold Time Input	(Note 9)			–25	0	ns
$t_{HD,DATO}$	Data Hold Time Output			300	600	900	ns
$t_{SU,DAT}$	Data Setup Time	(Note 9)			50	100	ns
t_{SP}	Pulse Width of Spikes Suppressed by the Input Filter	(Note 9)		50	150	250	ns
t_f	Data Fall Time	(Notes 7, 8, 9)		20 + $0.1C_B$		300	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The I_{CC} tests are performed with the backplane-to-card connection circuitry activated.

Note 3: When the GPIOs are in open-drain output or input mode, the logic high voltage can be provided by a pull-up supply voltage ranging from 2.2V to 5.5V, independent of the V_{CC} voltage.

Note 4: $I_{PULLUP,AC}$ varies with temperature and V_{CC} voltage as shown in the Typical Performance Characteristics section.

Note 5: The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.

Note 6: The specifications in this section illustrate the LTC4302-1/LTC4302-2's compatibility with the I^2C Fast Mode, the I^2C Standard Mode and SMBus specifications. See the Timing Diagram on page 5 for illustrations of the timing parameters.

Note 7: C_B = total capacitance of one bus line in pF.

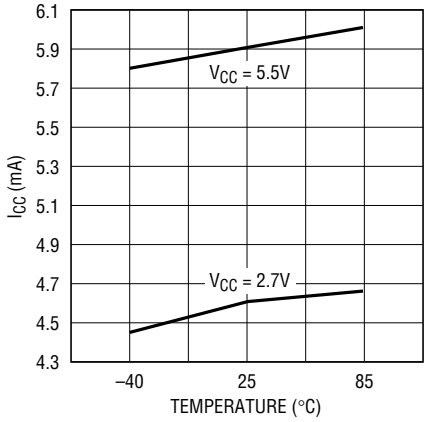
Note 8: The digital interface circuit controls the data fall time only when acknowledging or transmitting zeros during a read operation. The input-output connection data and clock outputs meet the fall time specification provided that the corresponding inputs meet the fall time specification.

Note 9: Guaranteed by design. Not subject to test.

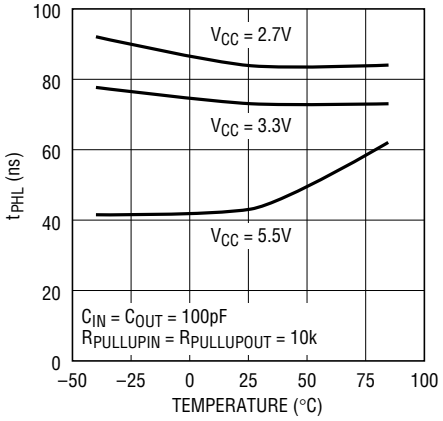
TYPICAL PERFORMANCE CHARACTERISTICS

(Specifications are at T_A = 25°C unless otherwise noted.)

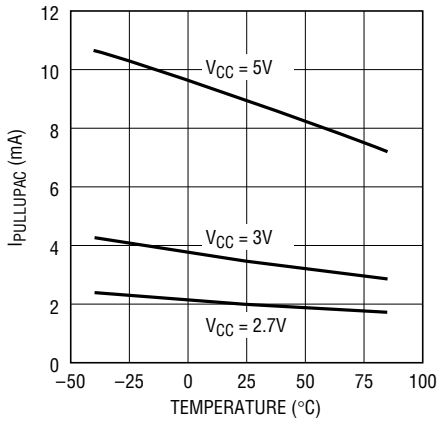
I_{CC} vs Temperature



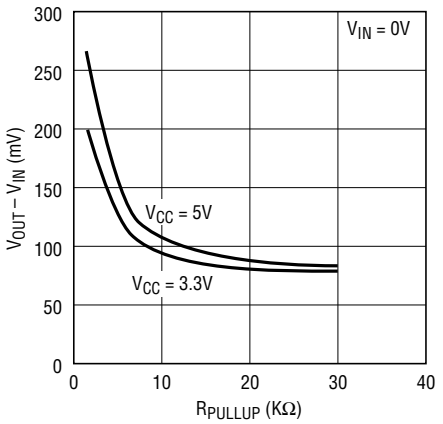
Input – Output t_{PHL} vs Temperature



$I_{PULLUPAC}$ vs Temperature



SDA, SCL V_{OS}



PIN FUNCTIONS

SDAIN (Pin 1): Serial Data Input. Connect this pin to the SDA bus on the backplane. Do not float.

SCLIN (Pin 2): Serial Clock Input. Connect this pin to the SCL bus on the backplane. Do not float.

CONN (Pin 3): Register Reset and Connection Sense Input. Driving this pin low resets the registers to their default state: GPIOs in output open-drain high impedance mode, rise time accelerators disabled and the input-to-output connection disabled. Communication with the LTC4302-1/LTC4302-2 is disabled when CONN is low. When CONN is brought back high, the registers remain in the default state and communication is enabled.

ADDRESS (Pin 4): 2-Wire Address Programming Input. The 2-wire address is programmed by connecting ADDRESS to a resistive divider between V_{CC} and ground. The voltage on ADDRESS is converted by an internal analog-to-digital (A/D) converter into a 5-bit digital word. This resulting digital code represents the least significant five bits of the 2-wire address. 1% resistors must be used to ensure accurate address programming. 32 unique addresses are possible. See Table 1 for 1% resistor values and corresponding addresses. Care must also be taken to minimize capacitance on ADDRESS. Resistors must be placed close to the LTC4302-1/LTC4302-2's V_{CC}, GND and ADDRESS pins.

GND (Pin 5): Ground. Connect this pin to a ground plane for best results.

GPIO1 (Pin 6): General Purpose Input/Output (GPIO1). GPIO1 can be used as an input, an open-drain output or a push-pull output. The N-Channel MOSFET pulldown device is capable of driving LEDs. When used in input or open-drain output mode, the I/O pin can be pulled up to a supply voltage ranging from 2.2V to 5.5V independent of the V_{CC} voltage.

GPIO2 (Pin 7, LTC4302-1): General Purpose Input/Output. GPIO2 can be used as an input, an open-drain output, or a push-pull output. The N-Channel MOSFET pulldown device is capable of driving LED's. When used in input or open-drain output mode, the I/O pin can be pulled up to a supply voltage ranging from 2.2V to 5.5V independent of the V_{CC} voltage.

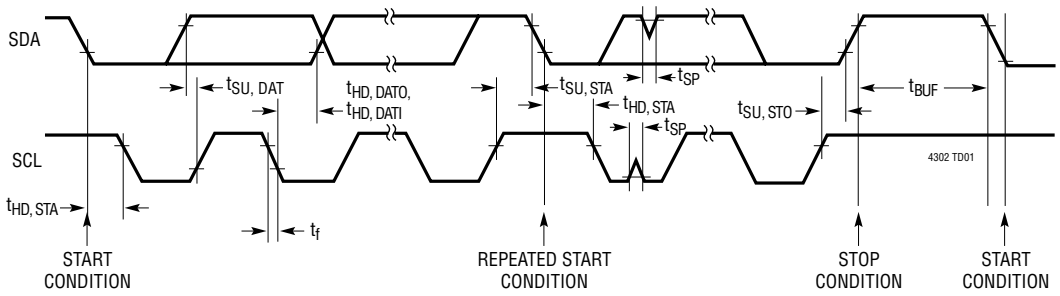
V_{CC2} (Pin 7, LTC4302-2): Card Side Supply Voltage. This pin is a power supply pin for the card side busses. Connect V_{CC2} to the card's V_{CC} and connect a bypass capacitor of at least 0.01µF directly between V_{CC2} and GND for best results.

V_{CC} (Pin 8): Main Input Power Supply from Backplane. Connect a bypass capacitor of at least 0.01µF directly between V_{CC} and GND for best results.

SCLOUT (Pin 9): Serial Clock Output. Connect this pin to the SCL bus on the I/O card. Do not float.

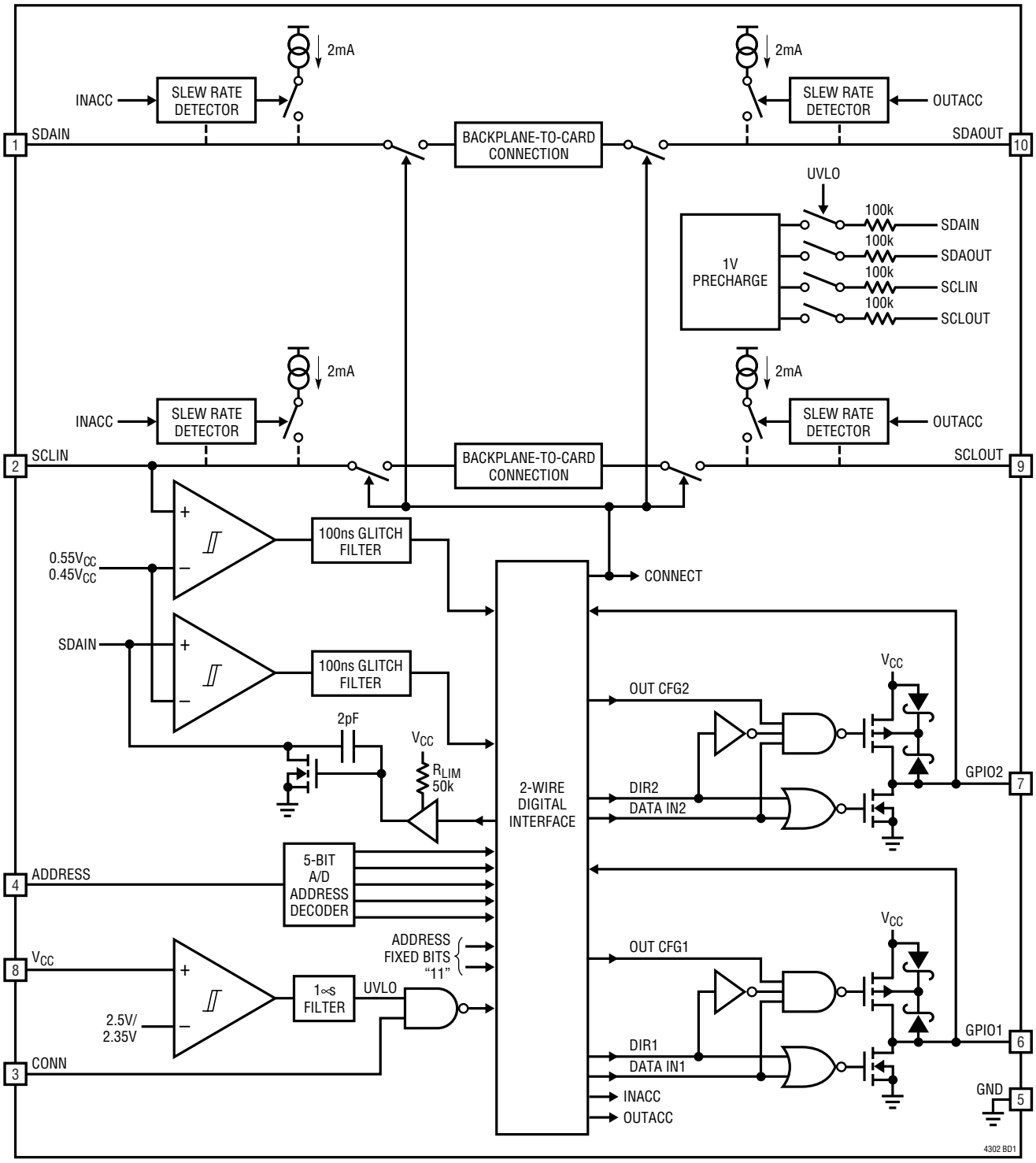
SDAOUT (Pin 10): Serial Data Output. Connect this pin to the SDA bus on the I/O card. Do not float.

TIMING DIAGRAM



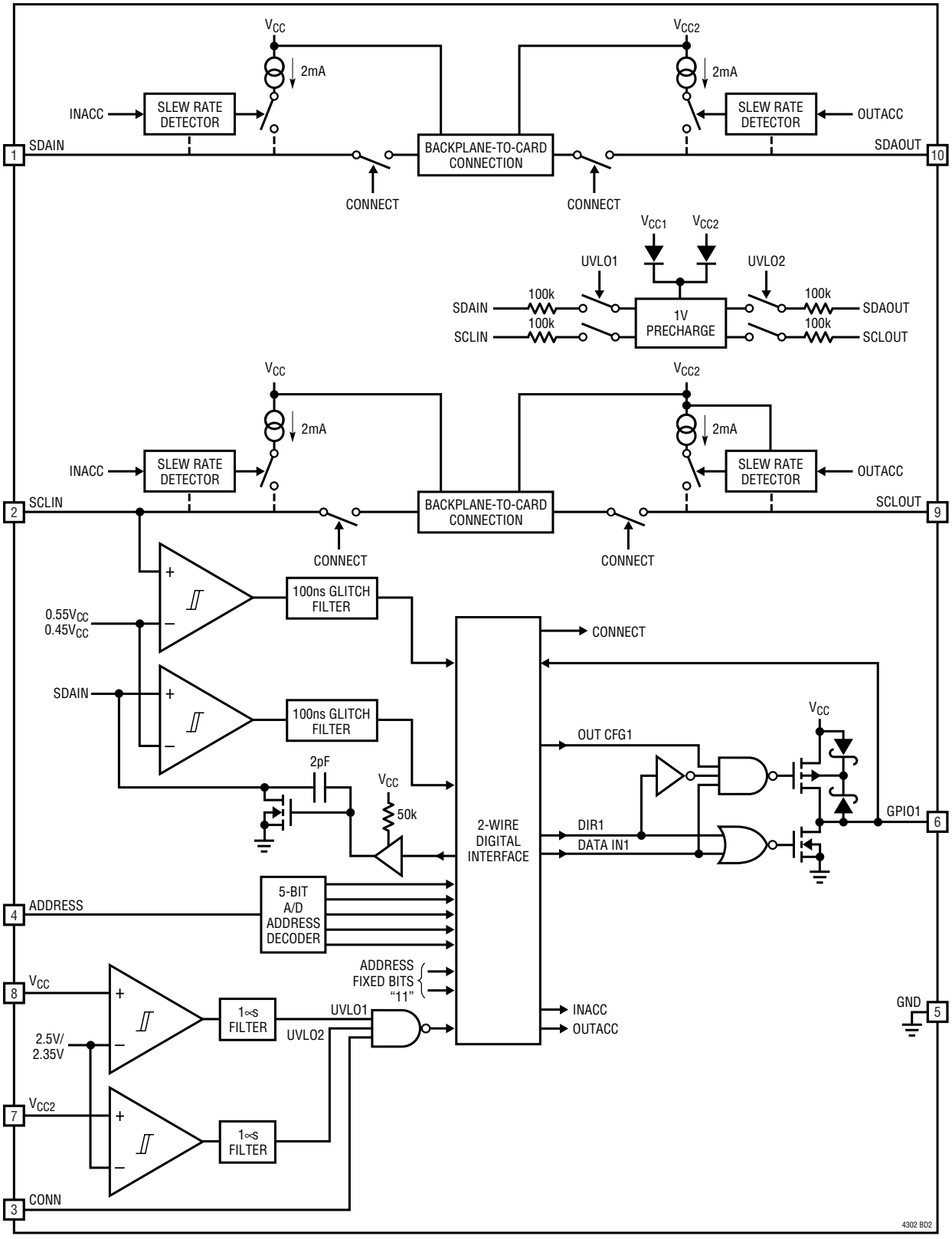
BLOCK DIAGRAMS

LTC4302-1 Addressable 2-Wire Bus Buffer



BLOCK DIAGRAMS

LTC4302-2 Addressable 2-Wire Bus Buffer



OPERATION

Live Insertion and Start-Up

The LTC4302 allows I/O card insertion into a live backplane without corruption of the data and clock busses (SDA and SCL). In its main application, the LTC4302 resides on the edge of a peripheral card with the SCLOUT pin connected to the card's SCL bus and the SDAOUT connected to the card's SDA bus. If a card is plugged into a live backplane via a staggered connector, ground and V_{CC} make connection first. The LTC4302 starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5V (typical). This ensures that the LTC4302 does not try to function until it has sufficient bias voltage.

During this time, the 1V precharge circuitry is also active and forces 1V through 100k nominal resistors to the SDA and SCL pins. The concept of initializing the SDA and SCL pins before they make contact with a live backplane is described in the CompactPCI™ specification. Because the I/O card is being plugged into a live backplane, the voltage on the SDA and SCL busses may be anywhere between 0V and V_{CC}. Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card. The LTC4302-1 precharges all four SDA and SCL pins whenever the V_{CC} voltage is below its UVLO threshold voltage. The LTC4302-2 precharges SDAIN and SCLIN whenever V_{CC} is below its UVLO threshold and precharges SDAOUT and SCLOUT whenever V_{CC2} is below its UVLO threshold.

After ground and V_{CC} connect, SDAIN and SCLIN make connection with the backplane SDA and SCL lines. Once the part comes out of UVLO, the precharge circuitry is shut off. Finally, the CONN pin connects to the short CONN pin on the backplane, the 2-wire bus digital interface circuitry is activated and a master on the bus can write to or read from the LTC4302.

General I²C Bus/SMBus Description

The LTC4302 is designed to be compatible with the I²C and SMBus two wire bus systems. I²C Bus and SMBus are reasonably similar examples of two wire, bidirectional, serial communication busses; however, calling them two wire is not strictly accurate, as there is an implied third wire which is the ground line. Large ground drops or spikes between the grounds of different parts on the bus can interrupt or disrupt communications, as the signals on the two wires are both inherently referenced to a ground which is expected to be common to all parts on the bus. Both bus types have one data line and one clock line which are externally pulled to a high voltage when they are not being controlled by a device on the bus. The devices on the bus can only pull the data and clock lines low, which makes it simple to detect if more than one device is trying to control the bus; eventually, a device will release a line and it will not pull high because another device is still holding it low. Pullups for the data and clock lines are usually provided by external discrete resistors, but external current sources can also be used. Since there are no dedicated lines to use to tell a given device if another device is trying to communicate with it, each device must have a unique address to which it will respond. The first part of any communication is to send out an address on the bus and wait to see if another device responds to it. After a response is detected, meaningful data can be exchanged between the parts.

Typically, one device controls the clock line at least most of the time and normally sends data to the other parts and polls them to send data back. This device is called the master. There can be more than one master, since there is an effective protocol to resolve bus contentions, and non-master (slave) devices can also control the clock to delay rising edges to give themselves more time to complete calculations or communications (clock stretching). Slave devices need to control the data line to acknowledge communications from the master. Some devices need to send data back to the master; they will be in control of the data line while they are doing so. Many slave devices have no need to stretch the clock signal, which is the case with the LTC4302.

Data is exchanged in the form of bytes, which are 8-bit packets. Any byte needs to be acknowledged by the slave or master (data line pulled low) or not acknowledged by the master (data line left high), so communications are

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OPERATION

broken up into 9-bit segments, one byte followed by one bit for acknowledging. For example, sending out an address consists of 7-bits of device address, 1-bit that signals whether a read or write operation will be performed and then 1 more bit to allow the slave to acknowledge. There is no theoretical limit to how many total bytes can be exchanged in a given transmission.

I^2C and SMBus are very similar specifications, SMBus having been derived from I^2C. In general, SMBus is targeted to low power devices (particularly battery powered ones) and emphasizes low power consumption while I^2C is targeted to higher speed systems where the power consumption of the bus is not as critical. I^2C has three different specifications for three different maximum speeds, these being standard mode (100kHz max), fast mode (400kHz max), and Hs mode (3.4MHz max). Standard and fast mode are not radically different, but Hs mode is very different from a hardware and software perspective and requires an initiating command at standard or fast speed before data can start transferring at Hs speed. SMBus simply specifies a 100kHz maximum speed.

The START and STOP Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge (LOW active) generated by the slave lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The transmitter master releases the SDA line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

When a slave-receiver doesn't acknowledge the slave address (for example, it's unable to receive because it's performing a real-time function), the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave not generating the acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition. When the master is reading data from the slave, the master acknowledges each byte read except for the last byte read. The master signals a not acknowledge when no other data is to be read and carries out the STOP condition.

Address Byte and Setting the LTC4302's Address

The LTC4302's address is set by connecting ADDRESS to a resistive divider between V_{CC} and ground. The voltage on ADDRESS is converted into a 5-bit digital word by an A/D converter, as shown in Figure 1. This 5-bit word sets the 5 LSB's of the LTC4302's address; its two MSB's are always "11". Using 1% resistors, the voltage at ADDRESS is set 0.5LSB away from each code transition. For example, with V_{CC}=5V, 1LSB=5V/32 codes = 156.25mV/code. To set an address of 00, set ADDRESS to 0V + 0.5LSB = 78.125mV.

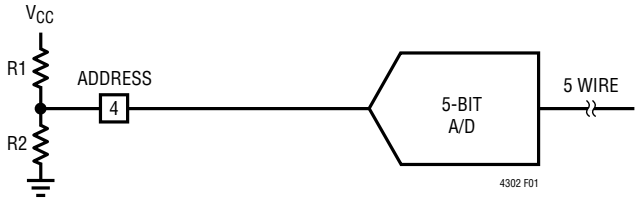


Figure 1. Address Compare Circuitry

OPERATION

Table 1. Suggested ADDRESS 1% Resistor Values (Refer to Figure 1 for R1 and R2)

ADDRESS CODE	$R_{1(TOP)}$ RESISTOR	$R_{2(BOTTOM)}$ RESISTOR	5V IDEAL VOLTAGE	ALLOWED ADDRESS VOLTAGE RANGE	3.3V IDEAL VOLTAGE	ALLOWED ADDRESS VOLTAGE RANGE
00	8660	137	0.078125	0.076 to 0.079	0.051563	0.050 to 0.052
01	2800	137	0.234375	0.229 to 0.238	0.154688	0.151 to 0.157
02	1180	100	0.390625	0.383 to 0.398	0.257813	0.253 to 0.263
03	1370	169	0.546875	0.539 to 0.559	0.360938	0.356 to 0.369
04	1070	174	0.703125	0.687 to 0.711	0.464063	0.454 to 0.470
05	1070	221	0.859375	0.842 to 0.870	0.567188	0.556 to 0.574
06	4120	1050	1.015625	0.999 to 1.032	0.670313	0.660 to 0.681
07	3320	1020	1.171875	1.157 to 1.193	0.773438	0.764 to 0.788
08	3160	1150	1.328125	1.315 to 1.354	0.876563	0.868 to 0.893
09	6490	2740	1.484375	1.464 to 1.505	0.979688	0.966 to 0.993
10	2150	1050	1.640625	1.619 to 1.663	1.082813	1.068 to 1.097
11	2050	1150	1.796875	1.774 to 1.820	1.185938	1.171 to 1.201
12	2150	1370	1.953125	1.922 to 1.970	1.289063	1.269 to 1.300
13	1960	1430	2.109375	2.085 to 2.134	1.392188	1.376 to 1.408
14	2100	1740	2.265625	2.241 to 2.290	1.495313	1.479 to 1.512
15	2000	1870	2.421875	2.391 to 2.441	1.598438	1.578 to 1.611
16	1870	2000	2.578125	2.559 to 2.609	1.701563	1.689 to 1.722
17	1740	2100	2.734375	2.710 to 2.759	1.804688	1.788 to 1.821
18	1430	1960	2.890625	2.866 to 2.915	1.907813	1.892 to 1.924
19	1370	2150	3.046875	3.030 to 3.078	2.010938	2.000 to 2.031
20	1150	2050	3.203125	3.180 to 3.226	2.114063	2.099 to 2.129
21	1050	2150	3.359375	3.337 to 3.381	2.217188	2.203 to 2.232
22	2740	6490	3.515625	3.495 to 3.537	2.320313	2.307 to 2.334
23	1150	3160	3.671875	3.646 to 3.685	2.423438	2.407 to 2.432
24	1020	3320	3.838125	3.807 to 3.843	2.526563	2.512 to 2.536
25	1050	4120	3.984375	3.968 to 4.001	2.629688	2.619 to 2.640
26	221	1070	4.140625	4.130 to 4.158	2.732813	2.726 to 2.744
27	174	1070	4.296875	4.289 to 4.313	2.835938	2.830 to 2.846
28	169	1370	4.453125	4.441 to 4.461	2.939063	2.931 to 2.944
29	100	1180	4.609375	4.602 to 4.617	3.042188	3.037 to 3.047
30	137	2800	4.765625	4.762 to 4.771	3.145313	3.143 to 3.149
31	137	8660	4.921875	4.921 to 4.924	3.248438	3.248 to 3.250

Select standard 1% tolerance resistor values that most closely match the ideal resistor values. Table 1 shows recommended values for each of the code segments. For code 00, RTOP=8660Ω, RBOTTOM=137Ω. This yields a voltage of 77.87mV. Resistors must be placed close to the LTC4302's V_{CC}, GND and ADDRESS pins. Care must also be taken to minimize capacitance on ADDRESS.

In two-wire bus systems, the master issues the Address Byte immediately following a Start Bit. The first seven bits contain the address of the slave device being targeted by the master. If the first two MSB's are 1's, and the next 5 bits match the output of the LTC4302's 5-bit address A/D, an address match occurs, and the LTC4302 acknowledges the Address Byte and continues communicating with the

OPERATION

master. The 8th bit of the Address Byte is the Read/Write bit (R/$\overline{W}$) and determines whether the master is writing to or reading from the slave. Figure 2 shows a timing diagram of the Start Bit and Address Byte required for both reading and writing the LTC4302.

Programmable Features

The two-wire bus can be used to connect and disconnect the card and backplane SDA and SCL busses, enable and disable the rise time accelerators on either or both the backplane and card sides, and configure and write to the two GPIO pins (only one GPIO for the LTC4302-2). The bits that control these features are stored in two registers. For ease of software coding, the bits that are expected to change more frequently are stored in the first register. In addition, the bus can be used to read back the logic states of the control bits. The maximum SCL frequency is 400kHz.

Writing to the LTC4302

The LTC4302 can be written using three different formats, which are shown in Figures 3, 5 and 6. Each format begins with a Start Bit, followed by the Address Byte as discussed above. The procedure for writing one data byte is given by the SMBus Send Byte protocol, illustrated in Figure 3. The bits of the Data Byte are stored in the LTC4302's Register 1. Table 2 defines the functions of these control bits. The MSB controls the connection between the backplane and card two-wire busses. The next two bits are used to write logic values to the two GPIO pins. Since the LTC4302-2 has only one GPIO pin, bit "DATA IN1" controls its logic value and bit "DATA IN2" is ignored. The 5 LSBs are not used in Write operations.

The LTC4302 can be written with two data bytes by using the format shown in Figure 5. The Address Byte and first Data Byte are exactly the same as they are for the Send Byte

Table 2. Register 1 Definition

BIT	NAME	TYPE	FUNCTION
7 (MSB)	CONNECT	Read/Write	Backplane-to-Card Connection; 0 = Disconnected, 1 = Connected
6	DATA IN2	Read/Write	Logic State of Input Signal to GPIO2 Block
5	DATA IN1	Read/Write	Logic State of Input Signal to GPIO1 Block
4	DATA2	Read Only	Logic State of GPIO2 Pin
3	DATA1	Read Only	Logic State of GPIO1 Pin
2	NA	Read Only	Never Used, Always 0
1	NA	Read Only	Never Used, Always 0
0	NA	Read Only	Never Used, Always 0

Default State (MSB First): 011DD000

Note: The second and third bits of the data byte are used to write the data value of the two GPIOs. During a write operation, the five read only bits are ignored. During a read operation, bits 7 to 3 will be shifted onto the data bus, followed by three 0s. Also note that DATA2 and DATA IN2 are meaningless for the LTC4302-2 because there is no GPIO2 pin for that option.

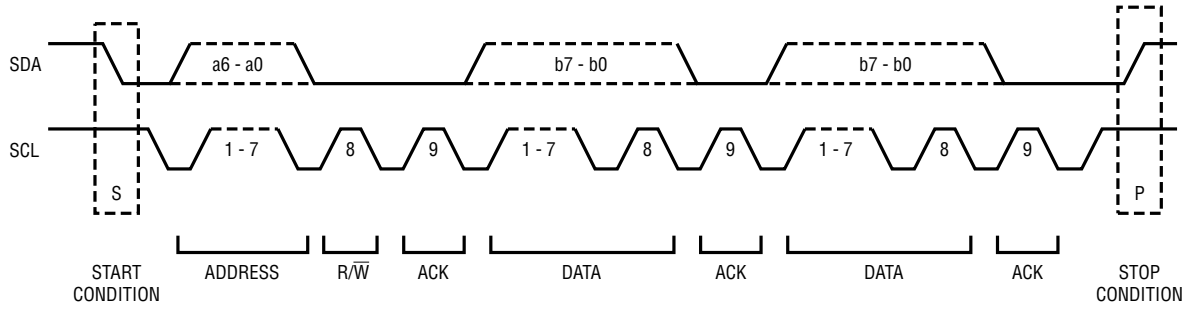


Figure 2. Data Transfer Over I²C or SMBus

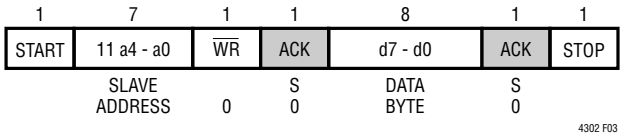


Figure 3. Writing One Byte Using Send Byte Protocol

OPERATION

Table 3. Register 2 Definition

BIT	NAME	TYPE	FUNCTION
7 (MSB)	DIR2	Read/Write	GPIO2 Mode; 0 = Output, 1 = Input*
6	DIR1	Read/Write	GPIO1 Mode; 0 = Output, 1 = Input
5	OUT CFG2	Read/Write	GPIO2 Output Mode; 0 = Open Drain, 1 = Push-Pull†*
4	OUT CFG1	Read/Write	GPIO1 Output Mode; 0 = Open Drain, 1 = Push-Pull†
3	OUTACC	Read/Write	Card Side Rise Time Accelerator Contol; 0 = Disabled, 1 = Active
2	INACC	Read/Write	Backplane Side Rise Time Accelerator Control; 0 = Disabled, 1 = Active
1	NA	Read Only	Never Used, Always 1
0	NA	Read Only	Never Used, Always 1

Default State (MSB First): 00000011

†OUT CFG1 has no effect when DIR1 = 1; OUT CFG2 has no effect when DIR2 = 1.

*DIR2 and OUT CFG2 apply only to the LTC4302-1; there is no GPIO2 for the LTC4302-2, so these bits are meaningless in this case.

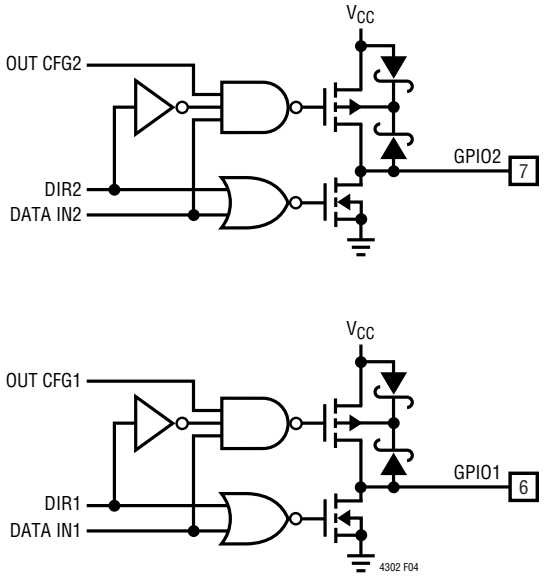


Figure 4. GPIO Circuits and Their Control Bits

protocol. After the first Data Byte, the master transmits a second Data Byte, followed by a Stop Bit. The bits of the second Data Byte are stored in the LTC4302's Register 2. Table 3 defines the functions of these control bits. The first 4 MSB's control the input/output configurations of the two GPIO pins. The next 2 bits control the enabling/disabling of the card side and backplane side rise time accelerators respectively. Since the LTC4302 -2 has only one GPIO pin, "DIR1" and "OUT CFG1" control its configuration, and "DIR2" and "OUT CFG2" are ignored. Figure 4 shows a schematic of the two GPIOs and the register bits that control their operation. The 2 LSB's are not used in Write operations.

The LTC4302 can also be written with two bytes using the SMBus Write Word protocol, as shown in Figure 6. The LTC4302 treats the first two bytes after the Address Byte (which the Write Word protocol refers to as "Command Code" and "Data Byte Low") as the two Data Bytes, and stores these bytes in Registers 1 and 2 respectively. After the master transmits the "Data Byte High" byte, the LTC4302 acknowledges reception of the byte but ignores the data contained therein.

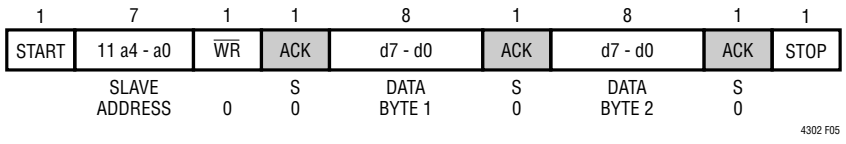


Figure 5. Writing Two Bytes

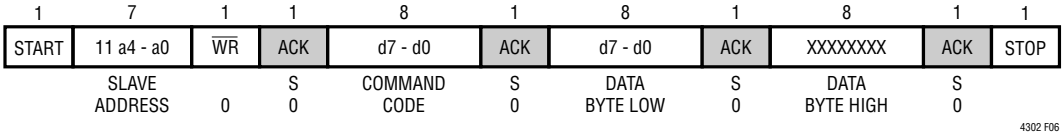


Figure 6. Writing Two Bytes Using SMBus Write Word Protocol

OPERATION

Data Transfer Timing for Write Commands

In order to help ensure that bad data is not written into the LTC4302, data from a write command is only stored after a valid Stop Bit has been performed. If a Start Bit occurs after new data bytes have been written but before a Stop Bit is issued, the new data bytes are lost. In this case, the master must readdress the part, rewrite the data bytes and issue a Stop Bit before issuing any Start Bits to properly update the registers. Also note that driving the CONN pin low asynchronously resets the registers to their default states, as specified in Tables 2 and 3. When CONN is driven back high, the registers remain in the default state.

Reading from the LTC4302

The LTC4302 can be read using three different formats, as shown in Figures 7 through 9. Each format begins with a Start Bit, followed by the Address Byte, as discussed above. The procedure for reading one data byte is given by the SMBus Receive Byte protocol, illustrated in Figure 7. The bits of the Data Byte are read from the LTC4302's Register 1. Table 2 defines the functions of these control bits. While only the first 3 bits of Register 1 can be written, the first 5 bits contain useful information to be read. The two added bits indicate the logic state of the GPIO pins. The 3 LSBs are not used and are always "000."

The format for reading two data bytes is shown in Figure 8. The Address Byte and first Data Byte are exactly the same as they are for the Receive Byte protocol. After the first Data Byte, the master transmits an Acknowledge indicating that it wants to read another data byte. The bits contained in Register 2 are then written onto the bus as "Data Byte 2." Table 3 defines the functions of these control bits. The 2 LSB's are not used and are always "11." The master signals a not acknowledge after the last byte read.

The SMBus Read Word protocol can also be used to read two bytes from the LTC4302, as shown in Figure 9. Note that the first Address Byte and the Command Code constitute a write operation. However, because these bytes are followed immediately by a Start Bit and not a Stop Bit, the data contained in the Command Code is not written into the LTC4302. After the second Start Bit, the format is exactly the same as shown in Figure 8.

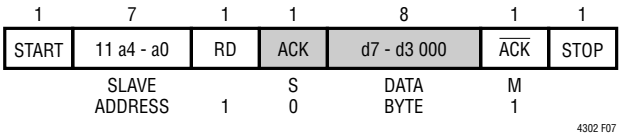


Figure 7. Reading One Byte Using Receive Byte Protocol

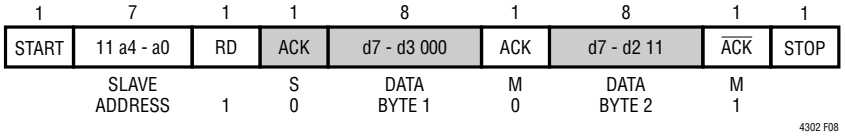


Figure 8. Reading Two Bytes

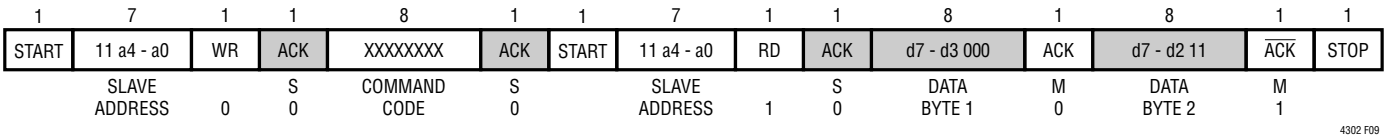


Figure 9. Reading Two Bytes Using SMBus Read Word Protocol

OPERATION

Connection Circuitry

Masters on the SDAIN and SCLIN busses can address the LTC4302 and command it to connect SDAIN to SDAOUT and SCLIN to SCLOUT as described in the "Write One or Two Bytes" section. Once this connection occurs, masters on the card are then able to read from and write to the part via the SDAOUT and SCLOUT pins. However, whenever the two sides are disconnected, the command to reconnect must come from SDAIN and SCLIN.

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. Masters must pull the bus voltages below 0.4V worst-case with respect to the LTC4302's ground pin to ensure proper operation. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT busses force a high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are connected to the LTC4302.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and the card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different from the corresponding card bus waveforms.

Input-to-Output Offset Voltage

When a logic low voltage, V_{LOW1} is driven on any of the LTC4302's data or clock pins, the LTC4302 regulates the voltage on the other side (V_{LOW2}) to a slightly higher voltage, as directed by the following equation:

$$V_{LOW2}\ (typical) = V_{LOW1} + 75mV + (V_{BUS}/R) \bullet 70\Omega$$

where R is the bus pull-up resistance on V_{LOW2} in ohms and V_{BUS} is the supply voltage to which R is connected. For example, if a device is forcing SDAOUT to 10mV, and if V_{CC} = 3.3V and the pull-up resistor R on SDAIN is 10k, then the voltage on SDAIN = 10mV + 75mV + (3.3V/10k) • 70Ω = 108mV (typical). See the Typical Performance Characteristics section for curves showing the offset voltage as a function of V_{CC} and R.

Propagation Delays

During a rising edge, the rise time on each side is determined by the combined pull-up current of the LTC4302 boost current and the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise time occurs that is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 10 for V_{CC} = 3.3V and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective t_{PLH} is negative.

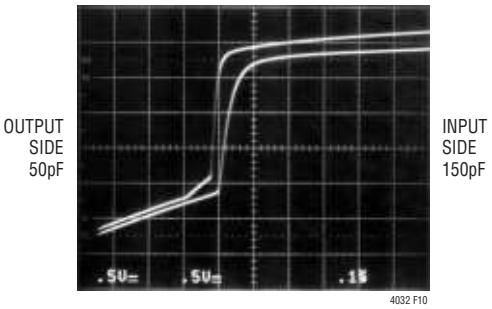


Figure 10. Input-Output Connection t_{PLH}

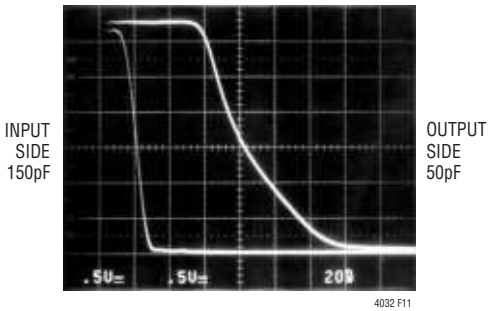


Figure 11. Input-Output Connection t_{PHL}

There is a finite propagation delay, t_{PHL}, through the connection circuitry for falling waveforms. Figure 11 shows the falling waveforms for the same V_{CC}, pull-up resistors and equivalent capacitance conditions used in Figure 10. An external N-Channel MOSFET device pulls down the voltage on the side with 150pF capacitance; the LTC4302

OPERATION

pulls down the voltage on the 50pF side with a delay of 55ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows t_{PHL} as a function of temperature and voltage for 10k pull-up resistors and 100pF equivalent bus capacitance on both sides of the part. Larger output capacitances translate to longer delays (up to 150ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

General Purpose Input/Outputs (GPIOs)

The LTC4302-1 provides two general purpose input/output pins (GPIOs) that can be configured as inputs, open-drain outputs or push-pull outputs. In push-pull mode, at V_{CC} = 2.7V, the typical pull-up impedance is 670Ω and the typical pull-down impedance is 35Ω, making the GPIO pull-downs capable of driving LEDs. The user must take care to minimize the power dissipation in the pulldown device. LEDs should have series resistors added to limit current and the voltage drop across the internal pulldown if their forward drop is less than about V_{CC}-0.7V. Pullup resistors should be sized to allow the internal pulldowns to pull the GPIO pins below 0.7V. In open-drain output mode, the user provides the logic high by connecting a resistor to an external supply voltage. The external supply voltage can range from 2.2V to 5.5V independent of the V_{CC} voltage.

The LTC4302-2 replaces one GPIO pin with a V_{CC2} pin and provides only one GPIO.

Rise Time Accelerators

Rise time accelerator circuits on all four SDA and SCL pins allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise time requirements. A master on the bus may activate the accelerators on the backplane side, the card side, neither or both, by writing the LTC4302's registers as described above. When activated, the accelerators switch in 2mA of current at V_{CC} = 2.7V and 9mA at V_{CC} = 5.5V during positive bus transitions to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6V and the initial rise rate on the pin exceeds 0.8V/µs. Using a general rule of 20pF of capacitance for every device on the bus (10pF for the device and 10pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 0.8V/µs to guarantee activation of the accelerators.

For example, assume an SMBus system with V_{CC} = 3.3V, a 10k pull-up resistor and equivalent bus capacitor of 200pF. The rise time of an SMBus system is calculated from ($V_{IL(MAX)}$ – 0.15V) to ($V_{IH(MIN)}$ + 0.15V) or 0.65V to 2.25V. It takes an RC circuit 0.92 time constants to traverse this voltage for a 3.3V supply; in this case, 0.92 • (10k • 200pF) = 1.84µs. Thus, the system exceeds the maximum allowed rise time of 1µs by 84%. However, using the rise time accelerators, which are activated at a DC threshold below 0.65V, the worst-case rise time is (2.25V – 0.65V) • 200pF/1mA = 320ns, which meets the 1µs rise time requirement.

CONN Register Reset

Grounding CONN resets the registers to their default state as specified in Tables 2 and 3. In the default state, the backplane side is disconnected from the card side, the rise time accelerators are disabled and the GPIOs are set in open-drain output mode with the N-Channel MOSFET open-drain pulldown turned off. Connecting a weak resistor from CONN to ground on the I/O card and using a staggered connector with CONN connecting to the shortest pin guarantee glitch-free live board insertion and removal. When the CONN voltage is brought back to V_{CC} the registers remain in the default state and can then be read or written to.

OPERATION

Glitch Filters

The LTC4302 provides glitch filters on both the SDAIN and SCLIN signals as required by the I^2C Fast Mode (400kHz) specification. The filters prevent signals of up to 50ns (minimum) time duration and rail-to-rail voltage magnitude from passing into the 2-wire bus digital interface circuitry.

Fall Time Control

Per the I^2C Fast Mode (400kHz) specification, the 2-wire bus digital interface circuitry provides fall time control when forcing logic lows onto the SDAIN bus. The fall time always meets the limits:

$$(20 + 0.1 \bullet C_B) < t_f < 300ns$$

where t_f is the fall time in ns and C_B is the equivalent capacitance on SDAIN in pF. Whenever the connection circuitry is passing logic lows from SDAOUT to SDAIN (and vice versa), its output signal will meet the fall time requirements, provided that its input signal meets the fall time requirements.

APPLICATIONS INFORMATION

Live Insertion and Removal, Capacitance Buffering

The application shown in Figure 12 highlights the live insertion and removal, and capacitance buffering features of the LTC4302. Note that if the I/O card were plugged directly into the backplane, the card capacitance would add directly to the backplane capacitance making rise and fall time requirements difficult to meet. Placing a LTC4302 on the edge of the card, however, isolates the card capacitance from the backplane. The LTC4302 drives the capacitance of everything on the card, and the backplane must drive only the capacitance of the LTC4302, which is less than 10pF.

Assuming that a staggered connector is available, make ground, V_{CC} and V_{CC2} the longest pins to guarantee that SDAIN and SCLIN receive the 1V precharge voltage before they connect. Make SDAIN and SCLIN medium length pins to ensure that they are firmly connected while CONN is low. Make CONN the shortest pin and connect a weak resistor from CONN to ground on the I/O card. This ensures that the LTC4302-1/LTC4302-2 remain in a high impedance state while SDAIN and SCLIN are making connection during live insertion. During live removal, having CONN disconnect first ensures that the LTC4302 enters a high impedance state in a controlled manner before SDAIN and SCLIN disconnect. Owing to the fact that the LTC4302 powers into a high impedance state, and also owing to the 1V precharge voltage and the less than 10pF pin capacitance, SDAIN and SCLIN cause minimal disturbance on the backplane busses when they make contact with the connector.

Address Expansion with Nested Addressing

Figure 13 illustrates how the LTC4302 can be used to expand the number of devices in a system by using nested addressing. Note that each I/O card contains a sensor device having address 1111 111. If the two cards are plugged directly into the backplane, the two sensors will require two different addresses. However, each LTC4302 isolates the devices on its card from the rest of the system until it is commanded to connect. If masters use the LTC4302s to connect only one I/O card at a time, then each I/O card can have a device with address 1111 111 and no problems will occur.

APPLICATIONS INFORMATION

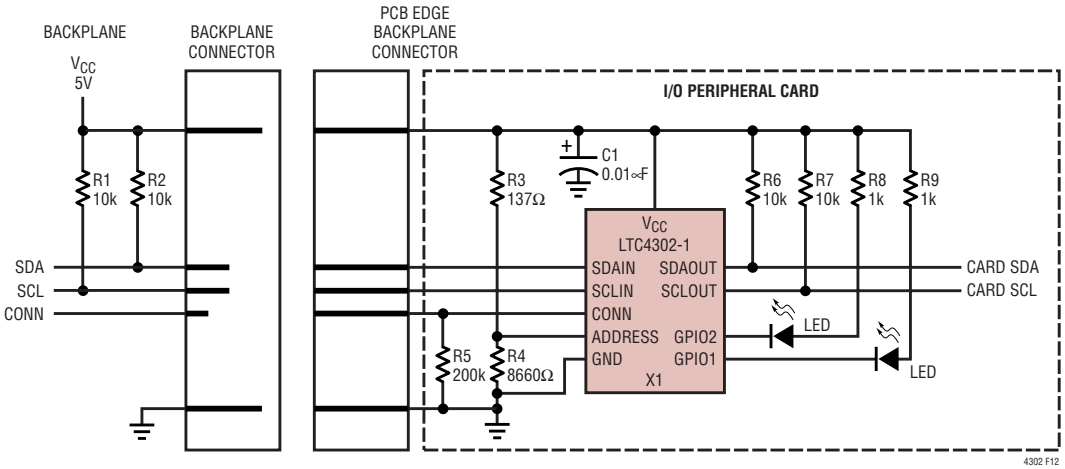


Figure 12. LTC4302-1 in a Live Insertion and Capacitance Buffering Application

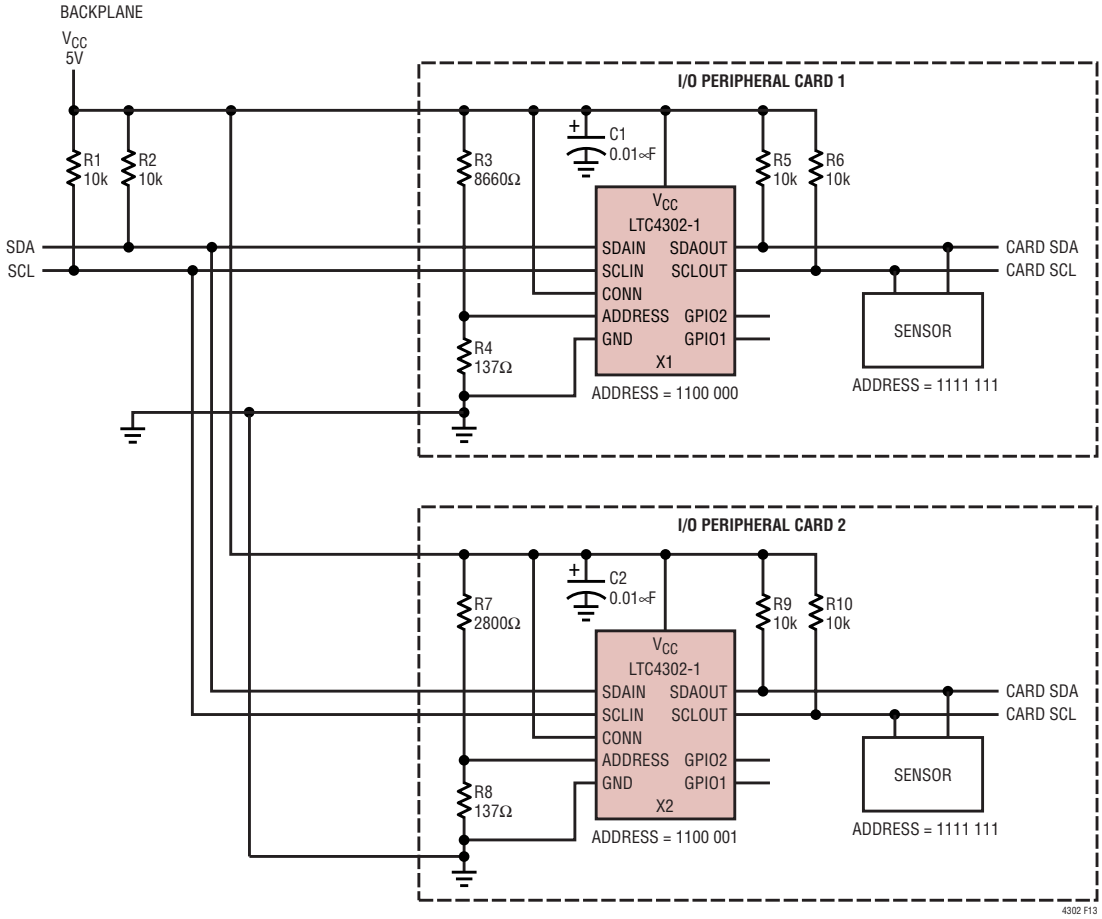


Figure 13. LTC4302-1 in a Nested Addressing Application

APPLICATIONS INFORMATION

5V to 3.3V Level Translator and Power Supply Redundancy (LTC4302-2)

Systems requiring different supply voltages for the backplane side and the card side can use the LTC4302-2 as shown in Figure 14. The pull-up resistors on the card side connect from SDAOUT and SCLOUT to V_{CC2} and those on the backplane side connect from SDAIN and SCLIN to V_{CC}. The LTC4302-2 functions for voltages ranging from 2.7V to 5.5V on both V_{CC} and V_{CC2}. There is no constraint on the voltage magnitudes of V_{CC} and V_{CC2} with respect to each other.

This application also provides power supply redundancy. If either the V_{CC} or V_{CC2} supply voltage falls below its UVLO threshold, the LTC4302-2 disconnects the backplane from the card so that the side that is still powered can continue to function.

Systems with Supply Voltage Droop (LTC4302-1)

In large 2-wire systems, the V_{CC} voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is modelled by a series resistor in the V_{CC} line as shown in Figure 15. For proper operation of the LTC4302-1, make sure that $V_{CC(BUS)} \geq V_{CC(LTC4302)} - 0.5V$.

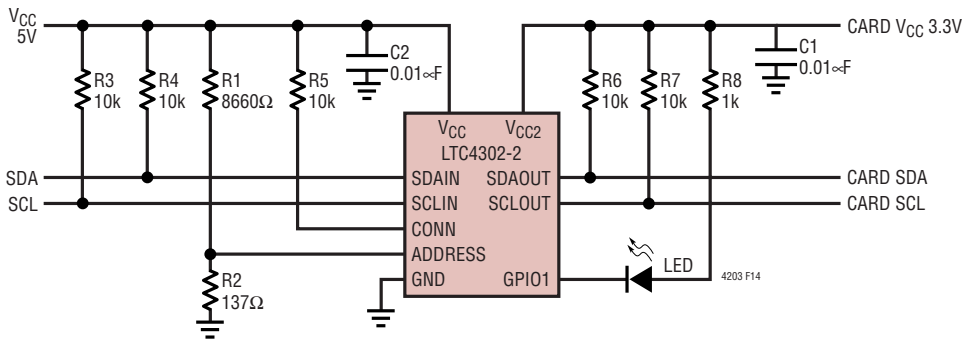


Figure 14. 5V to 3.3V Level Translator Application

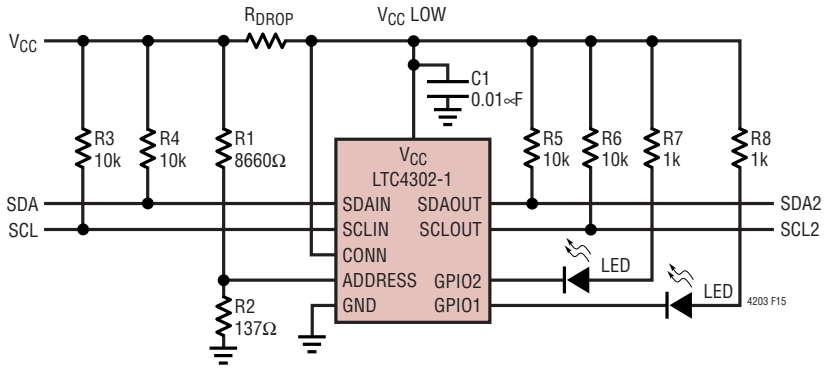


Figure 15. System with Supply Voltage Droop

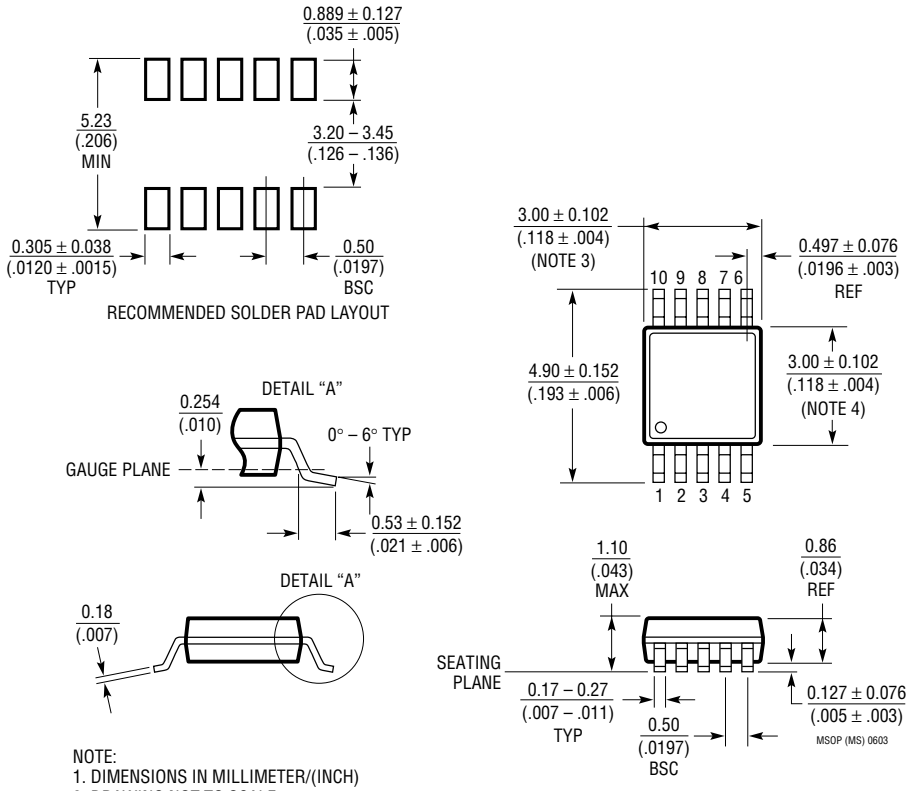
APPLICATIONS INFORMATION

Repeater/Bus Extender Application

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two LTC4302-1s back-to-back as shown in Figure 16. The I^2C specification allows for 400pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance; however, the limited impedances of devices connected to the bus require systems to remain small, if rise and fall time specifications are to be met. The strong pull-up and pull-down impedances of the LTC4302-1 are capable of meeting rise and fall time specifications for up to 1nF of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back LTC4302-1's add together, directly contributing to the same problem.

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

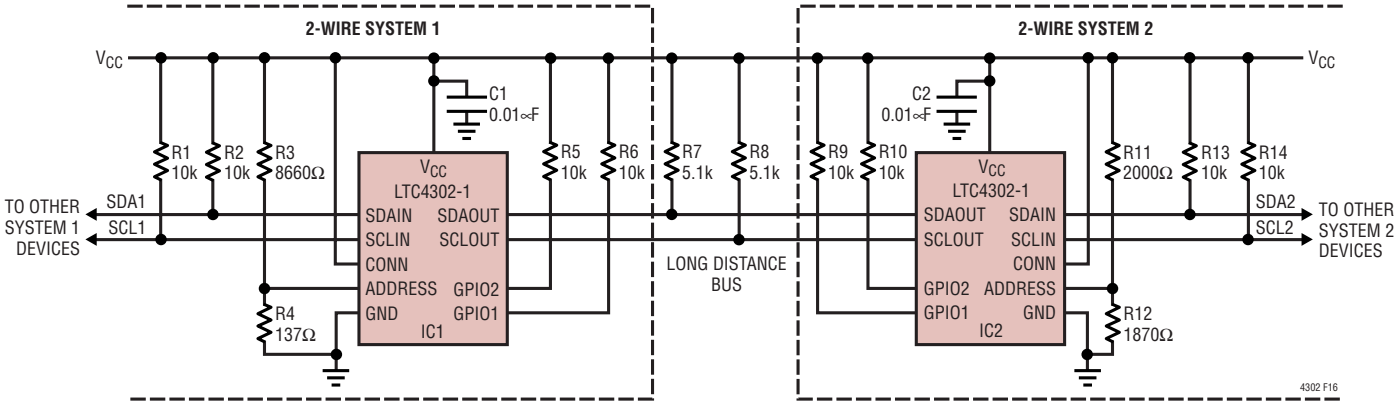


Figure 16. Repeater/Bus Extender Application

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface	Low R_{ON}: 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50µA ±2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16-Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LSB Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I²C Rise-Time, Ensures Data Integrity with Multiple SMBus/I²C Devices
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1695	SMBus/I²C Fan Speed Controller in ThinSOT™	0.75Ω PMOS 180mA Regulator, 6-Bit DAC
LTC1840	Dual I²C Fan Speed Controller	Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO
LTC4300A-1/ LTC4300A-2	Hot Swappable 2-Wire Bus Buffers	Provides Capacitance Buffering, SDA and SCL Hot Swapping, Level Shifting

ThinSOT is a trademark of Linear Technology Corporation.

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