14-Bit, 800ksps Sampling A/D Converter with Shutdown

FEATURES

- **Sample Rate: 800ksps**
- **Power Dissipation: 150mW**
- **81.5dB S/(N + D) and 93dB THD**
- **No Missing Codes**
- **No Pipeline Delay**
- Nap and Sleep Shutdown Modes
- Operates with 2.5V Internal 15ppm/°C Reference or External Reference
- True Differential Inputs Reject Common Mode Noise
- 20MHz Full-Power Bandwidth Sampling
- Bipolar Input Range: ±2.5V
- 28-Pin SSOP and SO Packages

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

DESCRIPTION

The LTC®1419 is a 1µs, 800ksps, 14-bit sampling A/D converter that draws only 150mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold and a precision reference. Two digitally selectable power shutdown modes provide flexibility for low power systems.

The LTC1419 has a full-scale input range of ±2.5V. Outstanding AC performance includes 81.5dB S/(N + D) and 93dB THD with a 100kHz input; 80dB S/(N + D) and 86dB THD at the Nyquist input frequency of 400kHz.

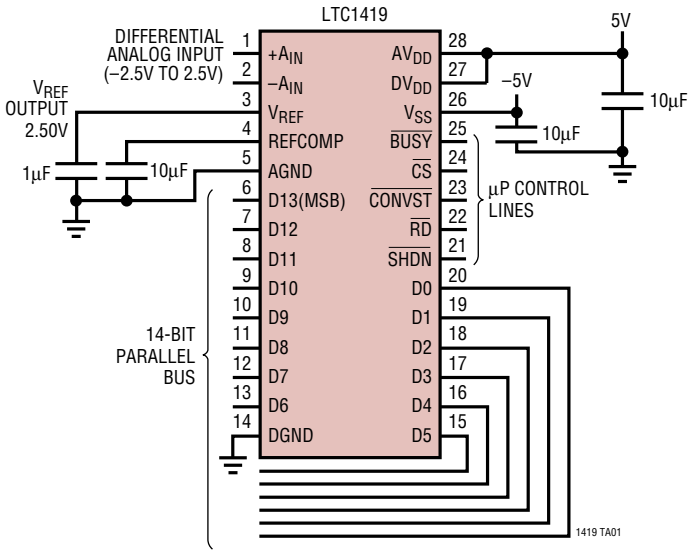
The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The ADC has a µP compatible, 14-bit parallel output port. There is no pipeline delay in the conversion results. A separate convert start input and data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

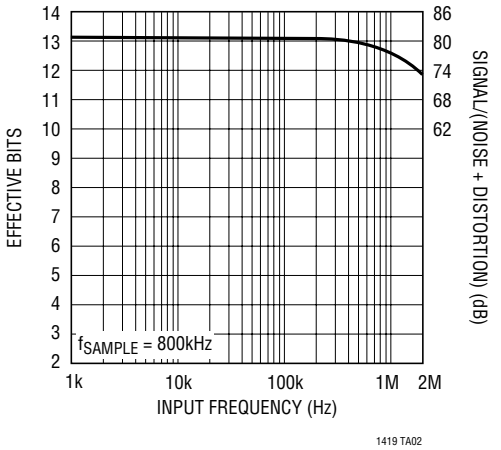
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TYPICAL APPLICATION

800kHz, 14-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

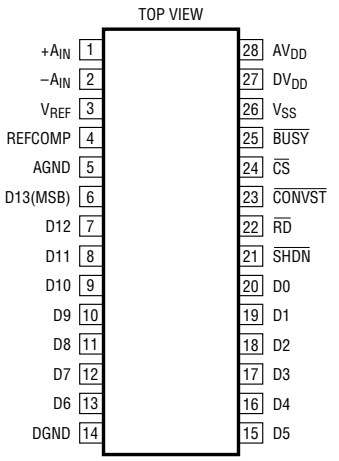


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = V_{DD} = DV_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) ..... (V_{SS} – 0.3V) to 10V
Digital Output Voltage ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC1419C ..... 0°C to 70°C
LTC1419I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

SW PACKAGE
28-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER

LTC1419ACG
LTC1419ACSW
LTC1419AIG
LTC1419AISW
LTC1419CG
LTC1419CSW
LTC1419IG
LTC1419ISW

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1419 MIN	LTC1419 TYP	LTC1419 MAX	LTC1419A MIN	LTC1419A TYP	LTC1419A MAX	UNITS
Resolution (No Missing Codes)		●	13			14			Bits
Integral Linearity Error	(Note 7)	●		±0.8	±2		±0.6	±1.25	LSB
Differential Linearity Error		●		±0.7	±1.5		±0.5	±1	LSB
Offset Error	(Note 8)	●		±5	±20		±5	±20	LSB
Full-Scale Error	Internal Reference External Reference = 2.5V			±10 ±5	±60		±10 ±5	±60	LSB LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0			±15			±15		ppm/°C

ANALOG INPUT

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25 ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			15 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		90	300	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				2		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (–A_{IN} = A_{IN}) < 2.5V			60		dB

DYNAMIC ACCURACY

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	100kHz Input Signal 390kHz Input Signal	●	78	81.5 80.0		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics 390kHz Input Signal, First 5 Harmonics	●		–93 –86	–86	dB dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal	●		–95	–86	dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–86		dB
	Full-Power Bandwidth				20		MHz
	Full-Linear Bandwidth	S/(N + D) ≥ 77dB			1		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0		±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V, –5.25 ≤ V_{SS} ≤ –4.75V		0.05		LSB/V
V_{REF} Output Resistance	–0.1mA ≤ $\lvert I_{OUT} \rvert$ ≤ 0.1mA		2		kΩ
REFCOMP Output Voltage	I_{OUT} = 0		4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V I_O = –10µA I_O = –200µA	 ●	 4.0	 4.5 	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●	 	 0.05 0.10	 0.4	 V V
I_{OZ}	Hi-Z Output Leakage D13 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D13 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 10)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current Nap Mode Sleep Mode	 $\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V $\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V	●		11 1.5 250	20	mA mA µA
I_{SS}	Negative Supply Current Nap Mode Sleep Mode	 $\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V $\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V	●		19 100 1	30	mA µA µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
P_{DIS}	Power Dissipation		●		150	240	mW
	Nap Mode	$\overline{SHDN}$ = 0V, $\overline{CS}$ = 0V			7.5	12	mW
	Sleep Mode	$\overline{SHDN}$ = 0V, $\overline{CS}$ = 5V			1.2		mW

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	800			kHz
t_{CONV}	Conversion Time		●		950	1150	ns
t_{ACQ}	Acquisition Time		●		90	300	ns
$t_{ACQ + CONV}$	Acquisition + Conversion Time		●		1040	1250	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	40			ns
t_3	$\overline{CS}\downarrow$ to $\overline{SHDN}\downarrow$ Setup Time	(Notes 9, 10)		40			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(Note 10)			400		ns
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			20		ns
			●			50	ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$			20	50		ns
			●	15			ns
t_8	Delay Between Conversions	(Note 10)	●	40			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	(Note 9)	●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF			15	25	ns
			●			35	ns
		C_L = 100pF			20	35	ns
			●			50	ns
t_{11}	Bus Relinquish Time				10	20	ns
		0°C ≤ T_A ≤ 70°C	●			25	ns
		–40°C ≤ T_A ≤ 85°C	●			30	ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	40			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliabilty and lifetime.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SAMPLE} = 800kHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended $+A_{IN}$ input with $-A_{IN}$ grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.

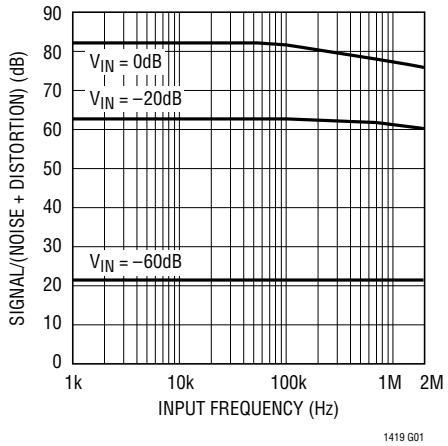
Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

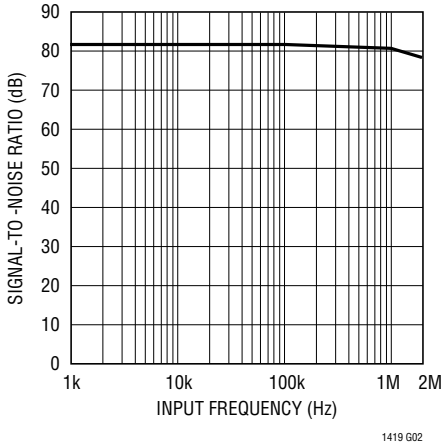
Note 11: The falling edge of CONVST starts a conversion. If CONVST returns high at a critical point during the conversion it can create small errors. For best performance ensure that CONVST returns high either within 650ns after the start of the conversion or after BUSY rises.

TYPICAL PERFORMANCE CHARACTERISTICS

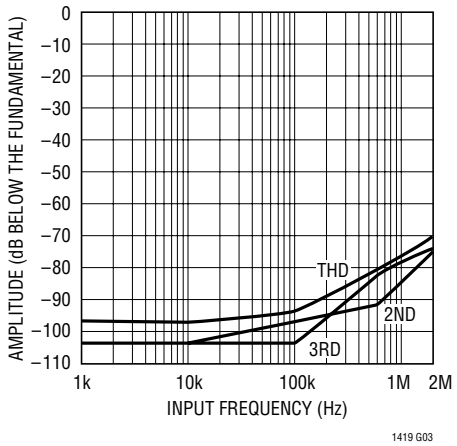
S/(N + D) vs Input Frequency and Amplitude



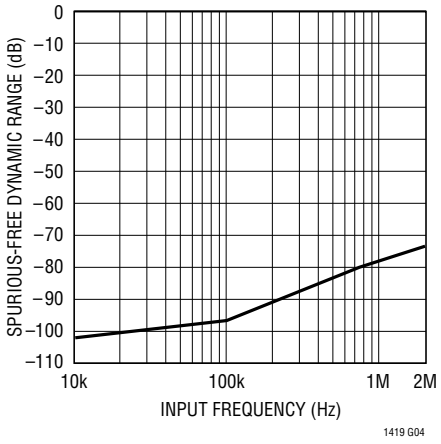
Signal-to-Noise Ratio vs Input Frequency



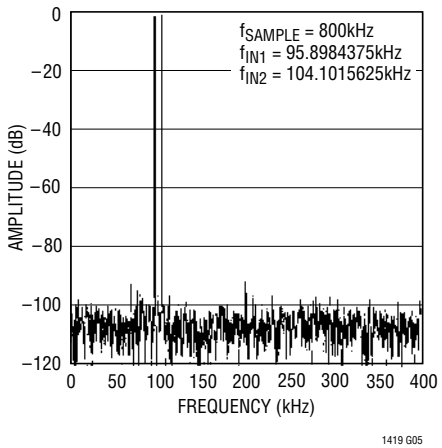
Distortion vs Input Frequency



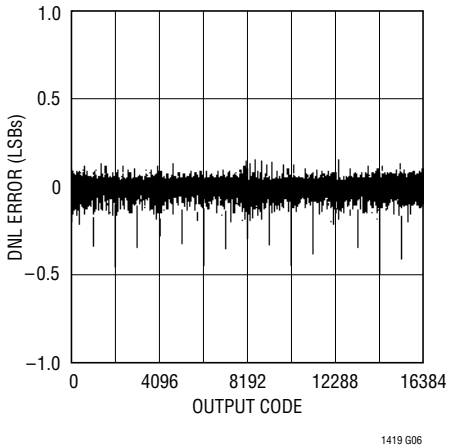
Spurious-Free Dynamic Range vs Input Frequency



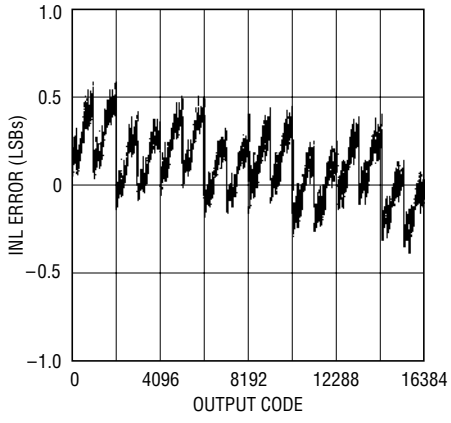
Intermodulation Distortion Plot



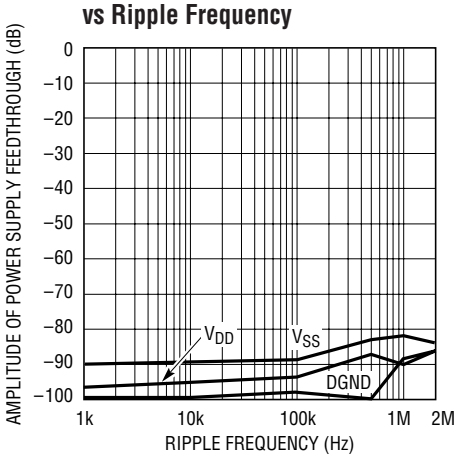
Differential Nonlinearity vs Output Code



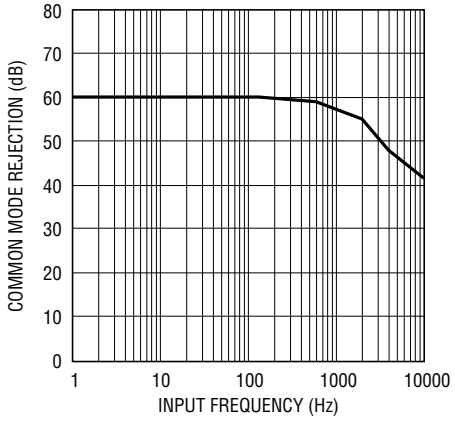
Integral Nonlinearity vs Output Code



Power Supply Feedthrough vs Ripple Frequency



Input Common Mode Rejection vs Input Frequency



PIN FUNCTIONS

+A_{IN} (Pin 1): ±2.5V Positive Analog Input.

–A_{IN} (Pin 2): ±2.5V Negative Analog Input.

V_{REF} (Pin 3): 2.5V Reference Output. Bypass to AGND with 1µF.

REFCOMP (Pin 4): 4.06V Reference Output. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

AGND (Pin 5): Analog Ground.

D13 to D6 (Pins 6 to 13): Three-State Data Outputs. The output format is 2's complement.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D5 to D0 (Pins 15 to 20): Three-State Data Outputs. The output format is 2's complement.

$\overline{SHDN}$ (Pin 21): Power Shutdown Input. Low selects shutdown. Shutdown mode selected by $\overline{CS}$. $\overline{CS}$ = 0 for nap mode and $\overline{CS}$ = 1 for sleep mode.

$\overline{RD}$ (Pin 22): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CONVST}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

$\overline{CS}$ (Pin 24): Chip Select. The input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs. $\overline{CS}$ also sets the shutdown mode when $\overline{SHDN}$ goes low. $\overline{CS}$ and $\overline{SHDN}$ low select the quick wake-up nap mode. $\overline{CS}$ high and $\overline{SHDN}$ low select sleep mode.

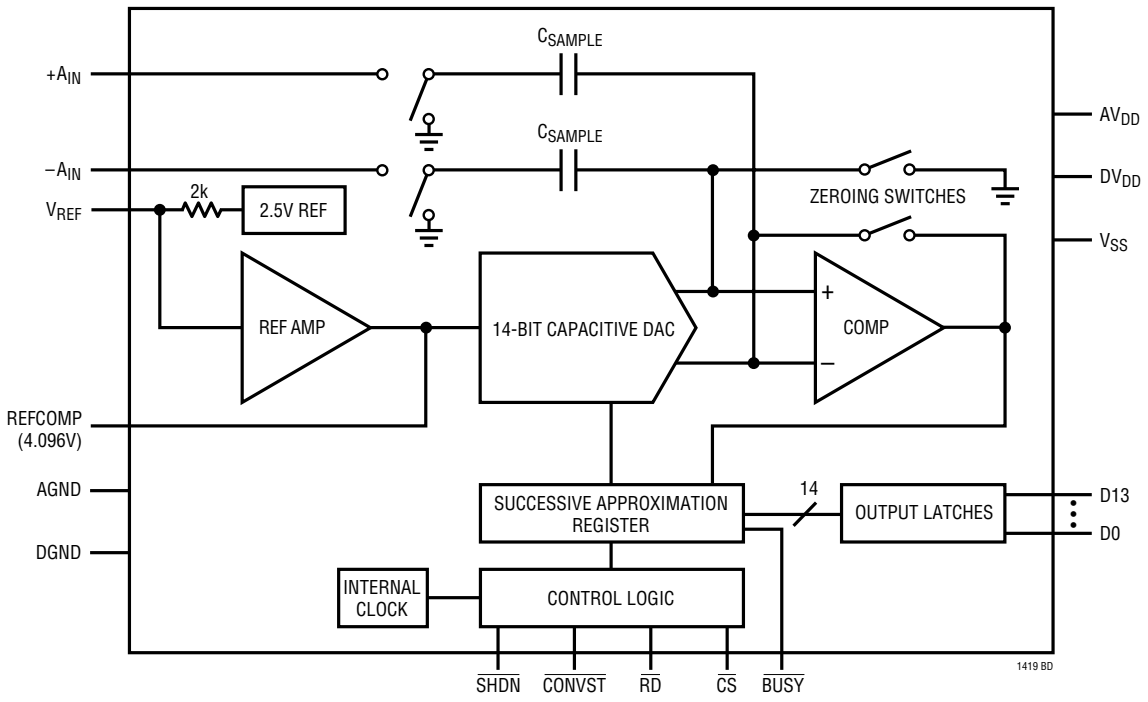
$\overline{BUSY}$ (Pin 25): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{BUSY}$.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to Pin 28.

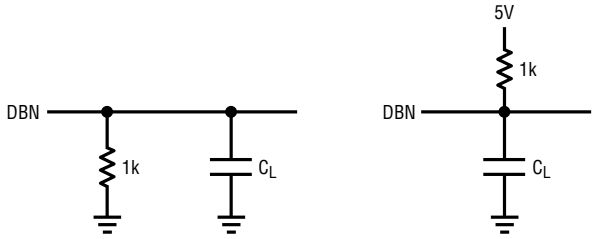
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

FUNCTIONAL BLOCK DIAGRAM

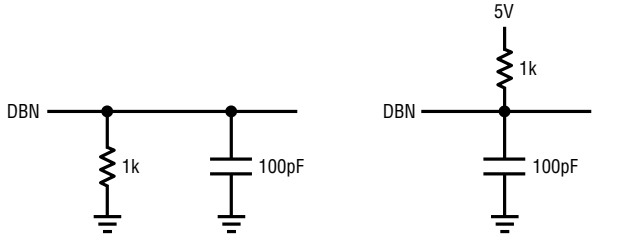


TEST CIRCUITS

Load Circuits for Access Timing



Load Circuits for Output Float Delay



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1419 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 14-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs (please refer to Digital Interface section for the data format).

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion, the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

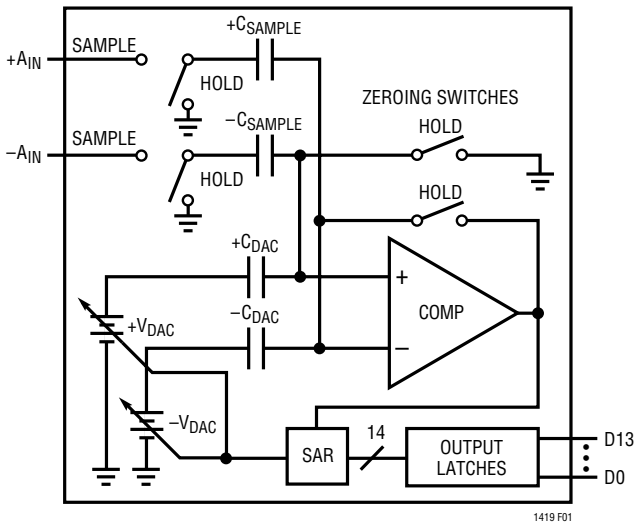


Figure 1. Simplified Block Diagram

During the conversion, the internal differential 14-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the $+A_{IN}$ and $-A_{IN}$ inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 200ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase, the comparator zeroing switches open, putting the comparator into compare mode. The input switches the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the $+A_{IN}$ and $-A_{IN}$ input charges. The SAR contents (a 14-bit data word) which represents the difference of $+A_{IN}$ and $-A_{IN}$ are loaded into the 14-bit output latches.

DYNAMIC PERFORMANCE

The LTC1419 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for

APPLICATIONS INFORMATION

frequencies outside the fundamental. Figure 2 shows a typical LTC1419 FFT plot.

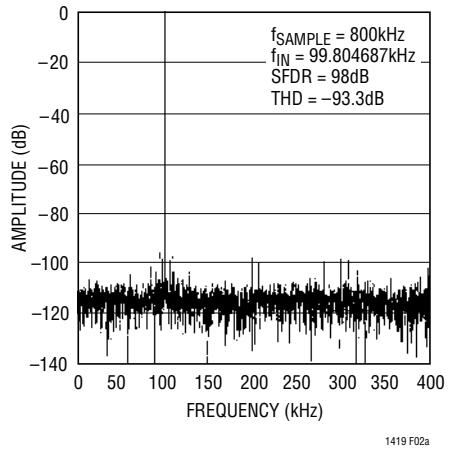


Figure 2a. LTC1419 Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz

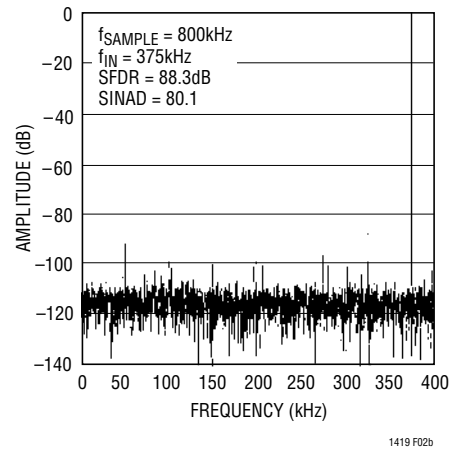


Figure 2b. LTC1419 Nonaveraged, 4096 Point FFT, Input Frequency = 375kHz

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 800kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist limit of 400kHz.

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 800kHz, the LTC1419 maintains near ideal ENOBs up to the Nyquist input frequency of 400kHz (refer to Figure 3).

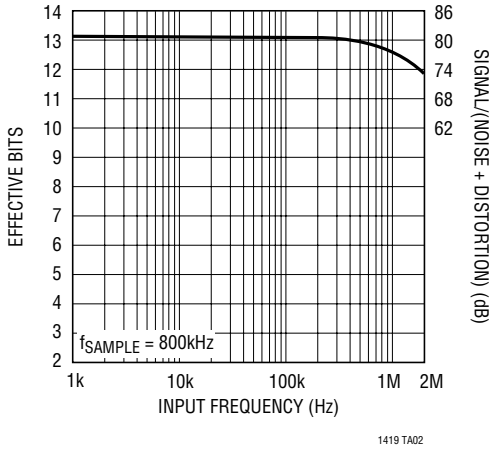


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs Input Frequency is shown in Figure 4. The LTC1419 has good distortion performance up to the Nyquist frequency and beyond.

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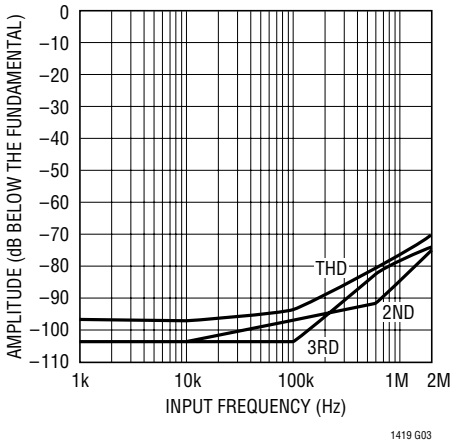


Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ±nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(fa+fb) = 20Log\frac{\text{Amplitude at } (fa+fb)}{\text{Amplitude at fa}}$$

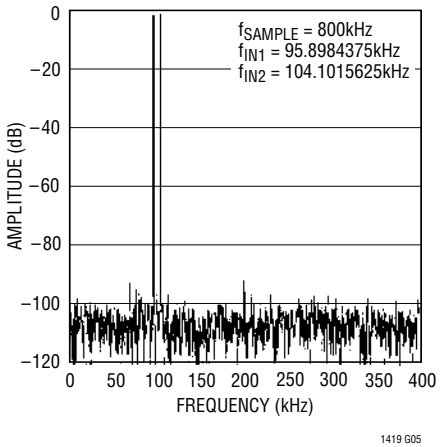


Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 77dB (12.5 effective bits). The LTC1419 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the LTC1419 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $-A_{IN}$ input is grounded). The $+A_{IN}$ and $-A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1419 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is

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that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 200ns for full throughput rate).

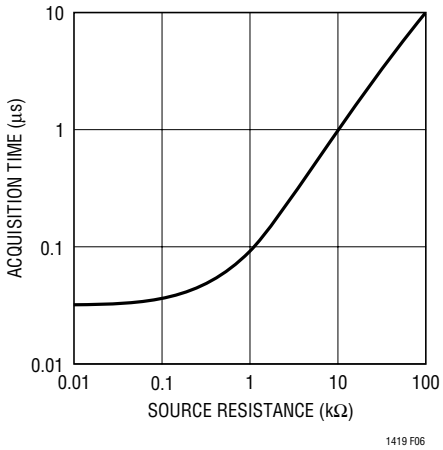


Figure 6. t_{ACQ} vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1419 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1419. More detailed information is available in the Linear Technology databooks, the LinearView™ CD-ROM and on our web site at www.linear-tech. com.

LinearView is a trademark of Linear Technology Corporation.

LT®1220: 30MHz unity-gain bandwidth voltage feedback amplifier. ±5V to ±15V supplies. Excellent DC specifications.

LT1223: 100MHz video current feedback amplifier. ±5V to ±15V supplies, 6mA supply current. Low distortion at frequencies above 400kHz. Low noise. Good for AC applications.

LT1227: 140MHz video current feedback amplifier. ±5V to ±15V supplies, 10mA supply current. Lowest distortion at frequencies above 400kHz. Low noise. Best for AC applications.

LT1229/LT1230: Dual/quad 100MHz current feedback amplifiers. ±2V to ±15V supplies, 6mA supply current each amplifier. Low noise. Good AC specs.

LT1360: 50MHz voltage feedback amplifier. ±5V to ±15V supplies, 3.8mA supply current. Good AC and DC specs.

LT1363: 70MHz, 1000V/µs op amps, 6.3mA supply current. Good AC and DC specs.

LT1364/LT1365: Dual and quad 70MHz, 1000V/µs op amps. 6.3mA supply current per amplifier.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1419 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for

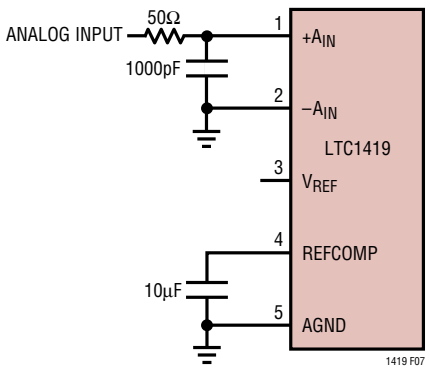


Figure 7. RC Input Filter

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many applications. For example, Figure 7 shows a 1000pF capacitor from +A_{IN} to ground and a 100Ω source resistor to limit the input bandwidth to 1.6MHz. The 1000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Range

The ±2.5V input range of the LTC1419 is optimized for low noise and low distortion. Most op amps also perform well over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1419 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The LTC1419 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3) see Figure 8a. A

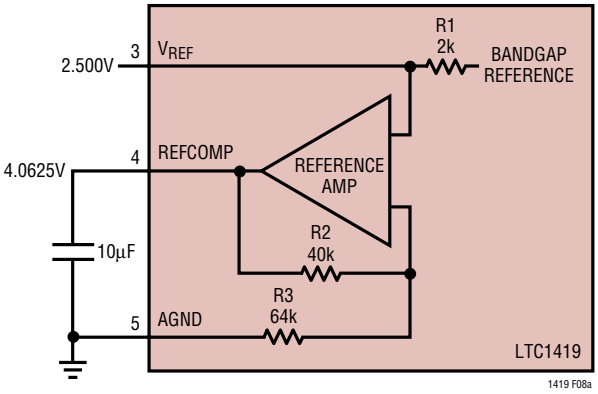


Figure 8a. LTC1419 Reference Circuit

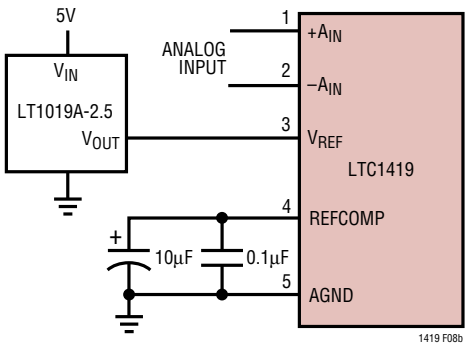


Figure 8b. Using the LT1019-2.5 as an External Reference

2k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry, see Figure 8b. The reference amplifier gains the voltage at the V_{REF} pin by 1.625 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin (REFCOMP, Pin 4) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or 10µF tantalum in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means shown in Figure 9. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1419 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed for after a reference adjustment.

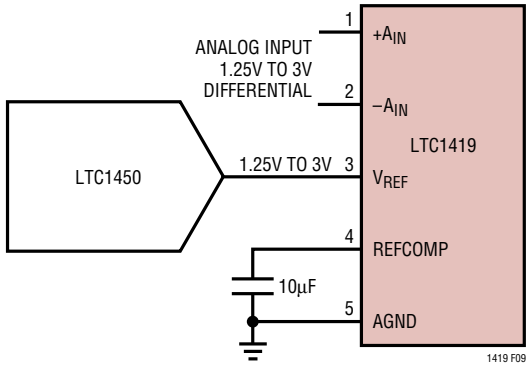


Figure 9. Driving V_{REF} with a DAC

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Differential Inputs

The LTC1419 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $+A_{IN} - (-A_{IN})$ independent of the common mode voltage (see Figure 11a). The common mode rejection holds up to extremely high frequencies, see Figure 10a. The only requirement is that both inputs can not exceed the AV_{DD} or AV_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common mode voltage. THD will degrade as the inputs approach either power supply rail, from 86dB with a common mode of 0V to 76dB with a common mode of 2.5V or –2.5V.

Differential inputs allow greater flexibility for accepting different input ranges. Figure 10b shows a circuit that converts a 0V to 5V analog input signal with only an additional buffer that is not in the signal path.

Full-Scale and Offset Adjustment

Figure 11a shows the ideal input/output characteristics for the LTC1419. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB,... FS – 1.5LSB, FS – 0.5LSB). The output is two's complement binary with 1LSB = FS – (–FS)/16384 = 5V/16384 = 305.2µV.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset

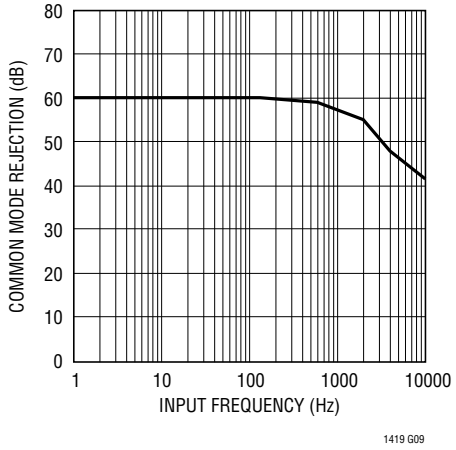


Figure 10a. CMRR vs Input Frequency

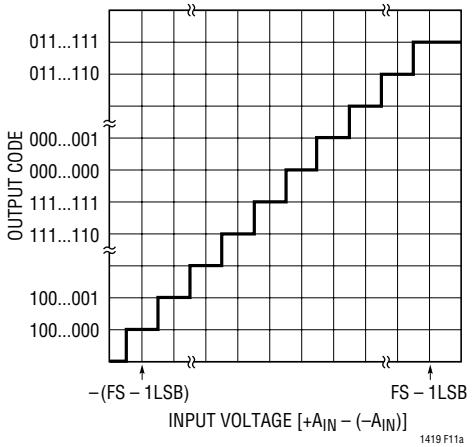


Figure 11a. LTC1419 Transfer Characteristics

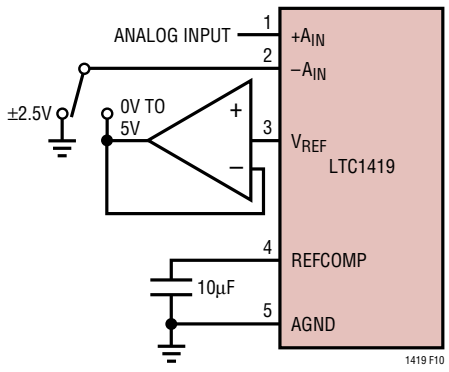


Figure 10b. Selectable 0V to 5V or ±2.5V Input Range

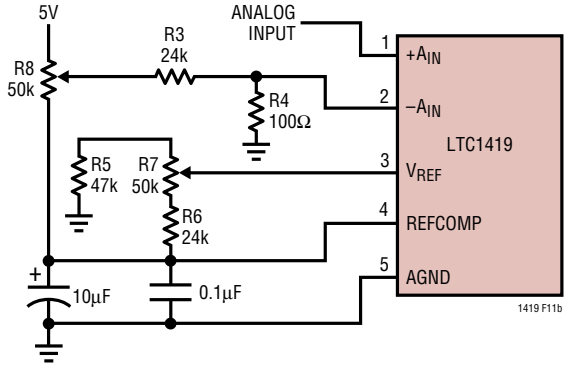


Figure 11b. Offset and Full-Scale Adjust Circuit

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applied to the $-A_{IN}$ input. For zero offset error, apply $-152\mu V$ (i.e., $-0.5LSB$) at $+A_{IN}$ and adjust the offset at the $-A_{IN}$ input until the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 2.499544V (FS/2 – 1.5LSBs) is applied to $+A_{IN}$ and R2 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.

BOARD LAYOUT AND GROUNDING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1419, a printed circuit board with ground plane is required. Layout should ensure that digital and analog signal lines are separated as much as possible. Particular care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.The analog input should be screened by AGND.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND), Pin 14 and Pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1419 has differential inputs to minimize noise coupling. Common mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the LTC1419 will hold and convert the difference voltage between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (Pin 1) and $-A_{IN}$ (Pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side by side to equalize coupling.

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins as shown in the Typical Application on the fist page of this data sheet. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively, 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Example Layout

Figures 13a, 13b, 13c and 13d show the schematic and layout of a suggested evaluation board. The layout demonstrates the proper use of decoupling capacitors and ground plane with a 2-layer printed circuit board.

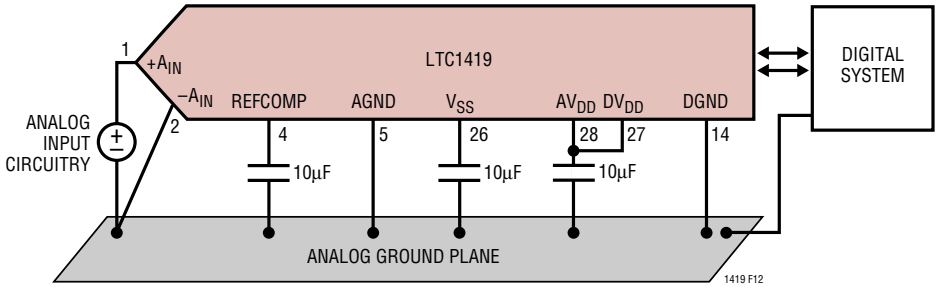


Figure 12. Power Supply Grounding Practice

APPLICATIONS INFORMATION

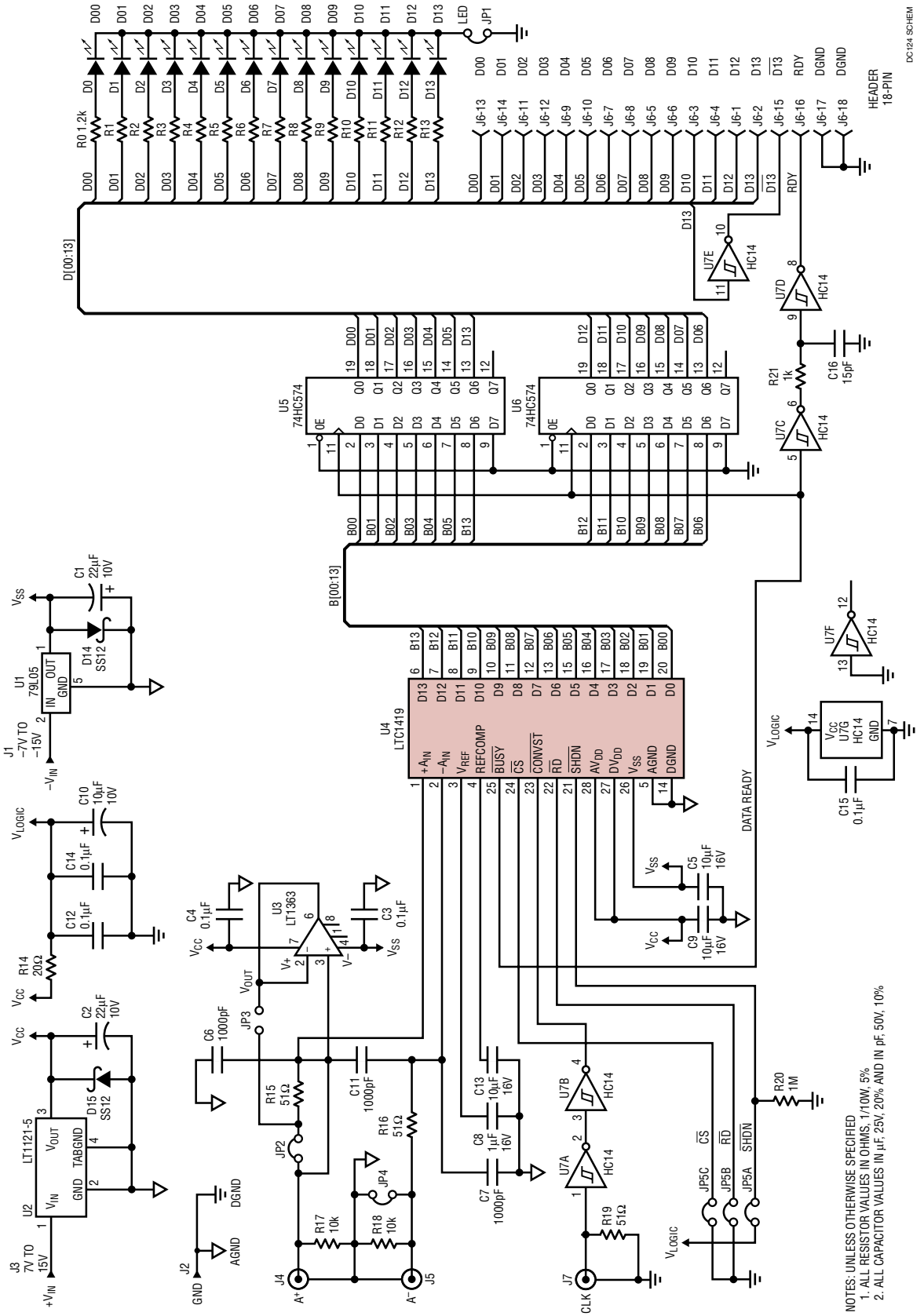


Figure 13a. Suggested Evaluation Circuit Schematic

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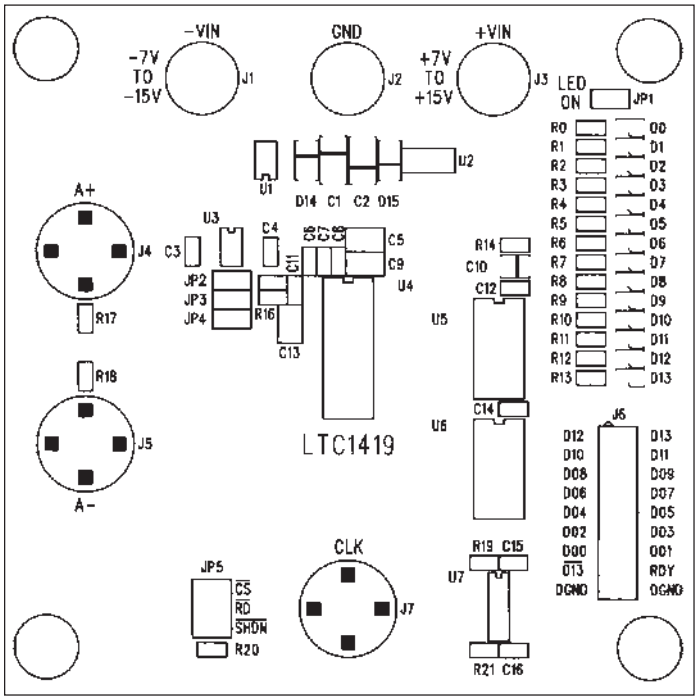


Figure 13b. Suggested Evaluation Circuit Board—Component Side Silkscreen

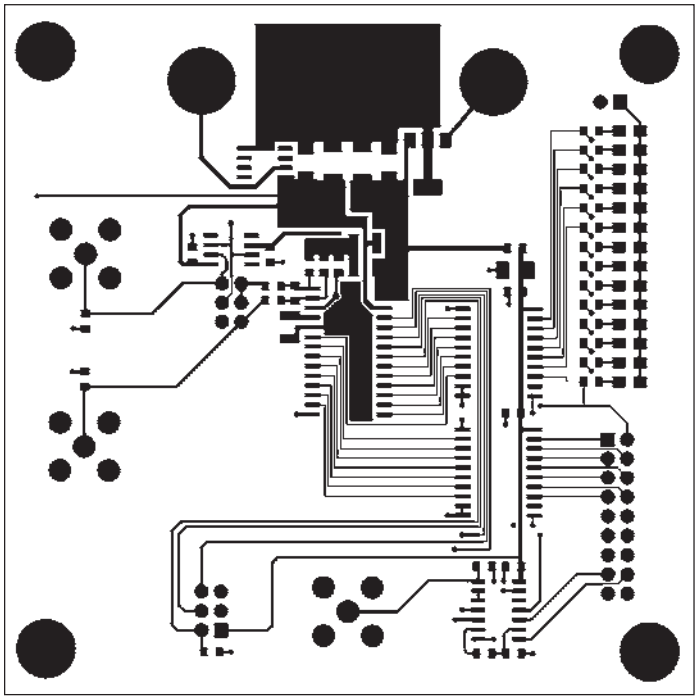


Figure 13c. Suggested Evaluation Circuit Board—Component Side Layout

APPLICATIONS INFORMATION

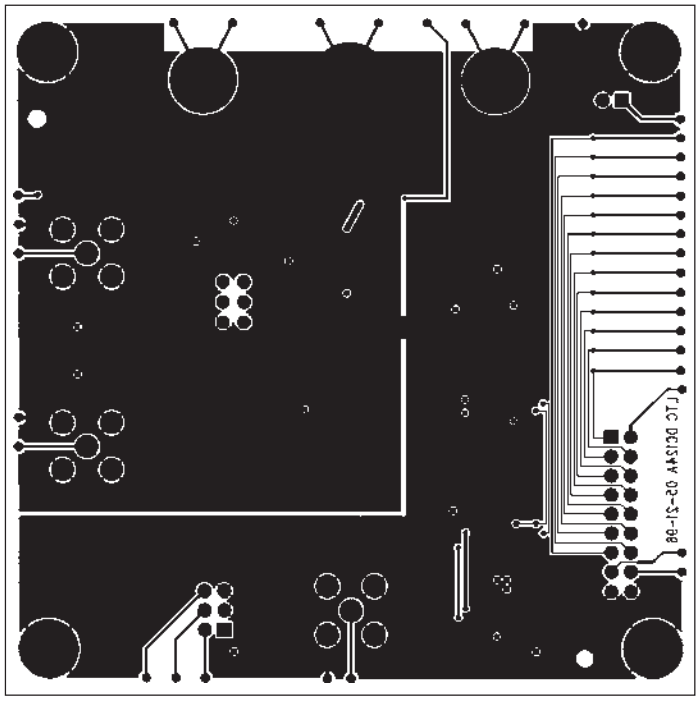


Figure 13d. Suggested Evaluation Circuit Board—Solder Side Layout

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.95µs and a maximum conversion time over the full operating temperature range of 1.15µs. No external adjustments are required. The guaranteed maximum acquisition time is 300ns. In addition, a throughput time of 1.25µs and a minimum sampling rate of 800ksps are guaranteed.

Power Shutdown

The LTC1419 provides two power shutdown modes, nap and sleep, to save power during inactive periods. The nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from nap to active is 400ns. In sleep mode, the reference is shut down and only a small current remains, about 250µA. Wake-up time from sleep mode is much slower since the reference circuit must power up and settle to 0.005% for full 14-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 10ms with the recommended 10µF capacitor. Shutdown is controlled by Pin 21 ($\overline{SHDN}$); the ADC is in shutdown when it is low. The shutdown mode is selected with Pin 20 ($\overline{CS}$); low selects nap.

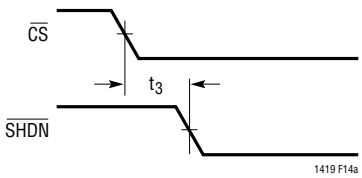


Figure 14a. $\overline{CS}$ to $\overline{SHDN}$ Timing

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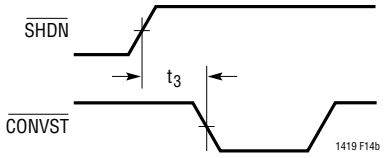


Figure 14b. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. A logic "0" applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

Figures 16 through 20 show several different modes of operation. In modes 1a and 1b (Figures 16 and 17), $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 18), $\overline{CS}$ is tied low. The falling edge of the $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 19 and 20), $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode, the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high, releasing the processor and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

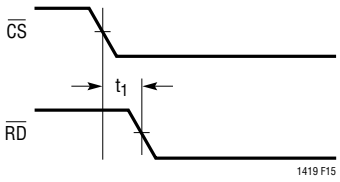


Figure 15. $\overline{CS}$ to $\overline{CONVST}$ Set-Up Timing

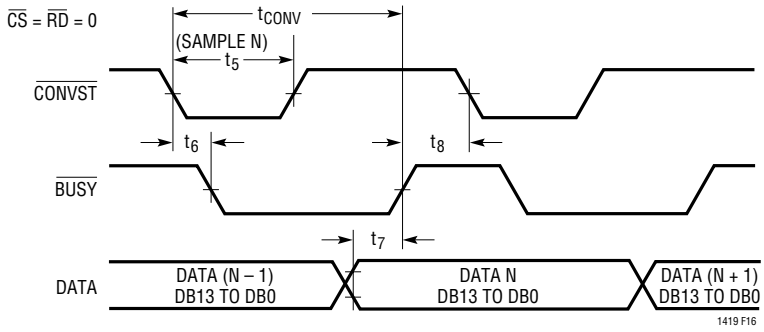


Figure 16. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⊓⊔⊓)

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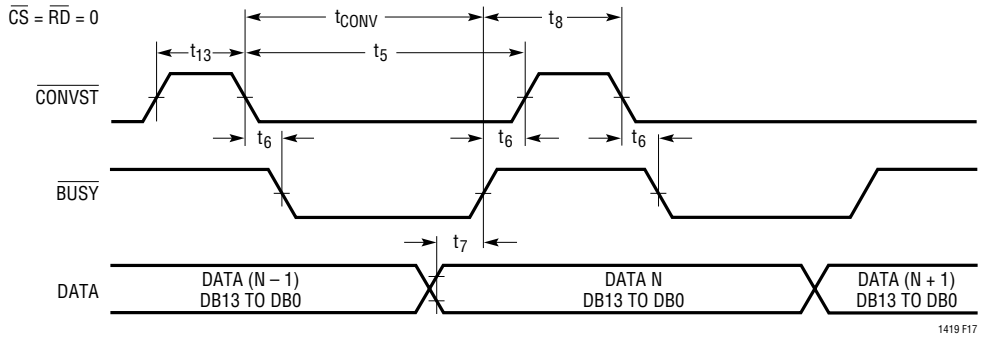


Figure 17. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⎍⎍)

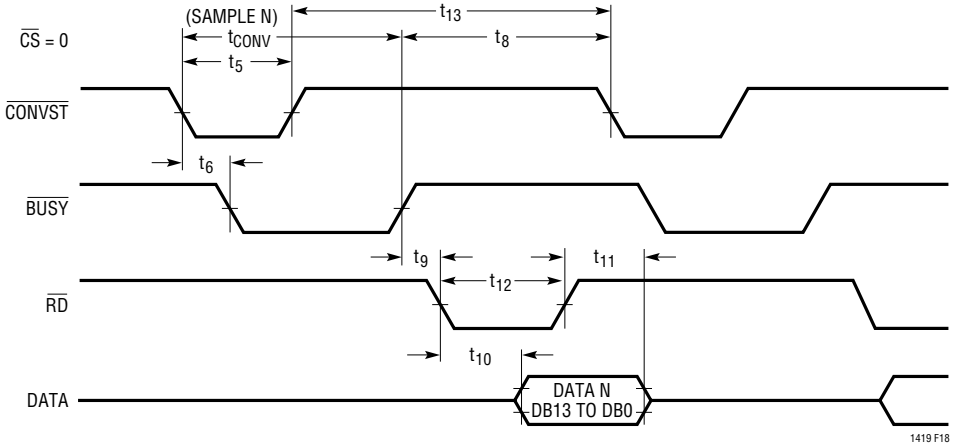


Figure 18. Mode 2. $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

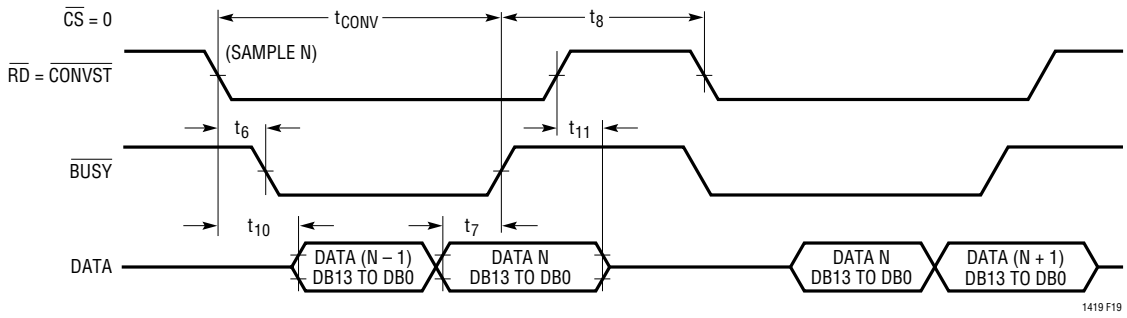


Figure 19. Slow Memory Mode Timing

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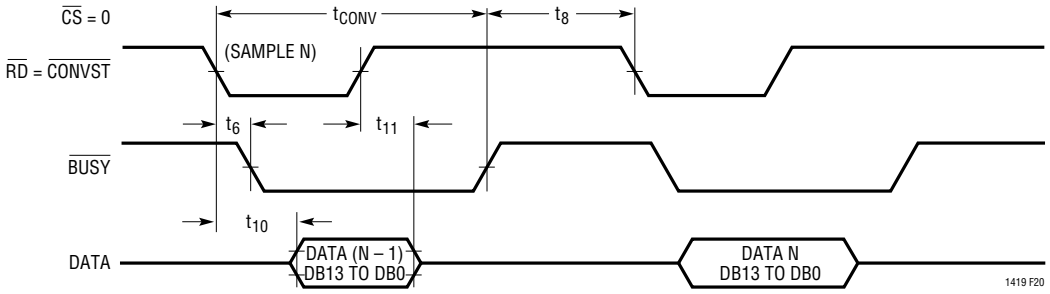
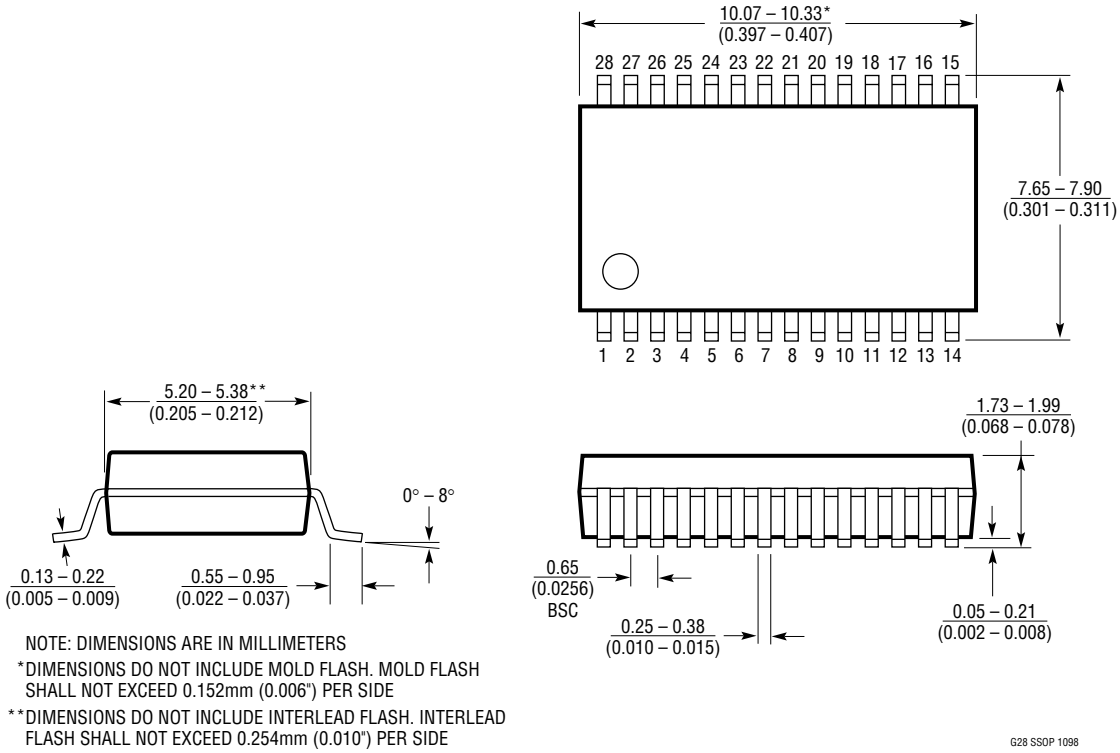


Figure 20. ROM Mode Timing

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

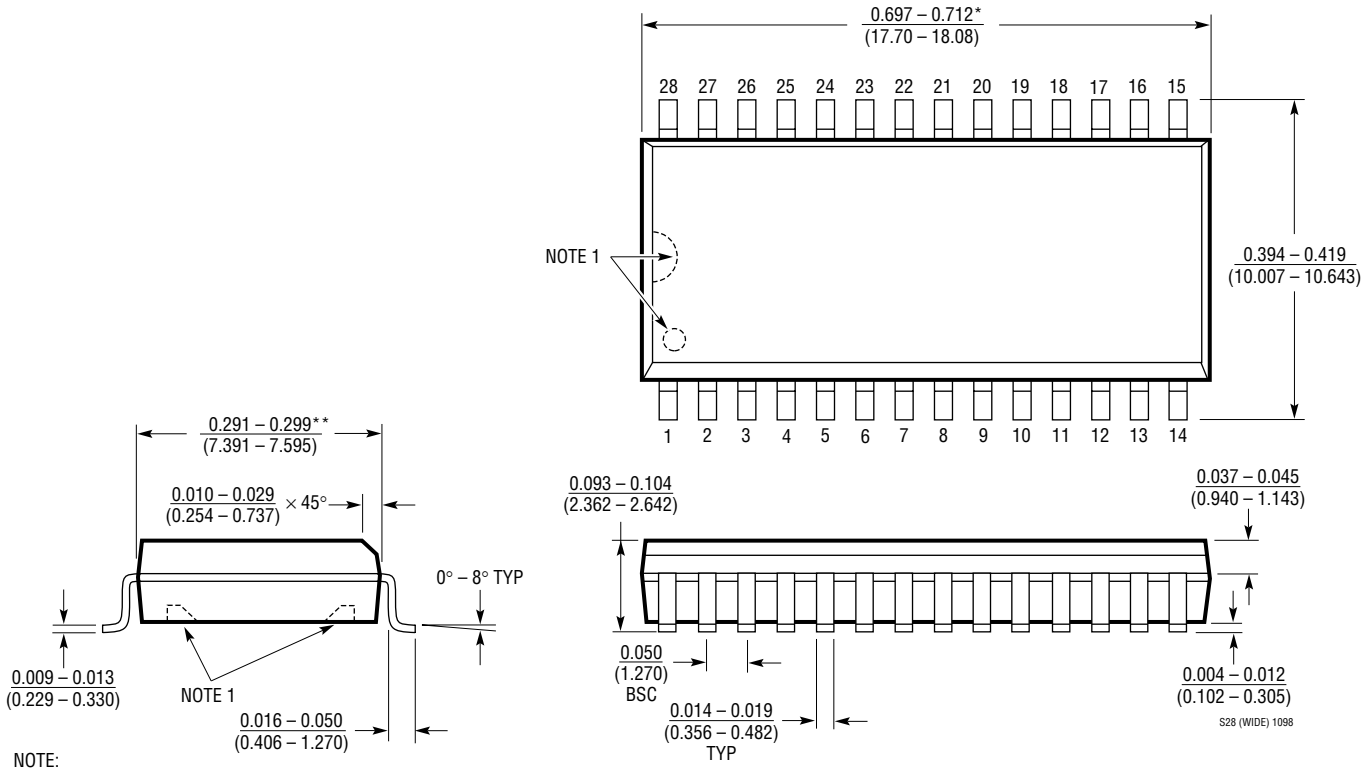
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
28-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1278/79	Single Supply, 500ksps/600ksps ADCs	Low Power, 5V or ±5V Supply
LTC1400	High Speed, Serial 12-Bit ADC	400ksps, Complete with Internal Reference, SO-8 Package
LTC1409	Low Power, 12-Bit, 800ksps Sampling ADC	Best Dynamic Performance, $f_{SAMPLE} \leq$ 800ksps, 80mW Dissipation
LTC1410	12-Bit, 1.25Msps Sampling ADC with Shutdown	Best Dynamic Performance, THD = 84dB and SINAD = 71dB at Nyquist
LTC1415	Single 5V, 12-Bit 1.25Msps ADC	Single Supply, 55mW Dissipation
LTC1604	16-Bit 333ksps ADC	±2.5V Inputs, Pin Compatible with the LTC1608
LTC1605	Single 5V, 16-Bit 100ksps ADC	Low Power, ±10V Inputs
LTC1606	16-Bit 250ksps ADC	±10V Inputs, Pin Compatible with the LTC1605
LTC1608	16-Bit 500ksps ADC	±2.5V Inputs, Pin Compatible with the LTC1604

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