# Octal 12-/10-/8-Bit SPI $V_{OUT}$ DACs with 10ppm/°C Reference

## FEATURES

- Integrated Precision Reference
  2.5V Full-Scale 10ppm/°C (LTC2636-L)
  4.096V Full-Scale 10ppm/°C (LTC2636-H)
- Maximum INL Error: 2.5LSB (LTC2636-12)
- Low Noise: 0.75mV$_{P-P}$ 0.1Hz to 200KHz
- Guaranteed Monotonic Over –40°C to 125°C Temperature Range
- Selectable Internal or External Reference
- 2.7V to 5.5V Supply Range (LTC2636-L)
- Ultralow Crosstalk Between DACs (<2.4nV•s)
- Low Power: 0.9mA at 3V (LTC2636-L)
- Power-On-Reset to Zero-Scale/Mid-Scale
- Double-Buffered Data Latches
- Tiny 14-Lead 4mm × 3mm DFN and 16-Lead MSOP Packages

## APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Automatic Test Equipment
- Portable Equipment
- Automotive
- Optical Networking

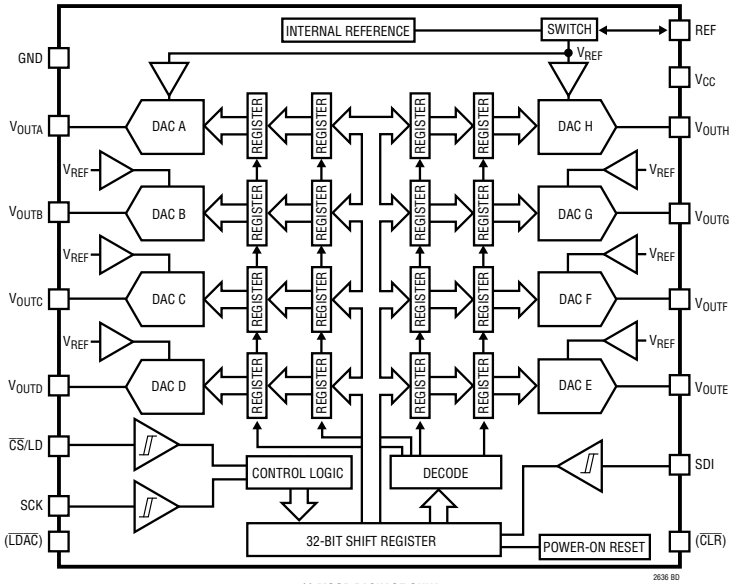
## DESCRIPTION

The LTC®2636 is a family of octal 12-, 10-, and 8-bit voltage-output DACs with an integrated, high-accuracy, low-drift 10ppm/°C reference in 14-lead DFN and 16-lead MSOP packages. It has a rail-to-rail output buffer and is guaranteed monotonic. The LTC2636-L has a full-scale output of 2.5V, and operates from a single 2.7V to 5.5V supply. The LTC2636-H has a full-scale output of 4.096V, and operates from a 4.5V to 5.5V supply. Each DAC can also operate with an external reference, which sets the DAC full-scale output to the external reference voltage.

These DACs communicate via an SPI/MICROWIRE-compatible 3-wire serial interface which operates at clock rates up to 50MHz. Hardware clear ($\overline{CLR}$) and asynchronous DAC update ($\overline{LDAC}$) pins are available in the MSOP package. The LTC2636 incorporates a power-on reset circuit. Options are available for reset to zero-scale or reset to mid-scale in internal reference mode, or reset to mid-scale in external reference mode after power-up.

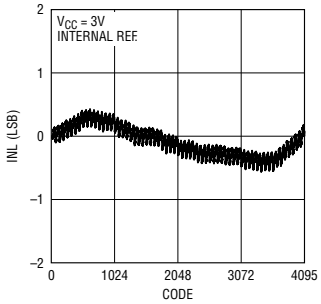
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## BLOCK DIAGRAM




( ) MSOP PACKAGE ONLY

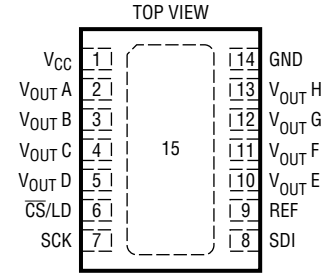
**12-Bit Integral Nonlinearity (LTC2636-LZ12)**



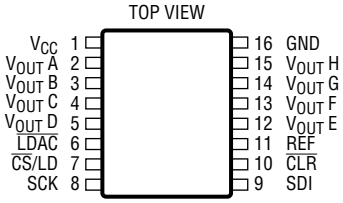
## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage ($V_{CC}$) ..... –0.3V to 6V
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$ ..... –0.3V to 6V
$V_{OUT}$ A–$V_{OUT}$ H .....–0.3V to Min($V_{CC}$ + 0.3V, 6V)
REF .....–0.3V to Min($V_{CC}$ + 0.3V, 6V)
Operating Temperature Range
LTC2636C ..... 0°C to 70°C
LTC2636I ..... –40°C to 85°C
LTC2636H (Note 3) ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS16-Lead Package ..... 300°C

## PIN CONFIGURATION



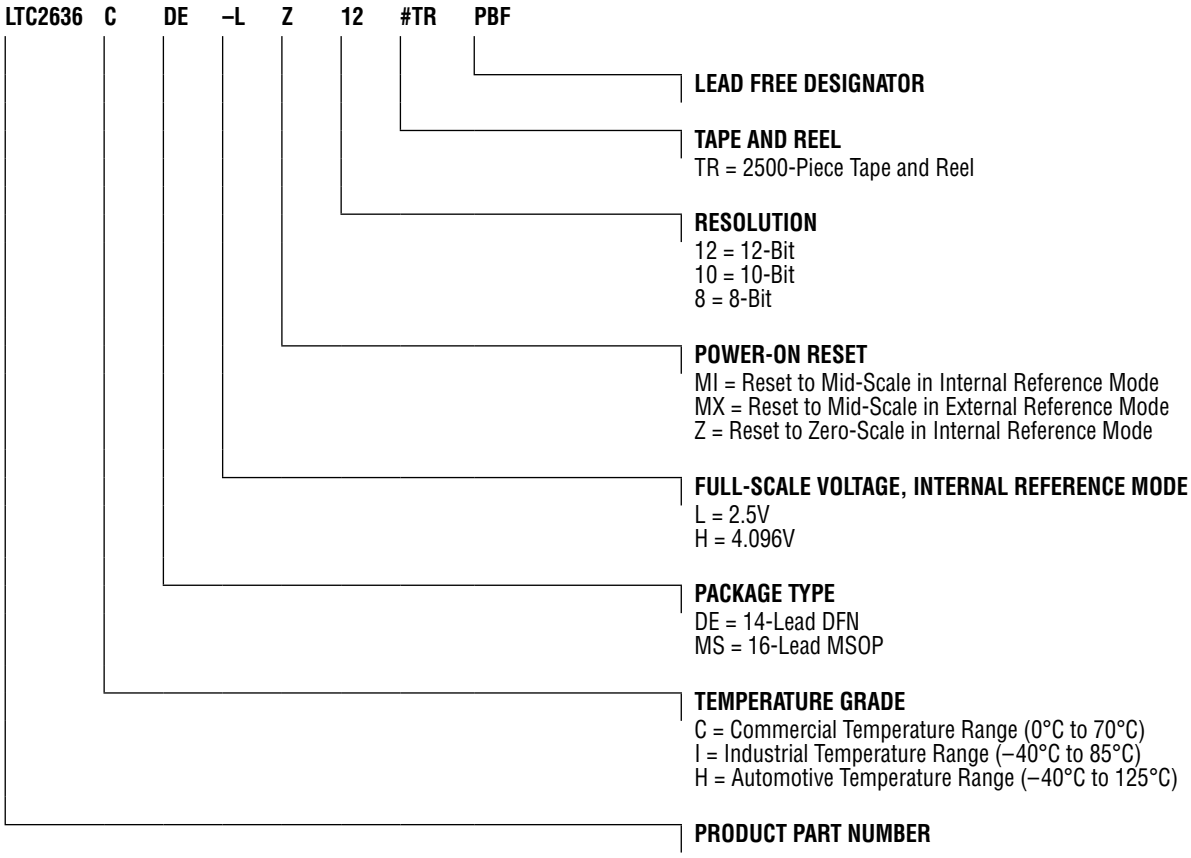

DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 37°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB




MS PACKAGE
16-LEAD (4mm × 5mm) PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 110°C/W

## ORDER INFORMATION

http://www.linear.com/product/LTC2636#orderinfo




Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# PRODUCT SELECTION GUIDE

| PART NUMBER | PART MARKING* | | $V_{FS}$ WITH INTERNAL REFERENCE | POWER-ON RESET TO CODE | POWER-ON REFERENCE MODE | RESOLUTION | $V_{CC}$ | MAXIMUM INL |
|---|---|---|---|---|---|---|---|---|
| | DFN | MSOP | | | | | | |
| LTC2636-LMI12 | LMI12 | 6LMI12 | 2.5V•(4095/4096) | Mid-Scale | Internal | 12-Bit | 2.7V-5.5V | ±2.5LSB |
| LTC2636-LMI10 | LMI10 | 6LMI10 | 2.5V•(1023/1024) | Mid-Scale | Internal | 10-Bit | 2.7V-5.5V | ±1LSB |
| LTC2636-LMI8 | 6LMI8 | 36LMI8 | 2.5V•(255/256) | Mid-Scale | Internal | 8-Bit | 2.7V-5.5V | ±0.5LSB |
| LTC2636-LMX12 | LMX12 | 6LMX12 | 2.5V•(4095/4096) | Mid-Scale | External | 12-Bit | 2.7V-5.5V | ±2.5LSB |
| LTC2636-LMX10 | LMX10 | 6LMX10 | 2.5V•(1023/1024) | Mid-Scale | External | 10-Bit | 2.7V-5.5V | ±1LSB |
| LTC2636-LMX8 | 6LMX8 | 36LMX8 | 2.5V•(255/256) | Mid-Scale | External | 8-Bit | 2.7V-5.5V | ±0.5LSB |
| LTC2636-LZ12 | 6LZ12 | 36LZ12 | 2.5V•(4095/4096) | Zero-Scale | Internal | 12-Bit | 2.7V-5.5V | ±2.5LSB |
| LTC2636-LZ10 | 6LZ10 | 36LZ10 | 2.5V•(1023/1024) | Zero-Scale | Internal | 10-Bit | 2.7V-5.5V | ±1LSB |
| LTC2636-LZ8 | 36LZ8 | 636LZ8 | 2.5V•(255/256) | Zero-Scale | Internal | 8-Bit | 2.7V-5.5V | ±0.5LSB |
| LTC2636-HMI12 | HMI12 | 6HMI12 | 4.096V•(4095/4096) | Mid-Scale | Internal | 12-Bit | 4.5V-5.5V | ±2.5LSB |
| LTC2636-HMI10 | HMI10 | 6HMI10 | 4.096V•(1023/1024) | Mid-Scale | Internal | 10-Bit | 4.5V-5.5V | ±1LSB |
| LTC2636-HMI8 | 6HMI8 | 36HMI8 | 4.096V•(255/256) | Mid-Scale | Internal | 8-Bit | 4.5V-5.5V | ±0.5LSB |
| LTC2636-HMX12 | HMX12 | 6HMX12 | 4.096V•(4095/4096) | Mid-Scale | External | 12-Bit | 4.5V-5.5V | ±2.5LSB |
| LTC2636-HMX10 | HMX10 | 6HMX10 | 4.096V•(1023/1024) | Mid-Scale | External | 10-Bit | 4.5V-5.5V | ±1LSB |
| LTC2636-HMX8 | 6HMX8 | 36HMX8 | 4.096V•(255/256) | Mid-Scale | External | 8-Bit | 4.5V-5.5V | ±0.5LSB |
| LTC2636-HZ12 | 6HZ12 | 36HZ12 | 4.096V•(4095/4096) | Zero-Scale | Internal | 12-Bit | 4.5V-5.5V | ±2.5LSB |
| LTC2636-HZ10 | 6HZ10 | 36HZ10 | 4.096V•(1023/1024) | Zero-Scale | Internal | 10-Bit | 4.5V-5.5V | ±1LSB |
| LTC2636-HZ8 | 36HZ8 | 636HZ8 | 4.096V•(255/256) | Zero-Scale | Internal | 8-Bit | 4.5V-5.5V | ±0.5LSB |

*Above options are available in a 14-lead DFN package (LTC2636-DE) or 16-lead MSOP package (LTC2636-MS).

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8 ($V_{FS}$ = 2.5V)**

| SYMBOL | PARAMETER | CONDITIONS | | LTC2636-8 MIN | LTC2636-8 TYP | LTC2636-8 MAX | LTC2636-10 MIN | LTC2636-10 TYP | LTC2636-10 MAX | LTC2636-12 MIN | LTC2636-12 TYP | LTC2636-12 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DC Performance** | | | | | | | | | | | | | |
| | Resolution | | ● | 8 | | | 10 | | | 12 | | | Bits |
| | Monotonicity | $V_{CC}$ = 3V, Internal Reference (Note 4) | ● | 8 | | | 10 | | | 12 | | | Bits |
| DNL | Differential Nonlinearity | $V_{CC}$ = 3V, Internal Reference (Note 4) | ● | | | ±0.5 | | | ±0.5 | | | ±1 | LSB |
| INL | Integral Nonlinearity | $V_{CC}$ = 3V, Internal Reference (Note 4) | ● | | ±0.05 | ±0.5 | | ±0.2 | ±1 | | ±1 | ±2.5 | LSB |
| ZSE | Zero-Scale Error | $V_{CC}$ = 3V, Internal Reference, Code = 0 | ● | | 0.5 | 5 | | 0.5 | 5 | | 0.5 | 5 | mV |
| $V_{OS}$ | Offset Error | $V_{CC}$ = 3V, Internal Reference (Note 5) | ● | | ±0.05 | ±5 | | ±0.05 | ±5 | | ±0.05 | ±5 | mV |
| $V_{OSTC}$ | $V_{OS}$ Temperature Coefficient | $V_{CC}$ = 3V, Internal Reference | | | ±10 | | | ±10 | | | ±10 | | µV/°C |
| GE | Gain Error | $V_{CC}$ = 3V, Internal Reference | ● | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | %FSR |
| $GE_{TC}$ | Gain Temperature Coefficient | $V_{CC}$ = 3V, Internal Reference (Note 10)<br>C-Grade<br>I-Grade<br>H-Grade | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | <br>ppm/°C<br>ppm/°C<br>ppm/°C |
| | Load Regulation | Internal Reference, Mid-Scale,<br>$V_{CC}$ = 3V±10%,<br>–5mA ≤ $I_{OUT}$ ≤ 5mA<br>$V_{CC}$ = 5V±10%, (Note 11)<br>–10mA ≤ $I_{OUT}$ ≤ 10mA | <br>●<br><br>● | | <br>0.009<br><br>0.009 | <br>0.016<br><br>0.016 | | <br>0.035<br><br>0.035 | <br>0.064<br><br>0.064 | | <br>0.14<br><br>0.14 | <br>0.256<br><br>0.256 | <br>LSB/mA<br><br>LSB/mA |
| $R_{OUT}$ | DC Output Impedance | Internal Reference, Mid-Scale,<br>$V_{CC}$ = 3V±10%,<br>–5mA ≤ $I_{OUT}$ ≤ 5mA<br>$V_{CC}$ = 5V±10%, (Note 11)<br>–10mA ≤ $I_{OUT}$ ≤ 10mA | <br>●<br><br>● | | <br>0.09<br><br>0.09 | <br>0.156<br><br>0.156 | | <br>0.09<br><br>0.09 | <br>0.156<br><br>0.156 | | <br>0.09<br><br>0.09 | <br>0.156<br><br>0.156 | <br>Ω<br><br>Ω |

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | DAC Output Span | External Reference<br>Internal Reference | | | 0 to $V_{REF}$<br>0 to 2.5 | | V<br>V |
| PSR | Power Supply Rejection | $V_{CC}$ = 3V±10% or 5V±10% | | | –80 | | dB |
| $I_{SC}$ | Short Circuit Output Current (Note 6)<br>Sinking<br>Sourcing | $V_{FS}$ = $V_{CC}$ = 5.5V<br>Zero-Scale; $V_{OUT}$ shorted to $V_{CC}$<br>Full-Scale; $V_{OUT}$ shorted to GND | <br>●<br>● | | <br>27<br>–28 | <br>48<br>–48 | <br>mA<br>mA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | For Specified Performance | ● | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply Current (Note 7) | $V_{CC}$ = 3V, $V_{REF}$ =2.5V, External Reference<br>$V_{CC}$ = 3V, Internal Reference<br>$V_{CC}$ = 5V, $V_{REF}$ =2.5V, External Reference<br>$V_{CC}$ = 5V, Internal Reference | ●<br>●<br>●<br>● | | 0.8<br>0.9<br>0.9<br>1 | 1.1<br>1.3<br>1.3<br>1.5 | mA<br>mA<br>mA<br>mA |
| $I_{SD}$ | Supply Current in Power-Down Mode (Note 7) | $V_{CC}$ = 5V, C-Grade, I-Grade<br>$V_{CC}$ = 5V, H-Grade | ●<br>● | | 0.5<br>0.5 | 20<br>30 | µA<br>µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8 ($V_{FS}$ = 2.5V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Reference Input** | | | | | | | |
| $V_{REF}$ | Input Voltage Range | | ● | 1 | | $V_{CC}$ | V |
| | Resistance | | ● | 120 | 160 | 200 | kΩ |
| | Capacitance | | | | 12 | | pF |
| $I_{REF}$ | Reference Current, Power-Down Mode | DAC Powered Down | ● | | 0.005 | 1.5 | µA |
| **Reference Output** | | | | | | | |
| | Output Voltage | | ● | 1.24 | 1.25 | 1.26 | V |
| | Reference Temperature Coefficient | | | | ±10 | | ppm/°C |
| | Output Impedance | | | | 0.5 | | kΩ |
| | Capacitive Load Driving | | | | 10 | | µF |
| | Short Circuit Current | $V_{CC}$ = 5.5V; REF Shorted to GND | | | 2.5 | | mA |
| **Digital I/O** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | $V_{CC}$ = 3.6V to 5.5V<br>$V_{CC}$ = 2.7V to 3.6V | ●<br>● | 2.4<br>2.0 | | | V<br>V |
| $V_{IL}$ | Digital Input Low Voltage | $V_{CC}$ = 4.5V to 5.5V<br>$V_{CC}$ = 2.7V to 4.5V | ●<br>● | | | 0.8<br>0.6 | V<br>V |
| $I_{LK}$ | Digital Input Leakage | $V_{IN}$ = GND to $V_{CC}$ | ● | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 8) | ● | | | 2.5 | pF |
| **AC Performance** | | | | | | | |
| $t_S$ | Settling Time | $V_{CC}$ = 3V (Note 9)<br>±0.39% (±1LSB at 8 Bits)<br>±0.098% (±1LSB at 10 Bits)<br>±0.024% (±1LSB at 12 Bits) | | | <br>3.4<br>4.0<br>4.4 | | <br>µs<br>µs<br>µs |
| | Voltage Output Slew Rate | | | | 1.0 | | V/µs |
| | Capacitive Load Driving | | | | 500 | | pF |
| | Glitch Impulse | At Mid-Scale Transition | | | 2.1 | | nV•s |
| | DAC-to-DAC Crosstalk | 1 DAC held at FS, 1 DAC Switch 0-FS | | | 2.1 | | nV•s |
| | Multiplying Bandwidth | External Reference | | | 320 | | kHz |
| $e_n$ | Output Voltage Noise Density | At f = 1kHz, External Reference<br>At f = 10kHz, External Reference<br>At f = 1kHz, Internal Reference<br>At f = 10kHz, Internal Reference | | | 180<br>160<br>200<br>180 | | nV/√Hz<br>nV/√Hz<br>nV/√Hz<br>nV/√Hz |
| | Output Voltage Noise | 0.1Hz to 10Hz, External Reference<br>0.1Hz to 10Hz, Internal Reference<br>0.1Hz to 200kHz, External Reference<br>0.1Hz to 200kHz, Internal Reference<br>$C_{REF}$ = 0.1µF | | | 35<br>40<br>680<br>730 | | $\mu V_{P-P}$<br>$\mu V_{P-P}$<br>$\mu V_{P-P}$<br>$\mu V_{P-P}$ |

## TIMING CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 2.7V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8 ($V_{FS}$ = 2.5V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| t1 | SDI Valid to SCK Setup | | ● | 4 | | | ns |
| t2 | SDI Valid to SCK Hold | | ● | 4 | | | ns |
| t3 | SCK High Time | | ● | 9 | | | ns |
| t4 | SCK Low Time | | ● | 9 | | | ns |
| t5 | $\overline{CS}$/LD Pulse Width | | ● | 10 | | | ns |
| t6 | LSB SCK High to $\overline{CS}$/LD High | | ● | 7 | | | ns |
| t7 | $\overline{CS}$/LD Low to SCK High | | ● | 7 | | | ns |
| t8 | $\overline{CLR}$ Pulse Width | | ● | 20 | | | ns |
| t9 | $\overline{LDAC}$ Pulse Width | | ● | 15 | | | ns |
| t10 | $\overline{CS}$/LD High to SCK Positive Edge | | ● | 7 | | | ns |
| | SCK Frequency | 50% Duty Cycle | ● | | | 50 | MHz |
| t11 | $\overline{CS}$/LD High to LDAC High or Low Transition | | ● | 200 | | | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | LTC2636-8 MIN | LTC2636-8 TYP | LTC2636-8 MAX | LTC2636-10 MIN | LTC2636-10 TYP | LTC2636-10 MAX | LTC2636-12 MIN | LTC2636-12 TYP | LTC2636-12 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DC Performance** | | | | | | | | | | | | | |
| | Resolution | | ● | 8 | | | 10 | | | 12 | | | Bits |
| | Monotonicity | $V_{CC}$ = 5V, Internal Reference (Note 4) | ● | 8 | | | 10 | | | 12 | | | Bits |
| DNL | Differential Nonlinearity | $V_{CC}$ = 5V, Internal Reference (Note 4) | ● | | | ±0.5 | | | ±0.5 | | | ±1 | LSB |
| INL | Integral Nonlinearity | $V_{CC}$ = 5V, Internal Reference (Note 4) | ● | | ±0.05 | ±0.5 | | ±0.2 | ±1 | | ±1 | ±2.5 | LSB |
| ZSE | Zero-Scale Error | $V_{CC}$ = 5V, Internal Reference, Code = 0 | ● | | 0.5 | 5 | | 0.5 | 5 | | 0.5 | 5 | mV |
| $V_{OS}$ | Offset Error | $V_{CC}$ = 5V, Internal Reference (Note 5) | ● | | ±0.05 | ±5 | | ±0.05 | ±5 | | ±0.05 | ±5 | mV |
| $V_{OSTC}$ | $V_{OS}$ Temperature Coefficient | $V_{CC}$ = 5V, Internal Reference | | | ±10 | | | ±10 | | | ±10 | | µV/°C |
| GE | Gain Error | $V_{CC}$ = 5V, Internal Reference | ● | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | | ±0.2 | ±0.8 | %FSR |
| $GE_{TC}$ | Gain Temperature Coefficient | $V_{CC}$ = 5V, Internal Reference (Note 10)<br>C-Grade<br>I-Grade<br>H-Grade | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | | <br>10<br>10<br>10 | | <br>ppm/°C<br>ppm/°C<br>ppm/°C |
| | Load Regulation | $V_{CC}$ = 5V±10%, (Note 11)<br>Internal Reference, Mid-Scale,<br>–10mA ≤ $I_{OUT}$ ≤ 10mA | ● | | 0.006 | 0.01 | | 0.022 | 0.04 | | 0.09 | 0.16 | LSB/mA |
| $R_{OUT}$ | DC Output Impedance | $V_{CC}$ = 5V±10%, (Note 11)<br>Internal Reference, Mid-Scale,<br>–10mA ≤ $I_{OUT}$ ≤ 10mA | ● | | 0.09 | 0.156 | | 0.09 | 0.156 | | 0.09 | 0.156 | Ω |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | DAC Output Span | External Reference<br>Internal Reference | | | 0 to $V_{REF}$<br>0 to 4.096 | | V<br>V |
| PSR | Power Supply Rejection | $V_{CC}$ = 5V±10% | | | –80 | | dB |
| $I_{SC}$ | Short Circuit Output Current (Note 6)<br>Sinking<br>Sourcing | $V_{FS}$ = $V_{CC}$ = 5.5V<br>Zero-Scale; $V_{OUT}$ Shorted to $V_{CC}$<br>Full-Scale; $V_{OUT}$ Shorted to GND | <br>●<br>● | | <br>27<br>–28 | <br>48<br>–48 | <br>mA<br>mA |
| **Power Supply** | | | | | | | |
| $V_{CC}$ | Positive Supply Voltage | For Specified Performance | ● | 4.5 | | 5.5 | V |
| $I_{CC}$ | Supply Current (Note 7) | $V_{CC}$ = 5V, $V_{REF}$ = 4.096V, External Reference<br>$V_{CC}$ = 5V, Internal Reference | ●<br>● | | 1.0<br>1.1 | 1.3<br>1.5 | mA<br>mA |
| $I_{SD}$ | Supply Current in Power-Down Mode (Note 7) | $V_{CC}$ = 5V, C-Grade, I-Grade<br>$V_{CC}$ = 5V, H-Grade | ●<br>● | | 0.5<br>0.5 | 20<br>30 | µA<br>µA |
| **Reference Input** | | | | | | | |
| $V_{REF}$ | Input Voltage Range | | ● | 1 | | $V_{CC}$ | V |
| | Resistance | | ● | 120 | 160 | 200 | kΩ |
| | Capacitance | | | | 12 | | pF |
| $I_{REF}$ | Reference Current, Power-Down Mode | DAC Powered Down | ● | | 0.005 | 1.5 | µA |
| **Reference Output** | | | | | | | |
| | Output Voltage | | ● | 2.032 | 2.048 | 2.064 | V |
| | Reference Temperature Coefficient | | | | ±10 | | ppm/°C |
| | Output Impedance | | | | 0.5 | | kΩ |
| | Capacitive Load Driving | | | | 10 | | µF |
| | Short Circuit Current | $V_{CC}$ = 5.5V; REF Shorted to GND | | | 4 | | mA |
| **Digital I/O** | | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | | ● | 2.4 | | | V |
| $V_{IL}$ | Digital Input Low Voltage | | ● | | | 0.8 | V |
| $I_{LK}$ | Digital Input Leakage | $V_{IN}$ = GND to $V_{CC}$ | ● | | | ±1 | µA |
| $C_{IN}$ | Digital Input Capacitance | (Note 8) | ● | | | 2.5 | pF |
| **AC Performance** | | | | | | | |
| $t_S$ | Settling Time | $V_{CC}$ = 5V (Note 9)<br>±0.39% (±1LSB at 8 Bits)<br>±0.098% (±1LSB at 10 Bits)<br>±0.024% (±1LSB at 12 Bits) | | | <br>3.8<br>4.3<br>4.8 | | <br>µs<br>µs<br>µs |
| | Voltage Output Slew Rate | | | | 1.0 | | V/µs |
| | Capacitive Load Driving | | | | 500 | | pF |
| | Glitch Impulse | At Mid-Scale Transition | | | 3.0 | | nV•s |
| | DAC-to-DAC Crosstalk | 1 DAC held at FS, 1 DAC Switch 0-FS | | | 2.4 | | nV•s |
| | Multiplying Bandwidth | External Reference | | | 320 | | kHz |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $e_n$ | Output Voltage Noise Density | At f = 1kHz, External Reference<br>At f = 10kHz, External Reference<br>At f = 1kHz, Internal Reference<br>At f = 10kHz, Internal Reference | | | 180<br>160<br>250<br>230 | | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| | Output Voltage Noise | 0.1Hz to 10Hz, External Reference<br>0.1Hz to 10Hz, Internal Reference<br>0.1Hz to 200kHz, External Reference<br>0.1Hz to 200kHz, Internal Reference<br>$C_{REF}$ = 0.1µF | | | 35<br>50<br>680<br>750 | | $\mu V_{P-P}$<br>$\mu V_{P-P}$<br>$\mu V_{P-P}$<br>$\mu V_{P-P}$ |

## TIMING CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 4.5V to 5.5V, $V_{OUT}$ unloaded unless otherwise specified.**

**LTC2636-HMI12/-HMI10/-HMI8/-HMX12/-HMX10/-HMX8/-HZ12/-HZ10/-HZ8 ($V_{FS}$ = 4.096V)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| t1 | SDI Valid to SCK Setup | | ● | 4 | | | ns |
| t2 | SDI Valid to SCK Hold | | ● | 4 | | | ns |
| t3 | SCK High Time | | ● | 9 | | | ns |
| t4 | SCK Low Time | | ● | 9 | | | ns |
| t5 | $\overline{CS}$/LD Pulse Width | | ● | 10 | | | ns |
| t6 | LSB SCK High to $\overline{CS}$/LD High | | ● | 7 | | | ns |
| t7 | $\overline{CS}$/LD Low to SCK High | | ● | 7 | | | ns |
| t8 | $\overline{CLR}$ Pulse Width | | ● | 20 | | | ns |
| t9 | $\overline{LDAC}$ Pulse Width | | ● | 15 | | | ns |
| t10 | $\overline{CS}$/LD High to SCK Positive Edge | | ● | 7 | | | ns |
| | SCK Frequency | 50% Duty Cycle | ● | | | 50 | MHz |
| t11 | $\overline{CS}$/LD High to LDAC High or Low Transition | | ● | 200 | | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltages are with respect to GND.

**Note 3:** Operating at temperatures above 90°C and with $V_{CC}$ > 4V requires $V_{CC}$ slew rates to be no greater than 110mV/µs.

**Note 4:** Linearity and monotonicity are defined from code kL to code $2^N$–1, where N is the resolution and $k_L$ is given by kL = 0.016•($2^N/V_{FS}$), rounded to the nearest whole code. For $V_{FS}$ = 2.5V and N = 12, $k_L$ = 26 and linearity is defined from code 26 to code 4,095. For $V_{FS}$ = 4.096V and N = 12, $k_L$ = 16 and linearity is defined from code 16 to code 4,095.

**Note 5:** Inferred from measurement at code 16 (LTC2636-12), code 4 (LTC2636-10) or code 1 (LTC2636-8), and at full-scale.

**Note 6:** This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 7:** Digital inputs at 0V or $V_{CC}$.

**Note 8:** Guaranteed by design and not production tested.

**Note 9:** Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 100pF to GND.

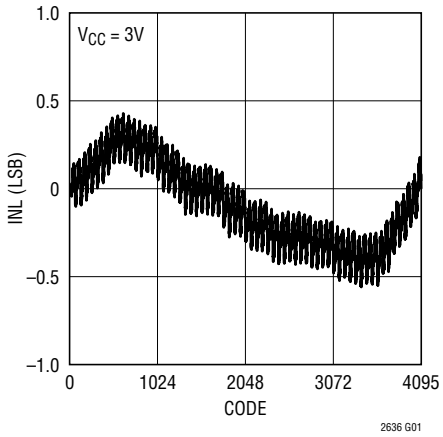
**Note 10:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

**Note 11:** Thermal resistance of MSOP package limits $I_{OUT}$ to –5mA ≤ $I_{OUT}$ ≤ 5mA for H-grade MSOP parts and $V_{CC}$ = 5V ±10%.

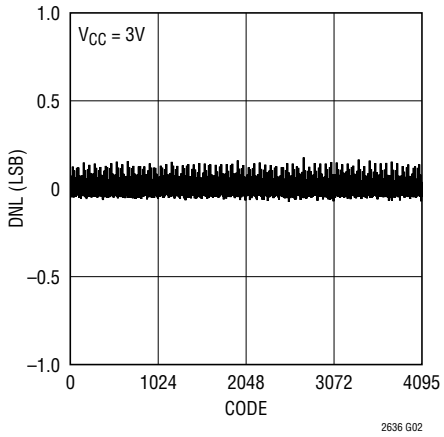
# TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. LTC2636-L12 (Internal Reference, $V_{FS}$ = 2.5V)**

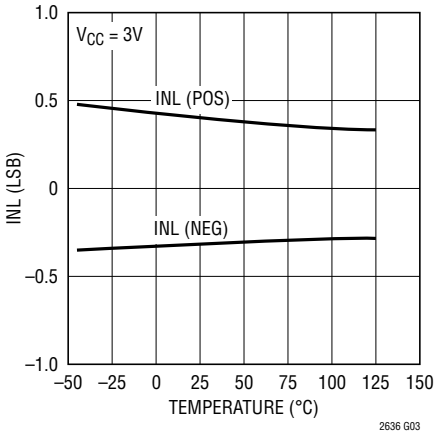
**Integral Nonlinearity (INL)**



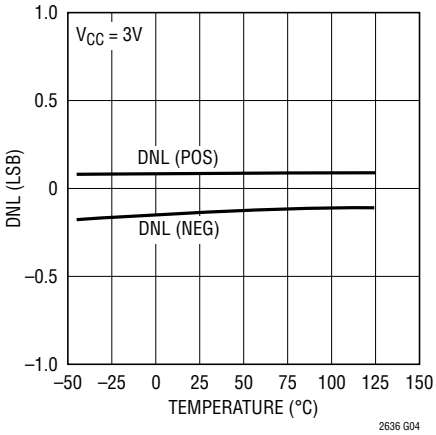

**Differential Nonlinearity (DNL)**



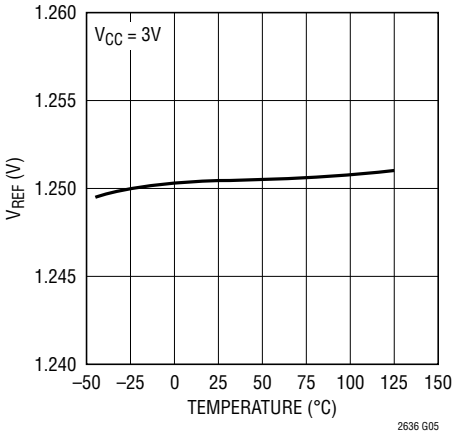

**INL vs Temperature**



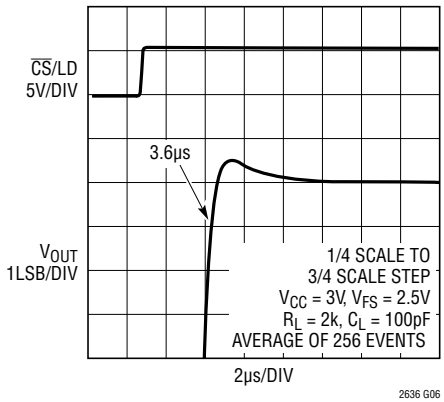

**DNL vs Temperature**



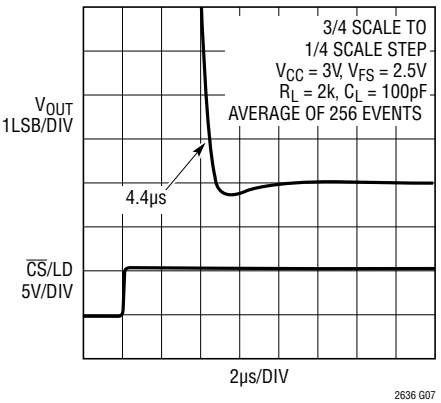

**Reference Output Voltage vs Temperature**




**Settling to ±1LSB Rising**



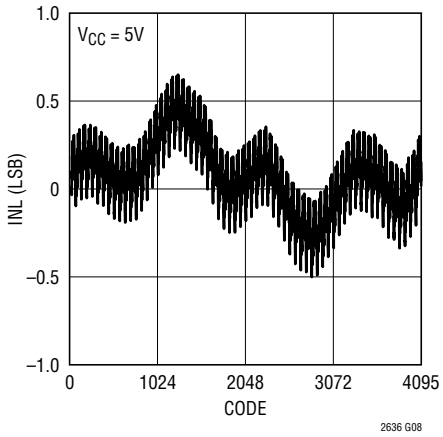

**Settling to ±1LSB Falling**



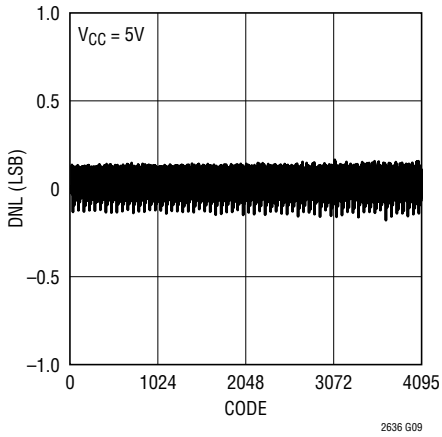
# TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. LTC2636-H12 (Internal Reference, $V_{FS}$ = 4.096V)**

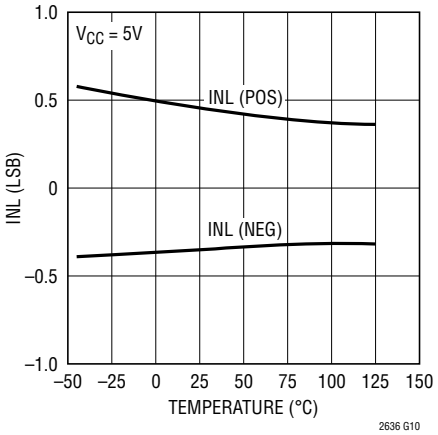
### Integral Nonlinearity (INL)



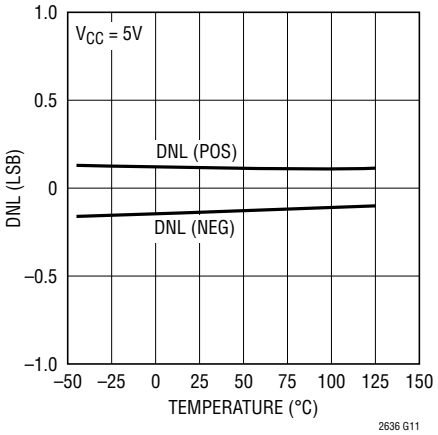

### Differential Nonlinearity (DNL)



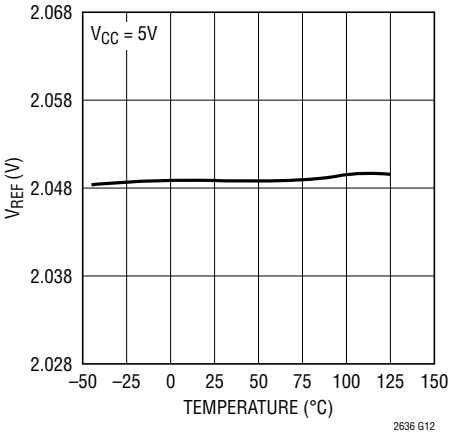

### INL vs Temperature



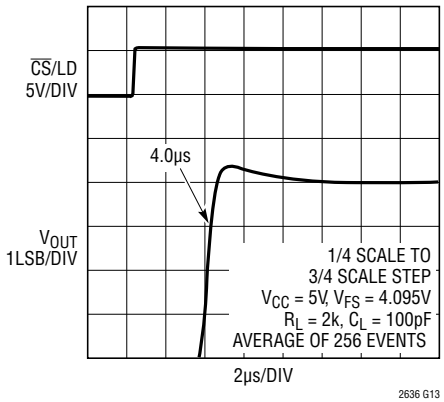

### DNL vs Temperature



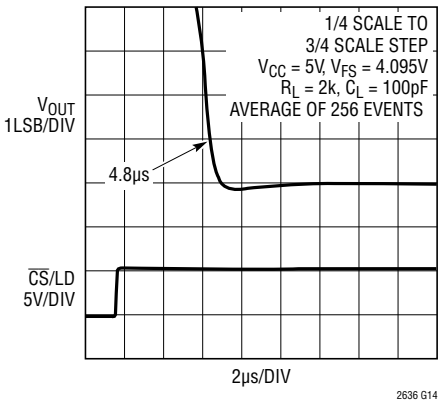

### Reference Output Voltage vs Temperature




### Settling to ±1LSB Rising



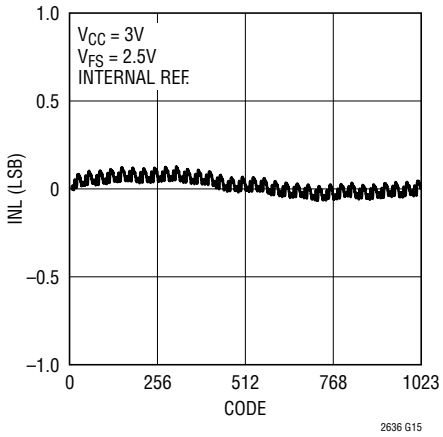

### Settling to ±1LSB Falling



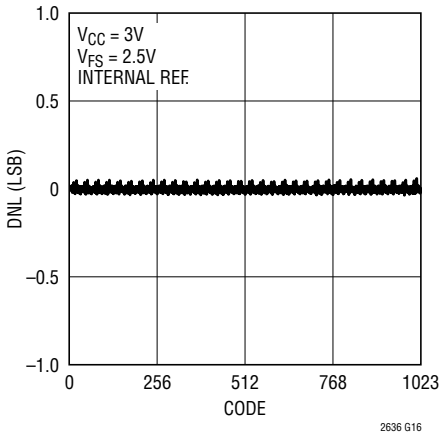
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### LTC2636-10

**Integral Nonlinearity (INL)**

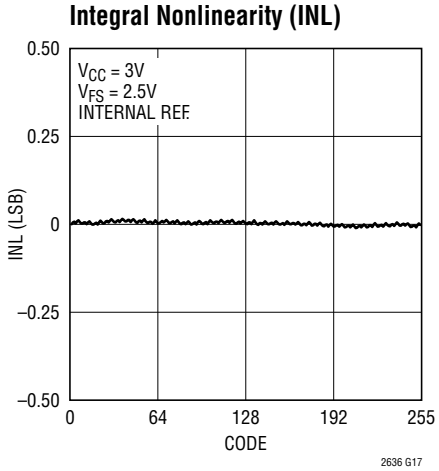



**Differential Nonlinearity (DNL)**

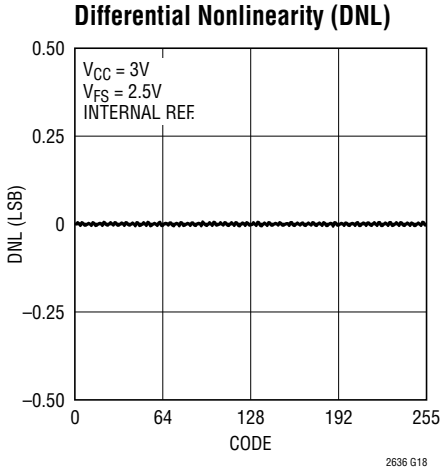



### LTC2636-8

**Integral Nonlinearity (INL)**

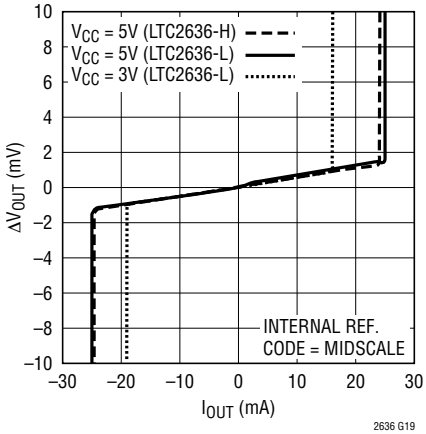



**Differential Nonlinearity (DNL)**

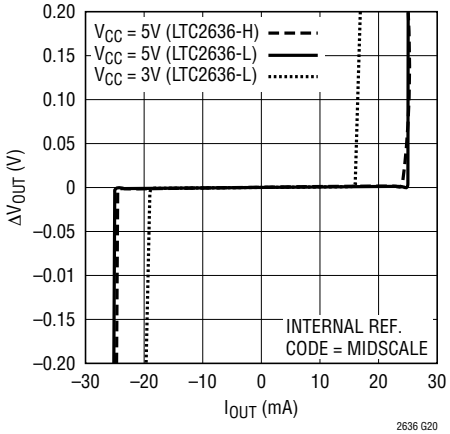



### LTC2636

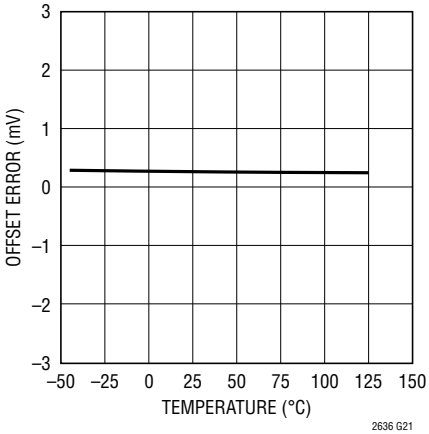
**Load Regulation**




**Current Limiting**



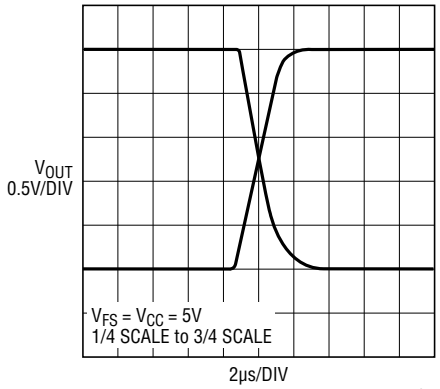

**Offset Error vs Temperature**



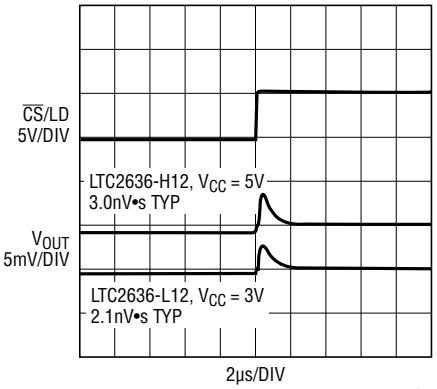
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

## LTC2636

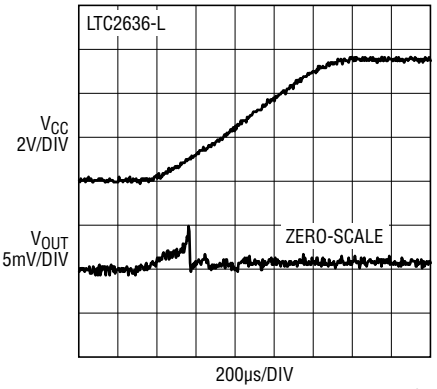
### Large-Signal Response



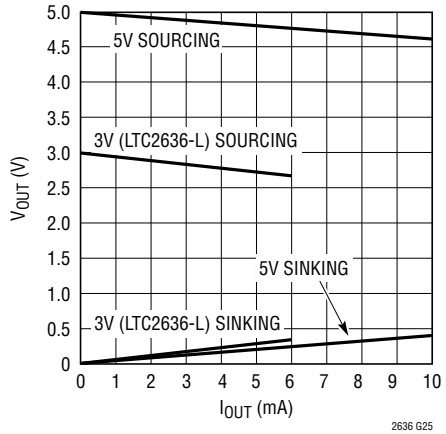

### Mid-Scale Glitch Impulse



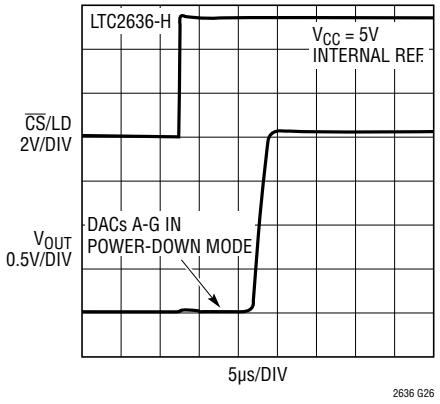

### Power-On Reset Glitch



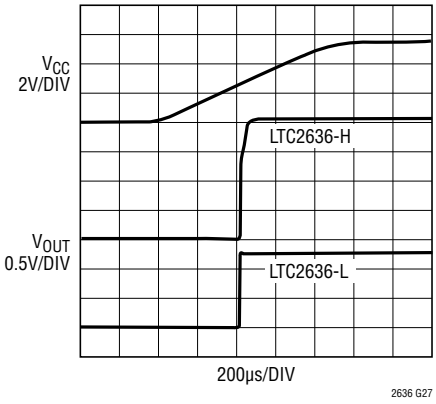

### Headroom at Rails vs Output Current



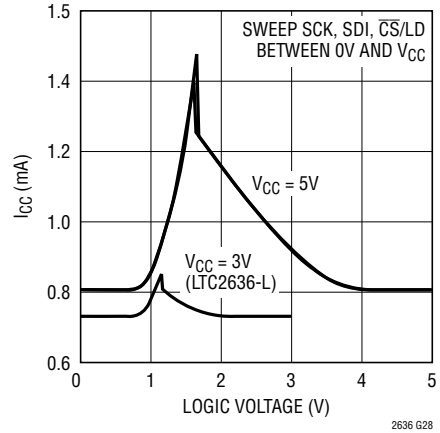

### Exiting Power-Down to Mid-Scale



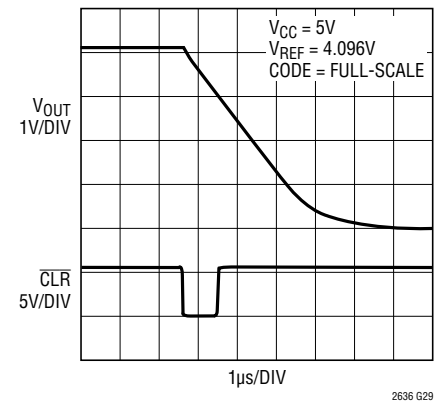

### Power-On Reset to Mid-Scale



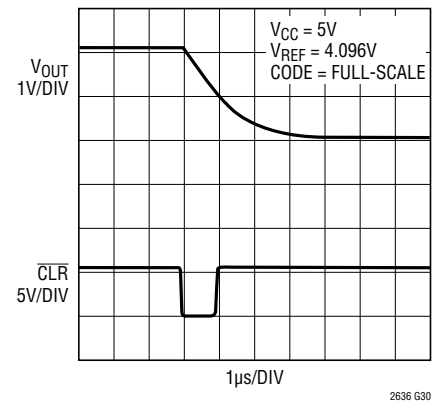

### Supply Current vs Logic Voltage




### Hardware $\overline{CLR}$



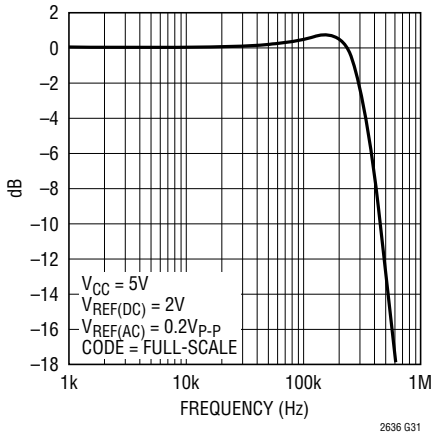

### Hardware $\overline{CLR}$ to Mid-Scale



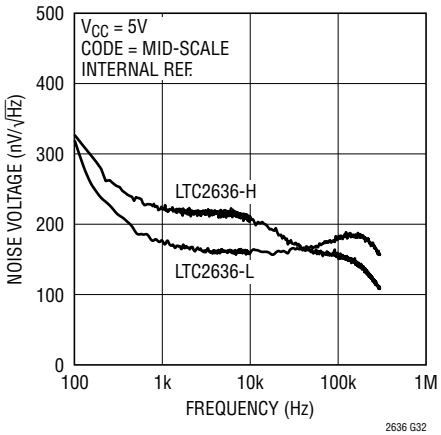
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

**LTC2636**

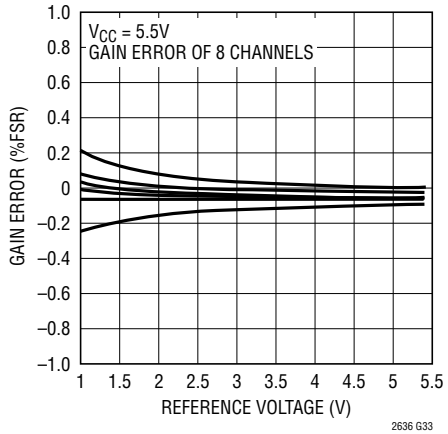
### Multiplying Bandwidth



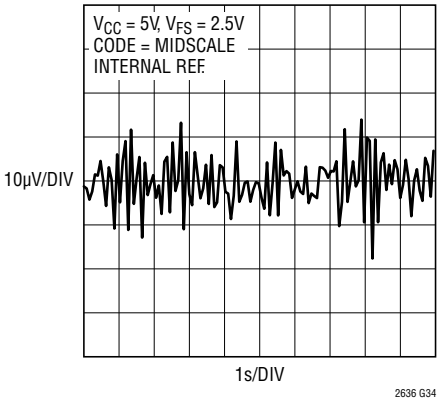

### Noise Voltage vs Frequency



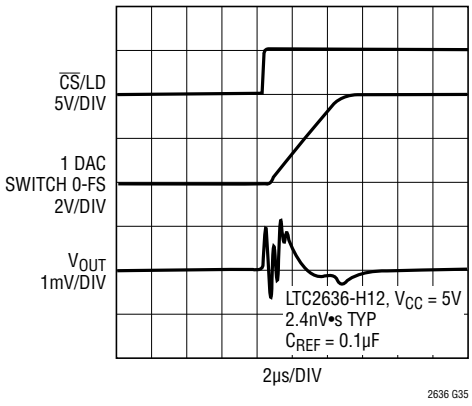

### Gain Error vs Reference Input



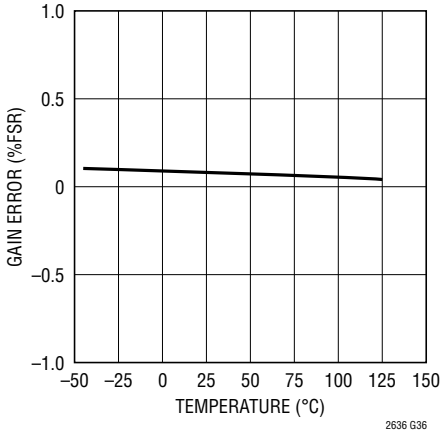

### 0.1Hz to 10Hz Voltage Noise




### DAC to DAC Crosstalk (Dynamic)




### Gain Error vs Temperature



## PIN FUNCTIONS (DFN/MSOP)

**$V_{CC}$ (Pin 1/1):** Supply Voltage Input. 2.7V ≤ $V_{CC}$ ≤ 5.5V (LTC2636-L) or 4.5V ≤ $V_{CC}$ ≤ 5.5V (LTC2636-H). Bypass to GND with a 0.1µF capacitor.

**$V_{OUT}$ A to $V_{OUT}$ H (Pins 2-5, 10-13/2-5, 12-15):** DAC Analog Voltage Outputs.

**$\overline{CS}$/LD (Pin 6/7):** Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

**SCK (Pin 7/8):** Serial Interface Clock Input. CMOS and TTL compatible.

**SDI (Pin 8/9):** Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2636 accepts input word lengths of either 24 or 32 bits.

**REF (Pin 9/11):** Reference Voltage Input or Output. When External Reference mode is selected, REF is an input (1V ≤ $V_{REF}$ ≤ $V_{CC}$) where the voltage supplied sets the full-scale DAC output voltage. When Internal Reference is selected, the 10ppm/°C 1.25V (LTC2636-L) or 2.048V (LTC2636-H) internal reference (half full-scale) is available at REF. This output may be bypassed to GND with up to 10µF, and must be buffered when driving external DC load current.

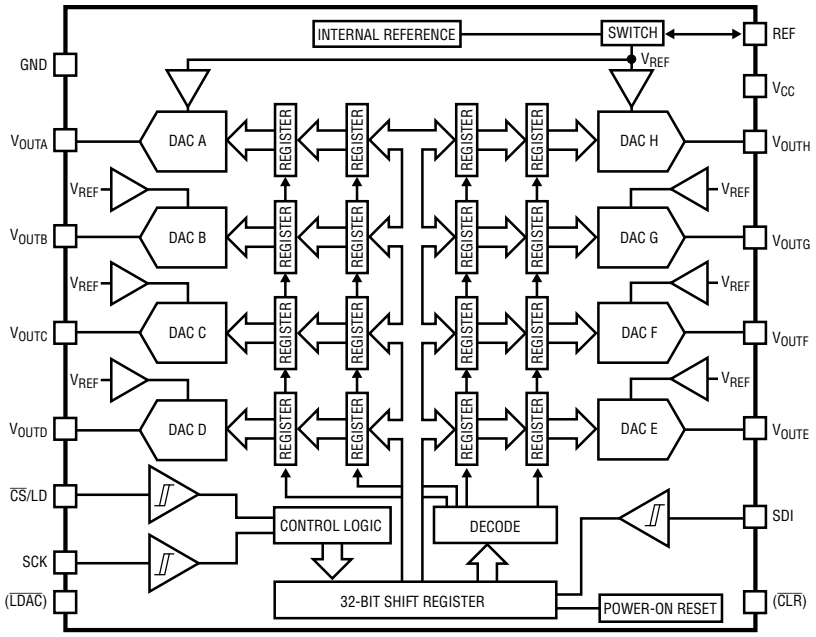
**GND (Pin 14/16):** Ground.

**$\overline{LDAC}$ (Pin 6, MSOP only):** Asynchronous DAC Update Pin. If $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ immediately updates the DAC registers with the contents of the input registers (similar to a software update). If $\overline{CS}$/LD is low when $\overline{LDAC}$ goes low, the DAC registers are updated after $\overline{CS}$/LD returns high. A low on the $\overline{LDAC}$ pin powers up the DACs. A software power down command is ignored if $\overline{LDAC}$ is low. If the $\overline{LDAC}$ functionality is not being used, the $\overline{LDAC}$ pin should be tied high.

**$\overline{CLR}$ (Pin 10, MSOP only):** Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage output to reset to Zero (LTC2636-Z) or Mid-scale (LTC2636-MI/-MX). CMOS and TTL compatible.

**Exposed Pad (Pin 15, DFN Only):** Ground. Must be soldered to PCB Ground.

## BLOCK DIAGRAM




**( ) MSOP PACKAGE ONLY**

## TIMING DIAGRAMS

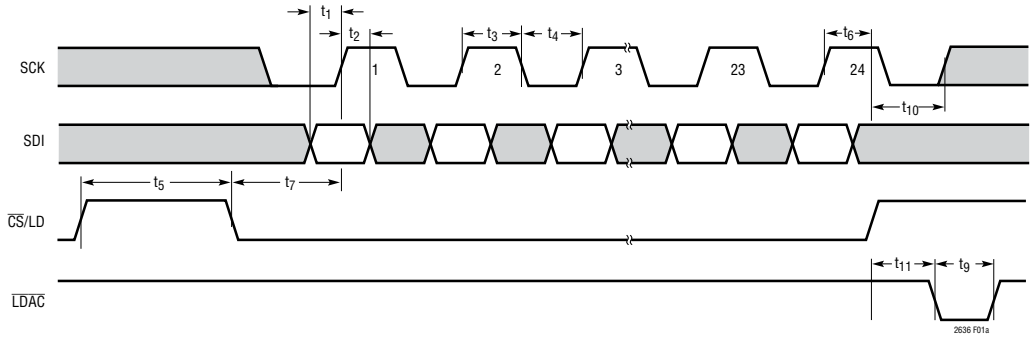



**Figure 1a**

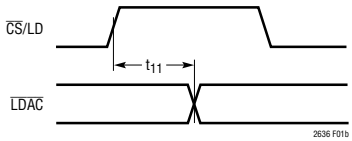



**Figure 1b**

# OPERATION

The LTC2636 is a family of octal voltage output DACs in 14-lead DFN and 16-lead MSOP packages. Each DAC can operate rail-to-rail using an external reference, or with its full-scale voltage set by an integrated reference. Eighteen combinations of accuracy (12-, 10-, and 8-bit), power-on reset value (zero-scale, mid-scale in internal reference mode, or mid-scale in external reference mode), and full-scale voltage (2.5V or 4.096V) are available. The LTC2636 is controlled using a 3-wire SPI/MICROWIRE compatible interface.

## Power-On Reset

The LTC2636-HZ/-LZ clear the output to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2636 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 5mV above zero-scale during power on. In general, the glitch amplitude decreases as the power supply ramp time is increased. See “Power-On Reset Glitch” in the Typical Performance Characteristics section.

The LTC2636-HMI/-HMX/-LMI/-LMX provide an alternative reset, setting the output to mid-scale when power is first applied. The LTC2636-LMI and LTC2636-HMI power up in internal reference mode, with the output set to a mid-scale voltage of 1.25V and 2.048V respectively. The LTC2636-LMX and LTC2636-HMX power-up in external reference mode, with the output set to mid-scale of the external reference. Default reference mode selection is described in the Reference Modes section.

## Power Supply Sequencing

The voltage at REF (Pin 9-DFN, Pin 11-MSOP) must be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at $V_{CC}$ is in transition.

## Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^n}\right) V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, n is the resolution, and $V_{REF}$ is either 2.5V (LTC2636-LMI/-LMX/-LZ) or 4.096V (LTC2636-HMI/-HMX/-HZ) when in Internal Reference mode, and the voltage at REF when in External Reference mode.

**Table 1. Command Codes**

| COMMAND* | | | | |
|---|---|---|---|---|
| **C3** | **C2** | **C1** | **C0** | |
| 0 | 0 | 0 | 0 | Write to Input Register n |
| 0 | 0 | 0 | 1 | Update (Power-Up) DAC Register n |
| 0 | 0 | 1 | 0 | Write to Input Register n, Update (Power-Up) All |
| 0 | 0 | 1 | 1 | Write to and Update (Power-Up) DAC Register n |
| 0 | 1 | 0 | 0 | Power-Down DAC n |
| 0 | 1 | 0 | 1 | Power-Down Chip (All DAC’s and Reference) |
| 0 | 1 | 1 | 0 | Select Internal Reference (Power-Up Reference) |
| 0 | 1 | 1 | 1 | Select External Reference (Power-Down Internal Reference) |
| 1 | 1 | 1 | 1 | No Operation |

*Command codes not shown are reserved and should not be used.

**Table 2. Address Codes**

| ADDRESS (n)* | | | | |
|---|---|---|---|---|
| **A3** | **A2** | **A1** | **A0** | |
| 0 | 0 | 0 | 0 | DAC A |
| 0 | 0 | 0 | 1 | DAC B |
| 0 | 0 | 1 | 0 | DAC C |
| 0 | 0 | 1 | 1 | DAC D |
| 0 | 1 | 0 | 0 | DAC E |
| 0 | 1 | 0 | 1 | DAC F |
| 0 | 1 | 1 | 0 | DAC G |
| 0 | 1 | 1 | 1 | DAC H |
| 1 | 1 | 1 | 1 | ALL DACS |

*Address codes not shown are reserved and should not be used.

## OPERATION

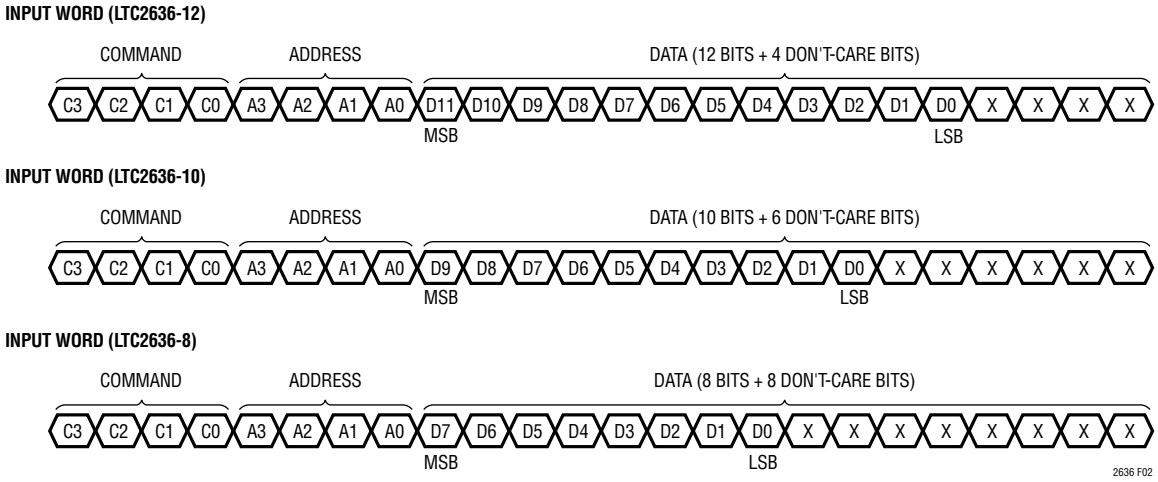



**Figure 2. Command and Data Input Format**

### Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the input shift register. Data (SDI input) is transferred into the LTC2636 on the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 12-, 10- or 8-bit input code, ordered MSB-to-LSB, followed by 4, 6 or 8 don't-care bits (LTC2636-12, -10 and -8 respectively; see Figure 2). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low, beginning on the first rising edge of SCK. SCK may be high or low at the falling edge of $\overline{CS}$/LD. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to execute the command specified in the 24-bit input sequence. The complete sequence is shown in Figure 3a.

The command (C3-C0) and address (A3-A0) assignments are shown in Tables 1 and 2. The first four commands in Table 1 consist of write and update operations. A Write operation loads a 16-bit data word from the 24-bit shift register into the input register of the selected DAC, n. An Update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 12-, 10-, or 8-bit input code, and is converted to an analog voltage at the DAC output. Write to and Update combines the first two commands. The Update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input sequence is 24 bits, it may optionally be extended to 32 bits to accommodate microprocessors that have a minimum word width of 16 bits (2 bytes). To use the 32-bit width, 8 don't-care bits must be transferred to the device first, followed by the 24-bit sequence described. Figure 3b shows the 32-bit sequence.

The 16-bit data word is ignored for all commands that do not include a Write operation.

### Reference Modes

For applications where an accurate external reference is either not available, or not desirable due to limited space, the LTC2636 has a user-selectable, integrated reference. The integrated reference voltage is internally amplified by 2x to provide the full-scale DAC output voltage range. The LTC2636-LMI/-LMX/-LZ provides a full-scale DAC output of 2.5V. The LTC2636-HMI/-HMX/-HZ provides a full-scale DAC output of 4.096V. The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal Reference mode can be selected by using command 0110b, and is the power-on default for LTC2636-HZ/-LZ, as well as for LTC2636-HMI/-LMI.

## OPERATION

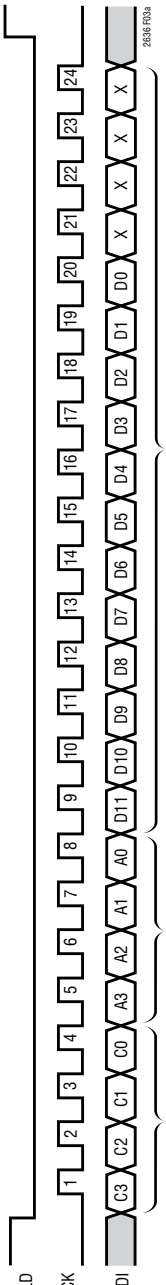



**Figure 3a. LTC2636-12 24-Bit Load Sequence (Minimum Input Word). LTC2636-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Care Bits; LTC2636-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Care Bits**

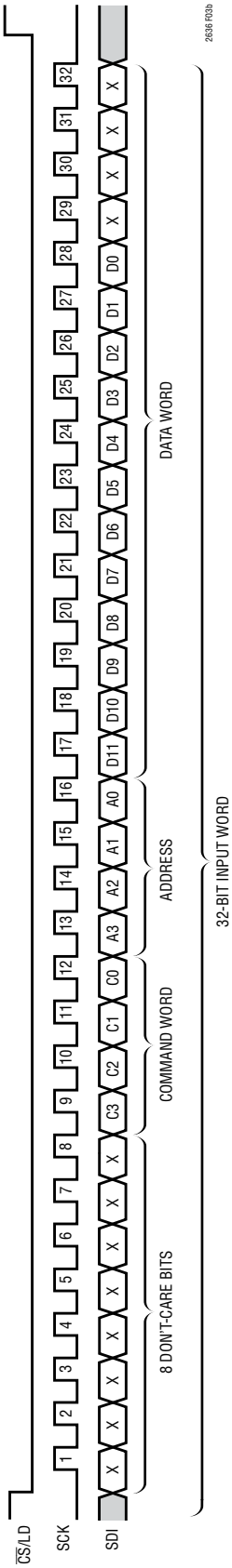



**Figure 3b. LTC2636-12 32-Bit Load Sequence. LTC2636-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Care Bits; LTC2636-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Care Bits**

## OPERATION

The 10ppm/°C, 1.25V (LTC2636-LMI/-LMX/-LZ) or 2.048V (LTC2636-HMI/-HMX/-HZ) internal reference is available at the REF pin. Adding bypass capacitance to the REF pin will improve noise performance; and up to 10µF can be driven without oscillation. The REF output must be buffered when driving an external DC load current.

Alternatively, the DAC can operate in External Reference mode using command 0111b. In this mode, an input voltage supplied externally to the REF pin provides the reference ($1V \leq V_{REF} \leq V_{CC}$) and the supply current is reduced. The external reference voltage supplied sets the full-scale DAC output voltage. External Reference mode is the power-on default for LTC2636-HMX/-LMX.

The reference mode of LTC2636-HZ/-LZ/-HMI/-LMI (Internal Reference power-on default), can be changed by software command after power-up. The same is true for LTC2636-HMX/-LMX (External Reference power-on default).

### Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than eight DAC outputs are needed. When in power-down, the buffer amplifiers, bias circuits, and integrated reference circuits are disabled, and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the output pins are passively pulled to ground through individual 200k resistors. Input- and DAC-register contents are not disturbed during power-down.

Any DAC channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, (n). The supply current is reduced approximately 10% for each DAC powered down. The integrated reference is automatically powered down when external reference is selected using command 0111b. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using Power Down Chip command 0101b. When the integrated reference and all DAC channels are in power-down mode, the REF pin becomes high impedance (typically > 1GΩ). For all power-down commands the 16- bit data word is ignored.

Normal operation resumes after executing any command that includes a DAC update, (as shown in Table 1) or using the asynchronous $\overline{LDAC}$ pin. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than eight DACs are in a powered-down state prior to the update command, the power-up delay time is 10µs. However, if all eight DACs and the integrated reference are powered down, then the main bias generation circuit block has been automatically shut down in addition to the DAC amplifiers and reference buffers. In this case, the power up delay time is 12µs. The power-up of the integrated reference depends on the command that powered it down. If the reference is powered down using the Select External Reference Command (0111b), then it can only be powered back up using Select Internal Reference Command (0110b). However, if the reference was powered down using Power Down Chip Command (0101b), then in addition to Select Internal Reference Command (0110b), any command (in software or using the $\overline{LDAC}$ pin) that powers up the DACs will also power up the integrated reference.

### Voltage Outputs

The LTC2636's integrated rail-to-rail amplifiers have guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph "Headroom at

## OPERATION

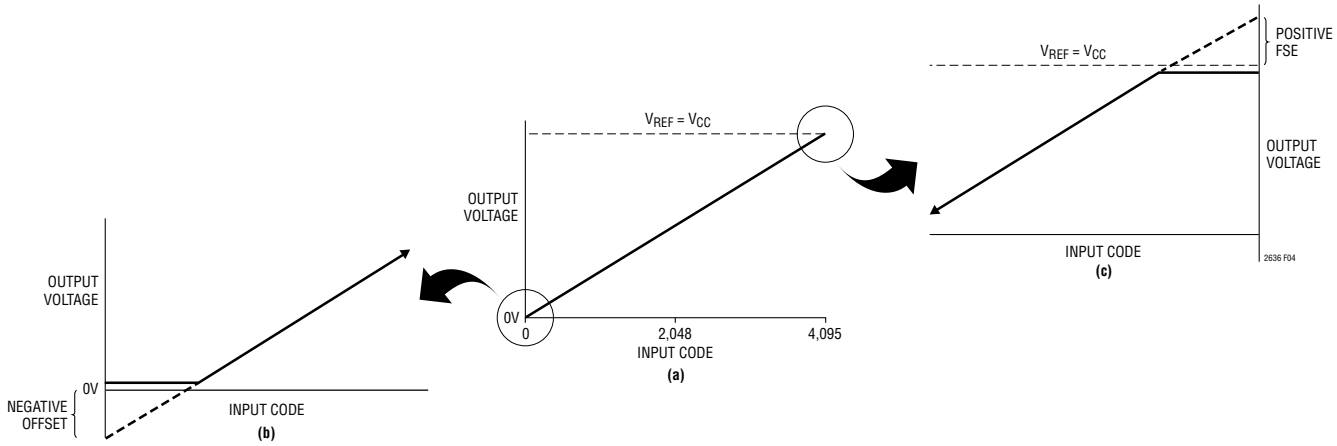



**Figure 4. Effects of Rail-to-Rail Operation On a DAC Transfer Curve (Shown for 12 Bits).**
**(a) Overall Transfer Function**
**(b) Effect of Negative Offset for Codes Near Zero**
**(c) Effect of Positive Full-Scale Error for Codes Near Full-Scale**

Rails vs. Output Current" in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

### Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit for the lowest codes as shown in Figure 4b. Similarly, limiting can occur near full-scale when the REF pin is tied to $V_{CC}$. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at $V_{CC}$, as shown in Figure 4c. No full-scale limiting can occur if $V_{REF}$ is less than $V_{CC}$–FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

### Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2636 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2636 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

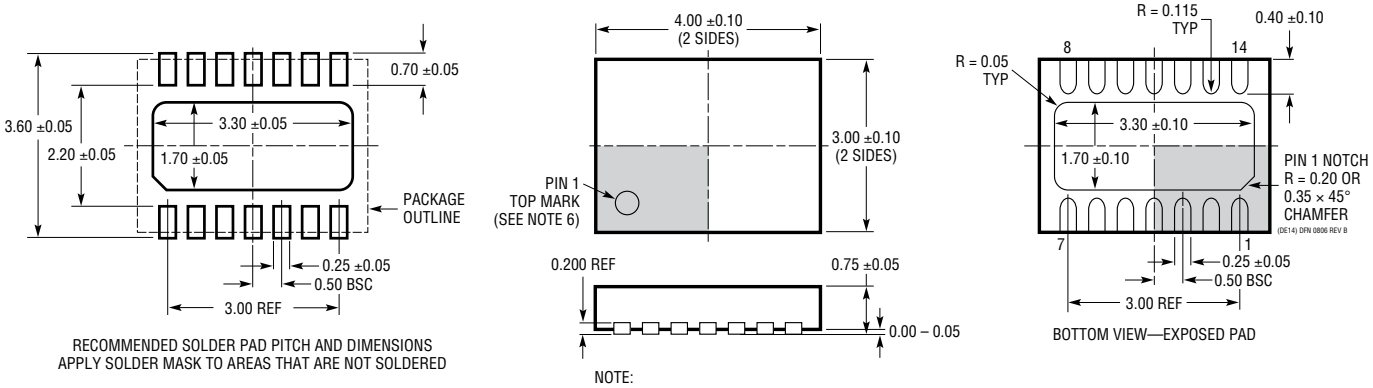
Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2636 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

# PACKAGE DESCRIPTION

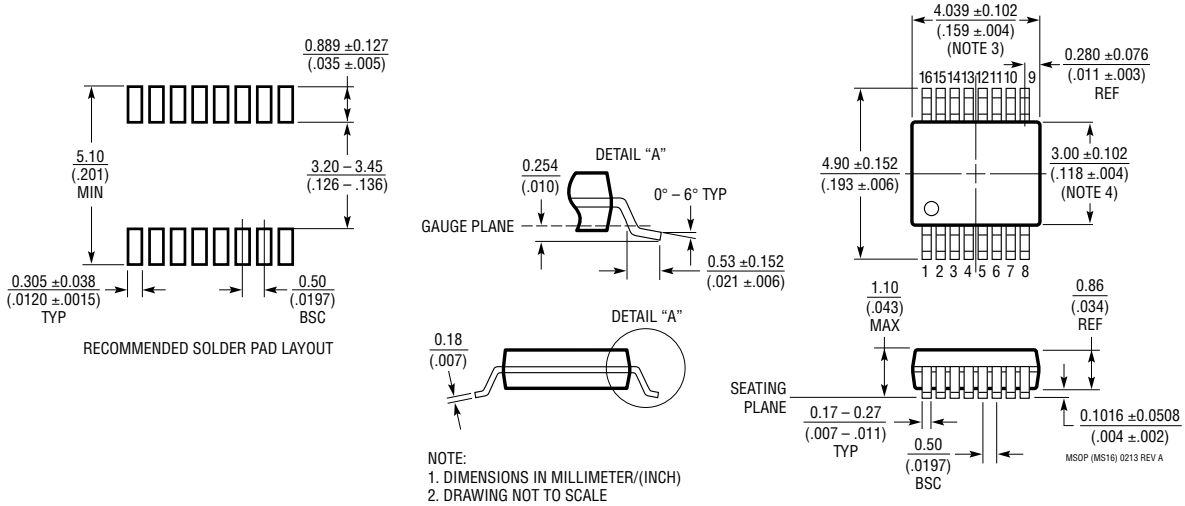
**Please refer to http://www.linear.com/product/LTC2636#packaging for the most recent package drawings.**

**DE Package**
**14-Lead Plastic DFN (4mm × 3mm)**
(Reference LTC DWG # 05-08-1708 Rev B)




NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

**MS Package**
**16-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1669 Rev A)




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

# REVISION HISTORY

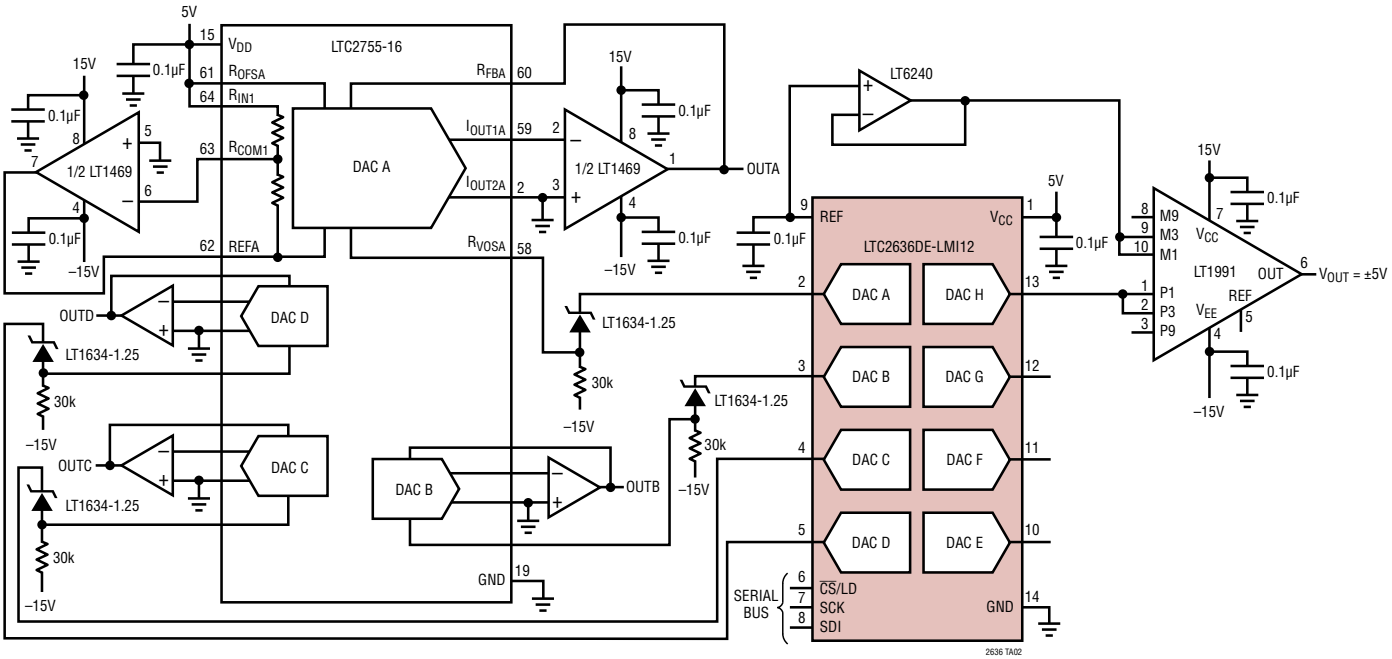
| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 12/09 | Update Electrical Characteristics. | 5, 6, 8 |
| B | 06/10 | Added details to Note 3.<br>Revised Typical Applications circuit. | 9<br>24 |
| C | 05/17 | Changed $V_{CC}$ slew rate number in Note 3. | 9 |
| D | 04/18 | Edits to Note 3. | 9 |



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## TYPICAL APPLICATION

**LTC2636 DACs Adjust LTC2755-16 Offsets, Amplified with LT1991 PGA to ±5V**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1660/LTC1665 | Octal 10/8-Bit $V_{OUT}$ DACs in 16-Pin Narrow SSOP | $V_{CC}$ = 2.7V to 5.5V, Micropower, Rail-to-Rail Output |
| LTC1664 | Quad 10-Bit $V_{OUT}$ DAC in 16-Pin Narrow SSOP | $V_{CC}$ = 2.7V to 5.5V, Micropower, Rail-to-Rail Output |
| LTC2600/LTC2610/ LTC2620 | Octal 16-/14-/12-Bit $V_{OUT}$ DACs in 16-Lead Narrow SSOP | 250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface |
| LTC2601/LTC2611/ LTC2621 | Single 16-/14-/12-Bit $V_{OUT}$ DACs in 10-Lead DFN | 300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface |
| LTC2602/LTC2612/ LTC2622 | Dual 16-/14-/12-Bit $V_{OUT}$ DACs in 8-Lead MSOP | 300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface |
| LTC2604/LTC2614/ LTC2624 | Quad 16-/14-/12-Bit $V_{OUT}$ DACs in 16-Lead SSOP | 250µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface |
| LTC2605/LTC2615/ LTC2625 | Octal 16-/14-/12-Bit $V_{OUT}$ DACs with $I^2C$ Interface | 250µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, $I^2C$ Interface |
| LTC2606/LTC2616/ LTC2626 | Single 16-/14-/12-Bit $V_{OUT}$ DACs with $I^2C$ Interface | 270µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, $I^2C$ Interface |
| LTC2609/LTC2619/ LTC2629 | Quad 16-/14-/12-Bit $V_{OUT}$ DACs with $I^2C$ Interface | 250µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output with Separate $V_{REF}$ Pins for Each DAC |
| LTC2630 | Single 12-/10-/8-Bit $V_{OUT}$ DACs with 10ppm/°C Reference in SC70 | 180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Rail-to-Rail Output, SPI Interface |
| LTC2631 | Single 12-/10-/8-Bit $I^2C$ $V_{OUT}$ DACs with 10ppm/°C Reference in ThinSOT | 180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Selectable External Ref. Mode, Rail-to-Rail Output, $I^2C$ Interface |
| LTC2640 | Single 12-/10-/8-Bit $V_{OUT}$ DACs with 10ppm/°C Reference in ThinSOT | 180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Selectable External Ref. Mode, Rail-to-Rail Output, SPI Interface |


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