December 1, 2011

LM10503

Triple Buck Converter Energy Management Unit (EMU) with PowerWise® 2.0 Adaptive Voltage Scaling (AVS) and ADC

General Description

LM10503 is an advanced EMU containing three configurable, high-efficiency bucks for supplying variable voltages to a diverse range of applications. The device is ideal for supporting ASIC and SOC designs which use voltage scaling for reducing power consumption.

The device is digitally controlled via the PWI® 2.0 open-standard interface. LM10503 operates cooperatively with a PowerWise® technology-compatible ASIC to optimize the supply voltage adaptively (AVS - Adaptive Voltage Scaling) over process and temperature variations. It also supports dynamic voltage-scaling (DVS) using frequency/voltage pairs from pre-characterized look-up tables.

Key Specifications

- Single input rail with wide range: 3.0V - 5.5V
- Buck 1 (AVS): Programmable output: 0.7V - 1.2V, 2A
- Bucks 2 & 3: Adjustable output: 1.0V - 3.5V, 1A
- ±2% Feedback voltage accuracy
- Up to 96% peak efficiency buck regulators
- 2MHz switching frequency for smaller inductor size
- LLP-36 package (36 pins, 6mm x 6mm x 0.8mm, 0.5mm pitch)

Features

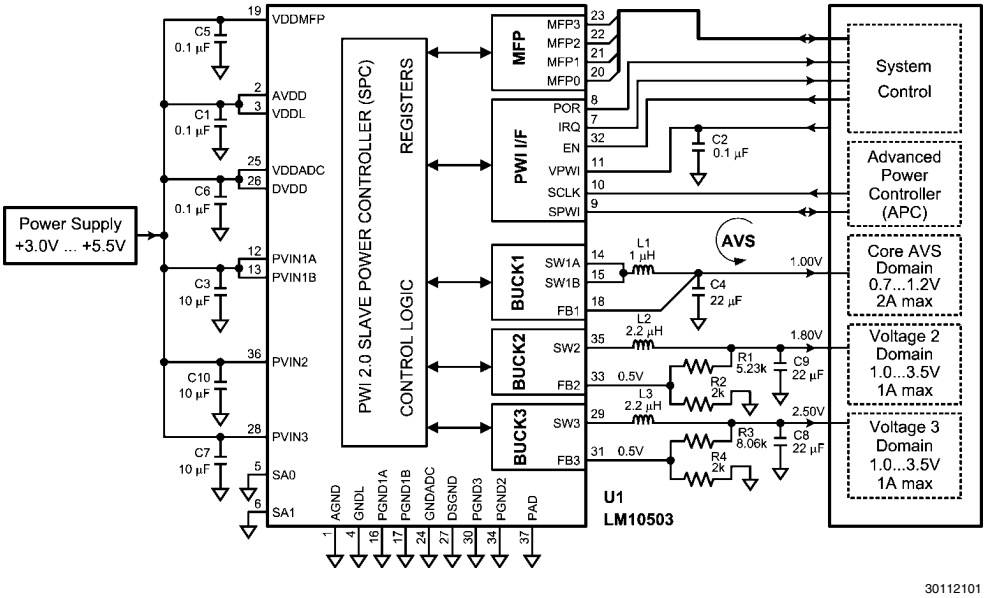
- Three high-efficiency programmable bucks:
  - Integrated FETs with low R_{DSON}
  - Bucks operate at 120° phase to reduce the input current ripple and capacitor size
  - Input Under Voltage Lock-out
  - Enable pin and internal soft start
  - Current overload and thermal shutdown
- 4-Channel Multi-Function Port (MFP) that includes:
  - 8-bit ADC with integrated reference
  - Comparator Input/General Purpose Output
  - Interrupt request output with multiple sources
- PWI® 2.0 Open-Standard Interface
- Power-On Reset (POR) open-drain output with delay
- LM10503-1 with start-up sequence option

Applications

The LM10503 and LM10503-1 are suitable for applications that require multiple supplies in the range of 0.7 to 3.5V and up to 2A:

- Point of Load Regulation for ASICs
- NVM Memory drives (HDD or FLASH)
- Servers and Networking Cards
- PCI cards, Set-Top-Box Processors
- Video Processors and Graphic Cards
- High-Performance Medical and Industrial Processors

Typical Application Circuit



30112101

Overview

The device contains three buck converters. The table below lists the output characteristics of the three converters.

SUPPLY SPECIFICATIONS

Supply	Output Voltage Range (V)	Output Voltage Programming Resolution (mV)	Maximum Output Current (A)	Typical Application
VSW1	0.700 to 1.208	4	2	Core Voltage Scaling Domain
VSW2,3	1.000 to 3.500	N/A	1	I/O, aux voltage

Connection Diagrams and Package Mark Information

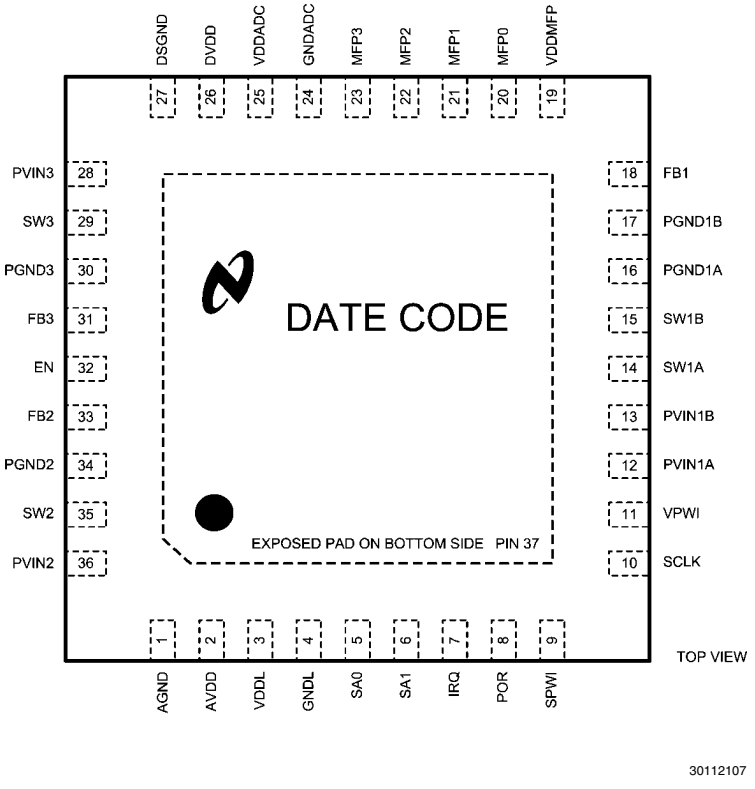


FIGURE 1. LLP-36 Package Number SQA36A
36 Pins, 6x6x0.8mm, 0.5mm pitch

Note: The actual physical placement of the package marking will vary from part to part.

DATE CODE: UZXYTT format: 'U' - wafer fab code; 'Z' - assembly plant code; 'XY' - 2-digit date code; and 'TT' - die run code. See http://www.national.com/quality/marking_conventions.html for more information on marking conventions.

Ordering Information

Order Number	Ordering Spec	Package Marking	Supplied As
LM10503SQE/NOPB	NOPB	LM10503	250 units Tape and Reel
LM10503SQ/NOPB		LM10503	1000 units Tape and Reel
LM10503SQX/NOPB		LM10503	2500 units Tape and Reel
LM10503SQ/S7002726	S7002726	10503-1	1000 units Tape and Reel
LM10503SQX/S7002727	S7002727	10503-1	2500 units Tape and Reel

Pin Descriptions

Pin #	Pin Name	I/O	Type	Functional Description	
1	AGND	G	G	Analog ground for Bucks 1, 2 and 3	
2	AVDD	P	P	Analog power for Bucks 1, 2 and 3	
3	VDDL	P	P	Power for logic block	
4	GNDL	G	G	Ground for logic block	
5	SA0	I	D	PWI Slave Address Bit 0. Tie to ground or VPWI for '0' or '1, respectively.	
6	SA1	I	D	PWI Slave Address Bit 1. Tie to ground or VPWI for '0' or '1, respectively.	
7	IRQ	O	OD	Interrupt request. This open drain output is asserted low on an interrupt event.	
8	POR	O	OD	Power On Reset. This open drain output is asserted low on reset.	
9	SPWI	I/O	D	PowerWise Interface (PWI) bi-directional data	
10	SCLK	I	D	PowerWise Interface (PWI) clock input	
11	VPWI	P	P	Power supply voltage input for PWI and logic interfaces	
12	PVIN1A	P	P	Power supply voltage input for power stage PFET	Buck #1
13	PVIN1B	P	P	Power supply voltage input for power stage PFET	
14	SW1A	O	O	Switching node, connect to inductor	
15	SW1B	O	O	Switching node, connect to inductor	
16	PGND1A	G	G	Power ground, connect to system ground.	
17	PGND1B	G	G	Power ground, connect to system ground.	
18	VFB1	I	A	Feedback input	
19	VDDMFP	P	P	Power supply voltage input for the multifunction pins, GPO mode.	
20	MFP0	I/O	A/D	Multifunction pin, ADC input, comparator input, GPO, channel 0	
21	MFP1	I/O	A/D	Multifunction pin, ADC input, comparator input, GPO, channel 1	
22	MFP2	I/O	A/D	Multifunction pin, ADC input, comparator input, GPO, channel 2	
23	MFP3	I/O	A/D	Multifunction pin, ADC input, comparator input, GPO, channel 3	
24	GNDADC	G	G	Ground for ADC. Connect to system Ground.	
25	VDDADC	P	P	Power for ADC	
26	DVDD	P	P	Power for digital block of Bucks 1, 2 and 3	
27	DSGND	G	G	Ground for digital block of Bucks 1, 2 and 3	
28	PVIN3	P	P	Power supply voltage input for power stage PFET	Buck #3
29	SW3	O	O	Switching node, connect to inductor.	
30	PGND3	G	G	Power ground, connect to system ground.	
31	VFB3	I	A	Feedback input	
32	EN	I	D	Enable input. Set this digital input high for normal operation.	
33	VFB2	I	A	Feedback input	Buck #2
34	PGND2	G	G	Power ground, connect to system ground.	
35	SW2	O	O	Switching node, connect to inductor.	
36	PVIN2	P	P	Power supply voltage input for power stage PFET	
37	PAD	G	G	Exposed pad, connect to system ground	

A: Analog Pin **D: Digital Pin** **G: Ground Pin** **P: Power Pin**
I: Input Pin **I/O: Input/Output Pin** **O: Output Pin** **OD: Open Drain Output Pin**

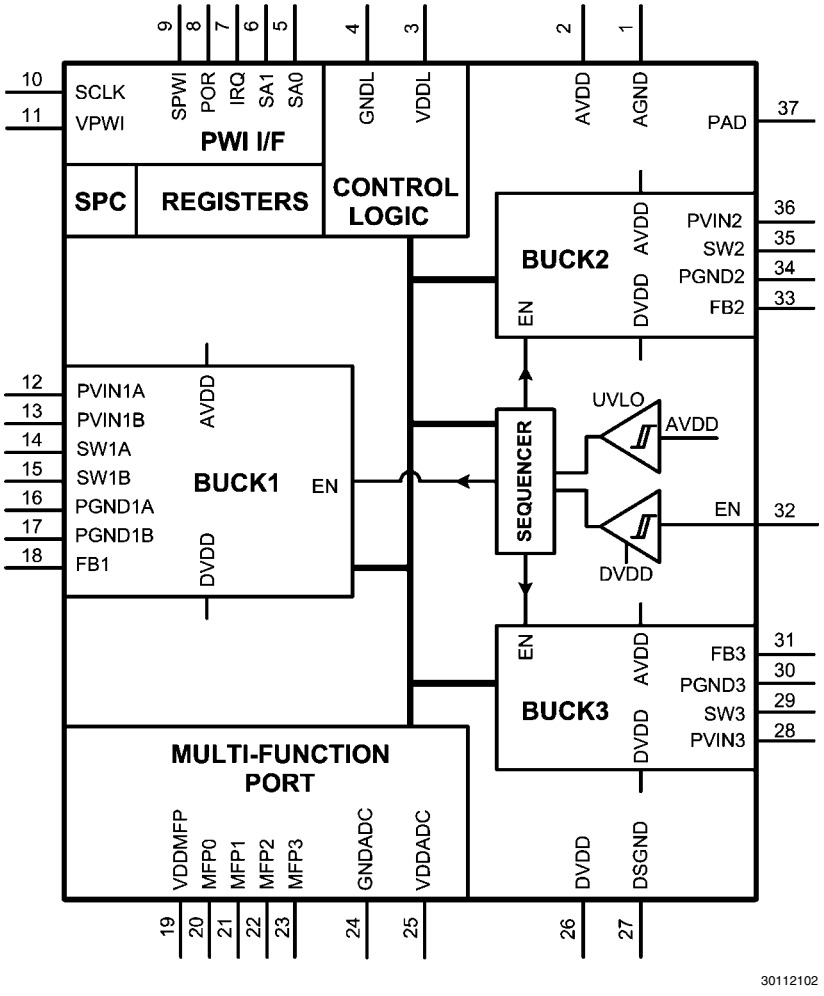


FIGURE 2. Simplfied Block Diagram

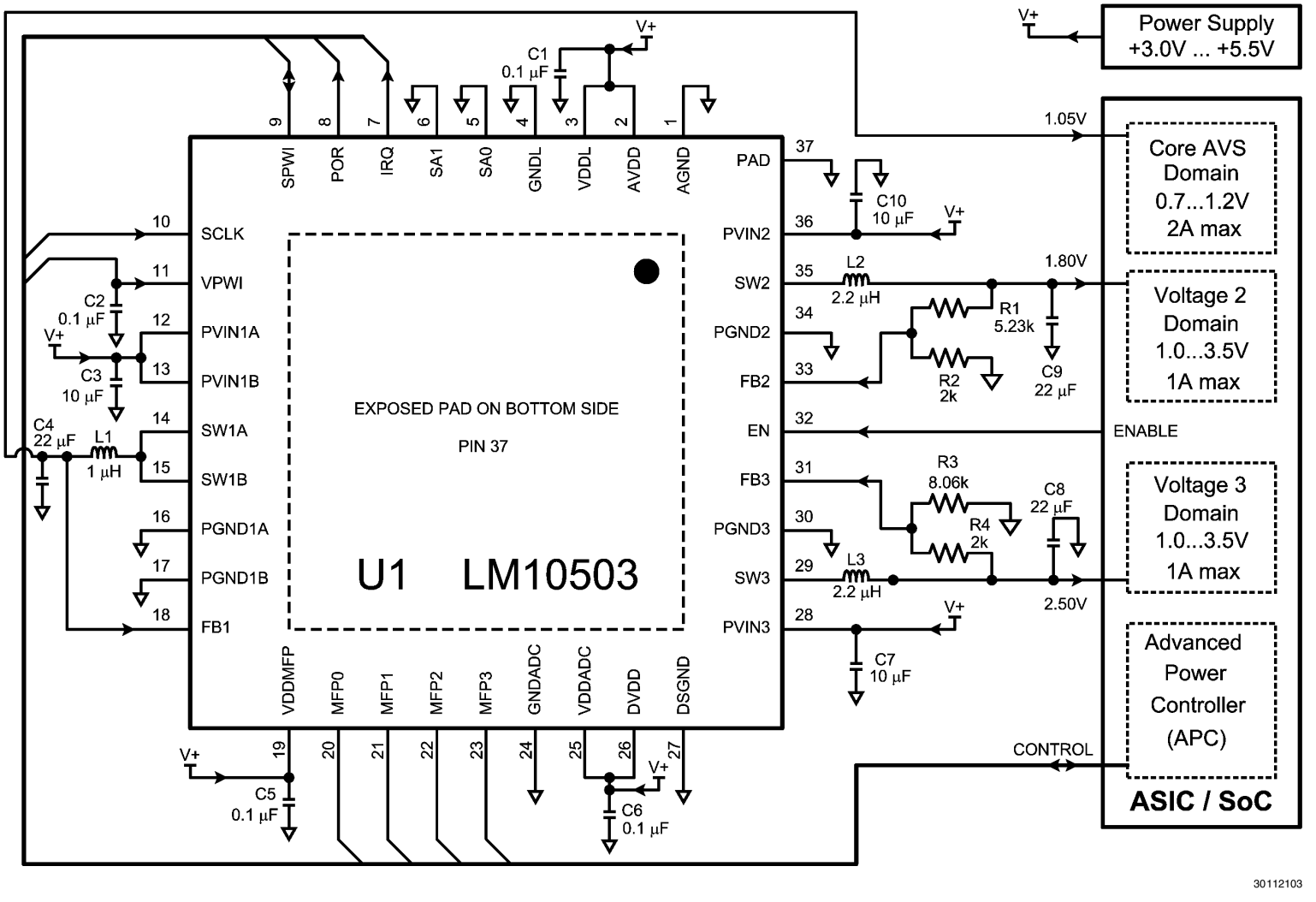


FIGURE 3. Typical Application Circuit (Detailed)

Absolute Maximum Ratings (, , , ,)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Any supply pin (VIN) to GND, Note 3.	-0.3 to +6.5V
Any signal pin, VPWI, VDDMFP	-0.3 to +(VIN +0.3V) but not over 6.5V
Between any GND pins ( )	-0.3 to +0.3V
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering 4 sec)	+260°C

ESD Ratings ( )

Human Body Model	2000V
Machine Model	200V

Recommended Operating Ratings

(, , ,)

VIN	3.0V to 5.5V
VPWI ( )	1.62V to 3.63V but not over VIN
VDDMFP ( )	1.62V to VIN
VFB1,2,3	0 to VOUT1,2,3
EN	0 to VIN
MFP0-3	0 to VDDMFP
SPWI, SCLK, SA0-1, POR, IRQ	0 to VPWI
Junction Temperature (T_J) Range	-40°C to +105°C
Ambient Temperature (T_A) Range (, , ,)	-40°C to +70°C
Maximum Continuous Power Dissipation (P_{D-MAX}) (, , ,)	1.33W

Thermal Properties

(, , ,)

Junction-to-Case Thermal Resistance (θ_{JC})	2.2°C/W
Junction-to-Board Thermal Resistance (θ_{JA})	12.4°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA})	27.0°C/W

General Electrical Characteristics (,)

Unless otherwise noted, V_{IN}= 5.0V where: V_{IN}=AVDD=VDDL=VDDADC=DVDD=VDDMFP=PVIN1A=PVIN1B=PVIN2=PVIN3, except VPWI=2.5V. The application circuit used is the one shown in . Limits in standard type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range −40°C ≤ T_J ≤ +105°C.

Symbol	Parameter	Conditions	Min	TYP	Max	Units
$I_{Q-VIN-SD}$	Quiescent supply current of all VIN supply pins combined; part is shut down	Device is shut down by: a) driving EN pin low or b) issuing the Shutdown Command		2	**20**	µA
$I_{Q-VIN-NO-LOAD}$	Quiescent supply current of all VIN supply pins combined; part is enabled, but not loaded	Switching in forced PWM, ADC disabled, MFP pins set as inputs, driven LOW		16	**25**	mA
$I_{Q-VPWI-SD}$	Quiescent supply current of VPWI supply pin; part is shut down	Device is shut down by: a) driving EN pin low or b) issuing the Shutdown Command		0.1	**1**	µA
$I_{Q-VPWI-IDLE}$	Quiescent supply current of VPWI supply pin; part is enabled, PWI bus is idle	Device is enabled, PWI bus is idle (no load on SPWI, SCLK)		0.1	**1**	
F_{SW}	Switching Frequency of all 3 bucks	PWM-mode measured at SW1, 2, 3 pins, 120° out of phase (by design)	1.75	2.00	2.30	MHz
$T_{POR-DELAY}$	Delay from EN-pin rising edge to POR-pin rising edge	All 3 bucks are unloaded		53		ms

Symbol	Parameter	Conditions	Min	TYP	Max	Units
EN, FB PINS						
T_{EN_LOW}	EN pin minimum low pulse	To trigger a startup sequence	100			nS
V_{IL-EN}	EN pin logic low input	VIN = 5V			**0.2**	V
V_{IH-EN}	EN pin logic high input		**2.0**			
I_{IH-EN}	EN pin input current, driven high	V_EN = VIN		+0.1	**+1**	µA
I_{IL-EN}	EN pin input current, driven low	V_EN = 0.0V	**–1**	–0.1		
$V_{IL_UVLO-AVDD}$	UVLO falling threshold	Measured on AVDD pin ramping, monitored at POR pin.	**2.4**	2.6		V
$V_{IH_UVLO-AVDD}$	UVLO rising threshold			2.8	**2.9**	
$V_{HYST_UVLO-AVDD}$	UVLO hysteresis window			0.24		
V_{POR-L}	POR pin is asserted when target voltage of Buck1 or 2 or 3 is lower than this level	Percentage values with respect to target values of $V_{FB1,2,3}$ monitored at the respective buck outputs		85		%
V_{POR-H}	POR pin is de-asserted when target voltage of Buck1 and 2 and 3 is higher than this level			94		
SPWI, SCLK, SA1-0, IRQ, POR PINS (These pins are powered from VPWI.)						
V_{IL}	Logic Input Low	SPWI, SCLK, SA1-0 pins			**30%**	VPWI
V_{IH}	Logic Input High		**70%**			
I_{IL}	Input Current, pin driven low	SPWI, SCLK, SA1-0 pins	**–2**			µA
I_{IH}	Input current, pin driven high (VPWI)	SA1-0 pins			**+2**	µA
		SPWI & SCLK have internal pulldown			**+5**	
V_{OL}	Logic Output Low	SPWI, IRQ, POR for $I_{SINK} \leq 2mA$			**0.2**	VPWI
					20%	
V_{OH}	Logic Output High	SPWI for $I_{SOURCE} \leq 2mA$	**80%**			
I_{OZ}	Output Leakage Current	IRQ, POR pins when open drain	**–2**		**+2**	µA
MFP0-3 PINS (Pins used in General Purpose Outputs (GPO) or comparator inputs; these pins are powered from VDDMFP)						
I_{IL}	Input current, pin driven low	Open drain or comparator input mode	**–2**			µA
I_{IH}	Input current, pin driven high (VDDMFP)				**+2**	
V_{OL}	Logic Output Low	Pin in GPO mode, $I_{SINK} \leq 1mA$			**0.2**	V
V_{OH}	Logic Output High	Pin in GPO mode, $I_{SOURCE} \leq 1mA$	**VDDMFP-0.2**			
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature			160		°C
$T_{SD-HYST}$	Thermal Shutdown Hysteresis			20		

Buck 1 Electrical Characteristics (, ,)

Unless otherwise noted, V_{IN}= 5.0V where: V_{IN}=AVDD=VDDL=VDDADC=DVDD=VDDMFP=PVIN1A=PVIN1B=PVIN2=PVIN3, except VPWI=2.5V. The application circuit used is the one shown in . Limits in standard type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range −40°C ≤ T_J ≤ +105°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{Q\text{-}NO\text{-}LOAD}$	Quiescent supply current of PVIN1A and PVIN1B pins combined	Buck 1 is enabled, but not loaded, V_{OUT1} = 1.05V, switching in PWM		1	**3**	mA
$I_{OUT\text{-}MAX}$	Continuous maximum load current	Buck 1 is enabled, V_{OUT1} = 1.05V, switching in PWM*	**2**			A
I_{PEAK}	Peak switching current limit	Buck 1 is enabled, V_{OUT1} = 1.05V, switching in PWM	**2.33**	2.75	**3.90**	
$\eta_{SW1\text{-}3V}$	Efficiency peak	V_{IN} = 3.3V, V_{OUT} = 1.05V, I_{OUT} = 0.2A		92%		%
$\eta_{SW1\text{-}5V}$		V_{IN} = 5V, V_{OUT} = 1.05V, I_{OUT} = 1A		82%		
C_{IN}	Input Capacitor	0mA ≤ I_{OUT} ≤ $I_{OUT\text{-}MAX}$	7	10		µF
C_{OUT}	Output Filter Capacitor		14	22	100	
	Output Filter Capacitor ESR		0		20	mΩ
L	Output Filter Inductance			1		µH
$V_{OUT\text{-}TOP}$	Output voltage top range, with Register R0 = 7Fh	Feedback pin connected to V_{OUT} V_{OUT} = $V_{OUT\text{-}TOP}$, I_{OUT} = 0.1*$I_{OUT\text{-}MAX}$		1.208		V
$V_{FB\text{-}TOP\text{-}TOL}$	Feedback pin voltage tolerance		**-2%**		**+2.5**	%
$V_{OUT\text{-}DEFAULT}$	Output voltage, power-up default	Feedback pin connected to V_{OUT} V_{OUT} = $V_{OUT\text{-}DEFAULT}$, I_{OUT} = 0.1*$I_{OUT\text{-}MAX}$		1.05		V
$V_{FB\text{-}DEFAULT\text{-}TOL}$	Feedback pin voltage tolerance		**-2%**		**+2**	%
$V_{OUT\text{-}BOTTOM}$	Output voltage bottom range, with Register R0 = 00h	Feedback pin connected to V_{OUT} V_{OUT} = $V_{OUT\text{-}BOTTOM}$, I_{OUT} = 0.1*$I_{OUT\text{-}MAX}$		0.7		V
$V_{FB\text{-}BOTTOM\text{-}TOL}$	Feedback pin voltage tolerance		**-2%**		**+2.5**	%
ΔV_{OUT}	DC Line regulation	3V ≤ V_{IN} ≤ 5V, V_{OUT} = $V_{OUT\text{-}DEFAULT}$, I_{OUT} = 0.5 * $I_{OUT\text{-}MAX}$		0.2		%/V
	DC Load regulation	V_{IN} = 5V, V_{OUT} = $V_{OUT\text{-}DEFAULT}$, 0.1 * $I_{OUT\text{-}MAX}$ ≤ I_{OUT} ≤ $I_{OUT\text{-}MAX}$		0.1		%/A
I_{FB}	Feedback pin input bias current	V_{FB} = 1.208V ; (pin has internal resistor divider)		2.3	5	µA
$R_{DS\text{-}ON\text{-}HS}$	High Side Switch On Resistance	Measured pin-to-pin		50	**105**	mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low Side Switch On Resistance			65	**100**	
$T_{SCALING}$	V_{OUT} Scaling Step Time	100 mV steps on V_{SW1}, $C_{OUT\text{-}TOTAL}$ = 22 µF		25		µS
STARTUP						
T_{START}	Internal soft-start (turn on time)			0.5		ms

* Specification guaranteed by design. Not tested during production.

Bucks 2 and 3 Electrical Characteristics (, ,)

Unless otherwise noted, V_{IN}= 5.0V where: V_{IN}=AVDD=VDDL=VDDADC=DVDD=VDDMFP=PVIN1A=PVIN1B=PVIN2=PVIN3, except VPWI=2.5V. The application circuit used is the one shown in . Limits in standard type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range –40°C ≤ T_J ≤ +105°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{Q\text{-}NO\text{-}LOAD\text{-}2}$	Quiescent supply current off PVIN2 pin	Buck 2 is enabled, but not loaded, switching in PWM		3	**8**	mA
$I_{Q\text{-}NO\text{-}LOAD\text{-}3}$	Quiescent supply current of PVIN3 pin	Buck 3 is enabled, but not loaded, switching in PWM		3	**8**	
$I_{OUT\text{-}MAX}$	Continuous maximum load current	Bucks 2 and 3 are enabled, switching in PWM*	**1**			A
I_{PEAK}	Peak switching current limit	Bucks 2 and 3 are enabled, switching in PWM	**1.25**	1.5	**1.75**	
$\eta_{SW2\text{-}5V}$	Efficiency peak, Buck 2	I_{OUT} = 0.4A, V_{IN} = 5.0V		92%		%
$\eta_{SW2\text{-}3.3V}$		I_{OUT} = 0.2A, V_{IN} = 3.3V		93%		
$\eta_{SW3\text{-}5V}$	Efficiency peak, Buck 3	I_{OUT} = 0.3A, V_{IN} = 5.0V		94%		%
$\eta_{SW3\text{-}3.3V}$		I_{OUT} = 0.2A, V_{IN} = 3.3V		97%		
C_{IN}	Input Capacitor	0mA ≤ I_{OUT} ≤ $I_{OUT\text{-}MAX}$	7	10		µF
C_{OUT}	Output Filter Capacitor		14	22	100	
	Output Filter Capacitor ESR		0		20	mΩ
L	Output Filter Inductance			1		µH
V_{FB}	Feedback voltage	I_{OUT} = 0.1*$I_{OUT\text{-}MAX}$, Output voltage set using external resistor divider to 1.0V...3.5V		0.5		V
$V_{FB\text{-}TOL}$	Feedback pin voltage tolerance		**-2%**		**+2**	%
$V_{OUT\text{-}TOP}$	Output voltage highest setting using external resistor divider	All supplies = 4.2 - 5.5V, I_{OUT} = 0 - $I_{OUT\text{-}MAX}$		3.5		V
$V_{OUT\text{-}BOTTOM}$	Output voltage lowest setting using external resistor divider	All supplies = 3.0 - 5.5V, I_{OUT} = 0 - $I_{OUT\text{-}MAX}$		1.0		
ΔV_{OUT}	DC Line regulation	3.3V ≤ V_{IN} ≤ 5V, I_{OUT} = $I_{OUT\text{-}MAX}$		0.2		%/V
	DC Load regulation	V_{IN} = 5V, 0.1 * $I_{OUT\text{-}MAX}$ ≤ I_{OUT} ≤ $I_{OUT\text{-}MIN}$		0.3		%/A
I_{FB}	Feedback pin input bias current	V_{FB} = 0.5V		0.1	1	µA
$R_{DS\text{-}ON\text{-}HS}$	High Side Switch On Resistance	Measured pin-to-pin		170	**300**	mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low Side Switch On Resistance			125	**190**	
STARTUP						
T_{START}	Start up from shutdown, V_{OUT} = 0V, no load, LC = recommended circuit, using software enable to V_{OUT} = 95% of final value			0.5		ms

* Specification guaranteed by design. Not tested during production.

ADC and Comparators Electrical Characteristics (, ,)

Unless otherwise noted, V_{IN}= 5.0V where: V_{IN}=AVDD=VDDL=VDDADC=DVDD=VDDMFP=PVIN1A=PVIN1B=PVIN2=PVIN3, except VPWI=2.5V. The application circuit used is the one shown in . Limits in standard type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full operating junction temperature range −40°C ≤ T_J ≤ +105°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{QSC-ADC-0}$	VDDADC pin quiescent current, part disabled	EN pin LOW		0.1	10	µA
$I_{QSC-ADC-1}$	VDDADC pin quiescent current, part enabled but ADC not enabled	EN pin HIGH, ADCEN=0		45		
I_{ADC-0}	VDDADC pin operating current with ADC enabled but not converting	EN pin HIGH, ADCEN=1, ADCSTART=0		260		
I_{ADC-1}	VDDADC pin operating current with ADC enabled and converting	EN pin HIGH, ADCEN=1, ADCSTART=1		150		
V_{REF}	Internal Reference Voltage	T = 25°C	1.220	1.225	1.230	V
		T= 0 to 105°C	**1.200**	1.225	**1.250**	
INL	Core ADC integral non-linearity	V_{REF} = 1.225*	-2		+2	LSB
DNL	Core ADC differential non-linearity	V_{REF} = 1.225*	-0.5		0.5	LSB
$V_{ADC_IN_TOP}$	ADC input voltage range, top			2 * V_{REF}		V
$V_{ADC_IN_BOTTOM}$	ADC input voltage range, bottom			V_{REF}		V
t_{CONV}	Conversion time				5	ms
$t_{WARM-REF}$	Warm-up time of reference	After EN pin high (Note 1)		2		ms
tu	Warm-up time of ADC	After enabling the ADC (Note 1)		2		ms
COMPARATOR (The comparators use the same reference as the ADC.)						
$I_{Q-VDDMFP}$	Quiescent current of VDDMFP pin	MFP pins are configured as comparator inputs, all grounded		0.1	1	µA
$V_{_comp_rise}$	Comparator rising edge trigger level	Hysteresis window bits CMPxHYS are 0.		V_{REF}		V
$V_{_comp_fall}$	Comparator falling edge trigger level			V_{REF}-0.08		
$V_{_comp_rise}$	Comparator rising edge trigger level	Hysteresis window bits CMPxHYS are 1.		V_{REF}		V
$V_{_comp_fall}$	Comparator falling edge trigger level			V_{REF}-0.05		

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: refers to these power pins connected together: AVDD = VDDL = VDDADC = DVDD = PVIN1A = PVIN1B = PVIN2 = PVIN3

Note 4: means all ground pins must be connected together: AGND = GNDL = PGND1A = PGND1B = GNDADC = DSGND = PGND3 = PGND2 = PAD.

Note 5: include SW1-3, SA0-1, IRQ, POR, SPWI, SCLK, FB1-3, MFP0-3 and EN.

Note 6: VPWI, VDDMFP sequencing requirements: voltage on VPWI and VDDMFP must be less than, or equal to, VIN, including during ramp up and ramp down of power supplies.

Note 7: Applies to all pins. The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin (MIL-STD-883 3015.7). The Machine Model (MM) is a 200 pF capacitor discharged directly into each pin (EAIJ).

Note 8: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187 Leadless Leadframe Package (LLP) http://www.national.com/an/AN/AN-1187.pdf.

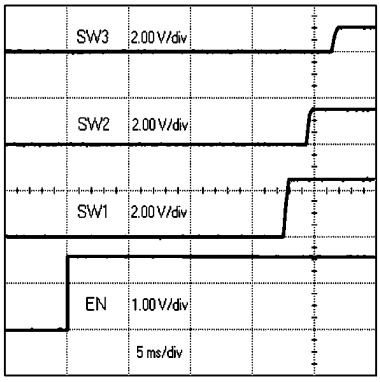
Note 9: The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, (1) where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)

Note 10: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 105°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$) and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$.

Note 11: θ_{JC} refers to the bottom metal surface of the LLP as the CASE. θ_{JB} is the junction-to-board thermal resistance. Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result and is based on a power dissipation of 1.33W, using a 4-layer FR-4 standard JEDEC thermal test board (4LJEDEC): 4"x3" (102 mm x 76 mm x 1.6 mm) in size. Ambient temperature in simulation is 22°C, under stationary airflow condition. The board has 2 internal copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one are: 36/18/18/36 [µm] (2/1/1/2 [oz]). A minimum number of 9 thermal vias are placed between the pad on the top side and the 2nd copper layer. Detailed description of the board can be found in JEDEC standard JESD 51-7 (High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages) and JESD51-5 (Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms). The junction-to-ambient thermal resistance (θ_{JA}) is highly dependent on application and board layout. The value of θ_{JA} of this product can vary significantly, depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to Application Note 1187: Leadless Leadframe Package (LLP) and the Power Efficiency and Power Dissipation section of this datasheet.

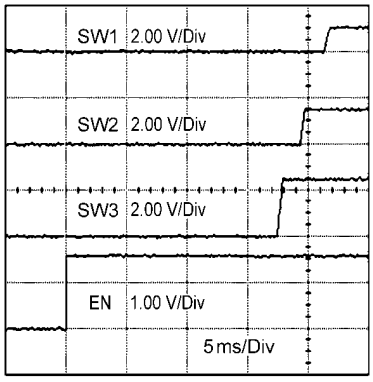
LM10503 - Typical Performance Characteristics

Power Up Sequence: LM10503-1



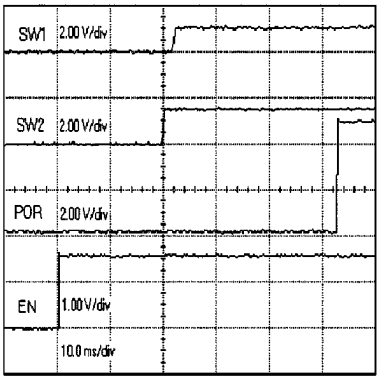
30112113

Power Up Sequence: LM10503



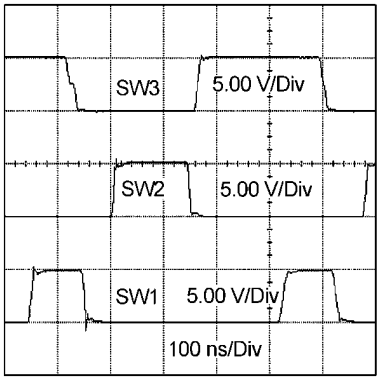
30112112

POR Pin Operation: LM10503



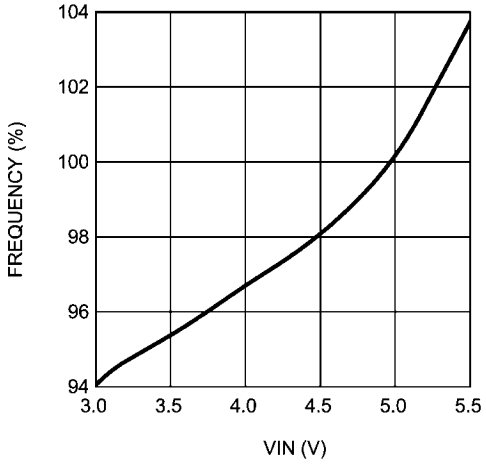
30112114

SW1, SW2 SW3 Phase Order



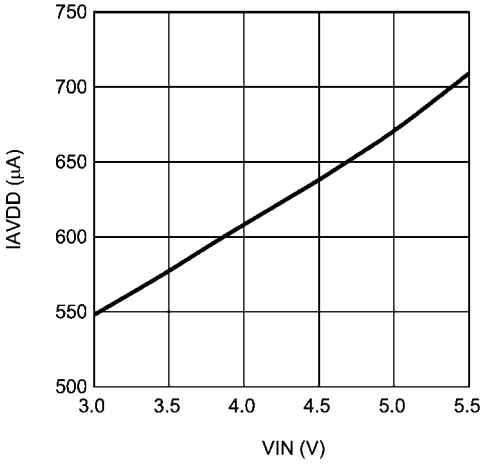
30112166

Switching Frequency vs. VIN Normalized to 2MHz



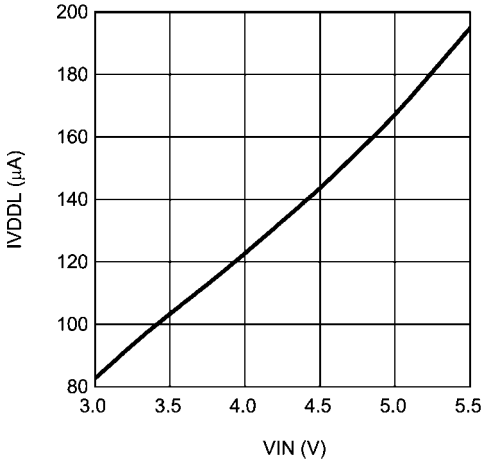
30112167

IAVDD vs. VIN



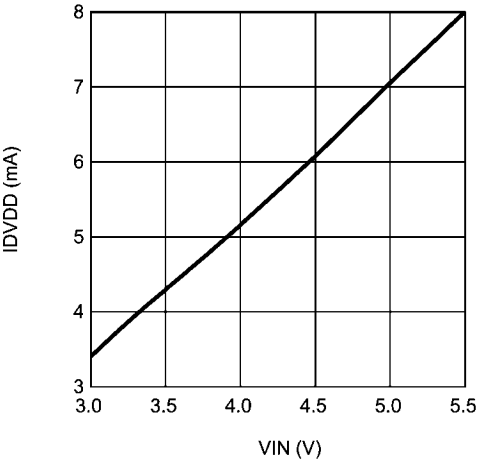
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IVDDL vs. VIN



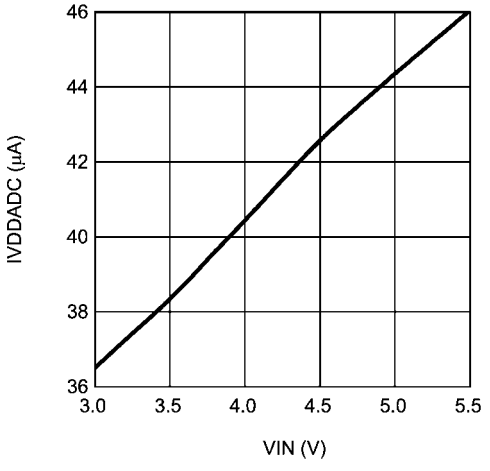
30112169

IDVDD vs. VIN



30112170

IVDDADC vs. VIN

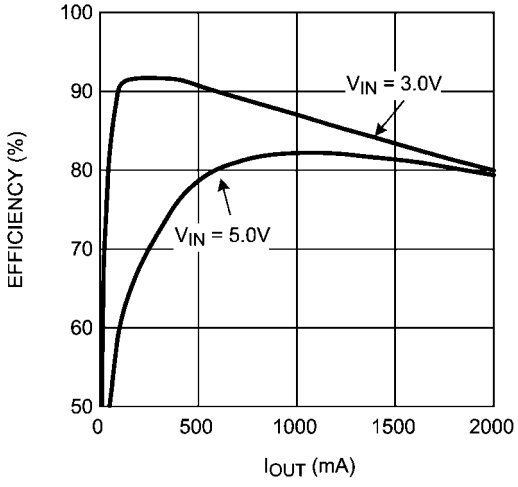


30112171

Typical Performance Characteristics Buck1

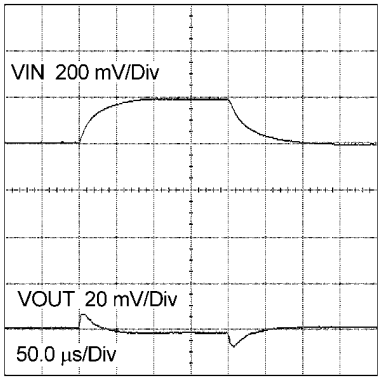
T_A = 25°C unless otherwise noted.

Efficiency: V_{OUT} = 1.05V



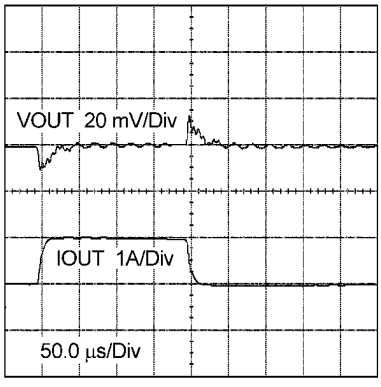
30112172

Line Transient: VIN = 3.2V - 3.4V Step, V_{OUT} = 1.05V, I_{OUT} = 1A



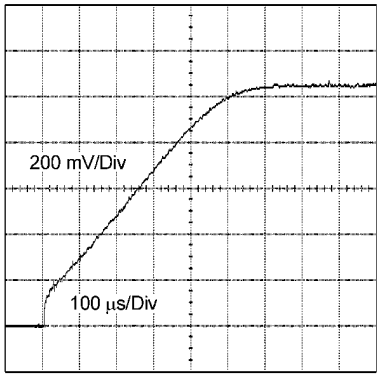
30112173

Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.05V I_{OUT}_step = 0.5A...1.5A



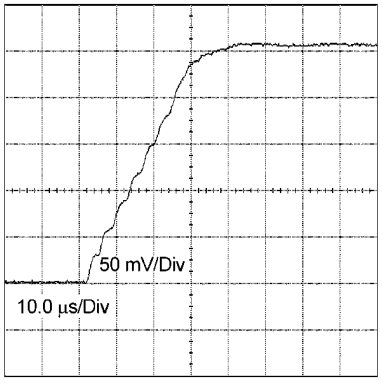
30112174

Startup, V_{OUT} = 1.05V, I_{OUT} = 2A



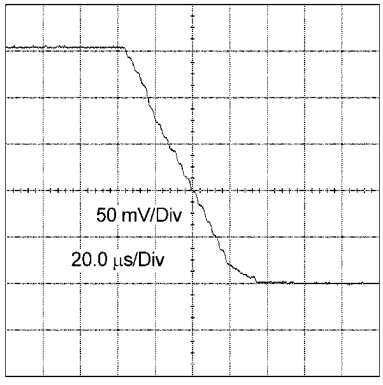
30112176

V_{OUT} Step-up Response to R0 MSB Change, V_{IN} = 5.0V, I_{OUT} = 2A



30112178

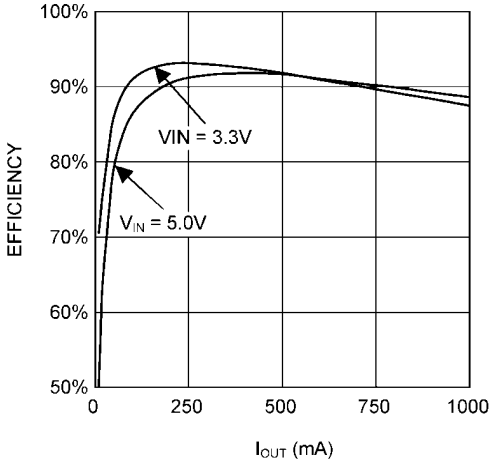
V_{OUT} Step-down Response to R0 MSB Change, V_{IN} = 5.0V, I_{OUT} = 2A



30112179

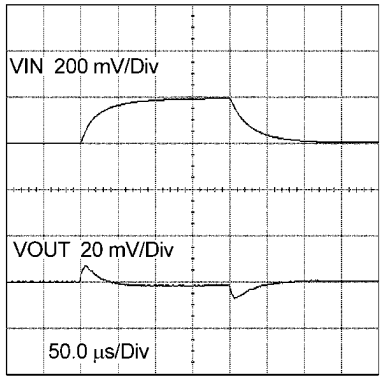
Typical Performance Characteristics, Buck 2

Efficiency: V_{OUT} = 1.8V



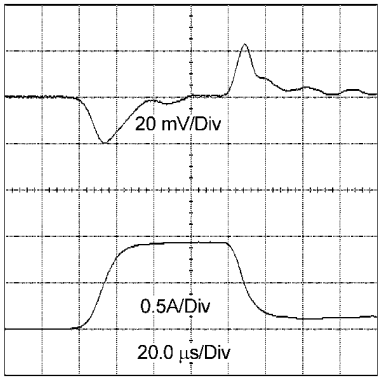
30112180

Line Transient: VIN = 3.2V - 3.4V Step, V_{OUT} = 1.8V, I_{OUT} = 1A



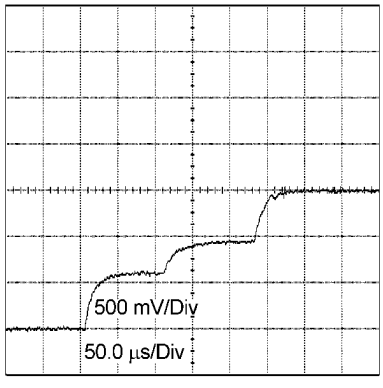
30112181

Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.8V I_{OUT}_step = 0A...1.0A



30112182

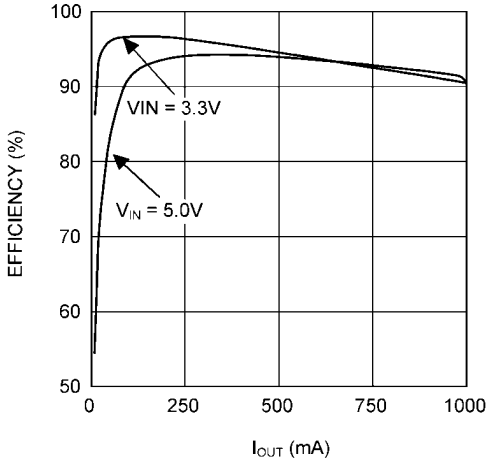
Startup, V_{OUT} = 1.5V



30112183

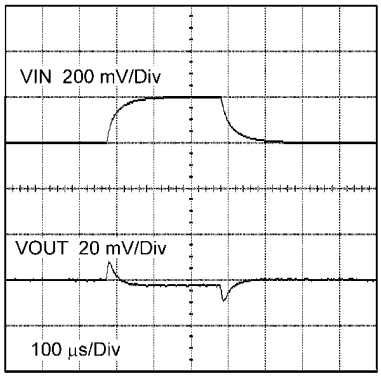
Typical Performance Characteristics, Buck 3

Efficiency: V_{OUT} = 2.5V



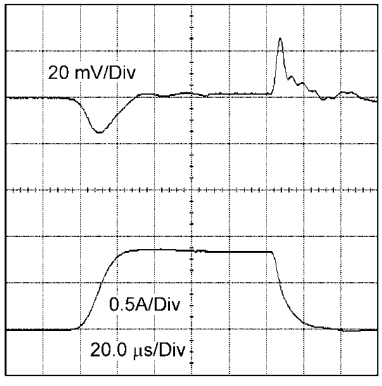
30112157

Line Transient: VIN = 3.2V - 3.4V Step, V_{OUT} = 2.5V, I_{OUT} = 1A



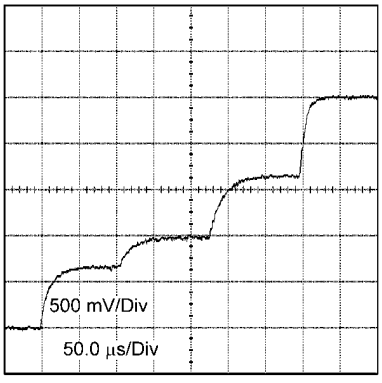
30112158

Load Transient: V_{IN} = 5.0V, V_{OUT} = 2.5V $I_{OUT_}$ step = 0A...1.0A



30112159

Startup, V_{OUT} = 2.5V, I_{OUT} = 1A



30112160

LM10503 General Description

LM10503 is a PWI 2.0 compliant Energy Management Unit for reducing power consumption of the digital core of Systems-on-a-Chip (SoCs), ASICs, and processors. It operates cooperatively with processors that incorporate National Semiconductor's Advanced Power Controller (APC) to provide Adaptive or Dynamic Voltage Scaling (AVS or DVS) which significantly improves the system efficiency when compared to fixed output voltage implementations.

The device incorporates three high-efficiency synchronous buck regulators that deliver three output voltages from a single power source. The device also includes a Multifunctional Block that comprises a 4-channel ADC, comparators and GPOs.

The following table summarizes the key features of the device:

TABLE 1. Feature Summary

Functionality	BUCK1	BUCK2	BUCK3
Power on output voltage default	1.05V	Configurable using an external resistor divider	
Output voltage, range minimum	0.7	1	1
Output voltage, range maximum	1.2	3.5	3.5
Output voltage programming resolution	4mV	N/A	N/A
Output voltage register	R0	N/A	N/A
Output voltage change with external resistor divider	No	Yes	Yes
Maximum output current	2A	1A	1A
Operation mode	PWM Only	PWM or PWM/PFM	
Enable pin LOW	All bucks disabled, FB pins pulled low with a 22 kΩ internal resistor.		
Enable pin HIGH	All bucks are enabled.		
Enable Bit	N/A	BUCK2EN	BUCK3EN
SHUTDOWN Command	Turns off all bucks		
RESET Command	Turns on all bucks and brings all registers to their power on default values		
SLEEP Command	Turns off this buck	No effect	
WAKEUP Command	Turns on this buck	No effect	

DIGITALLY ASSISTED VOLTAGE SCALING

The device is designed to be used in a voltage scaling system to lower the power dissipation by scaling the supply voltage with the clock frequency. Buck 1 supports two modes of voltage scaling: Dynamic Voltage Scaling (DVS) and Adaptive Voltage Scaling (AVS).

- DVS mode: the voltage changes are initiated by the system firmware as a result of changes in the operating frequency of the system. Pre-characterized voltage - clock frequency pairs are used. This is an open loop system because it does not adapt to temperature changes or other factors.
- • AVS mode: the voltage changes are initiated by the Advanced Power Controller (APC, residing in the powered IC) as a result of changes in the operating performance of the monitored system. Pre-characterized voltage - clock frequency pairs are not needed. AVS is a closed loop system that provides an automatic process and temperature compensation such that for any given process, temperature, or clock frequency, the minimum supply voltage is delivered. AVS systems continuously track the system's performance and immediately optimize the supply voltage to the required lowest value. An added benefit is the automatic compensation for voltage drops caused by the power routing from the AVS regulator all the way to the internal circuitry of the powered device. As a result, maximum power savings are achieved.

The device delivers fast and controlled voltage scaling transients with the help of a digital state machine. The state machine automatically optimizes the control loop of the buck regulator to provide large voltage steps with minimal over- and undershoot. This is an important characteristic for voltage scaling systems that rely on minimal over- and undershoot to set voltages as low as possible in order to maximize the energy savings.

DATA INTEFACE

The device is programmable via the low power, 2-wire PowerWise® Interface (PWI). The signals associated with this interface are SPWI and SCLK. Through this interface, the user can enable/disable the device as well as select between DVS and AVS modes. By accessing the registers in the device through this interface, the user can get access and control the operation of the buck controllers, ADC, comparators and GPOs in the device. For maximum flexibility, the logic levels of these signals can be matched with the host by supplying the corresponding I/O voltage level to the VPWI pin as shown in the figure below.

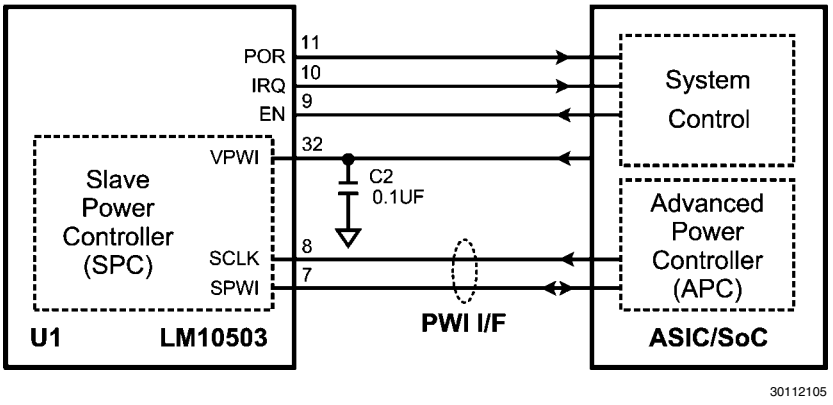


FIGURE 4. PowerWise Interface

The device supports the full command set as described in PWI 2.0 specification:

- Core Voltage Adjust
- Reset
- Sleep
- Shutdown
- Wakeup
- Register Read
- Register Write
- Authenticate

Please see the PWI 2.0 specification for a complete description located at http://www.pwistandard.org.

BUCK REGULATORS OPERATION

buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground and a feedback path. The following figure shows the block diagram of each of the three buck regulators integrated in the device.

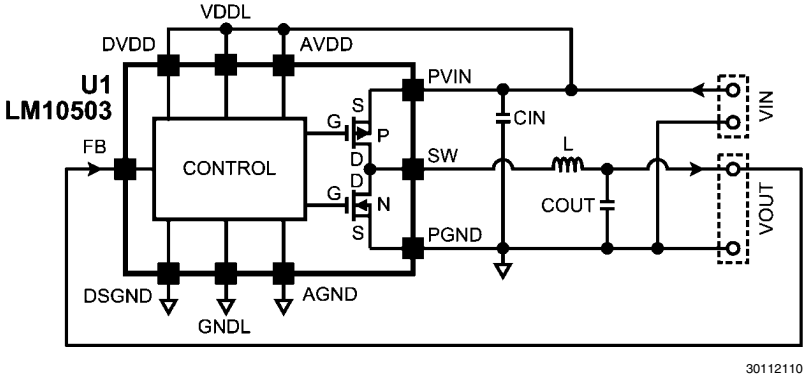


FIGURE 5. Buck Functional Diagram

During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} - V_{OUT})/L$ by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $-V_{OUT}/L$. The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

BUCK REGULATORS DESCRIPTION

The device incorporates three high efficiency synchronous switching buck regulators that deliver various voltages from a single DC input voltage. They include many advanced features to achieve excellent voltage regulation, high efficiency and fast transient response time. The bucks feature voltage mode architecture with synchronous rectification. Each of the switching regulators is specially designed for high efficiency operation throughout the load range. With a 2MHz typical switching frequency, the external L-C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents. All bucks can operate up to a 100% duty cycle allowing for the lowest possible input

voltage that still maintains the regulation of the output. The lowest input to output dropout voltage is achieved by keeping the PMOS switch on. Additional features include soft-start, under-voltage lock-out, and current and thermal overload protection. To reduce the input current ripple, the device employs a control circuit that operates the 3 bucks at 120° phase.

Buck 1 (AVS)

This buck can deliver up to 2A at voltages in the range of 0.700 -1.208V in 127 steps of 4mV resolution and features Adaptive and Dynamic Voltage Scaling (AVS and DVS). It operates in PWM mode only. Its output voltage can be programmed via the CORE VOLTAGE ADJUST command as described in the PWI Standard. The voltage setting is held in register R0 (see PWI register map). Alternately, the voltage output of Buck 1 can also be programmed by directly accessing the same R0 register.

Bucks 2 and 3

These two bucks are identical in performance and mode of operation. They can deliver up to 1A and operate in FPWM (forced PWM), or automatic mode (PWM/PFM).

In **FPWM Mode** the bucks always operate in PWM mode regardless of the output current.

In **Automatic Mode**, if the output current is lower than 70 mA, the bucks automatically transition into PFM (Pulse Frequency Modulation) operation to reduce the current consumption, while at higher than 70 mA they operate in PWM mode. This increases the efficiency at lower output currents. To configure this mode, the user needs to set BK2FPWM or BK3FPWM bits located in the Buck Control Register to 0.

The internal reference is fixed to 0.5V. An external resistor divider sets the output voltage to the desired value. The external resistor divider can be calculated using the following equations.

$$V_{FB} = V_{OUT} \times \frac{R_2}{R_1 + R_2}, \text{ where } V_{FB} = 0.5V$$

$$\text{or } V_{OUT} = V_{FB} \times \frac{R_1 + R_2}{R_2}$$

The recommended value for R2 is 2kΩ. For a desired value of V_{OUT}, the value of R1 is:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.5V} - 1\right)$$

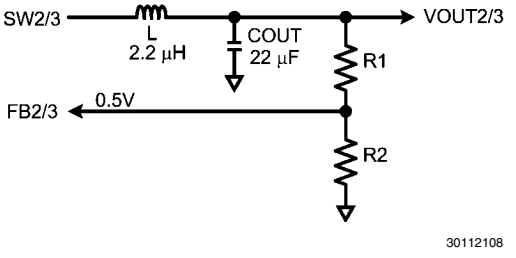


FIGURE 6. Bucks2/3 V_{OUT} Adjust

The following table shows the value of R1 resistor for output voltages in the range of 1.0V to 3.5V.

TABLE 2. Bucks 2/3 V_{OUT} Adjust Resistor Values

V_{OUT} (V)	R1 (kΩ)	R1 Standard 1% (kΩ)	V_{OUT} Actual (V)	V_{OUT} Error (%)
1	2	2	1	0.00%
1.1	2.4	2.4	1.1	0.00%
1.2	2.8	2.8	1.2	0.00%
1.3	3.2	3.24	1.31	0.77%
1.4	3.6	3.6	1.4	0.00%
1.5	**4**	**4.02**	**1.505**	**0.33%**
1.6	4.4	4.42	1.605	0.31%
1.7	4.8	4.75	1.6875	-0.74%
1.8	**5.2**	**5.23**	**1.8075**	**0.42%**
1.9	5.6	5.6	1.9	0.00%
2.0	6	6.04	2.01	0.50%
2.1	6.4	6.34	2.085	-0.71%
2.2	6.8	6.8	2.2	0.00%
2.3	7.2	7.15	2.2875	-0.54%
2.4	7.6	7.68	2.42	0.83%
2.5	**8.0**	**8.06**	**2.515**	**0.60%**
2.6	8.4	8.45	2.6125	0.48%
2.7	8.8	8.87	2.7175	0.65%
2.8	9.2	9.1	2.775	-0.89%
2.9	9.6	9.53	2.8825	-0.60%
3.0	10.0	10.00	3.000	0.00%
3.1	10.4	10.5	3.125	0.81%
3.2	10.8	10.7	3.175	-0.78%

V_{OUT} (V)	R1 (kΩ)	R1 Standard 1% (kΩ)	V_{OUT} Actual (V)	V_{OUT} Error (%)
3.3	**11.2**	**11.3**	**3.325**	**0.76%**
3.4	11.6	11.5	3.375	-0.74%
3.5	12	12	3.5	0.00%

DEFAULT STARTUP SEQUENCE

The 3 buck regulators are staggered during startup to avoid large inrush currents. There are 8 "starting times" with a Td = 2ms resolution. The first voltage starts to come up only after the internal circuitry has reached steady state. The default start sequence is shown in the table and below.

LM10503	LM10503-1	Start Time Slot (ms)
SW3	SW1	2
SW2	SW2	4
SW1	SW3	6

POWER-ON DEFAULT AND DEVICE ENABLE

The device can be enabled/disabled by driving the ENABLE pin high/low. Once enabled, the device engages the power-up sequence and the 3 output voltages settle to their default values. After the power up sequence is completed, and after an additional delay, the POR pin goes high. While the device is enabled, Buck2 and 3 can be individually disabled by accessing their corresponding BKEN bits in register R10 (BUCK CONTROL).

BUCK1 can only be turned off by issuing a SLEEP COMMAND. All three bucks can be turned off at once by using the SHUTDOWN COMMAND from PWI. To re-enable the part, either the ENABLE pin must be toggled (high – low – high), or a RESET COMMAND must be used. The part will then enter the power-up sequence and all voltages will return to their default values. The ENABLE pin resets all the previously programmed bits in the register set to their power-on default. The ENABLE pin provides flexibility for system control. In larger systems, it can be advantageous to enable/disable a subsystem independently. For example, the device may be powering an application processor, in which case the system controller can disable the application processor via the ENABLE pin, but leave other subsystems on. If the ENABLE pin function is not required (i.e., all the power states are controlled through the PWI bus), the pin should be tied to VIN. If the ENABLE pin is tied low, the part is disabled and the PWI interface is also disabled, and the access to PWI registers is not possible.

SHUTDOWN MODE

During shutdown the PFET and the NFET switches, the internal reference, and the control and bias circuitry of the converters are turned off. An internal 22 kΩ resistor (±30%) attached to the FB pin is activated to discharge any residual charge present in the output circuitry.

STARTUP SEQUENCE

The device incorporates an advanced startup circuit that ensures correct system boot.

The designer must ensure that VPWI and VDDMFP are always lower or equal to VIN, including during the initial power up of the device. If VDDMFP and VPWI are supplied from VIN or from one of the output voltages generated by the 3 bucks, than this requirement is automatically satisfied. Note the limitation of VPWI maximum supply is 3.63V. The VIN input voltage can ramp-up as fast as 25 µs and as slow as 10 ms, but it should not have a dip larger than 0.1V, while all 3 outputs are loaded at their maximum rated current.

When the input power supply reaches the UVLO level (which is sensed on the AVDD pin), and after a delay of about 15 ms ±30%, the internal sequencer will start counting. The 3 bucks can be enabled at any 2ms discrete points within the 16 ms maximum sequencer delay.

After the last power supply is up and running, a fixed delay of 32 ms is added after which the POR pin (reset output) is deasserted (pin goes in tri-state). This 32 ms delay allows a processor to stabilize its internal clocks, PLLs or other support circuits before its reset input driven from POR is released.

After the last buck is enabled, the internal sequencer waits a maximum of 8ms for all 3 bucks to fully start (as reflected by their respective BUCK#-OK bit). If at least one of the bucks is not starting up within 8ms (for example because of an overload), the device enters an “output fault” state, all 3 bucks are immediately shut down, and a 200 ms time delay is added before the sequencer will restart. The 200 ms delay is needed to allow all output capacitors to fully discharge, such that the next startup will not be under bias.

The sequencing timer is restarted and the 3 bucks are enabled according to the sequencer configuration. If the cause of the fault is still present, the 3 bucks will be shut down again, and the process repeats indefinitely. The power supply will be in a “hiccup” mode with a repetition period of about 214 ms. Of these 214 ms, the bucks are on for about 8 to 12 ms, so the duty cycle is about 3.7% to 5.6%, and this reduces the risk of damage to the system. The device will stay in this hiccup mode till the condition that caused the overload is removed.

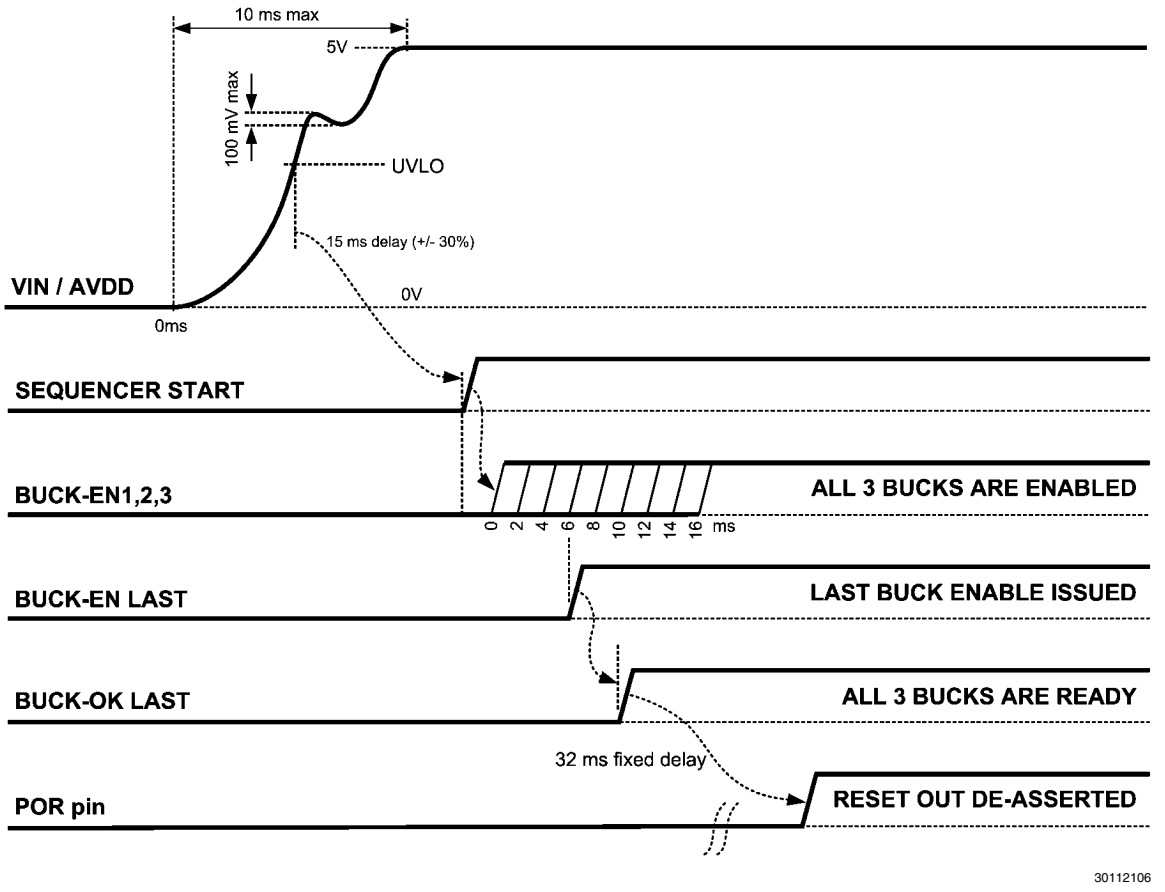


FIGURE 7. Startup Sequence

SOFT START

Each of the buck converters has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady state operating point, thus reducing start-up stresses and surges. During startup, the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high, after VIN is higher than the UVLO trip point.

For **Buck 1** the soft start is implemented as a linear output voltage ramp that takes about 500 µs. This soft start time in general doesn't vary with V_{OUT} level or the allowed C_{OUT} range (22 µF - 44 µF). During soft start, the load is expected to be light, or resistive, for example, if the final voltage is 1V at 2A, the buck expects the load at V_{OUT} = 0.1V to be about 200 mA.

For **Bucks 2 and 3** the soft start is implemented by increasing the switch current limit in steps that are gradually higher: 180 mA, 300 mA, and 720 mA. The startup time depends on the output capacitor size, load current and output voltage. Typical startup time with the recommended output capacitor of 22 µF is 0.2 - 1ms.

BUCK 1 DIGITALLY ASSISTED RAMP CONTROL

The slew rate of the Buck 1 output can be configured by setting the bits BK1RAMPMOD and BK1RAMPEN in the Buck Control register R10.

If BK1RAMPEN bit of register R10 (Buck Control) is 0, a new voltage setting in the R0 register will be immediately transferred to the Buck 1 analog circuitry. If the new voltage is very different from the previous one (large voltage step up or down), the output voltage may overshoot or undershoot. To prevent this, the user should increment the output voltage of SW1 in small enough steps.

Alternately, this can be done automatically by the logic inside the device by setting BK1RAMPEN bit of register R10 (Buck Control) to 1. In this case, the user has two options to select from: SLOW-RAMP and FAST-RAMP which can be selected by programming the BK1RAMPMOD bit (Buck 1 Ramp Mode) of the same register.

SLOW-RAMP: set BK1RAMPMOD to 0. In this case the voltage code is stepped up/down every 8µs.

FAST-RAMP: set BK1RAMPMOD to 1. In this case the voltage code is stepped up/down every 4µs (reset delay).

In both SLOW-RAMP and FAST-RAMP modes, the operation is as follows

- **Ramp up** will have a maximum of 8 voltage codes per step (4mV/code * 8 codes = 32 mV), but will have less voltage codes (4 or 2 or 1) if within 8 voltage codes of the target level. A full ramp-up from 7'h00 to 7'h7F will take ~144 µs for ramp mode 0 and 72 µs mode 1.
- **Ramp down** will have a maximum of 4 voltage codes per step (4mV/code * 4 codes = 16 mV), but will have a single voltage code if within 4 voltage codes of the target level. A full ramp-down from 7'h7F to 7'h00 will take ~272 µs for ramp mode 0 and 136 µs mode 1.

UNDER VOLTAGE LOCK OUT (UVLO)

The AVDD pin is monitored for a supply under voltage condition, for which the operation of the device can not be guaranteed. The part will automatically be disabled if the supply voltage is insufficient. To prevent unstable operation, the UVLO has a hysteresis window of about 200 mV. An under voltage lockout (UVLO) will force the device into the RESET state. Once the supply voltage is above the UVLO hysteresis, the device will initiate a power-up sequence and then enter the ACTIVE state.

THERMAL SHUTDOWN (TSD)

The temperature of the silicon die is monitored for an overtemperature condition, for which the operation of the device can not be guaranteed. The part will automatically be disabled if the temperature is too high. The thermal shutdown (TSD) will force the device into the RESET state. To prevent unstable operation, the TSD has a hysteresis window of about 20°C. Once the temperature has decreased below the TSD hysteresis, the device will initiate a power-up sequence and then enter the ACTIVE state.

POWER ON RESET (POR)

The device contains a voltage monitor on its input and output voltages and will assert POR pin whenever the voltages are too low. The pin is an open-drain type output, therefore it must be pulled-up via an external resistor. The device continues to assert this pin for about 32 ms after all output voltages are good, to ensure that the powered devices are properly reset. The POR pin remains asserted for as long as the error condition persists.

CURRENT LIMITING

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PWM OPERATION

While in PWM mode, the bucks use an internal NFET as a synchronous rectifier to reduce the rectifier forward voltage drop and the associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

PFM OPERATION (BUCKS 2 and 3)

At very light loads, Buck 2 and Buck 3 enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Bucks 2 and 3 will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous, or
2. The peak PMOS switch current drops below the I_{MODE} level. (Typically:

$$(\text{Typically } I_{MODE} < 66\ mA + \frac{V_{IN}}{160\Omega})$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_PFM level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 66\ mA + \frac{V_{IN}}{80\Omega}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see figure below) the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is less than 30 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

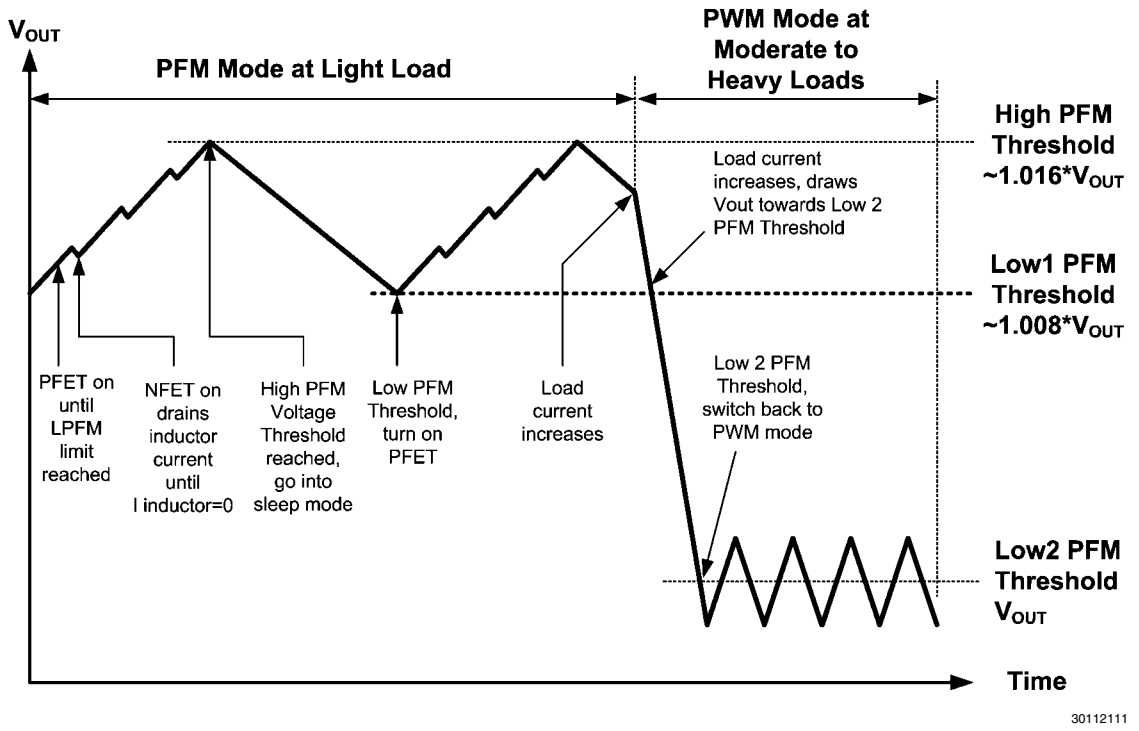


FIGURE 8. PFM vs. PWM Operation

PWM/PFM OPERATION AND SETTINGS (REGISTER R10) [BUCKS 2 and 3]

The switching converters in the device have two modes of operation: pulse width modulation (PWM) and pulse frequency modulation (PFM).

By default, the device stays in PWM mode. This register provides the ability to enable the automatic transition between PFM or PWM operation.

In PWM the converter switches at a fixed frequency determined by the frequency of the internal clock. Each period can be split into two cycles. During the first cycle, the high-side switch is on and the low-side switch is off, therefore the inductor current is rising. In the second cycle, the high-side switch is off and the low-side switch is on causing the inductor current to decrease. The output ripple voltage is lowest in PWM mode. As the load current decreases, the converter efficiency becomes worse due to the increased percentage of overhead current needed to operate in PWM mode.

At light load current the converter can enter PFM operation if R10 register BKxFPWM bit is zero, in which case the output stage operates alternately between tristate and the nominal PWM switching frequency. This mode of operation maintains high efficiency even at light load current.

In PFM mode, the converter begins to ramp up the output voltage after the output voltage falls below the PFM threshold (~1% above V_{OUT} nominal). When the output voltage has reached V_{OUT} nominal and the load current is still light, the converter tristates the output stage. The average output voltage in PFM mode is, therefore, slightly higher than V_{OUT} nominal.

The PWM-to-PFM transition occurs when the DC output current is equal to the ripple current:

$$I_{PWM/PFM} = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

where L is the output inductance and f_S is the switching frequency.

The converter will transition into PFM mode when the output switch current is negative for 4 consecutive clock cycles.

If the load current increases during PFM mode causing the output voltage to fall below the PFM threshold (~1% above V_{OUT} nominal) - the part will automatically transition into fixed-frequency PWM mode.

LOW DROPOUT OPERATION

The device can operate at 100% duty cycle (no switching; PMOS switch completely on) for low drop out support. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage: $V_{IN_MIN} = V_{OUT} + I_{LOAD} \times (R_{DSON_PFET} + R_{IND})$, where:

- I_{LOAD} = Load Current
- R_{DSON_PFET} = Drain to source resistance of PFET (high side) switch in the triode region
- R_{IND} = Inductor resistance

EXTERNAL COMPONENTS SELECTION

All three switchers require an input capacitor, and an output inductor-capacitor filter. These components are critical to the performance of the device. All three switchers are internally compensated and do not require external components to

achieve stable operation. The output voltage of Buck 1 can be programmed through the PWI pins. The output voltages of Bucks 2 and 3 can be modified using external resistor dividers connected from the output voltage to the FB pin.

OUTPUT INDUCTORS & CAPACITORS SELECTION

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Over current ruggedness

The device has been optimized for use with nominal LC values as shown in the .

INDUCTOR SELECTION

The recommended inductor values are shown in . It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current:

Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta I_{RIPPLE}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$$\approx I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times 2.2 \times 2.0} \text{ (A typ.)},$$

$$D = \frac{V_{IN}}{V_{OUT}},\ F_S = 2\ \text{MHz},\ L = 2.2\ \mu\text{H}$$

There are two methods to choose the inductor saturation current rating:

Recommended Method:

The best way to guarantee the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in the Electrical Characteristics. In this case the device will prevent inductor saturation by going into current limit before the saturation level is reached.

Alternate Method:

If the recommended approach cannot be used care must be taken to guarantee that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

I_{SAT}: Inductor saturation current at operating temperature

I_{LPEAK}: Peak inductor current during worst case conditions

I_{OUTMAX}: Maximum average inductor current

I_{RIPPLE}: Peak-to-Peak inductor current

V_{OUT}: Output voltage

V_{IN}: Input voltage

L: Inductor value in Henries at I_{OUTMAX}

F: Switching frequency, Hertz

D: Estimated duty factor

EFF: Estimated power supply efficiency

Suggested Inductors and Their Suppliers

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, etc. In general, smaller physical size inductors will have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low profile inductors may have even higher series resistance. The designer should try to find the best compromise between system performance and cost.

OUTPUT AND INPUT CAPACITORS CHARACTERISTICS

Special attention should be paid when selecting these components. As shown in the following figure, the DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

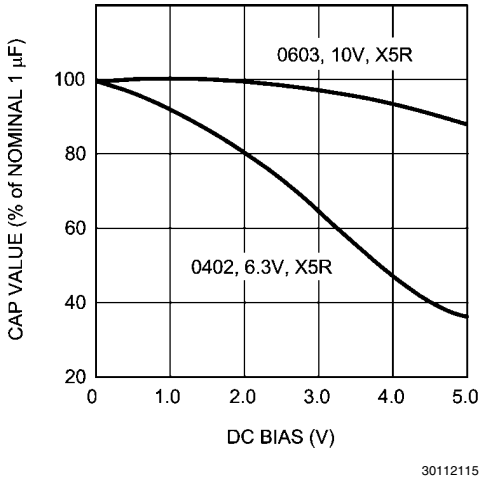


FIGURE 9. Typical Variation in Capacitance vs. DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics.

Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 44 µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

OUTPUT CAPACITOR SELECTION

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the frequency ranges the switcher operates.

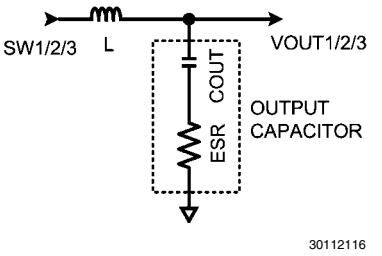


FIGURE 10. C_{OUT} ESR

The output-filter capacitor smooths out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor (ESR_{COUT}). Also note that the actual value of the capacitor's ESR_{COUT} is frequency and temperature dependent, as specified by its manufacturer. The ESR should be calculated at the applicable switching frequency and ambient temperature.

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \text{ where } \Delta I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S} \text{ and } D = \frac{V_{OUT}}{V_{IN}}$$

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Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor where:

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \sqrt{V^2_{ROUT} + V^2_{COUT}}$$

where:

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT} \text{ and } V_{COUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

$V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output ripple,

V_{ROUT}: estimated real output ripple,

V_{COUT} estimated real output ripple.

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 22 µF, 6.3V with an ESR of 2mΩ or less. The output capacitors need to be mounted as close as possible to the output/ground pins of the device.

TABLE 3. Recommended Output Capacitors

Model	Type Vendor	Vendor	Voltage Rating	Case Size
08056D226MAT2A	Ceramic, X5R	AVX Corporation	6.3V	0805, (2012)
C0805L226M9PACTU	Ceramic, X5R	Kemet	6.3V	0805, (2012)
ECJ-2FB0J226M	Ceramic, X5R	Panasonic - ECG	6.3V	0805, (2012)
JMK212BJ226MG-T	Ceramic, X5R	Taiyo Yuden	6.3V	0603, (1608)
C2012X5R0J226M	Ceramic, X5R	TDK Corporation	6.3V	0603, (1608)

INPUT CAPACITOR SELECTION

The input capacitors should be located as close as possible to their corresponding PVINx and PGNDx pins, where x designates the buck 1,2 or 3. The 3 buck regulators operate at 120° out of phase, which means that is they switch on at equally spaced intervals, in order to reduce the input power rail ripple. It is recommended to connect all the supply/ground pins of the buck regulators, PVIN1, 2 and 3 to two solid internal planes located under the device. In this way, the 3 input capacitors work together and further reduce the input current ripple. A larger tantalum capacitor can also be located in the proximity of the device. The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The input capacitor must be rated to handle this current:

$$I_{RMS_CIN} = I_{OUT} \frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}}$$

The power dissipated in the input capacitor is given by:

$$P_{D_CIN} = I^2_{RMS_CIN} \times R_{ESR_CIN}$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The minimum recommended value for the input capacitor is 10 µF with an ESR of 10 mΩ or less. The input capacitors need to be mounted as close as possible to the power/ground input pins of the device.

The input power source supplies the average current continuously. During the PFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the PFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current.

Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F_S} + I_{OUT} \times ESR_{CIN}$$

where:

V_{PPIN}: estimated input ripple voltage,

C_{IN}: Input capacitor value

ESR_{CIN}: input capacitor ESR.

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D \times \left(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right)}$$

I_{RMSCIN}: estimated input capacitor RMS current.

LARGE SIGNAL TRANSIENT

The switching converters in the device are designed to work in a voltage scaling system. This requires that the converters have a well controlled large signal transient response. Specifically, the under- and over-shoots have to be minimal or zero while maintaining settling times less than 0.1 msec. Typical response plots are shown in section Typical Performance Characteristics.

LM10503 OPERATIONAL STATE DIAGRAM

The device has four operating states: **Startup, Active, Sleep and Standby**; see next figure. The figure assumes that supply voltages are in the valid range.

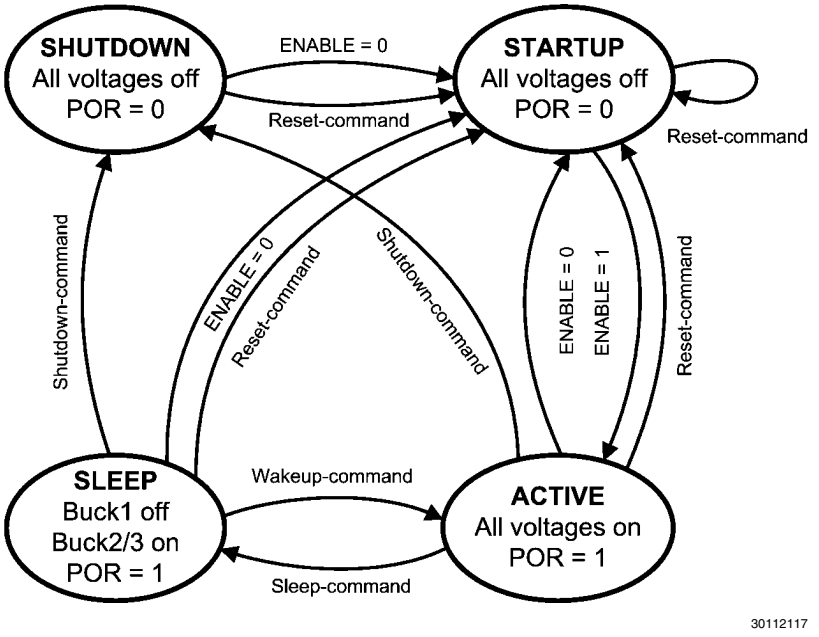


FIGURE 11. LM10503 State Diagram

The **Startup State** is the default state of the device after power is applied. All bucks are off and POR output is '0'. This state is entered when the external enable input pin is pulled low. It is a temporary state because the startup sequence is automatically executed initiated, and upon its completion, the device transfers into the Active State. It is possible to issue a Reset Command while still in Startup state, in which case the startup sequence will be re-started.

In **Active State** all bucks are on at their default voltages and the POR-output pin is high. From Active State the device can:

- Go back to Start-up State by setting the ENABLE pin low or by issuing the Reset Command.
- Go into Sleep State by issuing the Sleep Command over the PWI bus.
- Go into Shutdown State by issuing the Shutdown Command over the PWI bus.

In **Sleep State**, only the Buck 1 output voltage is off, but the POR output is still high. The other two bucks, Bucks 2 and 3, may be used to provide auxiliary voltages that need to be maintained during Sleep State. From the Sleep State, the device can:

- Be re-activated (go into Active State), by using the Wake-up Command. This resumes the power on default state configuration and voltages may need to be changed by firmware.
- Go into Shutdown State by issuing the Shutdown Command over the PWI bus.
- Go into to Start-up State by setting the ENABLE pin low or by issuing the Reset Command.

In **Shutdown State**, all buck regulators are off, and POR is low. This state has the lowest power consumption. The device can enter the Shutdown State by using the Shutdown Command, or by setting ENABLE to '0'. The device can exit the and go into Startup State by:

- Toggling the ENABLE pin high, or
- Issuing the over the PWI bus.

FAULT CONDITIONS

The device incorporates several advanced features that protect itself and the system from the following fault conditions.

Input Voltage is Too Low

If the input voltage is too low to guarantee accurate operation of the device, a UVLO detector will disable the device. When this error condition occurs, the internal logic goes into reset state and stays in reset for as long as the error condition is still active. When the error condition is removed, the device enters the startup sequencing.

Output Voltage is Too Low

If any of the output voltages are too low compared with the expected voltage, for example due to a short circuit, the device will enter a hiccup mode (will continuously try to restart). When any of the buck ready signals of the enabled bucks drop from high to low for more than 1ms, a restart is triggered. The external POR is asserted, and all bucks are disabled and re-enabled again sequentially after a wait time of 200 ms.

Startup Takes Too Long

During startup, after the bucks are enabled, a 8ms timeout counter is initialized. If any of the enabled bucks fails to return the OK signal within 8ms, it triggers a shutdown of all bucks. All bucks are disabled for 200 ms and re-enabled again sequentially.

Output Voltage is Too Low

If any of the output voltages are too low compared with the expected voltage, for example due to a short circuit, the device will enter a hiccup mode (will continuously try to restart).

When any of the buck ready signals of the enabled bucks drop from high to low for more than 1ms, a restart is triggered. The external POR is asserted, and all bucks are disabled and re-enabled again sequentially after a wait time of 200 ms.

Die Temperature is Too High

If the die junction temperature is too high, the device is automatically disabled to prevent damage. When this error condition occurs, the internal logic goes into reset state and stays in reset for as long as the error condition is still active. When the error condition is removed, the device enters the startup sequencing.

TABLE 4. LM10503 Fault Condition Management

Fault Type	Buck action	POR Pin
UVLO on AVDD input pin	Buck SW pins are tri-stated and a ~22 kΩ pulldown resistor is activated on FB pins.	Low
Output Under-voltage	Continues to try to regulate; enters hiccup mode	Low as long as voltage level goes out of the range
Over-temperature	Buck is tri-stated and restarts when the die has cooled down	Low until buck starts up again

Although the device is protected against these conditions, the system designer should not allow these conditions to occur.

MULTI FUNCTION PORT

The Multi-Function Pins (MFP3-0) can be configured to operate as

- ADC inputs
- Comparator inputs
- General Purpose Outputs (GPOs) in either push-pull mode or open-drain mode.

This architecture offers the system designer the necessary flexibility to allocate the device resources according to system's requirements. Any combination of functions is possible, including the change of the function during runtime.

Function Selection

- **ADC**: The ADC path is enabled unless MFP3:0 pin is configured as General Purpose Output pin. The pin connected to the ADC's input is the one selected by the ADCSEL1:0 field in register R11.
- **COMPARATOR**: The MFP3:0 pins can be configured as comparator inputs by setting the Comparator Enable Bits CMPxEN in register R15
- **GPO**: The MFP3:0 pins can be configured as GPO outputs by setting the GPO Enable Bits GPOxEN in register R15.

This setting supersedes the other two functions associated with the same pin.

Limitation: the same MFP pin should not simultaneously be configured as comparator and GPO, in which case the later takes precedence. In other words, the GPO function must be disabled in order to use the Multi-Function Pin as a comparator input pin. For accurate ADC measurements, a pin should only be configured as ADC input. The following figure shows a simplified block diagram of the Multi Function Port.

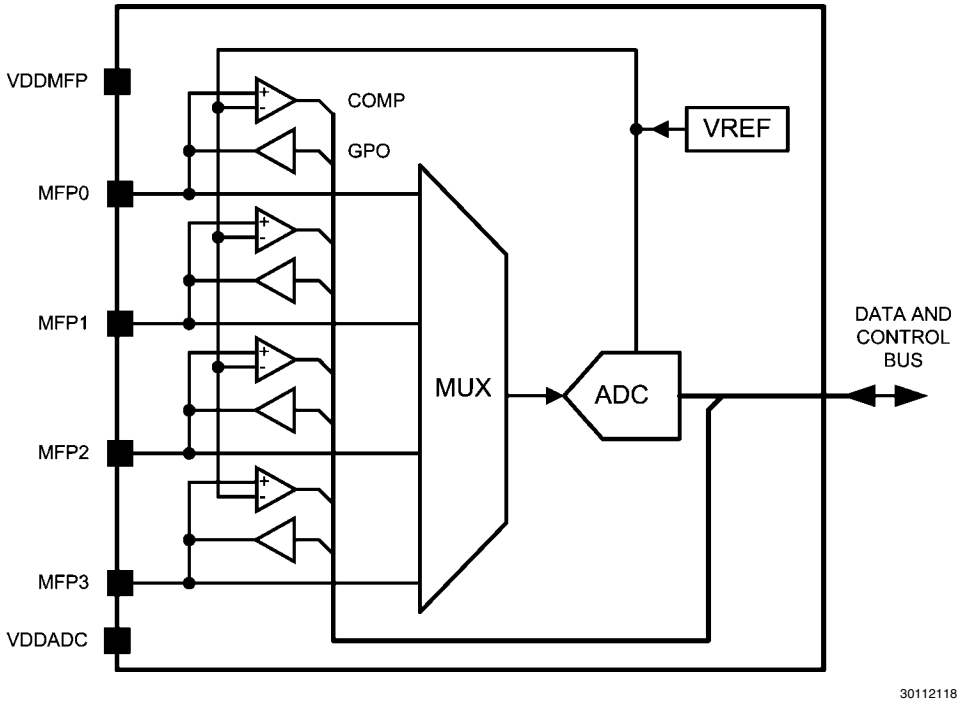


FIGURE 12. MFP Block Diagram

The comparator can generate an “edge” type interrupt, not a “level” interrupt. The comparator can not be used to immediately determine if the signal presented on the input is higher or lower than the VREF. It requires the input signal to change in time, i.e. to increase/decrease above/below the VREF, as configured by the polarity bit in R17. The comparator function is best used for a very slow changing event as for example the charging or discharging of a battery or supercapacitor, in which case an interrupt will be generated when the comparator trips. This method is more efficient than a continuous polling of a comparator or of an ADC. If the system designer needs to know the value of voltage presented on one of the MFP pins, it should use the ADC function to do an actual ADC measurement.

Analog-to-Digital Converter

The device is equipped with an 8-bit dual-slope integrating analog to digital converter. A dual-slope converter does not require a sample and hold stage and provides an effective filtering of the input signal noise components that are outside the range of 125 kHz to 500 kHz. The ADC digitizes the input signal ranging from VREF to 2*VREF, where VREF is the internal reference voltage. After an initial 2ms warm-up for the first activation of the ADC enable bit, the dual-slope converter integrates the input signal during the first phase for approximately 2 ms, followed by a second phase that integrates VREF for 0 ms to 2 ms depending on the level of the input signal. As a result the total conversion time varies from 2 ms to 4 ms.

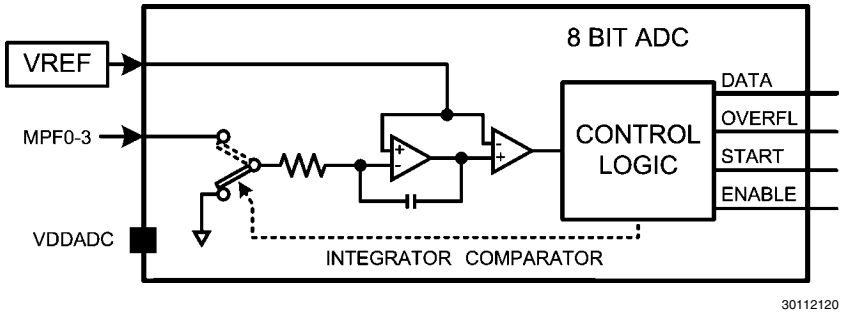


FIGURE 13. Simplified ADC Block Diagram

The ADC has a 4-channel multiplexer on the input that allows the system designer to assign any of the MFP0-3 pins as ADC inputs.

The voltage applied on MFP0-3 pins must match the input working voltage of the ADC: VREF to 2VREF. This can be accomplished by using external resistor dividers. To allow maximum flexibility, there are no internal resistor dividers.

The input impedance of the ADC is about 3MΩ, therefore the external resistor divider must be designed accordingly in order to reduce the error it can cause.

The system designer can use these ADC inputs for general purpose applications such as power rail measurements, resistive keyboard matrix scanning, temperature measurements, load currents, etc. The source selection and the access to the conversion results are established through the registers described in the Register Map section.

The power-up default of the ADC is disabled in order to minimize current consumption. It needs to be enabled by setting the ADCEN bit (register R11). Writing a logic 1 to bit 3 of R11 (ADCSTART) will initiate a conversion. It is advised to select the correct ADC source before a conversion is started. The ADC will set bit 4 of R11 (DATARDY) upon the completion of a conversion, which is 2-4ms after the start of the conversion. At the same time, an interrupt request will be generated. (See Interrupt Request Register).

To save power, disable the ADC by setting bit 2 of R11 to 0 (ADCEN). To initiate the start of a new conversion, or to make repetitive starts, set bit 3 of R11 (ADCSTART) to 0 then to 1. The interrupt driven protocol between the part and the system processor is the most efficient way to acquire data from successive measurements, as shown in the following flowchart. The ADC block includes its own reference which is enabled when the EN pin is high. This allows a quick startup time of the ADC after the ADCEN bit was set. The power consumption of the reference is about 50uA typical as it can be monitored on the VDDADC pin. This current can be reduced to a few uA by disabling the part either by driving EN low or by executing a SHUTDOWN command. Please note that ADCEN bit must be set to zero prior to executing a SHUTDOWN command.

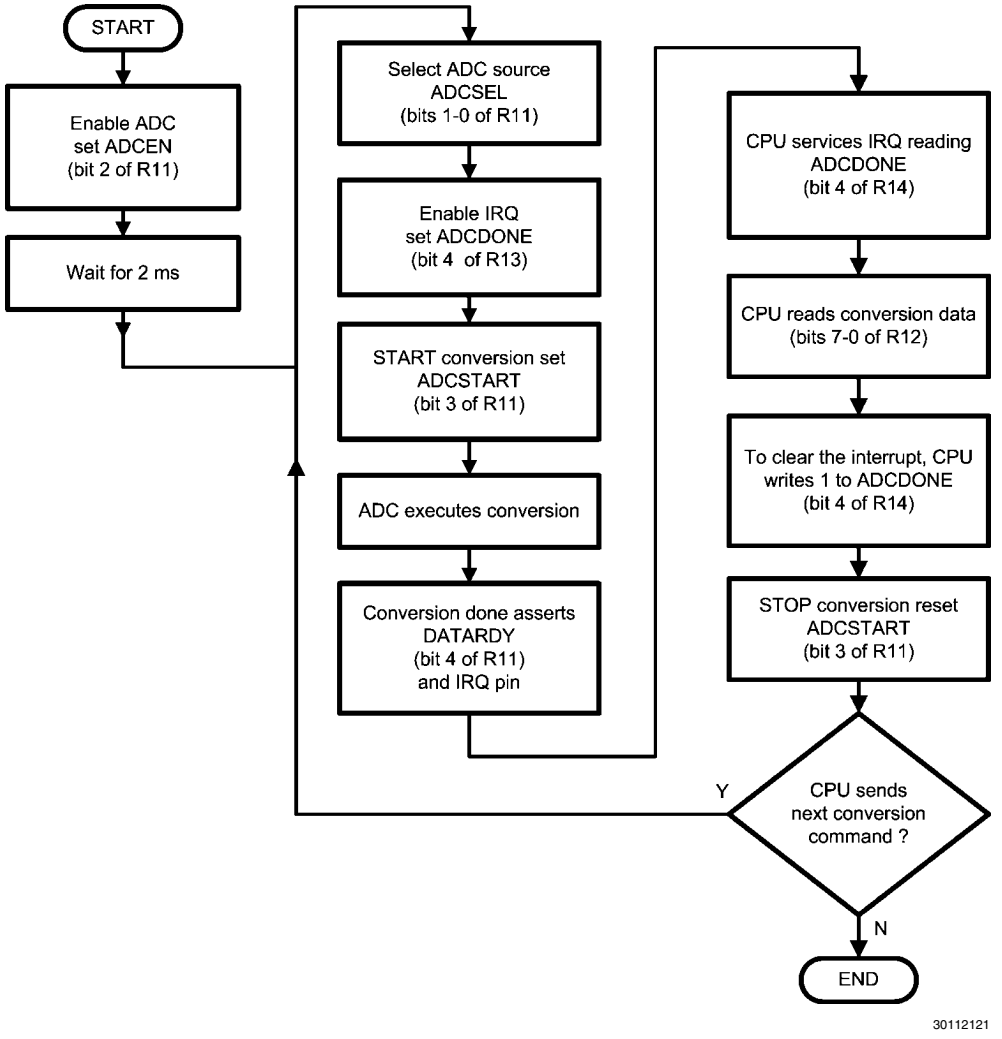


FIGURE 14. ADC Operation

INTERRUPT REQUEST OUTPUT

The part has the ability to interrupt the system processor through the open drain IRQ pin, which transitions to an active logic low level upon the following 8 events, as described in register R14, Interrupt Request Register:

7	VOUTUV	At least one of the 3 switchers has an output in under-voltage condition.
6	PWIUCMD	PWI undefined command.
5	PWIPERR	PWI parity error
4	ADCDONE	ADC conversion done, data ready
3:0	COMP3:0	MFP3:0 pin, if configured as comparator, will generate an interrupt if this bit is set 1.

All interrupt sources can be masked by the Interrupt Mask Register R13. Masking the interrupt prevents the interrupt event from asserting the IRQ pin, yet the event will still be captured in the IRQ register, which allows the processor to poll the interrupt sources. After an active low IRQ has been detected by the system processor, the latter services the interrupt and will access the IRQ register to determine which source(s) was (were) responsible for the interrupt request. To clear the IRQ register, a logic 1 must be written to the same location. Writing a logic 0 is disregarded. The interrupts are not hardware prioritized. In case more than one Interrupt Request is set, the priority must be determined by the system firmware.

Thermal Considerations

The thermal characteristics of the device are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$T_J = P_D \times \theta_{JA} + T_A$ where:

P_D is the total power dissipation of the device;

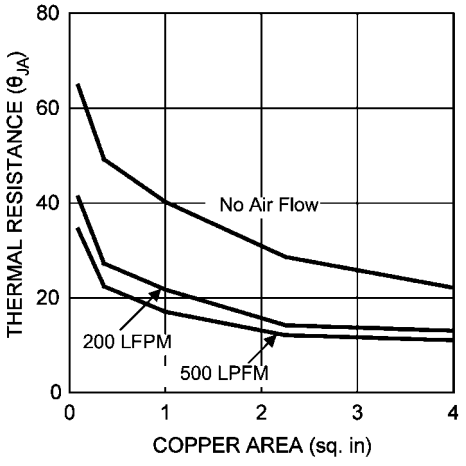
T_J is the junction temperature in °C;

θ_{JA} is the junction-to-ambient thermal resistance for the device;

T_A is the ambient temperature in °C.

It is important to always keep the operating junction temperature (T_J) below 105°C for reliable operation. If the junction temperature exceeds 160°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heat sinking or excessive power dissipation in the device.

The figure below provides a better approximation of the θ_{JA} for a given PCB copper area. The PCB heatsink area consists of 2oz. copper located on the bottom layer of the PCB directly under the exposed pad. The bottom copper area is connected to the exposed pad by means of a 4 x 4 array of 12 mil thermal vias.



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FIGURE 15. Thermal Resistance vs. PCB Area

PCB LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

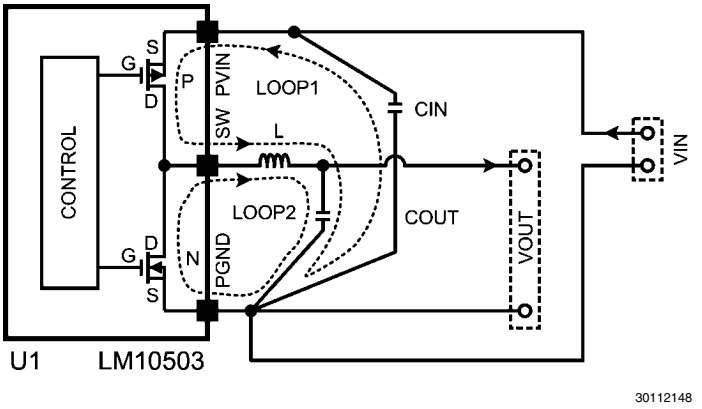


FIGURE 16. Schematic of LM10503 Highlighting Layout Sensitive Nodes

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the C_{IN} input capacitor, to the regulator PVIN pin, to the regulator SW pin, to the inductor then out to the output capacitor C_{OUT} and load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the inductor and then out to C_{OUT} and the load (see figure above). To minimize both loop areas the input capacitor should be placed as close as possible to the PVIN pin. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to PGND and the die attach pad (DAP). The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW pins should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW pin. The inductors should be placed as close as possible to the SW pins to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds located under the DAP. The ground connections for the feedback and external ADC components should be connected together then routed to the AGND pin of the device. The AGND pin should connect to PGND under the DAP. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB pin. Since the feedback node can have high impedance, the trace from the output resistor divider to FB pin should be as short as possible. This is most important when high value resistors are used to set the output voltage. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise. Locate the two resistors of the feedback resistor divider close to the FB pin and not to the output capacitor to improve noise immunity.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.
6. Provide adequate device heat sinking. Use as many vias as possible to connect the DAP to the power plane(s) heat sink. A recommended arrangement is a 4x4 via array with a minimum via diameter of 12 mils. See the Thermal Considerations section to make sure enough copper heat sinking area is used to keep the junction temperature below 105°C.

LM10503 PWI Register Map

Register Address	PWI Register Name	Register Usage	Bit ==>	7	6	5	4	3	2	1	0
0x00	R0	Core Voltage - Buck1	Name	--	Buck1 Voltage Code						
			Access	R/O	R/W						
			RST VAL	0	1	0	1	1	0	0	0
0x03	R3	Status	Name	--	--	--	--	Buck2 OK	Buck3 OK	1	Buck1 OK
			Access	R/O							
			RST VAL	0	0	0	0	1	1	1	1
0x04	R4	Device Capability	Name	Device Capability							
			Access	R/O							
			RST VAL	0	0	0	0	0	0	1	0
0x0A	R10	Buck Control	Name	--	BK1RAMP MOD	BK1RAMPE N	BK3FPWM	BK2FPWM	--	BK3EN	BK2EN
			Access	R/O	R/W				R/O	R/W	
			RST VAL	0	1	1	1	1	1	1	1
0x0B	R11	ADC Control	Name	--	--	ADCOVF	DATARDY	ADCSTART	ADCEN	ADCSEL1	ADCSEL0
			Access	R/O	R/O	R/O		R/W			
			RST VAL	0	0	0	0	0	0	0	0
0x0C	R12	ADC Data	Name	ADCDATA							
			Access	R/O							
			RST VAL	0	0	0	0	0	0	0	0
0x0D	R13	Interrupt Mask	Name	VOUTUV	PWIUCMD	PWIPERR	ADCDONE	COMP3	COMP2	COMP1	COMP0
			Access	R/W							
			RST VAL	0	0	0	0	0	0	0	0
0x0E	R14	Interrupt Request	Name	VOUTUV	PWIUCMD	PWIPERR	ADCDONE	COMP3	COMP2	COMP1	COMP0
			Access	R/C - Cleared by writing '1' to corresponding bit.							
			RST VAL	0	0	0	0	0	0	0	0
0x0F	R15	Comparator Control 1	Name	CMP3DGL	CMP2DBL	CMP1DGL	CMP0DGL	CMP3EN	CMP2EN	CMP1EN	CMP0EN
			Access	R/W							
			RST VAL	1	1	1	1	0	0	0	0
0x10	R16	Comparator Control 2	Name	CMP3DM1	CMP3DM0	CMP2DM1	CMP2DM0	CMP1DM1	CMP1DM0	CMP0DM1	CMP0DM0
			Access	R/W							
			RST VAL	1	1	1	1	1	1	1	1

Register Address	PWI Register Name	Register Usage	Bit ==>	7	6	5	4	3	2	1	0
0x11	R17	Comparator Control 3	Name	CMP3HYS	CMP2HYS	CMP1HYS	CMP0HYS	CMP3PL	CMP2PL	CMP1PL	CMP0PL
			Access	R/W							
			RST VAL	0	0	0	0	0	0	0	0
0x12	R18	GPO Control	Name	GPO3OD	GPO2OD	GPO1OD	GPO0OD	GPO3EN	GPO2EN	GPO1EN	GPO0EN
			Access	R/W							
			RST VAL	1	1	1	1	0	0	0	0
0x13	R19	GPO Data	Name	--	--	--	--	GPO3D	GPO2D	GPO1D	GPO0D
			Access	R/O				R/W			
			RST VAL	0	0	0	0	0	0	0	0

Note 1: Register R0 default value is 0x58 which corresponds to SW1 = 1.052V.
Note 2: RST VAL means power on default reset values.
Note 3: "– –" denoted unused bits. A write into unused bit position will be ignored. A read will produce '0' when register is partially used and a "no response frame" when register is completely unused. Please refer to PWI specification version 2.0 for further information.

R0 - Core Voltage Buck 1 Register

Bit	Field Name	Description or Comment	
7	Unused	Any data written into this bit is ignored.	
6:0	Voltage	Core voltage value with no external feedback resistor divider.	
		Voltage Data Code	Voltage Value (V)
		7h'00	0.7
		7h'xx	Linear scaling of 127 steps of 4mV
		7h7F	1.208

R3 - Status Register

Bit	Field Name	Description or Comment
7	Reserved	Reserved
6	Reserved	Reserved
5	Reserved	Reserved
4	Reserved	Reserved
3	Buck2 OK	Buck 2 is operating correctly
2	Buck3 OK	Buck 3 is operating correctly
1	Reserved	Reserved
0	Buck1 OK	Buck 1 is operating correctly

R4 - Device Capability Register

Bit	Field Name	Description or Comment
7:3	Reserved	Reserved
2:0	Version	Read transaction return '010' indicating PWI 2.0 specification.
		Write transactions to this register are ignored.

R10 - Buck Control Register

Bit	Field Name	Description
7	Reserved	Reserved
6	BK1RAMPMOD	Buck1 Ramp control Mode select If bit 5, BK1RAMPEN, is 1, the voltage code is stepped up/down every: 0: SLOW-RAMP. Ramp step is 8us 1: FAST-RAMP. Ramp step is 4us (reset default) In both SLOW-RAMP and FAST-RAMP modes, the operation is as follows: — **Ramp-up** will have a maximum of 8 voltage codes per step (4mV/code * 8 codes = 32mV), but will have less voltage codes (4 or 2 or 1) if within 8 voltage codes of the target level. A full ramp-up from 7'h00 to 7'h7F will take ~144 µs for ramp mode 0 and 72 µs mode 1. — **Ramp-down** will have a maximum of 4 voltage codes per step (4mV/code * 4 codes = 16 mV), but will have a single voltage code if within 4 voltage codes of the target level. A full ramp-down from 7'h7F to 7'h00 will take ~272 µs for ramp mode 0 and 136 µs mode 1.
5	BK1RAMPEN	Buck 1 Ramp Control Enable. If set, enables stepping control for voltage going up/down, as described in bit 6 above.
4		Buck 3 forced to be always in PWM mode.
3		Buck 2 forced to be always in PWM mode.
2		Reserved
1		Buck 3 Enable
0		Buck 2 Enable

R11 - ADC Control Register

Bit	Field Name	Description or Comment
7:6	Reserved	Reserved
5	ADCOVF	ADC Overflow indicator (status), input is higher than 2*VREF, read only: 0: no overflow 1: overflow The overflow bit is cleared on the next conversion cycle start.
4	DATARDY	ADC Data Ready indicator (status), read only 0: data not ready 1: data ready The ADC will set bit 4 upon the completion of a conversion. At the same time, the ADCDONE bit in R14 Interrupt Request Register will be set, and an interrupt request will be generated if the ADCDONE bit is un-masked in the Interrupt Mask Register.
3	ADCSTART	Start ADC conversion 0: default 1: start conversion: writing 1 to this bit will initiate the conversion. It must be toggled in order to start a conversion. Once the bit is set, it will remain set. To start a new conversion the bit must be reset to zero and than to a one. Make sure to set ADC source before setting this bit.
2	ADCEN	ADC Enable 0: ADC disabled 1: ADC enabled
1:0	ADCSEL	ADC source selection: 0: MFP0 pin 1: MFP1 pin 2: MFP2 pin 3: MFP3 pin Make sure the same pin is not used as a GPO (bit GPOEN3:0 are not set).

R12 - ADC Data Register

This register holds the last ADC conversion value.

Bit	Field Name	Description or Comment
7:0	ADC DATA	This register holds the last conversion value. A value of 00 corresponds to VREF voltage. A value of FF corresponds to 2*VREF voltage.

R13 - Interrupt Mask Register

Bit	Field Name	Description	
7	VOUTUV	Any of the 3 bucks has an output under-voltage event	1. enable the respective interrupt source to pull the IRQ pin low 0. the respective interrupt source will be masked (no interrupt will be generated).
6	PWIUCMD	A PWI undefined command was received.	
5	PWIPERR	A PWI parity error was detected.	
4	ADCDONE	ADC conversion is done, data ready.	
3:0	COMP3:0	MFP3:0 pin, if configured as comparator, generated a comparator trigger.	

R14 - Interrupt Request Register

Bit	Field Name	Description	
7	VOUTUV	Any of the 3 bucks has an output under-voltage event	1. reading high indicate the respective source was the cause of that interrupt 2. reading low indicate the respective source was not the cause of that interrupt.
6	PWIUCMD	PWI undefined command.	
5	PWIPERR	PWI parity error	
4	ADCDONE	ADC conversion done, data ready	
3:0	COMP3:0	Comparator 3:0 tripped for the respective MFP3:0 pin, if that pins was configured as a comparator input in register R15.	

R15 - Comparator Control 1 Register

This register controls the operation of the 4 MFP pins when configured as comparator input pins.

Bit	Field Name	Description	
7	CMP3DGL	Comparator deglitching circuit for MFP3 pin.	1: four consecutive samples spaced at intervals defined in register R16, must all return the same value before the comparator data in corresponding COMP3:0 bit is updated (register R14). 0: four consecutive samples spaced at ~1µs interval, must all return the same value before the comparator data in corresponding COMP3:0 bit is updated (register R14).
6	CMP2DGL	Comparator deglitching circuit for MFP2 pin.	
5	CMP1DGL	Comparator deglitching circuit for MFP1 pin.	
4	CMP0DGL	Comparator deglitching circuit for MFP0 pin.	
3	CMP3EN	Comparator enable for MFP3 pin.	
2	CMP2EN	Comparator enable for MFP2 pin.	
1	CMP1EN	Comparator enable for MFP1 pin.	
0	CMP0EN	Comparator enable for MFP0 pin.	

The comparator is an edge triggered comparator, i.e. it checks for the input transition crossing the reference voltage level. The direction of the transition can be configured by the polarity bits in register R17. When a transition crossing the reference is detected, the corresponding comparator tripped bit in the R14 Interrupt Status Register is set. Once the comparator is tripped, the Comparator Enable bit must be set to '0' to reset the comparator logic, and then set to '1' to re-arm for the next compare.

A number of 4 consecutive samples are required to validate the tripping after the comparator output changes state. The sampling interval is configured by the select bits in register R16. The GPO function must be disabled in order to use the Multi-Function Pin as a comparator input pin.

R16 - Comparator Control 2 Register

Bit	Field Name	Description	
7:6	CMP3DM1:0	Comparator 3 deglitching sampling interval select	This register controls the deglitching sampling interval used for filtering out spurious interrupts generated by the comparators: 00: 1ms 01: 2ms 10: 4ms 11: 8ms
5:4	CMP2DM1:0	Comparator 2 deglitching sampling interval select	
3:2	CMP1DM1:0	Comparator 1 deglitching sampling interval select	
1:0	CMP0DM1:0	Comparator 0 deglitching sampling interval select	

R17 - Comparator Control 3 Register

This register controls the hysteresis and polarity of the 4 MFP pins when configured as comparator input pins.

Bit	Field Name	Description	
7	CMP3HYS	Comparator 3	Hysteresis window select: 1: 60 mV 0: 100 mV
6	CMP2HYS	Comparator 2	
5	CMP1HYS	Comparator 1	
4	CMP0HYS	Comparator 0	
3	CMP3PL	Comparator 3	Polarity select bit: 1: Compare on going up 0: Compare on going down In both polarity modes the comparator works as an edge detector: the corresponding input signal must rise above or fall below the trigger level in order the activate the interrupt. Once the comparator is tripped, the enable bit must be set to '0' to reset the comparator logic, and then set to '1' to re-arm for the next compare.
2	CMP2PL	Comparator 2	
1	CMP1PL	Comparator 1	
0	CMP0PL	Comparator 0	

R18 - GPO Control Register

This register controls the operation of the 4 MFP pins when configured as GPO output pins.

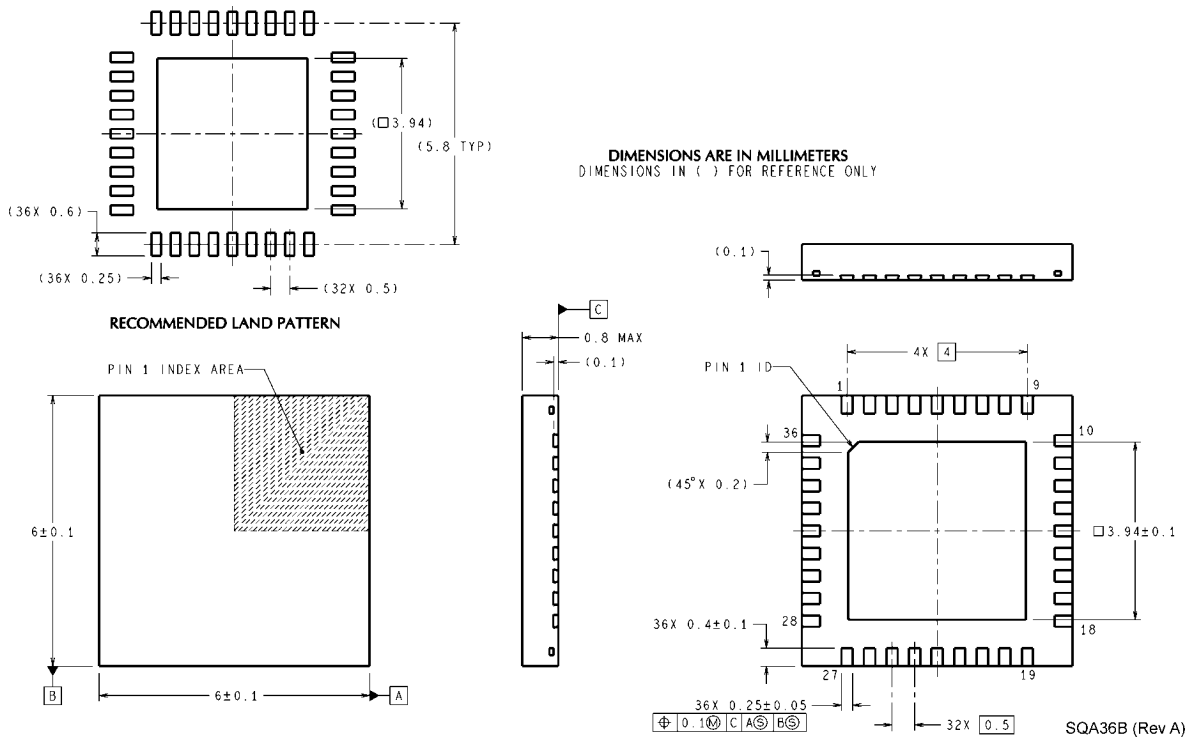
Bit	Field Name	Description	
7	GPO3OD	GPO3 Open Drain	1: GPO pin is open drain 0: GPO pin is push-pull
6	GPO2OD	GPO2 Open Drain	
5	GPO1OD	GPO1 Open Drain	
4	GPO0OD	GPO0 Open Drain	
3	GPO3EN	GPO3 Enable	1: Enable the corresponding Multi-Function Pin to be GPO 0: Disable the corresponding Multi-Function Pin to be GPO and allow the pin to be used as ADC or Comparator input pin.
2	GPO2EN	GPO2 Enable	
1	GPO1EN	GPO1 Enable	
0	GPO0EN	GPO0 Enable	

R19 - GPO Data Register

This register controls the output value of the 4 MFP pins when configured as GPO output pins and according to the settings defined in R18.

Bit	Field Name	Description	
7:4	Unused	Return zero.	
3	GPO3D	GPO3 Data Output	Write to this register to change the corresponding MFP pin state: 1: Enable the corresponding Multi-Function Pin to be GPO 0: Disable the corresponding Multi-Function Pin to be GPO and allow the pin to be used as ADC or Comparator input pin.
2	GPO2D	GPO2 Data Output	
1	GPO1D	GPO1 Data Output	
0	GPO0D	GPO0 Data Output	

Physical Dimensions inches (millimeters) unless otherwise noted



LLP Package SQA36B

Notes

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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