LM224A-LM324A

Low power quad operational amplifiers

Features

- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current/amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset voltage: 3 mV max.
- Low input offset current: 2 nA
- Wide power supply range:
  Single supply: +3 V to +30 V
  Dual supplies: ±1.5 V to ±15 V

N
DIP14
(Plastic package)

D
SO-14
(Plastic micropackage)

P
TSSOP-14
(Thin shrink small outline package)

Description

These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Order codes

Part number	Temperature range	Package	Packaging
LM224AN	-40° C, +105° C	DIP	Tube
LM224AD/ADT		SO	Tube or tape & reel
LM224APT		TSSOP (Thin shrink outline package)	Tape & reel
LM324AN	0° C, +70° C	DIP	Tube
LM324AD/ADT		SO	Tube or tape & reel
LM324APT		TSSOP (Thin shrink outline package)	Tape & reel

Contents

1 Pin connections and schematic diagram 3

2 Absolute maximum ratings 4

3 Electrical characteristics 5

4 Typical single-supply applications 11

5 Macromodels 13

6 Package mechanical data 15

6.1 DIP14 package 16

6.2 SO-14 package 17

6.3 TSSOP14 package 18

7 Revision history 19

1 Pin connections and schematic diagram

Figure 1. Pin connections (top view)

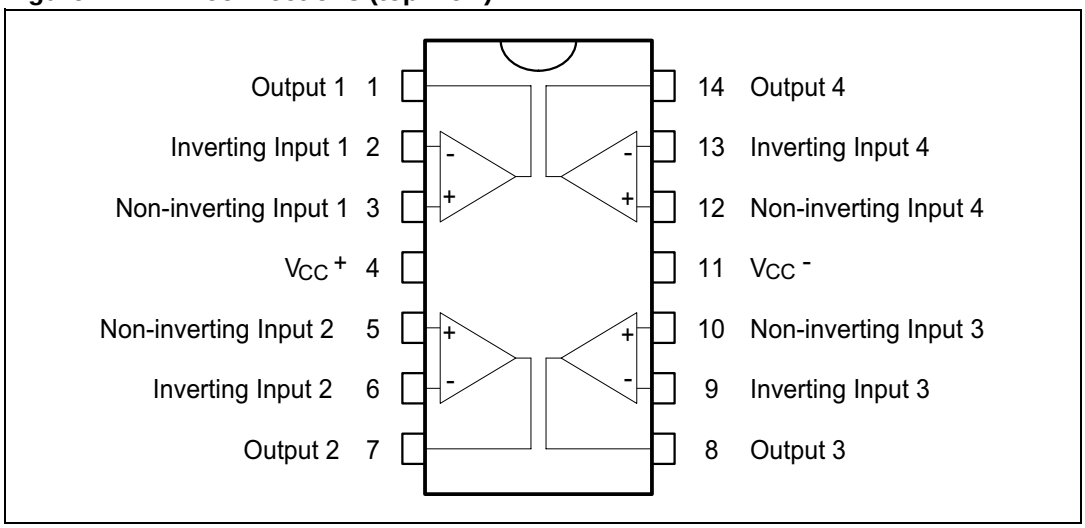
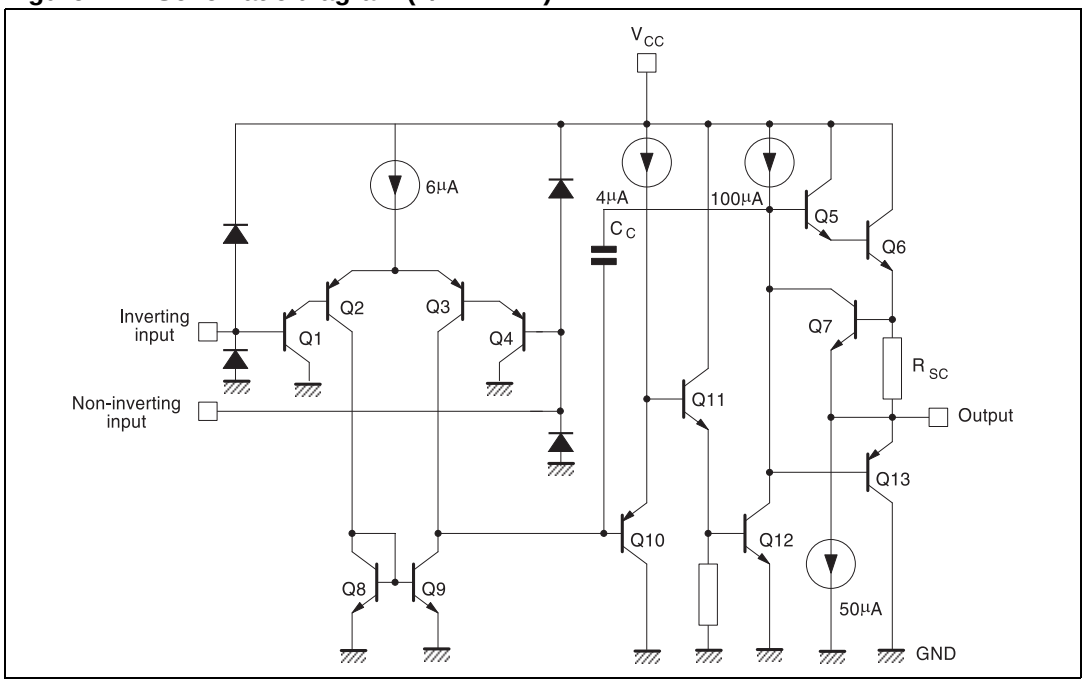


Figure 2. Schematic diagram (1/4 LM124)



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	LM224A	LM324A	Unit
V_{CC}	Supply voltage	±16 or 32		V
V_i	Input voltage	-0.3 to V_{CC} + 0.3		V
V_{id}	Differential input voltage (1)	32		V
P_{tot}	Power dissipation: N suffix D suffix	 500 400	 500 400	mW
	Output short-circuit duration (2)	Infinite		
I_{in}	Input current (3)	50		mA
T_{oper}	Operating free-air temperature range	-40 to +105	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150		°C
T_j	Maximum junction temperature	150		°C
R_{thja}	Thermal resistance junction to ambient(4): SO14 TSSOP14 DIP14	 103 100 83		°C/W
R_{thjc}	Thermal resistance junction to case: SO14 TSSOP14 DIP14	 31 32 33		°C/W
ESD	HBM: human body model(5)	700		V
	MM: machine model(6)	150		
	CDM: charged device model	1500		

1. Neither of the input voltages must exceed the magnitude of V_{CC}^+ or V_{CC}^-.
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These are typical values given for a single layer board (except for TSSOP which is a two-layer board).
5. Human body model, 100 pF discharged through a 1.5 kΩ resistor into pin of device.
6. Machine model ESD, a 200 pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin-to-pin of device.

3 Electrical characteristics

Table 2. V_{CC}^{+} = +5V, V_{CC}^{-}= Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1): T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$		2	3 5	mV
I_{io}	Input offset current: T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$		2	20 40	nA
I_{ib}	Input bias current (2): T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$		20	100 200	nA
A_{vd}	Large signal voltage gain: V_{CC}^{+} = +15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_s \leq$ 10 kΩ): V_{CC}^{+} = 5 V to 30 V T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 65 65	110		dB
I_{CC}	Supply current, all Amp, no load: – T_{amb} = +25° C V_{CC} = +5V V_{CC} = +30 V – $T_{min} \leq T_{amb} \leq T_{max}$ V_{CC} = +5 V V_{CC} = +30 V		 0.7 1.5 0.8 1.5	 1.2 3 1.2 3	mA
V_{icm}	Input common mode voltage range: V_{CC} = +30 V (3) T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 0 0		 V_{CC} -1.5 V_{CC} -2	V
CMR	Common mode rejection ratio ($R_s \leq$10 kΩ): T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	70 60	80		dB
I_{source}	Output current source (V_{id} = +1 V): V_{CC} = +15 V, V_o = +2 V	20	40	70	mA
I_{sink}	Output sink current (V_{id} = -1 V): V_{CC} = +15 V, V_o = +2 V V_{CC} = +15 V, V_o = +0.2 V	10 12	20 50		mA µA

Table 2. V_{CC}^+ = +5V, V_{CC}^-= Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage V_{CC} = +30 V, R_L = 2 kΩ T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	 26 26	27		V
	V_{CC} = +30 V, R_L = 10 kΩ T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 27 27	28		V
	V_{CC} = +5 V, R_L = 2 kΩ T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 3.5 3			V
V_{OL}	Low level output voltage (R_L = 10kΩ): T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		5	 20 20	mV
SR	Slew rate: V_{CC} = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		0.4		V/µs
GBP	Gain bandwidth product: V_{CC} = 30 V, f =100 kHz, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100pF		1.3		MHz
THD	Total harmonic distortion: f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, V_{CC} = 30V		0.015		%
e_n	Equivalent input noise voltage: f = 1 kHz, R_s = 100 Ω, V_{CC} = 30 V		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	30	µV/°C
DI_{io}	Input offset current drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel separation(4) - 1kHz ≤ f ≤ 20 kHZ		120		dB

1. V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no load change on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5 V, but either or both inputs can go to +32 V without damage.
4. Due to the proximity of external components, ensure that there is no coupling originating from stray capacitance between these external parts. Typically, this can be detected at higher frequencies because this type of capacitance increases.

Figure 3. Input bias current vs. ambient temperature

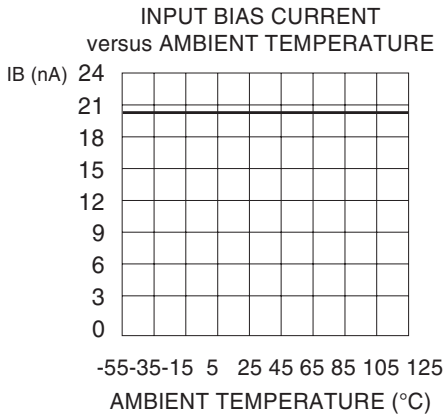


Figure 4. Current limiting

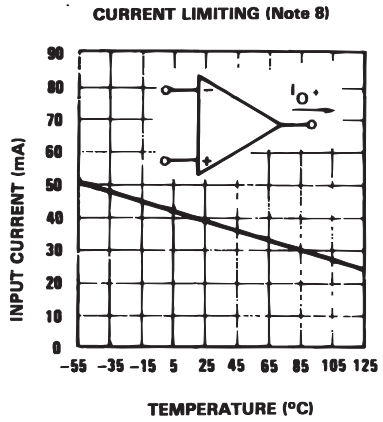


Figure 5. Input voltage range

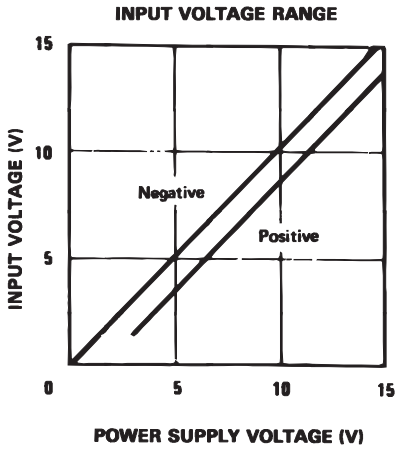


Figure 6. Supply current

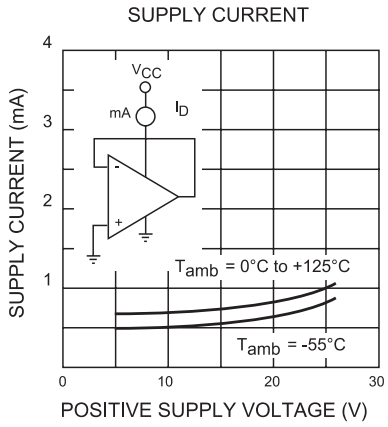


Figure 7. Gain bandwidth product

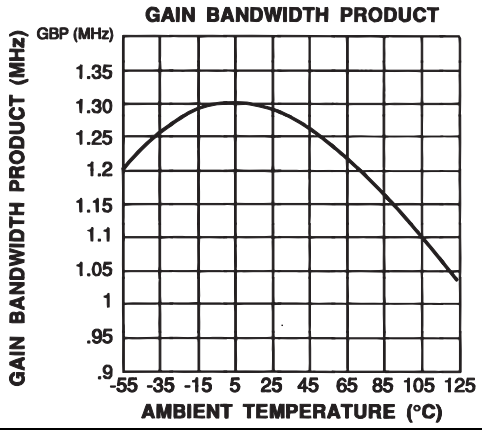


Figure 8. Common mode rejection ratio

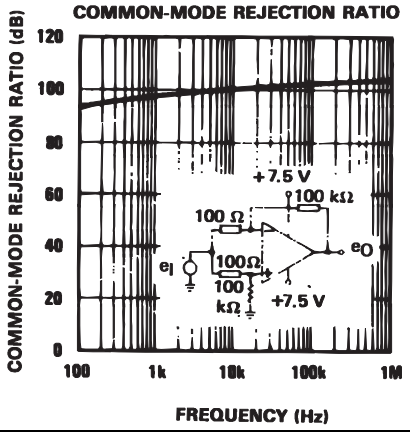


Figure 9. Input bias current vs. ambient temperature

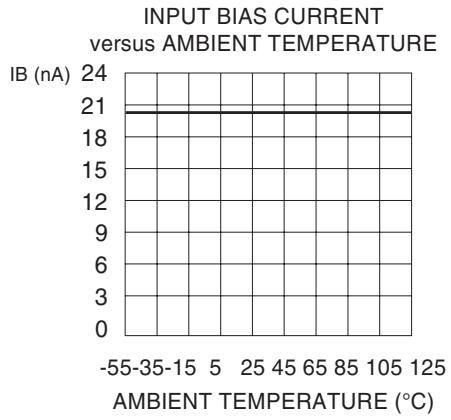


Figure 10. Current limiting

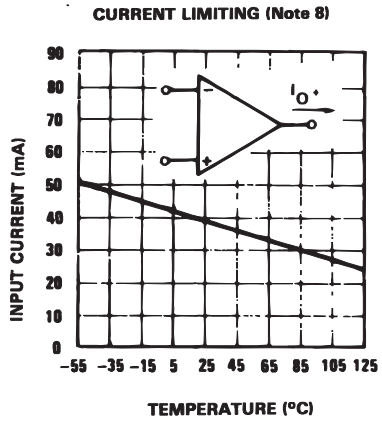


Figure 11. Input voltage range

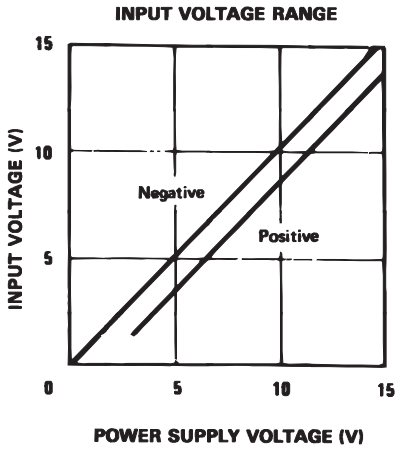


Figure 12. Supply current

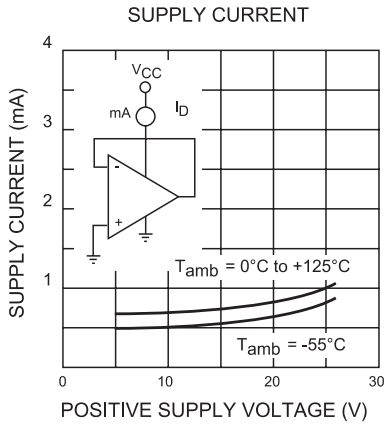


Figure 13. Gain bandwidth product

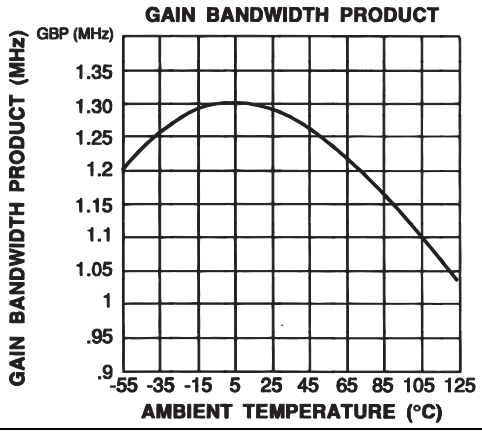


Figure 14. Common mode rejection ratio

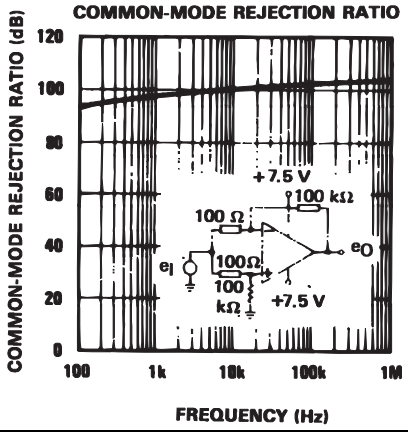


Figure 15. Electrical curves

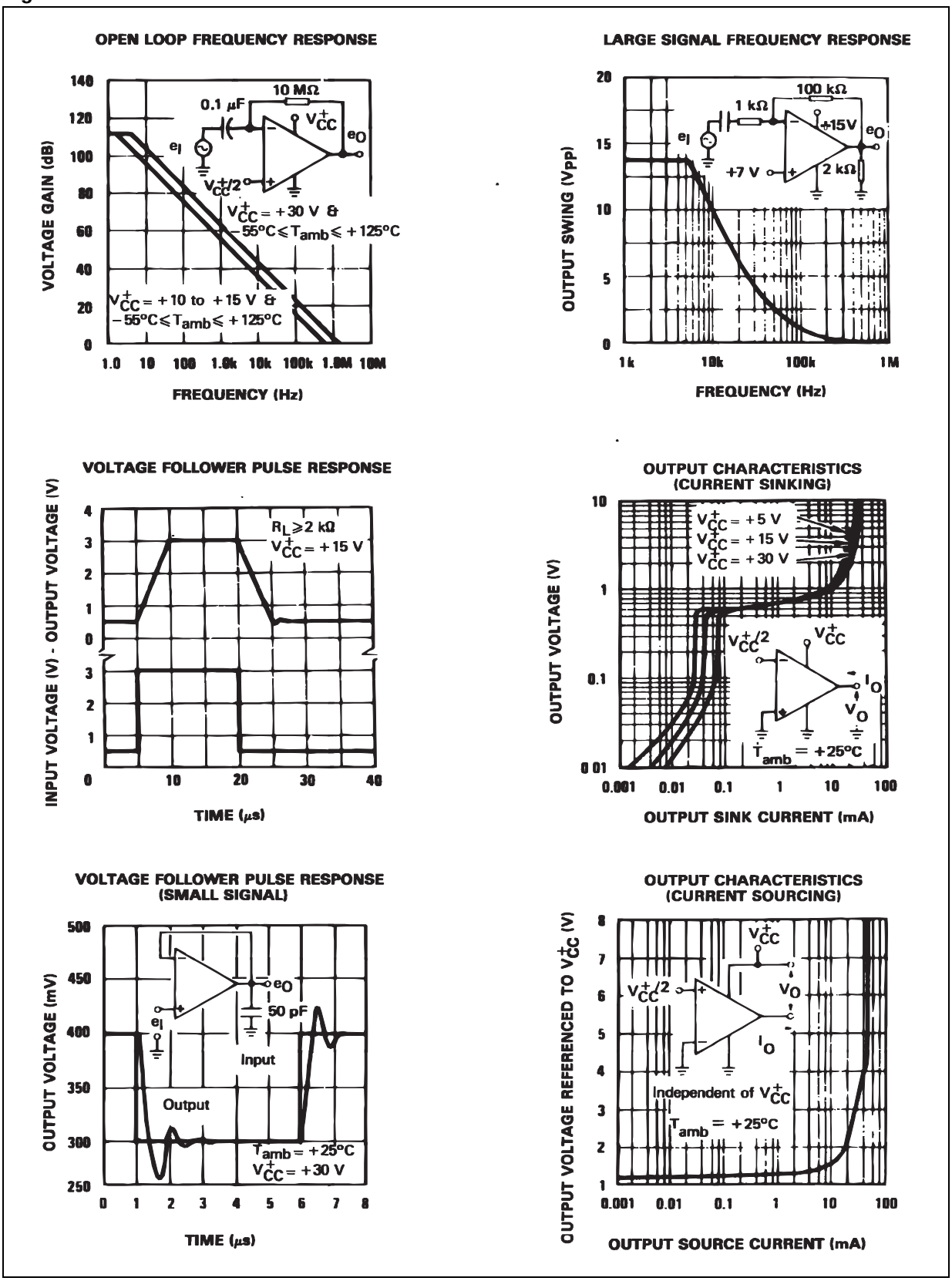


Figure 16. Input current

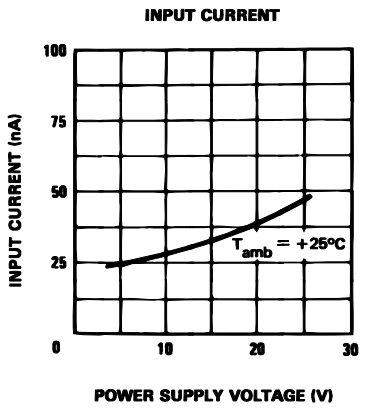


Figure 17. Large signal voltage gain

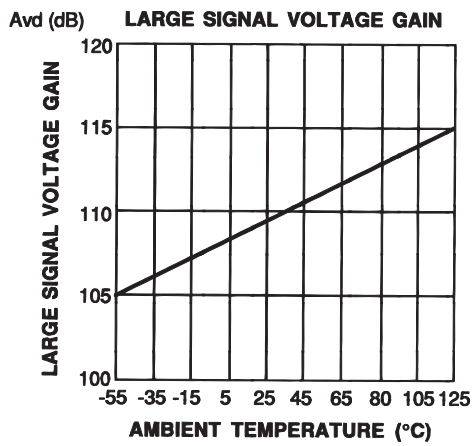


Figure 18. Power supply & common mode rejection ratio

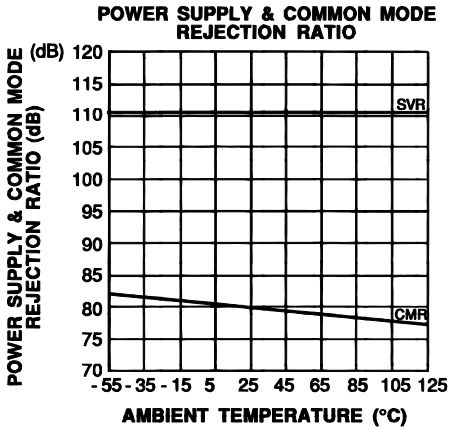
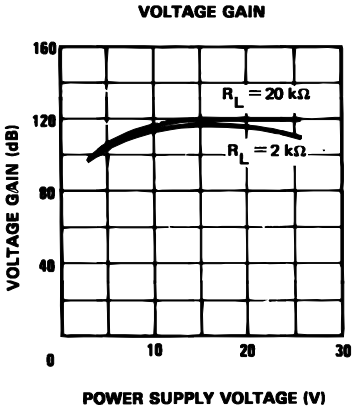


Figure 19. Voltage gain



4 Typical single-supply applications

Figure 20. AC coupled inverting amplifier

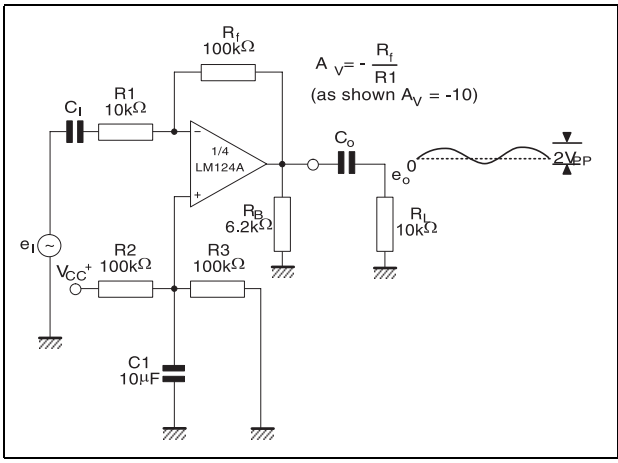


Figure 21. High input Z adjustable gain DC instrumentation amplifier

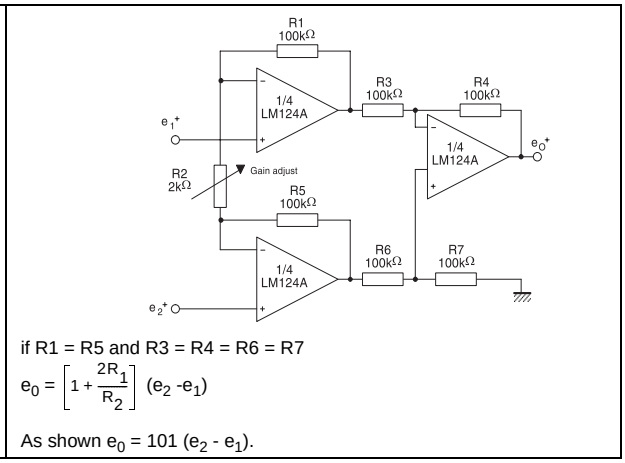


Figure 22. AC coupled non inverting amplifier

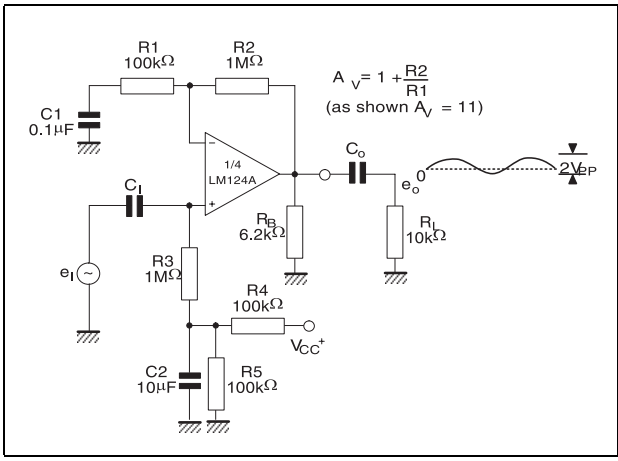


Figure 23. DC summing amplifier

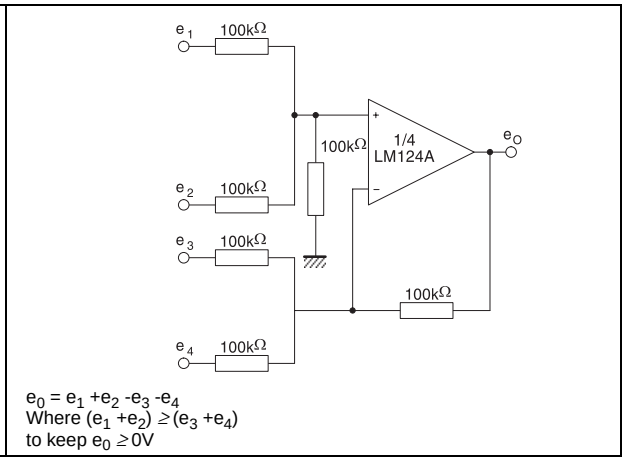


Figure 24. Non-inverting DC gain

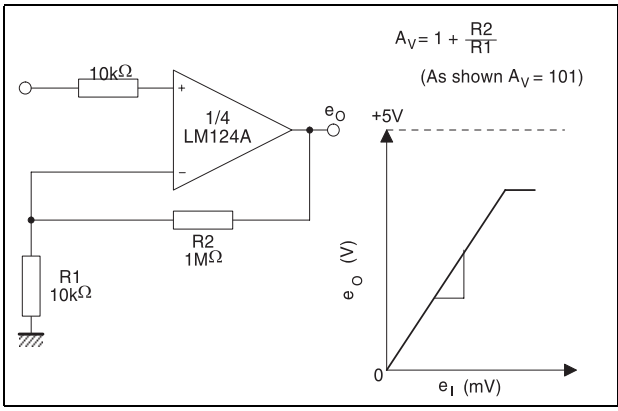


Figure 25. Low drift peak detector

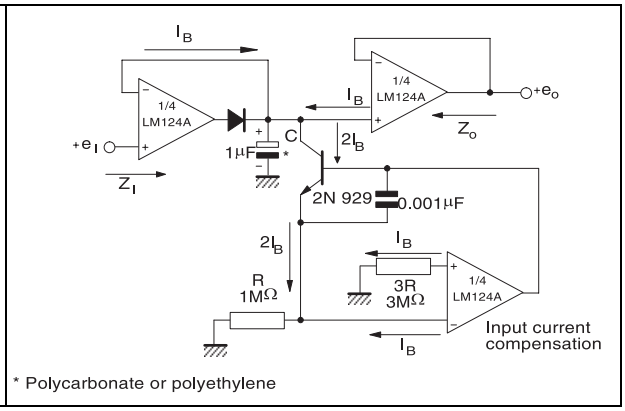
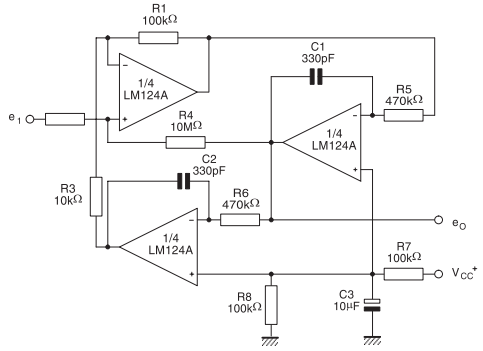


Figure 26. Active bandpass filter

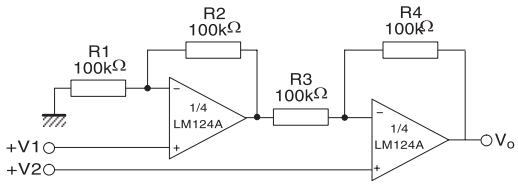


Fo = 1kHz
Q = 50
Av = 100 (40dB)

Figure 27. High input Z, DC differential amplifier

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$

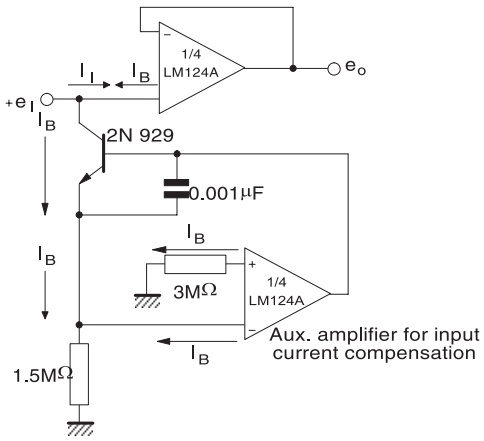
(CMRR depends on this resistor ratio match)



$e_0 \left(1 + \frac{R_4}{R_3}\right) (e_2 - e_1)$

As shown $e_0 = (e_2 - e_1)$

Figure 28. Using symmetrical amplifiers to reduce input current (general concept)



5 Macromodels

Note: *Please consider the following before using this macromodel:*

All models are a trade-off between accuracy and complexity (i.e. simulation time).

Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.

*A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.*

Data issued from macromodels that is used outside of the specified conditions (V_{CC}, temperature, etc.) or even worse, outside of the device operating conditions (V_{CC}, V_{icm}, etc.) is not reliable in any way.

```
** Standard Linear Ics Macromodels, 1993.

** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY


.SUBCKT LM124 1 3 2 4 5

*******************************************************

.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F

* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
```

```
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

The values provided in *Table 3* are derived from this macromodel.

Table 3. V_{cc}^{+} = +15V, V_{cc}^{-} = 0V, T_{amb} = 25°C (unless otherwise specified)

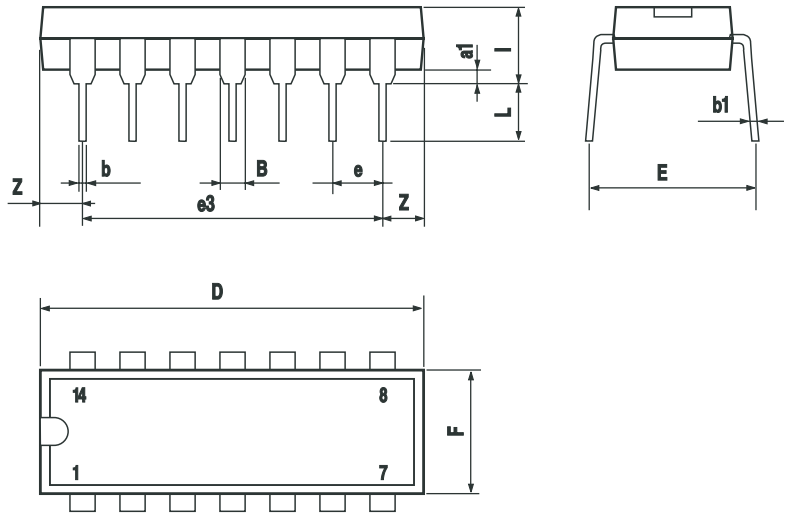
Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 2 kΩ	100	V/mV
I_{cc}	No load, per amplifier	350	µA
V_{icm}		0 to +13.5	V
V_{OH}	R_L = 2 kΩ (V_{CC}^{+}=15 V)	+13.5	V
V_{OL}	R_L = 10 kΩ	5	mV
I_{os}	V_o = +2 V, V_{CC} = +15 V	+40	mA
GBP	R_L = 2 kΩ, C_L = 100 pF	1.3	MHz
SR	R_L = 2 kΩ, C_L = 100 pF	0.4	V/µs

6 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP14 package

Plastic DIP-14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

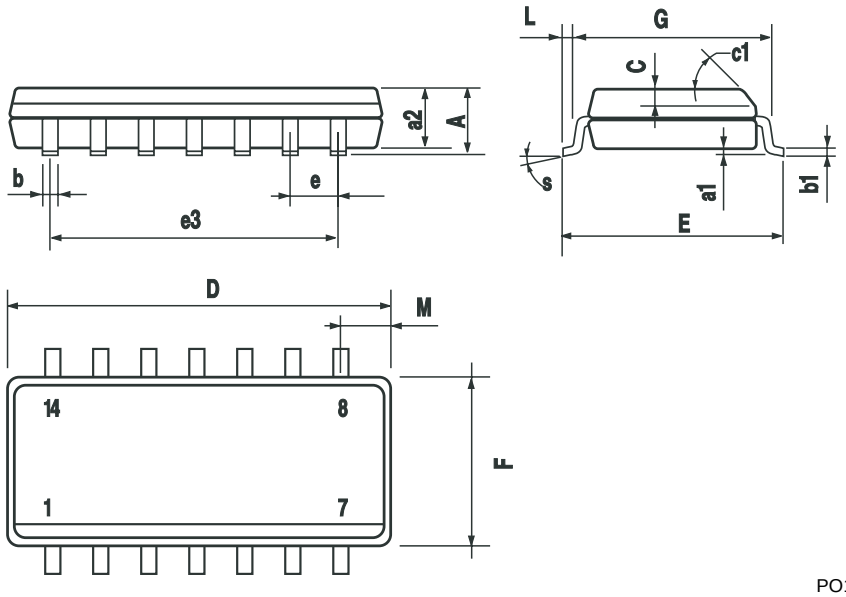


P001A

6.2 SO-14 package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45˚ (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8˚ (max.)					

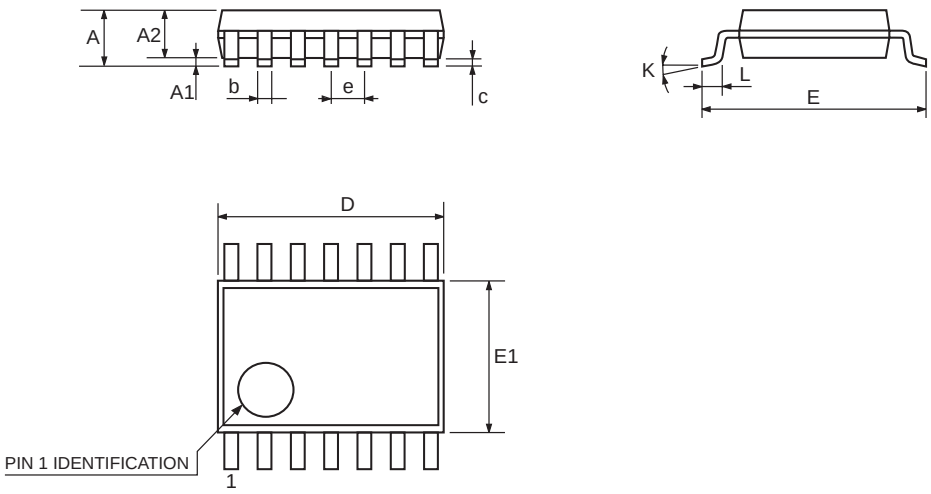


PO13G

6.3 TSSOP14 package

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080337D

7 Revision history

Table 4. Document revision history

Date	Revision	Changes
1-Mar-2001	1	First Release
1-Feb-2005	2	Added explanation of V_{id} and V_i limits in *Table 1 on page 4*. Updated macromodel.
1-Jun-2005	3	ESD protection inserted in *Table 1 on page 4*.
25-Sep-2006	4	Editorial update.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com