LM75x Digital Temperature Sensor and Thermal Watchdog With Two-Wire Interface

1 Features

- No External Components Required
- Shutdown Mode to Minimize Power Consumption
- Up to Eight LM75s Can be Connected to a Single Bus
- Power Up Defaults Permit Stand-alone Operation as Thermostat
- UL Recognized Component (LM75B and LM75C)
- Key Specifications:
  - Supply Voltage
    - LM75B, LM75C: 3 V to 5.5 V
  - Supply Current
    - Operating: 280 µA (typical)
    - Shutdown: 4 µA (typical)
  - Temperature Accuracy
    - −25°C to 100°C: ±2°C (maximum)
    - −55°C to 125°C: ±3°C (maximum)

2 Applications

- General System Thermal Management
- Communications Infrastructure
- Electronic Test Equipment
- Environmental Monitoring

3 Description

The LM75B and LM75C are industry-standard digital temperature sensors with an integrated Sigma-Delta analog-to-digital converter and I^2C interface. The LM75 provides 9-bit digital temperature readings with an accuracy of ±2°C from -25°C to 100°C and ±3°C over –55°C to 125°C.

Communication is accomplished over a 2-wire interface which operates up to 400kHz. The LM75 has three address pins, allowing up to eight LM75 devices to operate on the same 2-wire bus. The LM75 has a dedicated over-temperature output (O.S.) with programmable limit and hystersis. This output has programmable fault tolerance, which allows the user to define the number of consecutive error conditions that must occur before O.S. is activated.

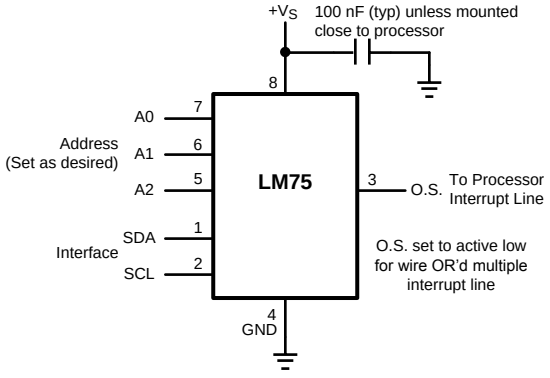
The wide temperature and supply range and I^2C interface make the LM75 ideal for a number of applications including base stations, electronic test equipment, office electronics, personal computers, and any other system where thermal management is critical to performance. The LM75B and LM75C are available in an SOIC package or VSSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM75B	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (January 2015) to Revision D — **Page**

- Updated *Thermal Information* table. ... 4
- Corrected UNIT error in *I^2C Digital Switching Characteristics* table. ... 7
- Added *Community Resources* section. ... 23

Changes from Revision B (March 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

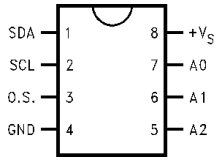
Changes from Revision A (March 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 20

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5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC, VSSOP
Top View



Pin Functions

PIN		DESCRIPTION	TYPICAL CONNECTION
NO.	NAME		
1	SDA	I^2C Serial Bi-Directional Data Line. Open Drain.	From Controller, tied to a pullup resistor or current source
2	SCL	I^2C Clock Input	From Controller, tied to a pullup resistor or current source
3	O.S.	Over temperature Shutdown. Open Drain Output	Pullup Resistor, Controller Interrupt Line
4	GND	Power Supply Ground	Ground
5	A2	User-Set I^2C Address Inputs	Ground (Low, 0) or $+V_S$ (High, 1)
6	A1		
7	A0		
8	$+V_S$	Positive Supply Voltage Input	DC Voltage from 3 V to 5.5 V; 100-nF bypass capacitor with 10-µF bulk capacitance in the near vicinity

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage Pin ($+V_S$)	−0.3	6.5	V
Voltage at A0, A1and A2 Pins	−0.3	($+V_S$ + 0.3) and must be ≤ 6.5	V
Voltage at O.S., SCL and SDA Pins	−0.3	6.5	V
Input Current at any Pin(2)		5	mA
Package Input Current(2)		20	mA
O.S. Output Sink Current		10	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > $+V_S$) the current at that pin should be limited to 5 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

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6.2 ESD Ratings

			VALUE	UNIT
LM75B				
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM)	±2500	V
		Machine model	±250	
LM75C				
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM)	±1500	V
		Machine Model	±100	

(1) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. The Charged Device Model (CDM) is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Specified Temperature Range	T_{MIN}	T_{MAX}	
	–55	125	°C
Supply Voltage Range ($+V_S$) LM75B, LM75C	3	5.5	V

(1) Soldering process must comply with Texas Instruments Incorporated Reflow Temperature Profile specifications. Refer to
(2) Reflow temperature profiles are different for lead-free and non-lead-free packages.

6.4 Thermal Information

THERMAL METRIC(1)		LM75B		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	158.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.2	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	78.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.8	77.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for: $+V_S$ = 5 Vdc for LM75BIM-5, LM75BIMM-5, LM75CIM-5, and LM75CIMM-5; and $+V_S$ = 3.3 Vdc for LM75BIM-3, LM75BIMM-3, LM75CIM-3, and LM75CIMM-3(1). $T_A = T_J$ = 25°C, unless otherwise noted.(2)

PARAMETER		TEST CONDITIONS	MIN(3)	TYP(4)	MAX(3)	UNIT
Accuracy		T_A = −25°C to 100°C	–2		2	°C
		T_A = −55°C to 125°C	–3		3	
Resolution				9		Bits
Temperature Conversion Time		See(5)		100		ms
		See(5), –55°C ≤ T_A ≤ 125°C			300	
Quiescent Current	LM75B	I^2C Inactive		0.25		mA
		I^2C Inactive, –55°C ≤ T_A ≤ 125°C			0.5	
		Shutdown Mode, $+V_S$ = 3 V		4		µA
		Shutdown Mode, $+V_S$ = 5 V		6		
	LM75C	I^2C Inactive		0.25		mA
		I^2C Inactive, –55°C ≤ T_A ≤ 125°C			1	
		Shutdown Mode, $+V_S$ = 3 V		4		µA
		Shutdown Mode, $+V_S$ = 5 V		6		
O.S. Output Saturation Voltage		I_{OUT} = 4.0 mA, –55°C ≤ T_A ≤ 125°C			0.8	V
O.S. Delay		See (6), –55°C ≤ T_A ≤ 125°C	1		6	Conversions
T_{OS} Default Temperature		See (7)		80		°C
T_{HYST} Default Temperature				75		

(1) All part numbers of the LM75 will operate properly over the $+V_S$ supply voltage range of 3 V to 5.5 V. The devices are tested and specified for rated accuracy at their nominal supply voltage. Accuracy will typically degrade 1°C/V of variation in $+V_S$ as it varies from the nominal value.
(2) For best accuracy, minimize output loading. Higher sink currents can affect sensor accuracy with internal heating. This can cause an error of 0.64°C at full rated sink current and saturation voltage based on junction-to-ambient thermal resistance.
(3) Limits are specified to AOQL (Average Outgoing Quality Level).
(4) Typicals are at T_A = 25°C and represent most likely parametric norm.
(5) The conversion-time specification is provided to indicate how often the temperature data is updated. The LM75 can be accessed at any time and reading the Temperature Register will yield result from the last temperature conversion. When the LM75 is accessed, the conversion that is in process will be interrupted and it will be restarted after the end of the communication. Accessing the LM75 continuously without waiting at least one conversion time between communications will prevent the device from updating the Temperature Register with a new temperature conversion result. Consequently, the LM75 should not be accessed continuously with a wait time of less than 300 ms.
(6) O.S. Delay is user programmable up to 6 “over limit” conversions before O.S. is set to minimize false tripping in noisy environments.
(7) Default values set at power up.

6.6 Digital DC Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = 5 Vdc for LM75BIM-5, LM75BIMM-5, LM75CIM-5, and LM75CIMM-5; and $+V_S$ = 3.3 Vdc for LM75BIM-3, LM75BIMM-3, LM75CIM-3, and LM75CIMM-3(1). $T_A = T_J$ = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
$V_{IN(1)}$	Logical “1” Input Voltage	–55°C ≤ T_A ≤ 125°C	$+V_S$ × 0.7		$+V_S$ + 0.3	V
$V_{IN(0)}$	Logical “0” Input Voltage	–55°C ≤ T_A ≤ 125°C	−0.3		$+V_S$ × 0.3	V
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = +V_S$		0.005		µA
		$V_{IN} = +V_S$, –55°C ≤ T_A ≤ 125°C			1	
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0 V		−0.005		µA
		V_{IN} = 0 V, –55°C ≤ T_A ≤ 125°C			−1	

(1) All part numbers of the LM75 will operate properly over the $+V_S$ supply voltage range of 3 V to 5.5 V. The devices are tested and specified for rated accuracy at their nominal supply voltage. Accuracy will typically degrade 1°C/V of variation in $+V_S$ as it varies from the nominal value.
(2) Limits are specified to AOQL (Average Outgoing Quality Level).
(3) Typicals are at T_A = 25°C and represent most likely parametric norm.

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Digital DC Characteristics (continued)

Unless otherwise noted, these specifications apply for $+V_S$ = 5 Vdc for LM75BIM-5, LM75BIMM-5, LM75CIM-5, and LM75CIMM-5; and $+V_S$ = 3.3 Vdc for LM75BIM-3, LM75BIMM-3, LM75CIM-3, and LM75CIMM-3[1]. $T_A = T_J$ = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
C_{IN}	All Digital Inputs				5		pF
I_{OH}	High Level Output Current	LM75B	V_{OH} = 5 V, –55°C ≤ T_A ≤ 125°C			10	µA
		LM75C	V_{OH} = 5 V, –55°C ≤ T_A ≤ 125°C			100	µA
V_{OL}	Low Level Output Voltage		I_{OL} = 3 mA, –55°C ≤ T_A ≤ 125°C			0.4	V
t_{OF}	Output Fall Time		C_L = 400 pF I_O = 3 mA, –55°C ≤ T_A ≤ 125°C			250	ns

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6.7 I²C Digital Switching Characteristics

Unless otherwise noted, these specifications apply for V_S = 5 Vdc for LM75BIM-5, LM75BIMM-5, LM75CIM-5, and LM75CIMM-5; and $+V_S$ = 3.3 Vdc for LM75BIM-3, LM75BIMM-3, LM75CIM-3, and LM75CIMM-3, C_L (load capacitance) on output lines = 80 pF unless otherwise specified. $T_A = T_J$ = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN(1)(2)	TYP(3)	MAX(1)(2)	UNIT
t_1	SCL (Clock) Period, See Figure 1		–55°C ≤ T_A ≤ 125°C	2.5			µs
t_2	Data in Set-Up Time to SCL High, See Figure 1		–55°C ≤ T_A ≤ 125°C	100			ns
t_3	Data Out Stable after SCL Low, See Figure 1		–55°C ≤ T_A ≤ 125°C	0			ns
t_4	SDA Low Set-Up Time to SCL Low (Start Condition), See Figure 1		–55°C ≤ T_A ≤ 125°C	100			ns
t_5	SDA High Hold Time after SCL High (Stop Condition), See Figure 1		–55°C ≤ T_A ≤ 125°C	100			ns
$t_{TIMEOUT}$	SDA Time Low for Reset of Serial Interface(4)	LM75B	–55°C ≤ T_A ≤ 125°C	75		325	ms
		LM75C				Not Applicable	

(1) Limits are specified to AOQL (Average Outgoing Quality Level).
(2) Timing specifications are tested at the bus input logic levels (Vin(0)=0.3xVA for a falling edge and Vin(1)=0.7xVA for a rising edge) when the SCL and SDA edge rates are similar.
(3) Typicals are at T_A = 25°C and represent most likely parametric norm.
(4) Holding the SDA line low for a time greater than $t_{TIMEOUT}$ will cause the LM75B to reset SDA to the IDLE state of the serial bus communication (SDA set High).

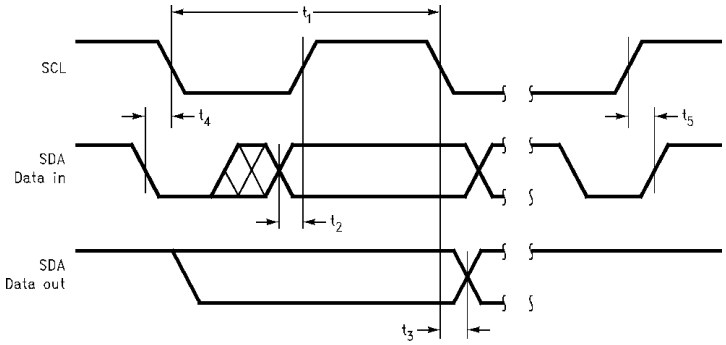


Figure 1. Timing Diagram

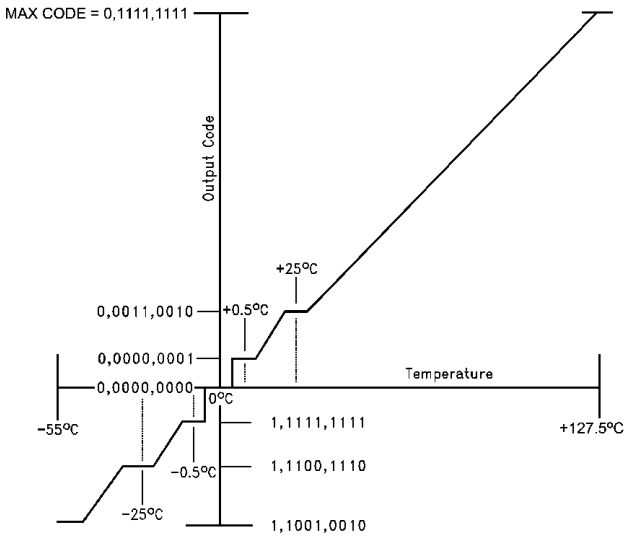
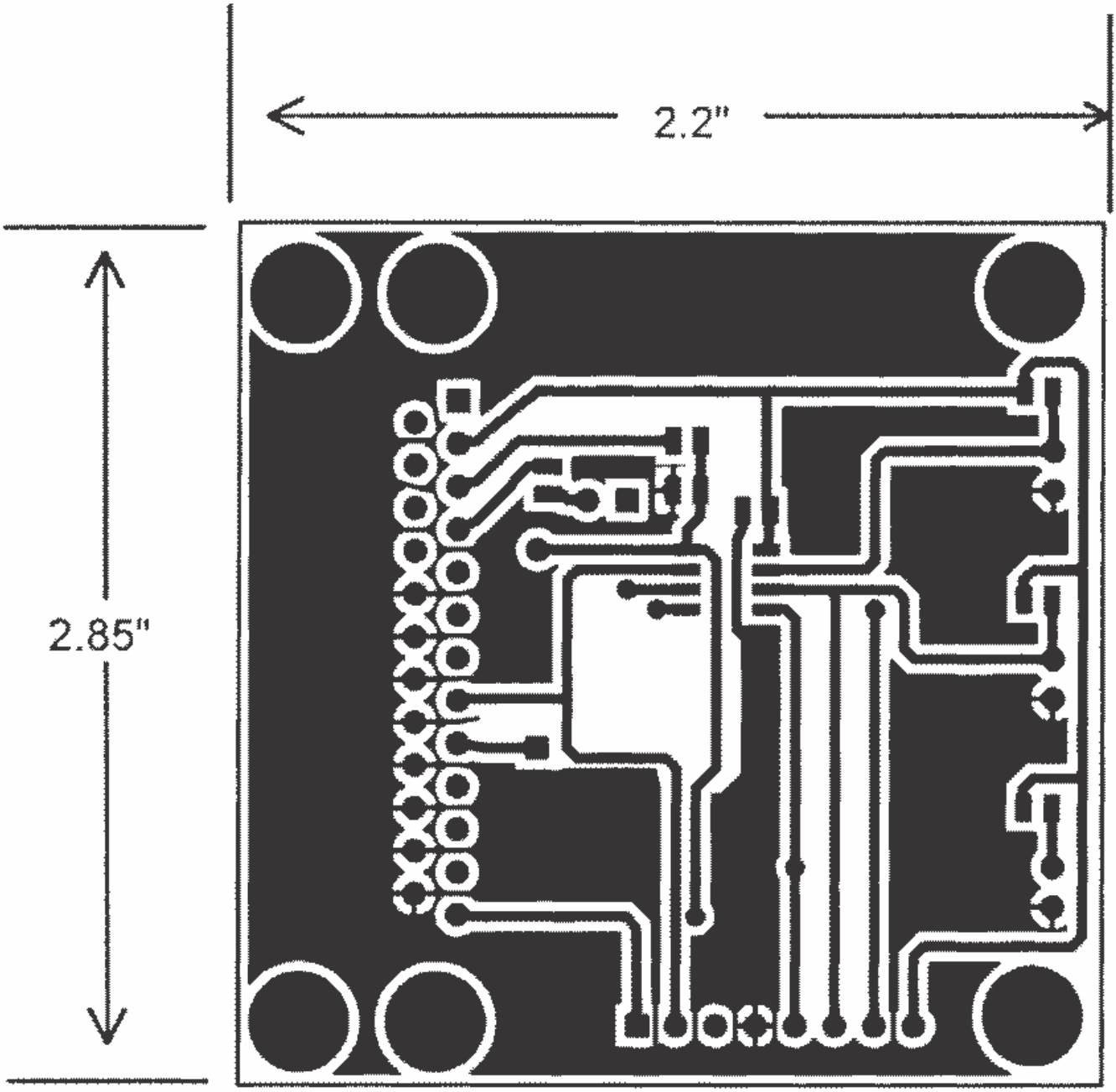


Figure 2. Temperature-to-Digital Transfer Function (Non-Linear Scale for Clarity)

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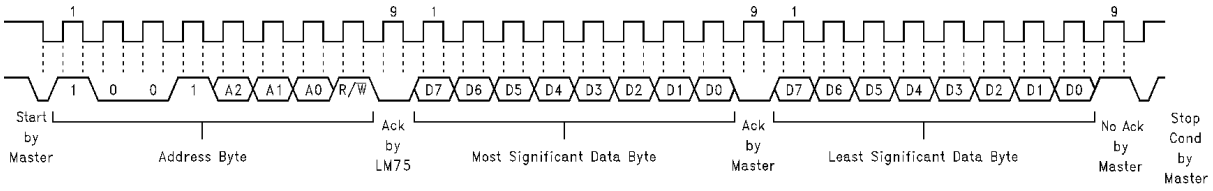


LM75C θ_{JA} (thermal resistance, junction-to-ambient) when attached to a printed circuit board with 2 oz. foil similar to the one shown. Summarized below:

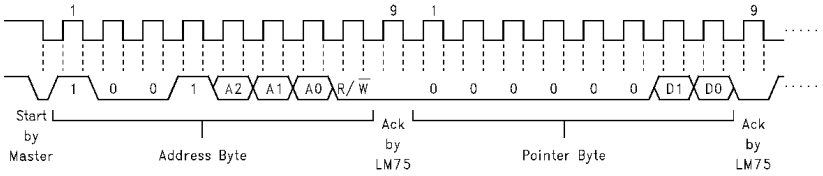
Device Number	Package Number	Thermal Resistance (θ_{JA})
LM75BIM-3, LM75BIM-5, LM75CIM-3, LM75CIM-5	D (R-PDSO-G8)	200°C/W
LM75BIMM-3, LM75BIMM-5, LM75CIMM-3, LM75CIMM-5	DGK (S-PDSO-G8)	250°C/W

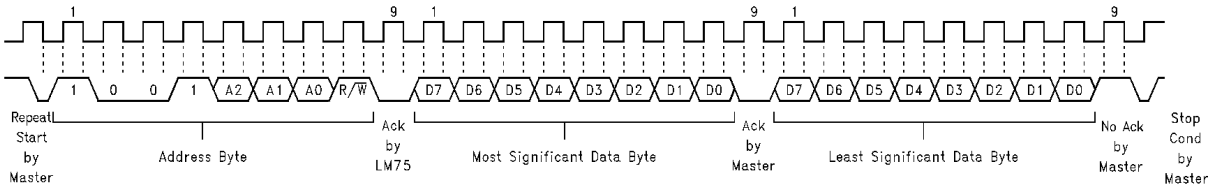
Figure 3. Printed Circuit Board Used for Thermal Resistance Specifications

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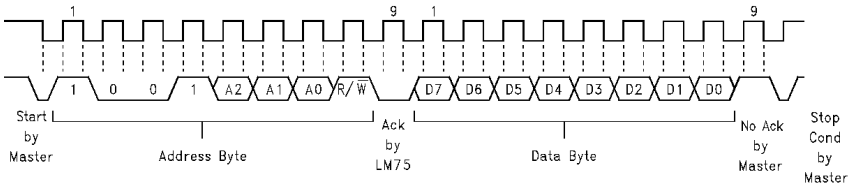


(a) Typical 2-Byte Read From Preset Pointer Location Such as Temp, T_{OS}, T_{HYST}





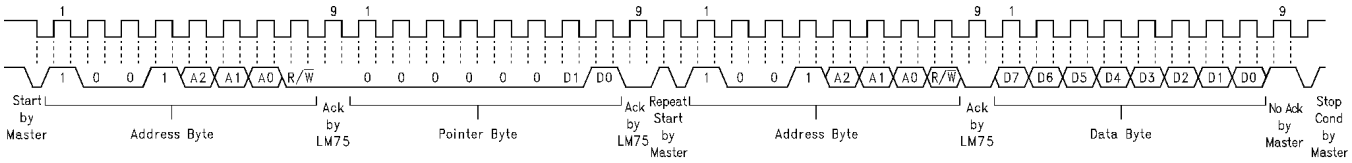
(b) Typical Pointer Set Followed by Immediate Read for 2-Byte Register such as Temp, T_{OS}, T_{HYST}



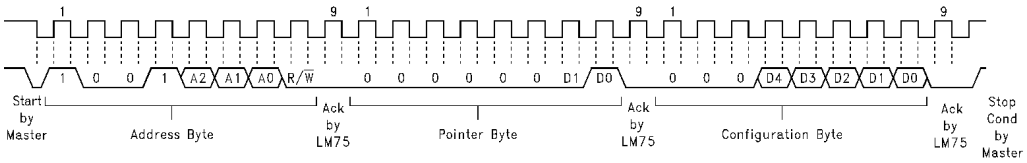
(c) Typical 1-Byte Read From Configuration Register With Preset Pointer

Figure 4. I^2C Timing Diagrams

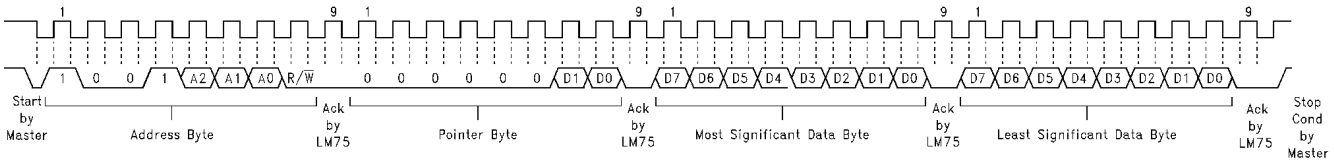
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(a) Typical Pointer Set Followed by Immediate Read from Configuration Register



(b) Configuration Register Write



(c) T_{OS} and T_{HYST} Write

Figure 5. I²C Timing Diagrams (Continued)

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6.8 Typical Characteristics

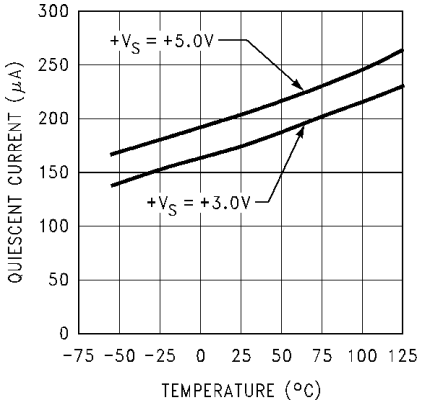


Figure 6. Static Quiescent Current vs Temperature (LM75C)

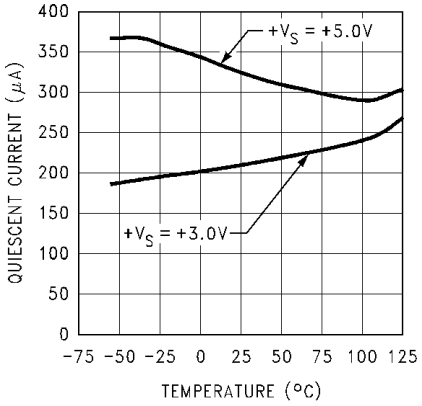


Figure 7. Dynamic Quiescent Current vs Temperature (LM75C)

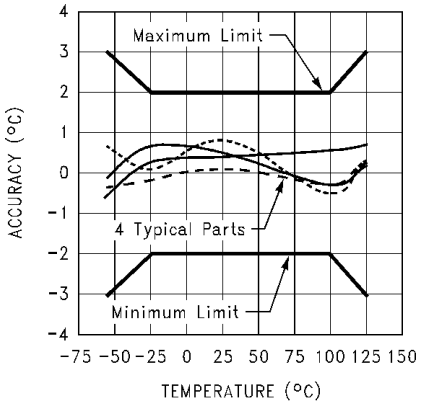


Figure 8. Accuracy vs Temperature (LM75C)

7 Detailed Description

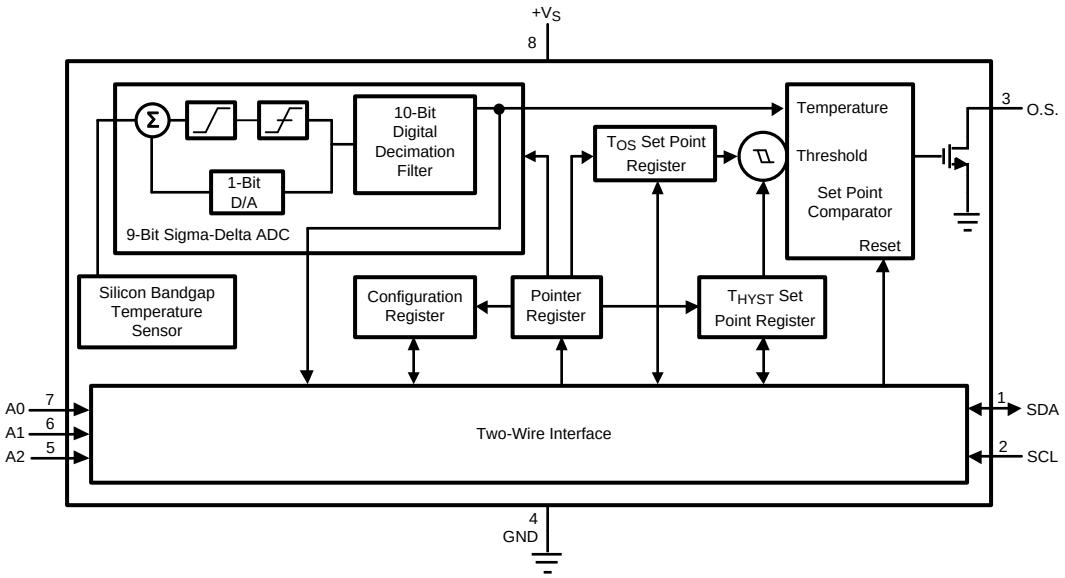
7.1 Overview

The LM75 temperature sensor incorporates a band-gap type temperature sensor and 9-bit ADC (Sigma-Delta Analog-to-Digital Converter). The temperature data output of the LM75 is available at all times via the I^2C bus. If a conversion is in progress, it will be stopped and restarted after the read. A digital comparator is also incorporated that compares a series of readings, the number of which is user-selectable, to user-programmable setpoint and hysteresis values. The comparator trips the O.S. output line, which is programmable for mode and polarity.

The LM75B contains all the functionality of the LM75C, plus two additional features:

- The LM75B has an integrated low-pass filter on both the SDA and the SCL line. These filters increase communications reliability in noisy environments.
- The LM75B also has a bus fault timeout feature. If the SDA line is held low for longer than $t_{TIMEOUT}$ (see *I^2C Digital Switching Characteristics*) the LM75B will reset to the IDLE state (SDA set to high impedance) and wait for a new start condition. The TIMEOUT feature is not functional in Shutdown Mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Sensor

The LM75 is an industry-standard digital temperature sensor with an integrated Sigma-Delta analog-to-digital converter and I^2C interface. The LM75 provides 9-bit digital temperature readings with an accuracy of ±2°C from –25°C to 100°C and ±3°C over –55°C to 125°C.

The LM75 operates with a single supply from 2.7 V to 5.5 V. Communication is accomplished over a 2-wire interface which operates up to 400kHz. The LM75 has three address pins, allowing up to eight LM75 devices to operate on the same 2-wire bus. The LM75 has a dedicated over-temperature output (O.S.) with programmable limit and hysteresis. This output has programmable fault tolerance, which allows the user to define the number of consecutive error conditions that must occur before O.S. is activated.

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7.4 Device Functional Modes

In Comparator mode the O.S. Output behaves like a thermostat. The output becomes active when temperature exceeds the T_{OS} limit, and leaves the active state when the temperature drops below the T_{HYST} limit. In this mode the O.S. output can be used to turn a cooling fan on, initiate an emergency system shutdown, or reduce system clock speed. Shutdown mode does not reset O.S. state in a comparator mode.

In Interrupt mode exceeding T_{OS} also makes O.S. active but O.S. will remain active indefinitely until reset by reading any register via the I^2C interface. Once O.S. has been activated by crossing T_{OS}, then reset, it can be activated again only by Temperature going below T_{HYST}. Again, it will remain active indefinitely until being reset by a read. Placing the LM75 in shutdown mode also resets the O.S. Output.

The LM75B always powers up in a known state. The power up default conditions are:

1. Comparator mode
2. T_{OS} = 80°C
3. T_{HYST} = 75°C
4. O.S. active low
5. Pointer = “00”

When the supply voltage is less than about 1.7V, the LM75 is considered powered down. As the supply voltage rises above the nominal 1.7V power up threshold, the internal registers are reset to the power up default values listed above.

If the LM75 is *not connected* to the I^2C bus on power up, it will act as a stand-alone thermostat with the power up default conditions listed above. It is optional, but recommended, to connect the address pins (A2, A1, A0) and the SCL and SDA pins together and to a 10k pull-up resistor to $+V_S$ for better noise immunity. Any of these pins may also be tied high separately through a 10k pull-up resistor.

7.5 Programming

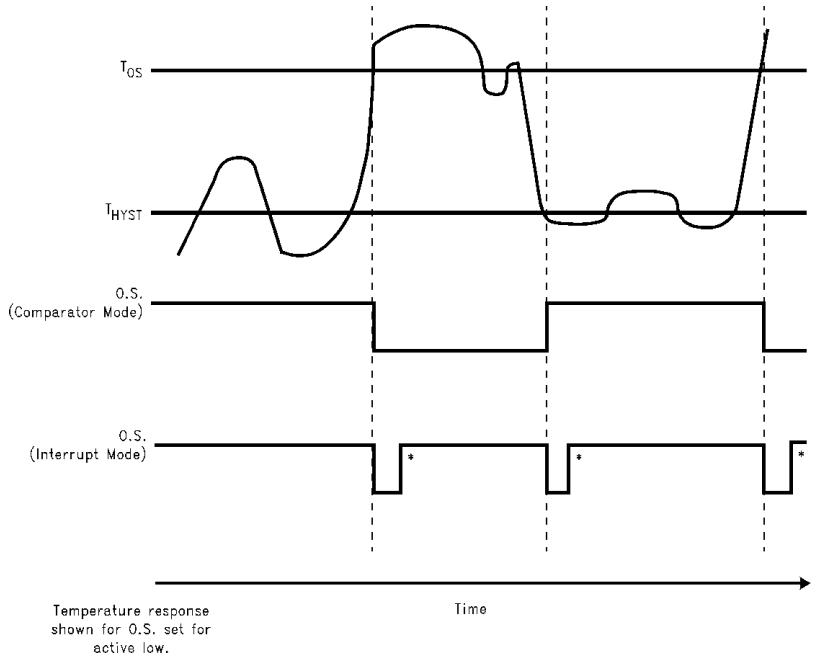
7.5.1 I^2C Bus Interface

The LM75 operates as a slave on the I^2C bus, so the SCL line is an input (no clock is generated by the LM75) and the SDA line is a bi-directional serial data path. According to I^2C bus specifications, the LM75 has a 7-bit slave address. The four most significant bits of the slave address are hard wired inside the LM75 and are “1001”. The three least significant bits of the address are assigned to pins A2–A0, and are set by connecting these pins to ground for a low, (0); or to $+V_S$ for a high, (1).

Therefore, the complete slave address is:

1	0	0	1	A2	A1	A0
MSB						LSB

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These interrupt mode resets of O.S. occur only when LM75 is read or placed in shutdown. Otherwise, O.S. would remain active indefinitely for any event.

Figure 9. O.S. Output Temperature Response Diagram

7.5.2 Temperature Data Format

Temperature data can be read from the Temperature, T_{OS} Set Point, and T_{HYST} Set Point registers; and written to the T_{OS} Set Point, and T_{HYST} Set Point registers. Temperature data is represented by a 9-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.5°C:

Temperature	Digital Output	
	Binary	Hex
125°C	0 1111 1010	0FAh
25°C	0 0011 0010	032h
0.5°C	0 0000 0001	001h
0°C	0 0000 0000	000h
−0.5°C	1 1111 1111	1FFh
−25°C	1 1100 1110	1CEh
−55°C	1 1001 0010	192h

7.5.3 Shutdown Mode

Shutdown mode is enabled by setting the shutdown bit in the Configuration register via the I^2C bus. Shutdown mode reduces power supply current significantly. See specified quiescent current specification in the *Temperature-to-Digital Converter Characteristics* table. In Interrupt mode O.S. is reset if previously set and is undefined in Comparator mode during shutdown. The I^2C interface remains active. Activity on the clock and data lines of the I^2C bus may slightly increase shutdown mode quiescent current. T_{OS}, T_{HYST}, and Configuration registers can be read from and written to in shutdown mode.

For the LM75B, the TIMEOUT feature is turned off in Shutdown Mode.

7.5.4 Fault Queue

A fault queue of up to 6 faults is provided to prevent false tripping of O.S. when the LM75 is used in noisy environments. The number of faults set in the queue must occur consecutively to set the O.S. output.

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7.5.5 Comparator and Interrupt Mode

As indicated in the O.S. Output Temperature Response Diagram, Figure 9, the events that trigger O.S. are identical for either Comparator or Interrupt mode. The most important difference is that in Interrupt mode the O.S. will remain set indefinitely once it has been set. To reset O.S. while in Interrupt mode, perform a read from any register in the LM75.

7.5.6 O.S. Output

The O.S. output is an open-drain output and does not have an internal pull-up. A “high” level will not be observed on this pin until pull-up current is provided from some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible. This will minimize any errors due to internal heating of the LM75. The maximum resistance of the pull up, based on LM75 specification for High Level Output Current, to provide a 2V high level, is 30 kΩ.

7.5.7 O.S. Polarity

The O.S. output can be programmed via the configuration register to be either active low (default mode), or active high. In active low mode the O.S. output goes low when triggered exactly as shown on the O.S. Output Temperature Response Diagram, Figure 9. Active high simply inverts the polarity of the O.S. output.

7.5.8 Internal Register Structure

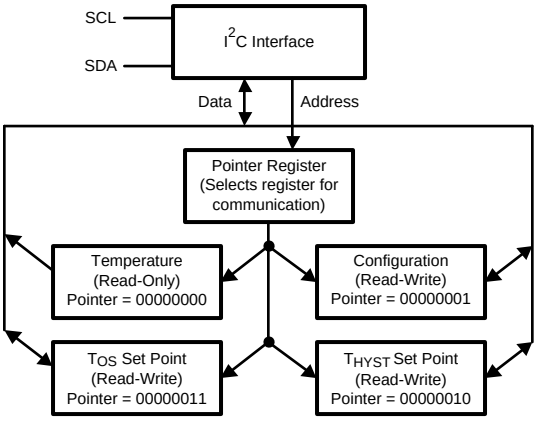


Figure 10. Iternal Register Structure

There are four data registers in the LM75B and LM75C selected by the Pointer register. At power-up the Pointer is set to “000”; the location for the Temperature Register. The Pointer register latches whatever the last location it was set to. In Interrupt Mode, a read from the LM75, or placing the device in shutdown mode, resets the O.S. output. All registers are read and write, except the Temperature register which is a read only.

A write to the LM75 will always include the address byte and the Pointer byte. A write to the Configuration register requires one data byte, and the T_{OS} and T_{HYST} registers require two data bytes.

Reading the LM75 can take place either of two ways: If the location latched in the Pointer is correct (most of the time it is expected that the Pointer will point to the Temperature register because it will be the data most frequently read from the LM75), then the read can simply consist of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For instance, if the first four bits of the temperature data indicates an overtemperature condition, the host processor could immediately take action to remedy the excessive temperatures. At the end of a read, the LM75 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

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An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the LM75 to stop in a state where the SDA line is held low as shown in Figure 11. This can prevent any further bus communication until at least 9 additional clock cycles have occurred. Alternatively, the master can issue clock cycles until SDA goes high, at which time issuing a “Stop” condition will reset the LM75.

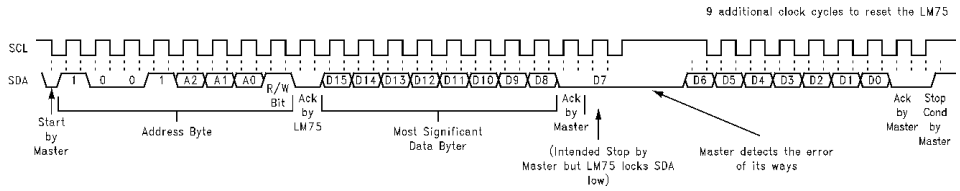


Figure 11. Inadvertent 8-Bit Read from 16-Bit Register where D7 is Zero (“0”)

7.6 Register Maps

7.6.1 Pointer Register (Selects Which Registers Will Be Read From or Written to):

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register Select		

P0-P1: Register Select:

P2	P1	P0	Register
0	0	0	Temperature (Read only) (Power-up default)
0	0	1	Configuration (Read/Write)
0	1	0	T_{HYST} (Read/Write)
0	1	1	T_{OS} (Read/Write)

P3–P7: Must be kept zero.

7.6.2 Temperature Register (Read Only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB	X	X	X	X	X	X	X

D0–D6: Undefined. D7–D15: Temperature Data. One LSB = 0.5°C. Two's complement format.

7.6.3 Configuration Register (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Fault Queue		O.S. Polarity	Cmp/Int	Shutdown

Power up default is with all bits “0” (zero).

D0: Shutdown: When set to 1 the LM75 goes to low power shutdown mode.

D1: Comparator/Interrupt mode: 0 is Comparator mode, 1 is Interrupt mode.

D2: O.S. Polarity: 0 is active low, 1 is active high. O.S. is an open-drain output under all conditions.

D3–D4: Fault Queue: Number of faults necessary to detect before setting O.S. output to avoid false tripping due to noise. Faults are determind at the end of a conversion. See specified temperature conversion time in the *Temperature-to-Digital Converter Characteristics* table.

D4	D3	Number of Faults
0	0	1 (Power-up default)
0	1	2
1	0	4

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D4	D3	Number of Faults
1	1	6

D5–D7: These bits are used for production testing and must be kept zero for normal operation.

7.6.4 T_{HYST} and T_{OS} Register (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB	X	X	X	X	X	X	X

D0–D6: Undefined D7–D15: T_{HYST} Or T_{OS} Trip Temperature Data. Power up default is T_{OS} = 80°C, T_{HYST} = 75°C

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8 Application and Implementation

NOTE

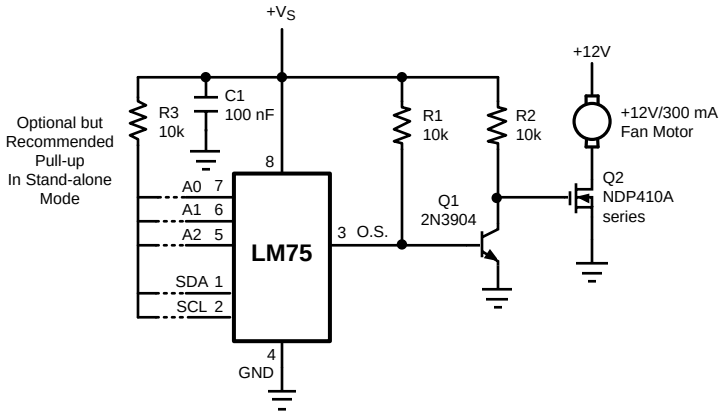
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The wide temperature and supply range and I^2C interface make the LM75 ideal for a number of applications including base stations, electronic test equipment, office electronics, personal computers, and any other system where thermal management is critical to performance.

8.2 Typical Application

8.2.1 Simple Fan Controller, Interface Optional



When using the two-wire interface: program O.S. for active high and connect O.S. directly to Q2's gate.

Figure 12. Simple Fan Controller, Interface Optional

8.2.1.1 Design Requirements

The LM75 requires a positive supply voltage of 2.7 V to 5.5 V to be applied between +Vs and GND. For best results, bypass capacitors of 100 nF and 10 µF are recommended. Pull-up resistors of 10 kΩ are required on SCL and SDA.

8.2.1.2 Detailed Design Procedure

Accessing the conversion result of the LM75 consists of writing an address byte followed by retrieving the corresponding number of data bytes. The first data byte is the most significant byte with the most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For instance, if the first four bits of the temperature data indicates an overtemperature condition, the host processor could immediately take action to remedy the excessive temperatures. At the end of a read, the LM75 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). Temperature data is two's complement format and one LSB is equivalent to 0.5°C.

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Typical Application (continued)

8.2.1.3 Application Curve

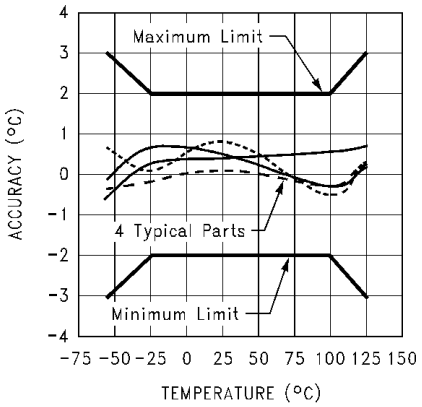


Figure 13. Temperature Accuracy

8.3 System Examples

8.3.1 Simple Thermostat, Interface Optional

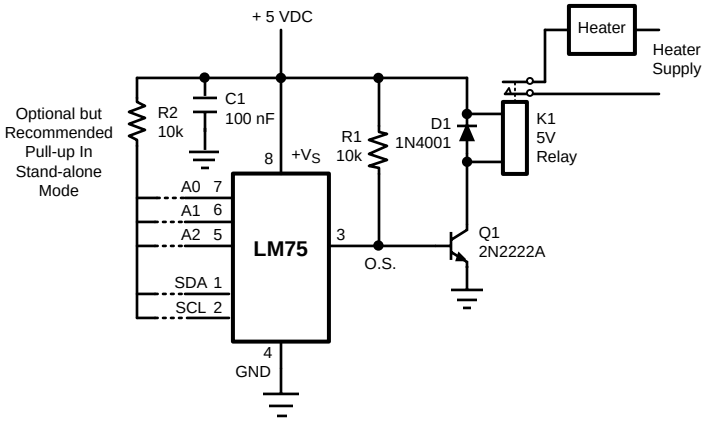


Figure 14. Simple Thermostat, Interface Optional

System Examples (continued)

8.3.2 Temperature Sensor with Loudmouth Alarm (Barking Watchdog)

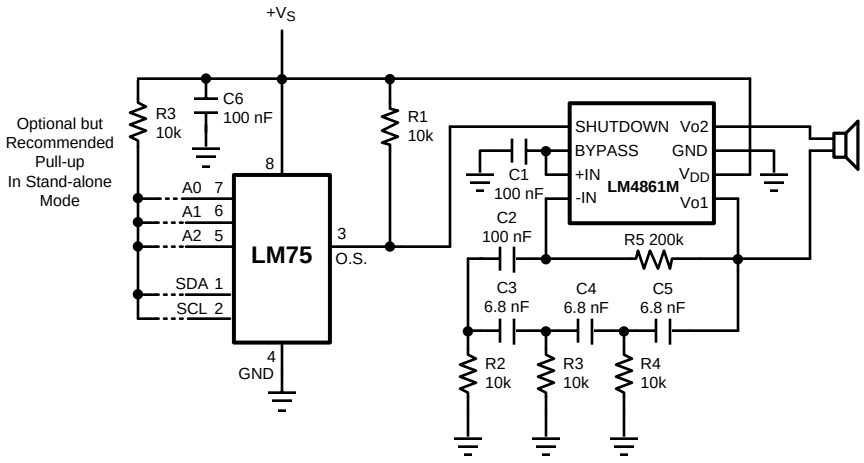


Figure 15. Temperature Sensor with Loudmouth Alarm (Barking Watchdog)

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9 Power Supply Recommendations

The LM75 is specified for operation from 2.7 V to 5.5 V. Place a 100-nF and 10-µF capacitor close to +Vs in order to reduce errors coupling in from noisy or high impedance supplies.

10 Layout

10.1 Layout Guidelines

To achieve the expected results when measuring temperature with an integrated circuit temperature sensor like the LM75, it is important to understand that the sensor measures its own die temperature. For the LM75, the best thermal path between the die and the outside world is through the LM75's pins. In the VSSOP package for the LM75B and LM75C, the GND pin is directly connected to the die, so the GND pin provides the best thermal path. If the other pins are at different temperatures (unlikely, but possible), they will affect the die temperature, but not as strongly as the GND pin. In the SOIC package, none of the pins is directly connected to the die, so they will all contribute similarly to the die temperature. Because the pins represent a good thermal path to the LM75 die, the LM75 will provide an accurate measurement of the temperature of the printed circuit board on which it is mounted. There is a less efficient thermal path between the plastic package and the LM75 die. If the ambient air temperature is significantly different from the printed circuit board temperature, it will have a small effect on the measured temperature.

In probe-type applications, the LM75 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM75 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM75 or its connections.

10.1.1 Digital Noise Issues

The LM75B features an integrated low-pass filter on both the SCL and the SDA digital lines to mitigate the effects of bus noise. Although this filtering makes the LM75B communication robust in noisy environments, good layout practices are always recommended. Minimize noise coupling by keeping digital traces away from switching power supplies. Also, ensure that digital lines containing high-speed data communications cross at right angles to the SDA and SCL lines.

Excessive noise coupling into the SDA and SCL lines on the LM75C-specifically noise with amplitude greater than 400 mV_{pp} (the LM75's typical hysteresis), overshoot greater than 300 mV above $+V_s$, and undershoot more than 300 mV below GND-may prevent successful serial communication with the LM75C. Serial bus no-acknowledge is the most common symptom, causing unnecessary traffic on the bus. The layout procedures mentioned above apply also to the LM75C. Although the serial bus maximum frequency of communication is only 400 kHz, care must be taken to ensure proper termination within a system with long printed circuit board traces or multiple parts on the bus. Resistance can be added in series with the SDA and SCL lines to further help filter noise and ringing. A 5 kΩ resistor should be placed in series with the SCL line, placed as close as possible to the SCL pin on the LM75C. This 5 kΩ resistor, with the 5 pF to 10 pF stray capacitance of the LM75 provides a 6 MHz to 12 MHz low pass filter, which is sufficient filtering in most cases.

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10.2 Layout Example

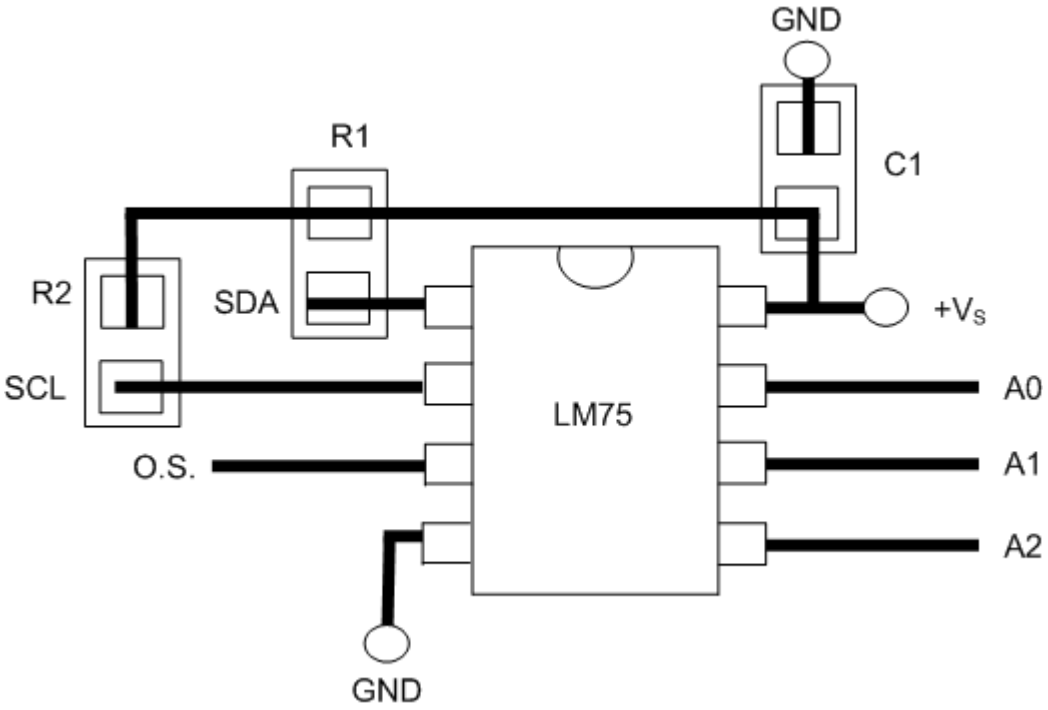


Figure 16. Typical Layout

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM75B	Click here	Click here	Click here	Click here	Click here
LM75C	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM75BIM-3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-55 to 125	LM75 BIM-3	
LM75BIM-3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	LM75 BIM-3	Samples
LM75BIM-5	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-55 to 125	LM75 BIM-5	
LM75BIM-5/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	LM75 BIM-5	Samples
LM75BIMM-3	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-55 to 125	T01B	
LM75BIMM-3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	T01B	Samples
LM75BIMM-5	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-55 to 125	T00B	
LM75BIMM-5/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	T00B	Samples
LM75BIMMX-3	NRND	VSSOP	DGK	8		TBD	Call TI	Call TI	-55 to 125	T01B	
LM75BIMMX-3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	T01B	Samples
LM75BIMMX-5/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	T00B	Samples
LM75BIMX-3	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125	LM75 BIM-3	
LM75BIMX-3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	LM75 BIM-3	Samples
LM75BIMX-5	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125	LM75 BIM-5	
LM75BIMX-5/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	LM75 BIM-5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

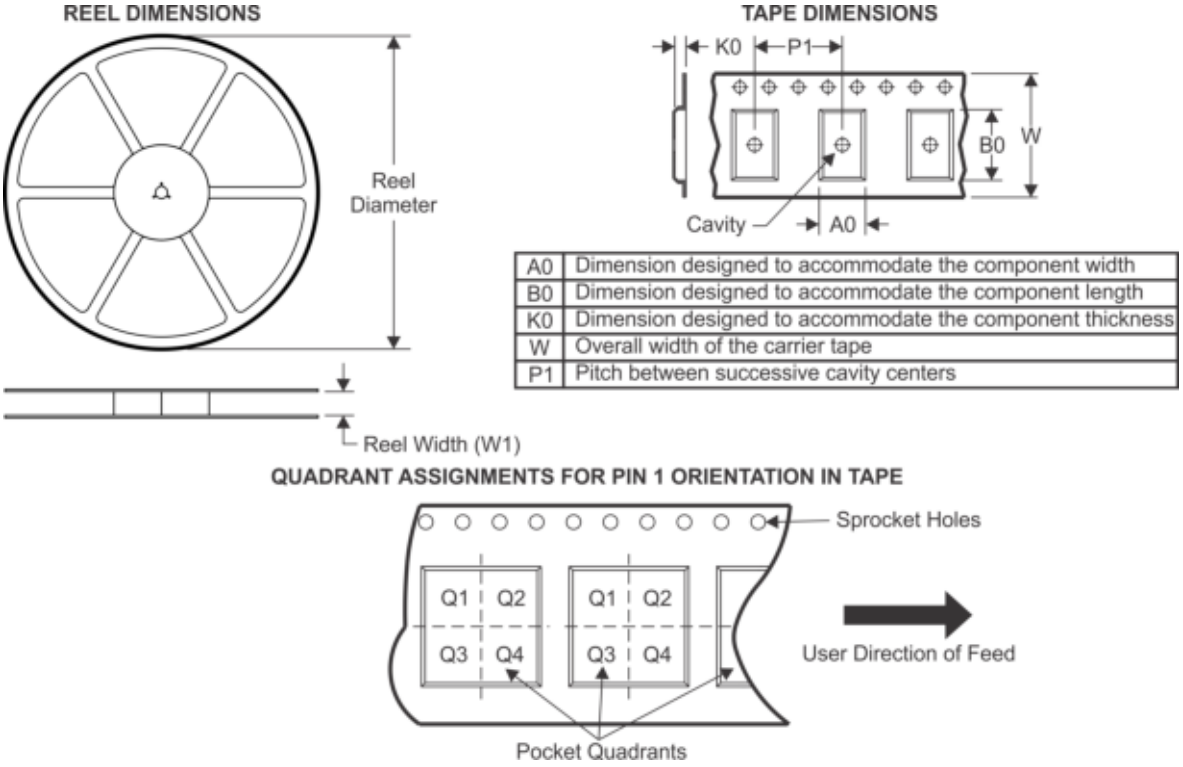
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

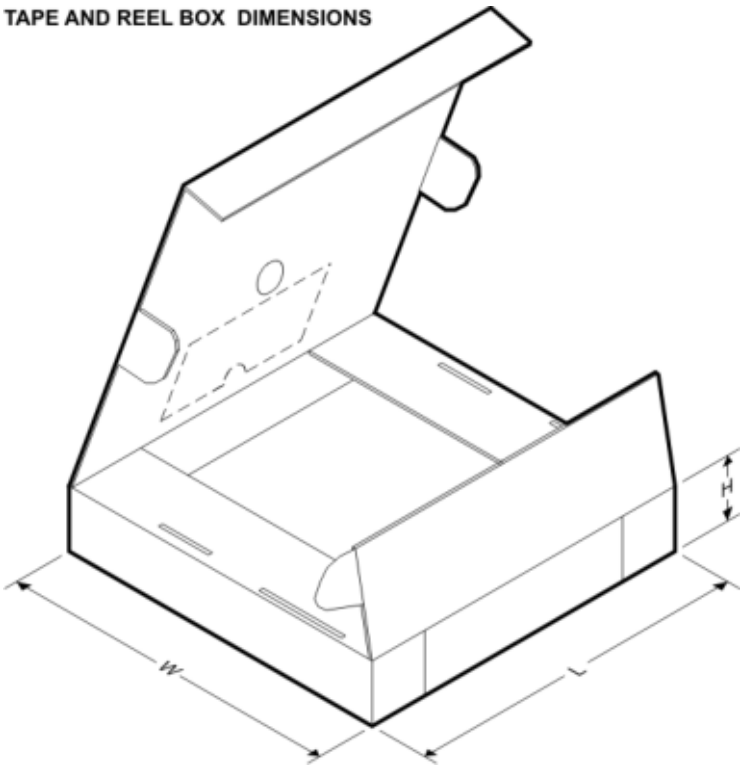


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM75BIMM-3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75BIMM-3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75BIMM-5	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75BIMM-5/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75BIMMX-3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75BIMMX-5/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75BIMX-3	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM75BIMX-3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM75BIMX-5	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM75BIMX-5/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

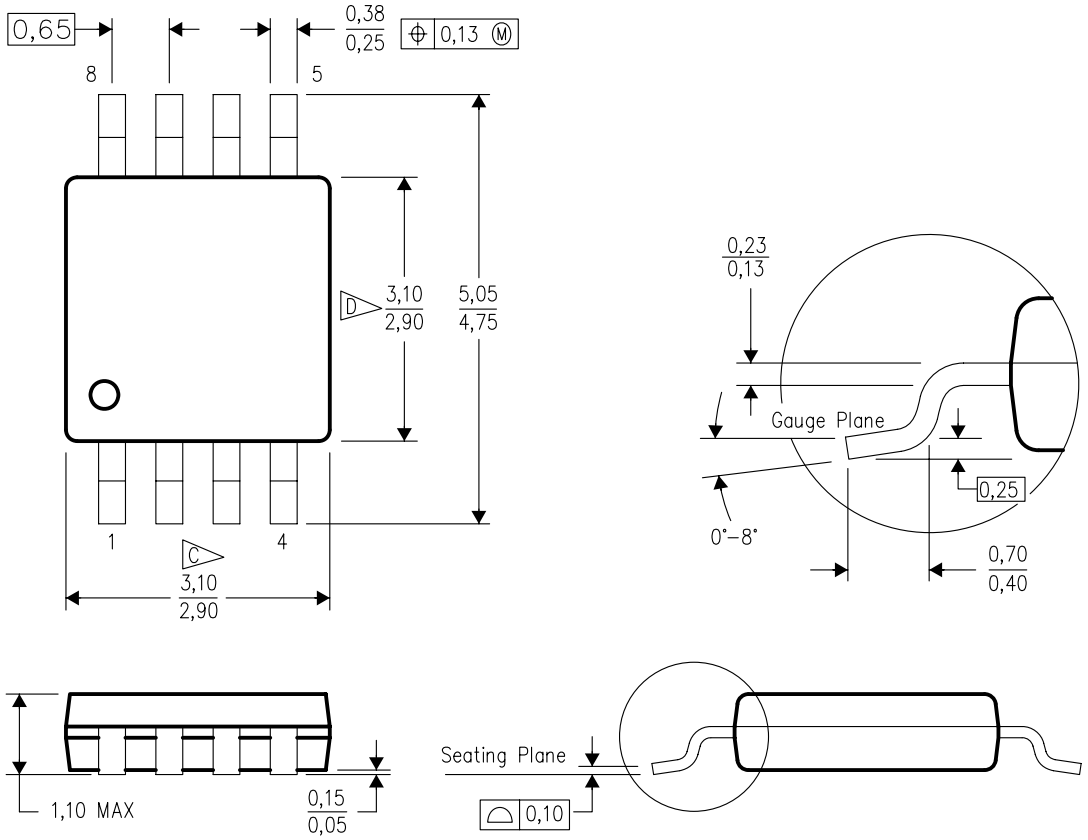
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM75BIMM-3	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM75BIMM-3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM75BIMM-5	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM75BIMM-5/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM75BIMMX-3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM75BIMMX-5/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM75BIMX-3	SOIC	D	8	2500	367.0	367.0	35.0
LM75BIMX-3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM75BIMX-5	SOIC	D	8	2500	367.0	367.0	35.0
LM75BIMX-5/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

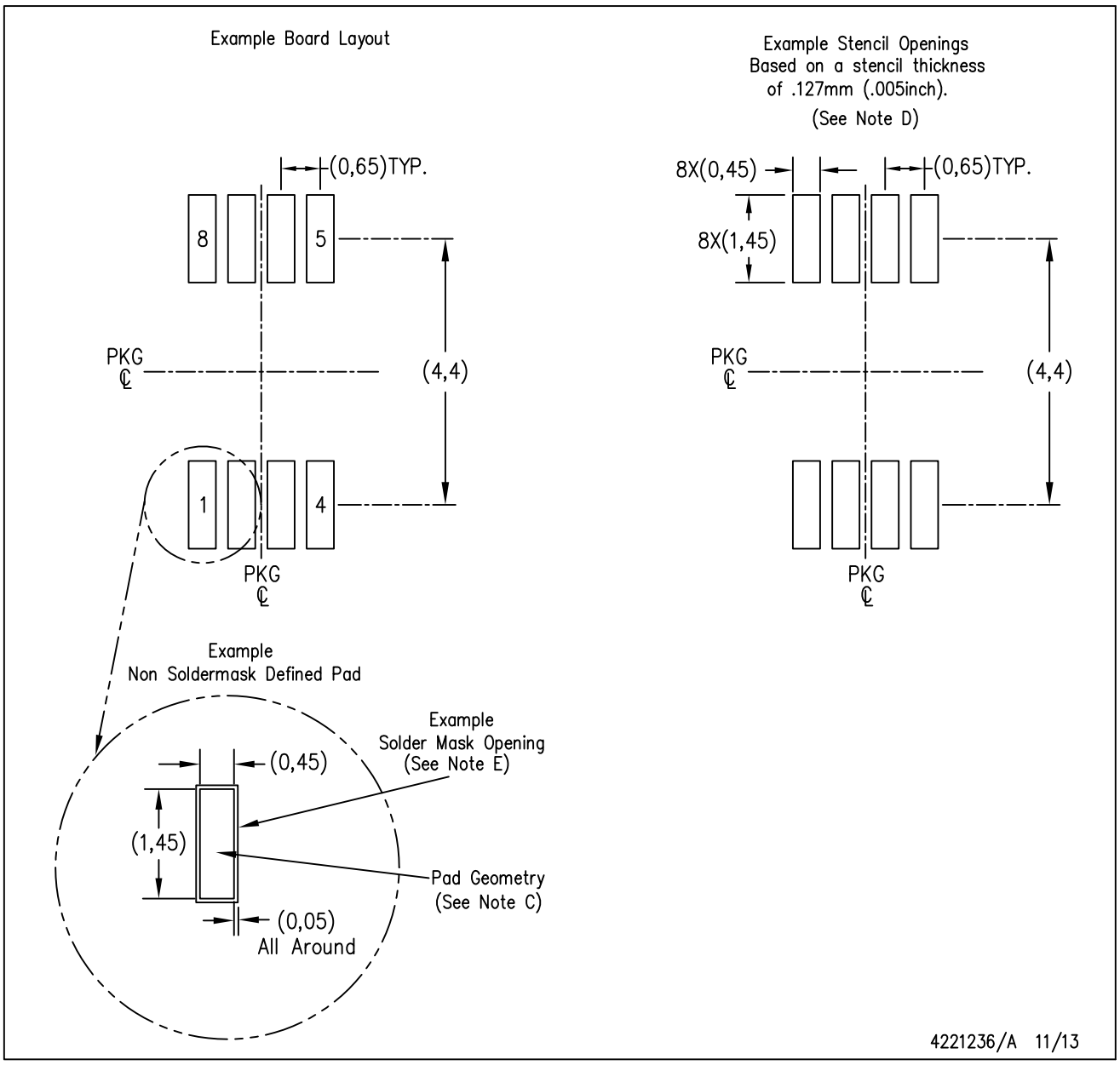
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

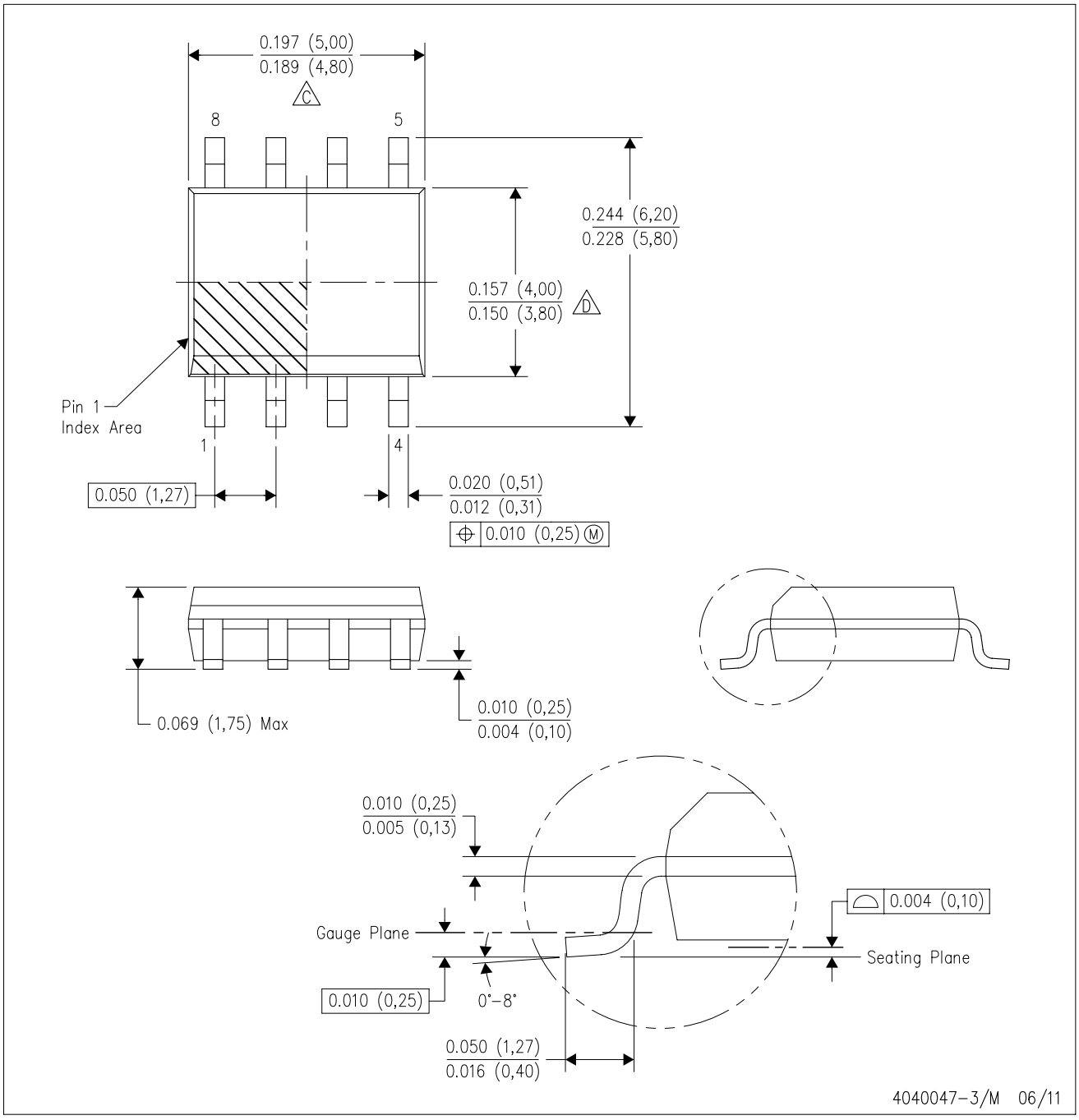
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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