# PRECISION CMOS SINGLE MICROPOWER OPERATIONAL AMPLIFIER

**Check for Samples: LMC6061**

## FEATURES

**(Typical Unless Otherwise Noted)**

- **Low Offset Voltage: 100 µV**
- **Ultra Low Supply Current: 20 µA**
- **Operates From 4.5V to 15V Single Supply**
- **Ultra Low Input Bias Current: 10 fA**
- **Output Swing Within 10 mV of Supply Rail, 100k Load**
- **Input Common-mode Range Includes $V^-$**
- **High Voltage Gain: 140 dB**
- **Improved Latchup Immunity**

## APPLICATIONS

- **Instrumentation Amplifier**
- **Photodiode and Infrared Detector Preamplifier**
- **Transducer Amplifiers**
- **Hand-held Analytic Instruments**
- **Medical Instrumentation**
- **D/A Converter**
- **Charge Amplifier for Piezoelectric Transducers**

## DESCRIPTION

The LMC6061 is a precision single low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6061 ideally suited for battery powered applications.

Other applications using the LMC6061 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with TI's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6081 precision single operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6062 or LMC6064 respectively.

**PATENT PENDING**

## Connection Diagrams

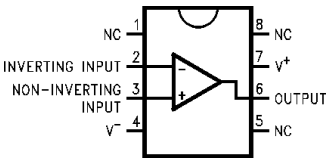



**Figure 1. 8-Pin PDIP/SOIC Top View**

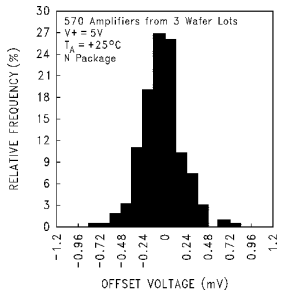



**Figure 2. Distribution of LMC6061 Input Offset Voltage ($T_A$ = +25°C)**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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## Absolute Maximum Ratings[1][2][3]

| | | |
|---|---|---|
| Differential Input Voltage | | ±Supply Voltage |
| Voltage at Input/Output Pin | | ($V^+$) +0.3V, |
| | | ($V^-$) −0.3V |
| Supply Voltage ($V^+ - V^-$) | | 16V |
| Output Short Circuit to $V^+$ | | See[4] |
| Output Short Circuit to $V^-$ | | See[5] |
| Lead Temperature (Soldering, 10 sec.) | Storage Temp. Range | −65°C to +150°C |
| | Junction Temperature | 150°C |
| ESD Tolerance[6] | | 2 kV |
| Current at Input Pin | | ±10 mA |
| Current at Output Pin | | ±30 mA |
| Current at Power Supply Pin | | 40 mA |
| Power Dissipation | | See[7] |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) For specified Military Temperature Range parameters see RETSMC6061X.
(4) Do not connect output to $V^+$, when $V^+$ is greater than 13V or reliability witll be adversely affected.
(5) Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(6) Human body model, 1.5 kΩ in series with 100 pF.
(7) The maximum power dissipation is a function of $T_{J(Max)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

## Operating Ratings[1]

| | | |
|---|---|---|
| Temperature Range | LMC6061AM | $-55°C \le T_J \le +125°C$ |
| | LMC6061AI, LMC6082I | $-40°C \le T_J \le +85°C$ |
| Supply Voltage | | $4.5V \le V^+ \le 15.5V$ |
| Thermal Resistance ($\theta_{JA}$)[2] | P0008E Package, 8-Pin PDIP | 115°C/W |
| | D0008A Package, 8-Pin SOIC | 193°C/W |
| Power Dissipation | | See[3] |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) All numbers apply for packages soldered directly into a PC board.
(3) For operating at elevated temperatures the device must be derated based on the thermal resistance $\theta_{JA}$ with $P_D = (T_J - T_A)/\theta_{JA}$.


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## DC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J$ = 25°C. **Boldface** limits apply at the temperature extremes. $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = 2.5V and $R_L$ > 1M unless otherwise specified.

| Symbol | Parameter | Conditions | | Typ[1] | LMC6061AM Limit[2] | LMC6061AI Limit[2] | LMC6061I Limit[2] | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | 100 | 350<br>**1200** | 350<br>**900** | 800<br>**1300** | µV<br>Max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | | 1.0 | | | | µV/°C |
| $I_B$ | Input Bias Current | | | 0.010 | <br>**100** | <br>**4** | <br>**4** | pA<br>Max |
| $I_{OS}$ | Input Offset Current | | | 0.005 | <br>**100** | <br>**2** | <br>**2** | pA<br>Max |
| $R_{IN}$ | Input Resistance | | | >10 | | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 12.0V<br>$V^+$ = 15V | | 85 | 75<br>**70** | 75<br>**72** | 66<br>**63** | dB<br>Min |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ $V^+$ ≤ 15V<br>$V_O$ = 2.5V | | 85 | 75<br>**70** | 75<br>**72** | 66<br>**63** | dB<br>Min |
| −PSRR | Negative Power Supply Rejection Ratio | 0V ≤ $V^-$ ≤ −10V | | 100 | 84<br>**70** | 84<br>**81** | 74<br>**71** | dB<br>Min |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 5V and 15V<br>for CMRR ≥ 60 dB | | −0.4 | −0.1<br>**0** | −0.1<br>**0** | −0.1<br>**0** | V<br>Max |
| | | | | $V^+$ − 1.9 | $V^+$ − 2.3<br>**$V^+$ − 2.6** | $V^+$ − 2.3<br>**$V^+$ − 2.5** | $V^+$ − 2.3<br>**$V^+$ − 2.5** | V<br>Min |
| $A_V$ | Large Signal Voltage Gain | $R_L$ = 100 kΩ[3] | Sourcing | 4000 | 400<br>**200** | 400<br>**300** | 300<br>**200** | V/mV<br>Min |
| | | | Sinking | 3000 | 180<br>**70** | 180<br>**100** | 90<br>**60** | V/mV<br>Min |
| | | $R_L$ = 25 kΩ[3] | Sourcing | 3000 | 400<br>**150** | 400<br>**150** | 200<br>**80** | V/mV<br>Min |
| | | | Sinking | 2000 | 100<br>**35** | 100<br>**50** | 70<br>**35** | V/mV<br>Min |

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance $\theta_{JA}$ with $P_D = (T_J – T_A)/\theta_{JA}$
(2) All limits are specified by testing or statistical analysis.
(3) $V^+$ = 15V, $V_{CM}$ = 7.5V and $R_L$ connected to 7.5V. For Sourcing tests, 7.5V ≤ $V_O$ ≤ 11.5V. For Sinking tests, 2.5V ≤ $V_O$ ≤ 7.5V.

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## DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C. **Boldface** limits apply at the temperature extremes. $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = 2.5V and $R_L$ > 1M unless otherwise specified.

| Symbol | Parameter | Conditions | Typ(1) | LMC6061AM Limit(2) | LMC6061AI Limit(2) | LMC6061I Limit(2) | Units |
|---|---|---|---|---|---|---|---|
| $V_O$ | Output Swing | $V^+$ = 5V<br>$R_L$ = 100 kΩ to 2.5V | 4.995 | 4.990<br>**4.970** | 4.990<br>**4.980** | 4.950<br>**4.925** | V<br>Min |
| | | | 0.005 | 0.010<br>**0.030** | 0.010<br>**0.020** | 0.050<br>**0.075** | V<br>Max |
| | | $V^+$ = 5V<br>$R_L$ = 25 kΩ to 2.5V | 4.990 | 4.975<br>**4.955** | 4.975<br>**4.965** | 4.950<br>**4.850** | V<br>Min |
| | | | 0.010 | 0.020<br>**0.045** | 0.020<br>**0.035** | 0.050<br>**0.150** | V<br>Max |
| | | $V^+$ = 15V<br>$R_L$ = 100 kΩ to 7.5V | 14.990 | 14.975<br>**14.955** | 14.975<br>**14.965** | 14.950<br>**14.925** | V<br>Min |
| | | | 0.010 | 0.025<br>**0.050** | 0.025<br>**0.035** | 0.050<br>**0.075** | V<br>Max |
| | | $V^+$ = 15V<br>$R_L$ = 25 kΩ to 7.5V | 14.965 | 14.900<br>**14.800** | 14.900<br>**14.850** | 14.850<br>**14.800** | V<br>Min |
| | | | 0.025 | 0.050<br>**0.200** | 0.050<br>**0.150** | 0.100<br>**0.200** | V<br>Max |
| $I_O$ | Output Current<br>$V^+$ = 5V | Sourcing, $V_O$ = 0V | 22 | 16<br>**8** | 16<br>**10** | 13<br>**8** | mA<br>Min |
| | | Sinking, $V_O$ = 5V | 21 | 16<br>**7** | 16<br>**8** | 16<br>**8** | mA<br>Min |
| $I_O$ | Output Current<br>$V^+$ = 15V | Sourcing, $V_O$ = 0V | 25 | 15<br>**9** | 15<br>**10** | 15<br>**10** | mA<br>Min |
| | | Sinking, $V_O$ = 13V(4) | 26 | 20<br>**7** | 20<br>**8** | 20<br>**8** | mA<br>Min |
| $I_S$ | Supply Current | $V^+$ = +5V, $V_O$ = 1.5V | 20 | 24<br>**35** | 24<br>**32** | 32<br>**40** | µA<br>Max |
| | | $V^+$ = +15V, $V_O$ = 7.5V | 24 | 30<br>**40** | 30<br>**38** | 40<br>**48** | µA<br>Max |

(4) Do not connect output to $V^+$, when $V^+$ is greater than 13V or reliability witll be adversely affected.

## AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, **Boldface** limits apply at the temperature extremes. $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = 2.5V and $R_L$ > 1M unless otherwise specified.

| Symbol | Parameter | Conditions | Typ(1) | LMC6061AM Limit(2) | LMC6061AI Limit(2) | LMC6061I Limit(2) | Units |
|---|---|---|---|---|---|---|---|
| SR | Slew Rate | See(3) | 35 | 20<br>**8** | 20<br>**10** | 15<br>**7** | V/ms<br>Min |
| GBW | Gain-Bandwidth Product | | 100 | | | | kHz |
| $\theta_m$ | Phase Margin | | 50 | | | | Deg |
| $e_n$ | Input-Referred Voltage Noise | F = 1 kHz | 83 | | | | nV/√Hz |
| $i_n$ | Input-Referred Current Noise | F = 1 kHz | 0.0002 | | | | pA/√Hz |

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) $V^+$ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.


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## AC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, **Boldface** limits apply at the temperature extremes. $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = 2.5V and $R_L$ > 1M unless otherwise specified.

| Symbol | Parameter | Conditions | Typ[1] | LMC6061AM Limit[2] | LMC6061AI Limit[2] | LMC6061I Limit[2] | Units |
|---|---|---|---|---|---|---|---|
| T.H.D. | Total Harmonic Distortion | F = 1 kHz, $A_V$ = −5<br>$R_L$ = 100 kΩ, $V_O$ = 2 $V_{PP}$<br>±5V Supply | 0.01 | | | | % |

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## Typical Performance Characteristics

$V_S$ = ±7.5V, $T_A$ = 25°C, Unless otherwise specified

**Distribution of LMC6061 Input Offset Voltage ($T_A$ = +25°C)**

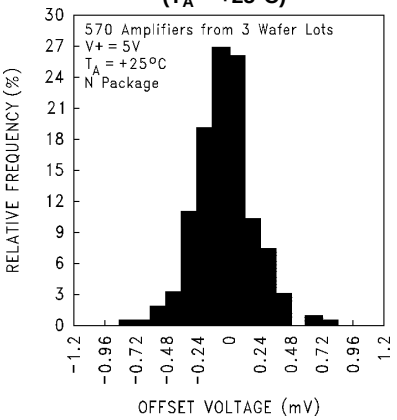



**Figure 3.**

**Distribution of LMC6061 Input Offset Voltage ($T_A$ = −55°C)**

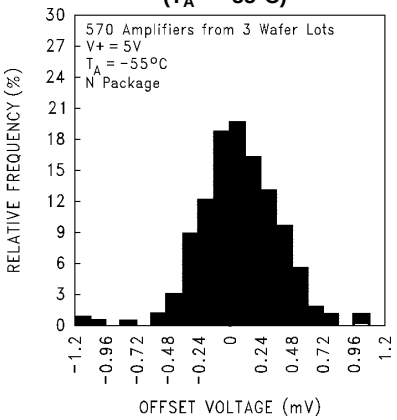



**Figure 4.**

**Distribution of LMC6061 Input Offset Voltage ($T_A$ = +125°C)**

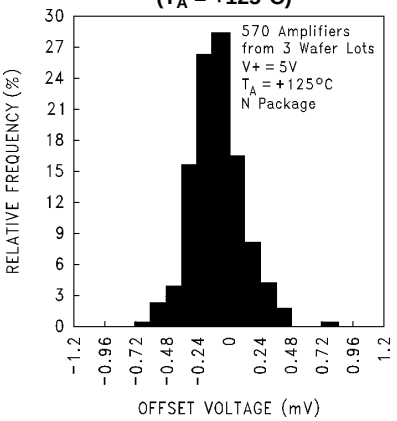



**Figure 5.**

**Input Bias Current vs Temperature**

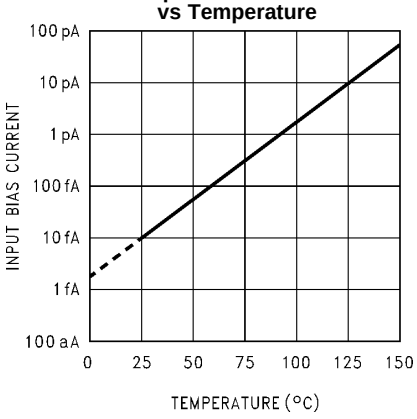



**Figure 6.**

**Supply Current vs Supply Voltage**

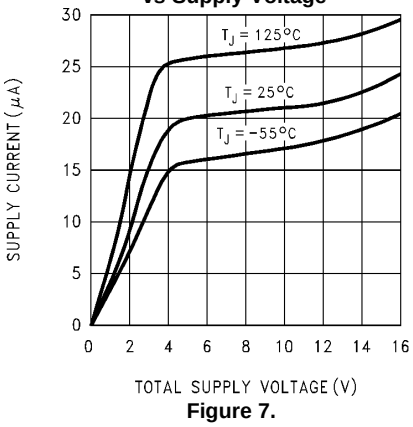



**Figure 7.**

**Input Voltage vs Output Voltage**

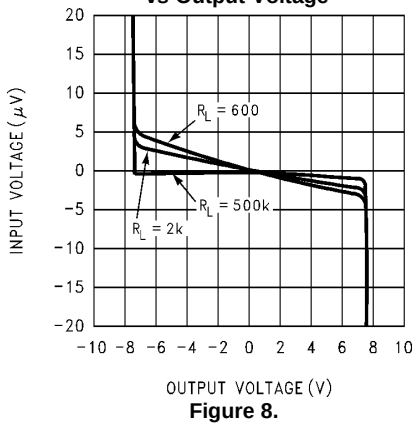



**Figure 8.**


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## Typical Performance Characteristics (continued)

$V_S$ = ±7.5V, $T_A$ = 25°C, Unless otherwise specified

**Common Mode Rejection Ratio vs Frequency**

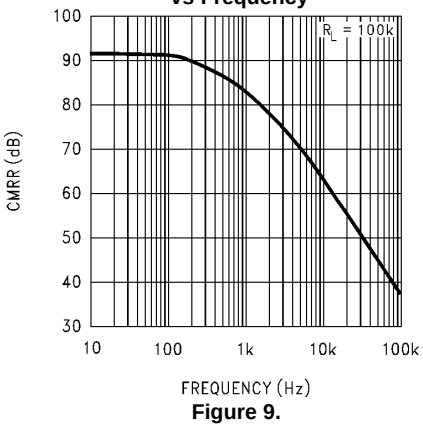



**Figure 9.**

**Power Supply Rejection Ratio vs Frequency**

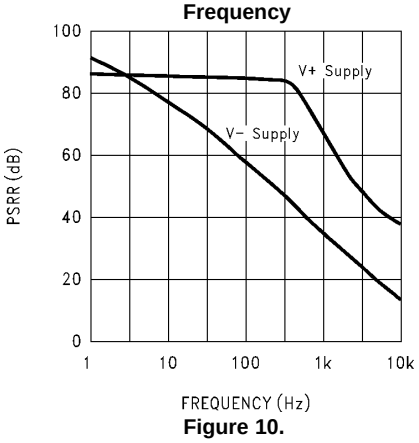



**Figure 10.**

**Input Voltage Noise vs Frequency**

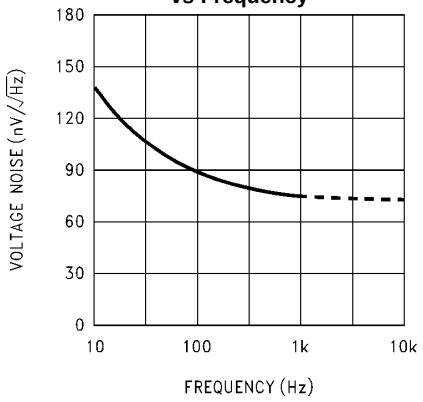



**Figure 11.**

**Output Characteristics Sourcing Current**

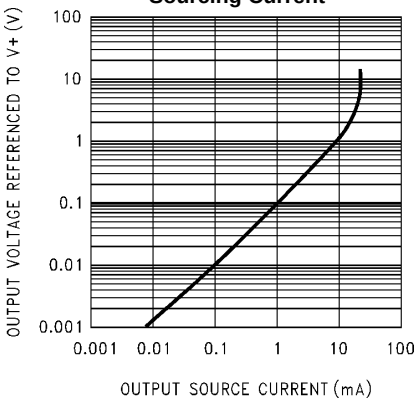



**Figure 12.**

**Output Characteristics Sinking Current**

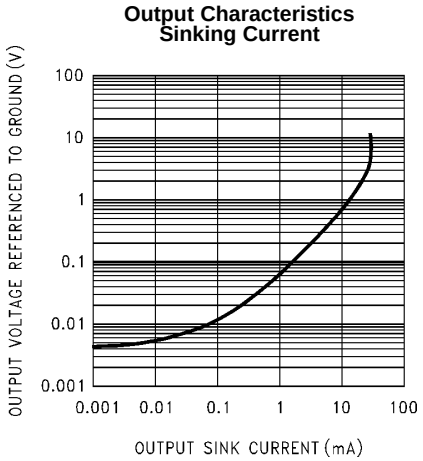



**Figure 13.**

**Gain and Phase Response vs Temperature (−55°C to +125°C)**

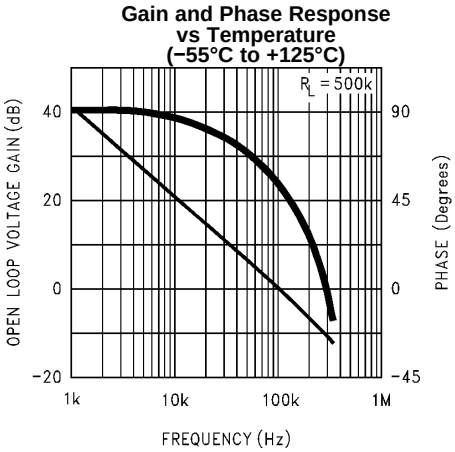



**Figure 14.**

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## Typical Performance Characteristics (continued)

$V_S$ = ±7.5V, $T_A$ = 25°C, Unless otherwise specified

**Gain and Phase Response vs Capacitive Load with $R_L$ = 20 kΩ**

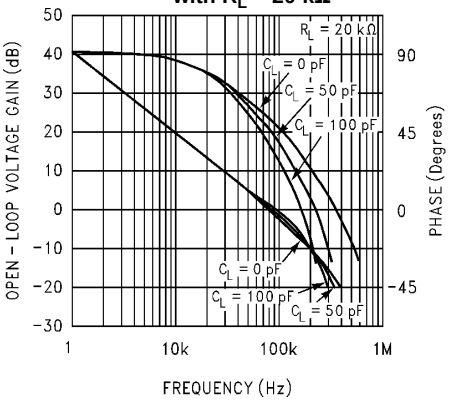



**Figure 15.**

**Gain and Phase Response vs Capacitive Load with $R_L$ = 500 kΩ**

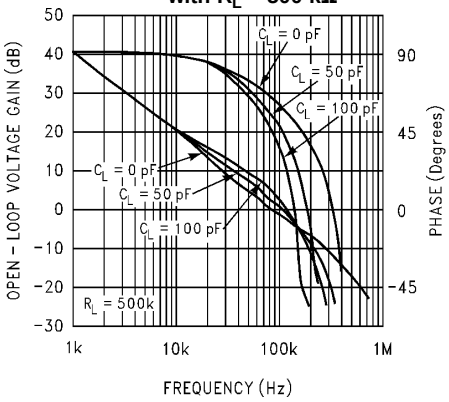



**Figure 16.**

**Open Loop Frequency Response**

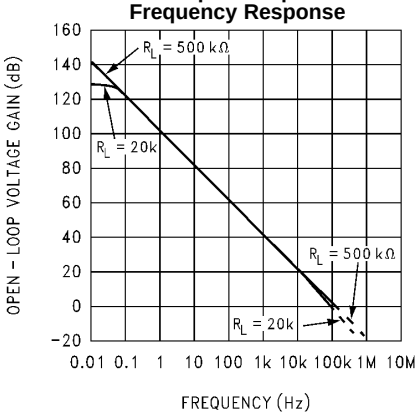



**Figure 17.**

**Inverting Small Signal Pulse Response**

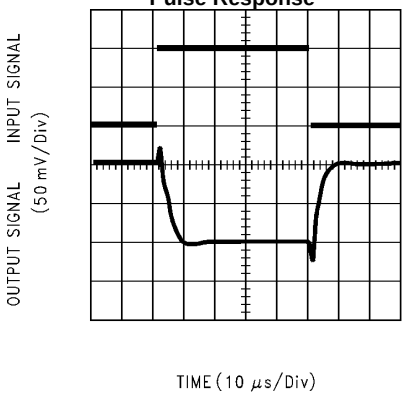



**Figure 18.**

**Inverting Large Signal Pulse Response**

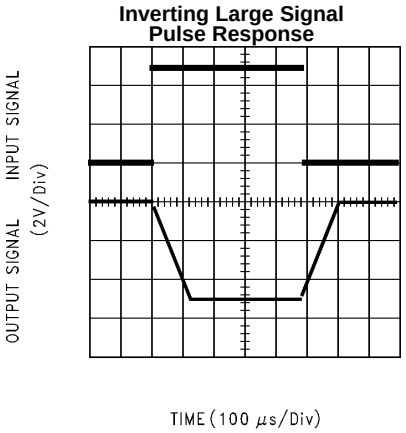



**Figure 19.**

**Non-Inverting Small Signal Pulse Response**

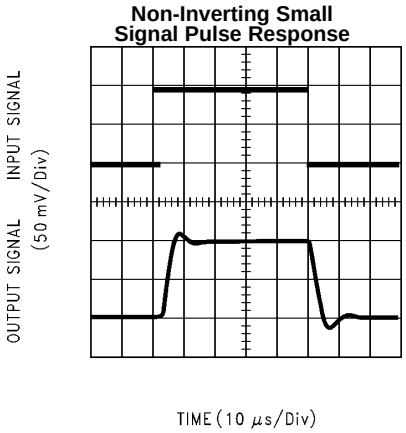



**Figure 20.**


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## Typical Performance Characteristics (continued)

$V_S$ = ±7.5V, $T_A$ = 25°C, Unless otherwise specified

**Non-Inverting Large Signal Pulse Response**

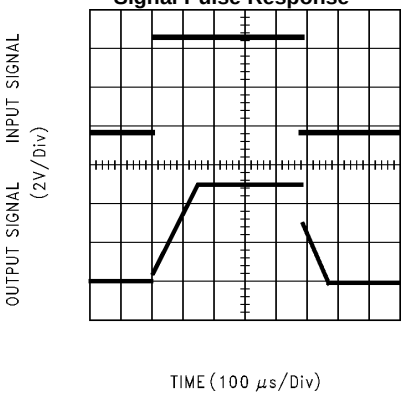



**Figure 21.**

**Stability vs Capacitive Load, $R_L$ = 20 kΩ**

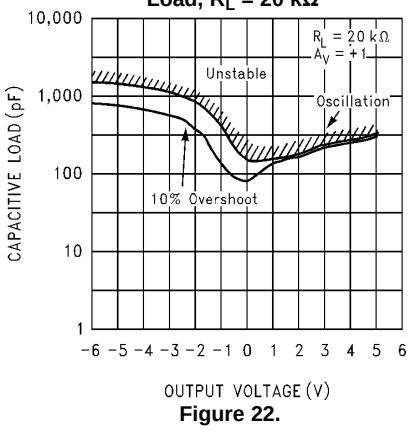



**Figure 22.**

**Stability vs Capacitive Load $R_L$ = 1 MΩ**

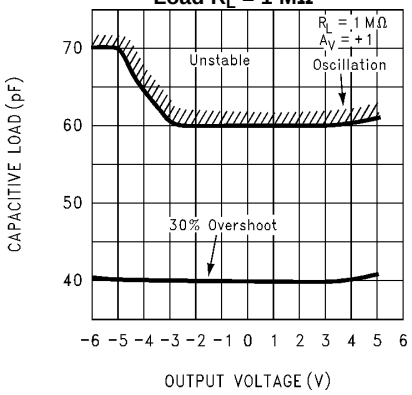



**Figure 23.**

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## APPLICATIONS HINTS

### Amplifier Topology

The LMC6061 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6061 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

### Compensating for Input Capacitance

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6061.

Although the LMC6061 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6061 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See Printed-Circuit-Board Layout For High-Impedance Work).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, $C_f$, around the feedback resistor (as in Figure 24) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

Since it is often difficult to know the exact value of $C_{IN}$, $C_f$ can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

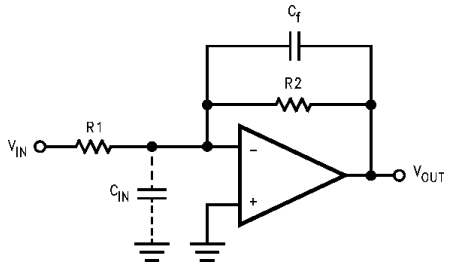



**Figure 24. Canceling the Effect of Input Capacitance**

### Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 25.


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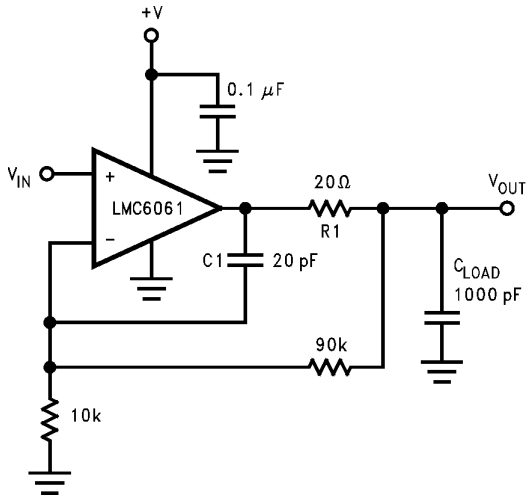



**Figure 25. LMC6061 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads**

In the circuit of Figure 25, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to $V^+$ Figure 26. Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

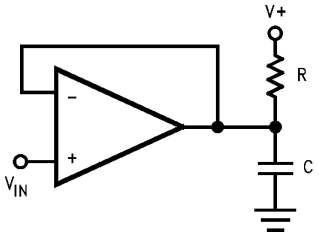



**Figure 26. Compensating for Large Capacitive Loads with a Pull Up Resistor**

## Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6061, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6061's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in Figure 27. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6061's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 28 for typical connections of guard rings for standard op-amp configurations..

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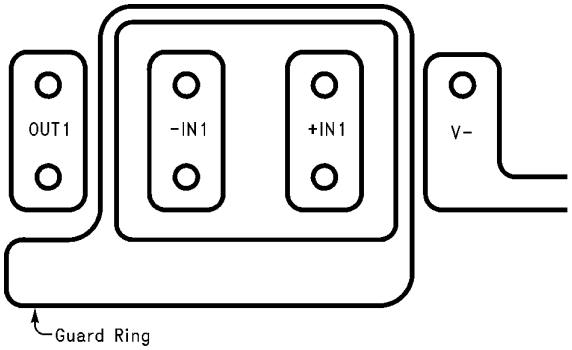



**Figure 27. Example of Guard Ring in P.C. Board Layout**

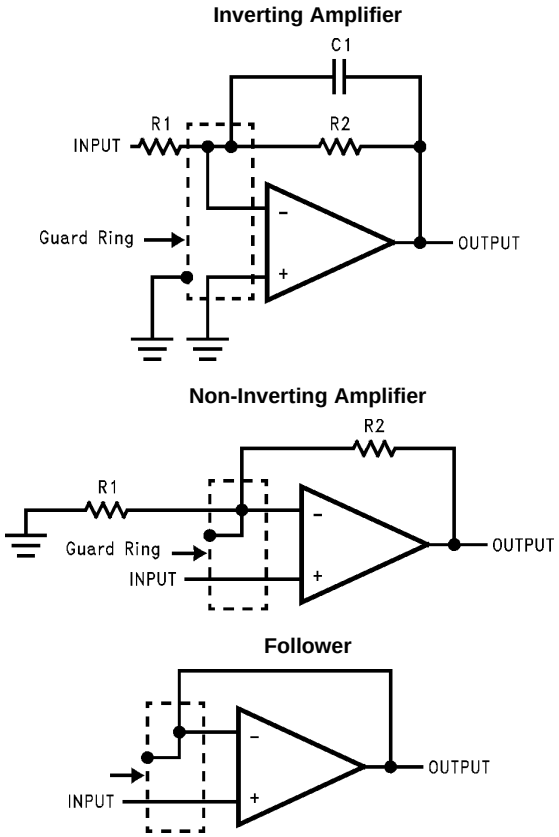
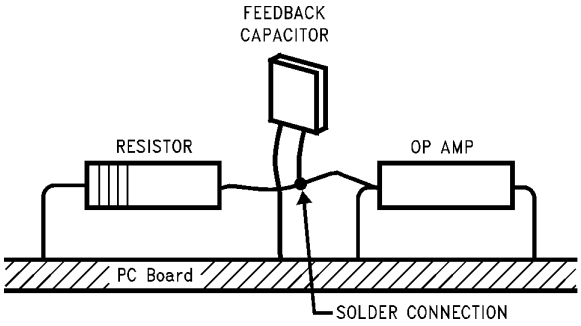



**Figure 28. Typical Connections of Guard Rings**

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 29.


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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

**Figure 29. Air Wiring**

## Latchup

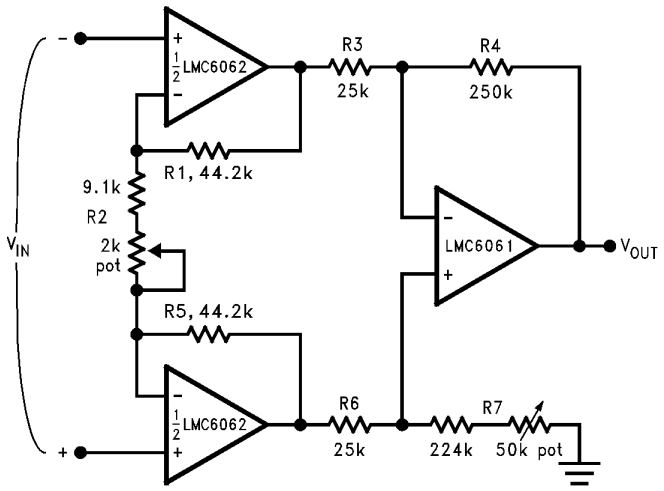
CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

## Typical Single-Supply Applications

($V^+$ = 5.0 $V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6061 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 30 shows an instrumentation amplifier that features high differential and common mode input resistance (>$10^{14}$Ω), 0.01% gain accuracy at $A_V$ = 100, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 µV/°C. $R_2$ provides a simple means of adjusting gain over a wide range without degrading CMRR. $R_7$ is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.




If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2$ = 9.822k).

**Figure 30. Instrumentation Amplifier**

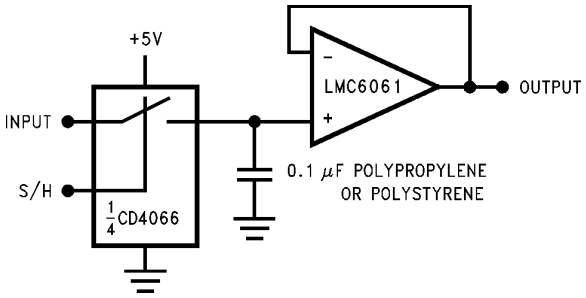



**Figure 31. Low-Leakage Sample and Hold**

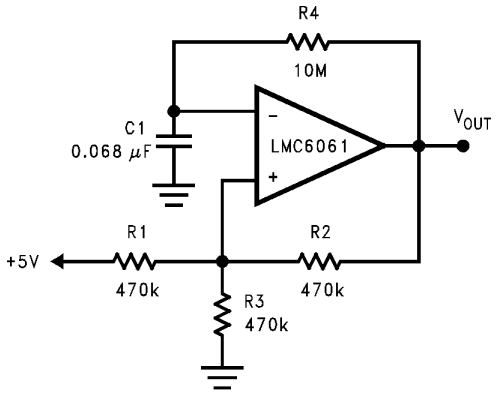



**Figure 32. 1 Hz Square Wave Oscillator**


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## REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 14 |

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC6061AIM | ACTIVE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | LMC60 61AIM | Samples |
| LMC6061AIM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC60 61AIM | Samples |
| LMC6061AIMX | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LMC60 61AIM | Samples |
| LMC6061AIMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC60 61AIM | Samples |
| LMC6061IM | ACTIVE | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | LMC60 61IM | Samples |
| LMC6061IM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC60 61IM | Samples |
| LMC6061IMX | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | LMC60 61IM | Samples |
| LMC6061IMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC60 61IM | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

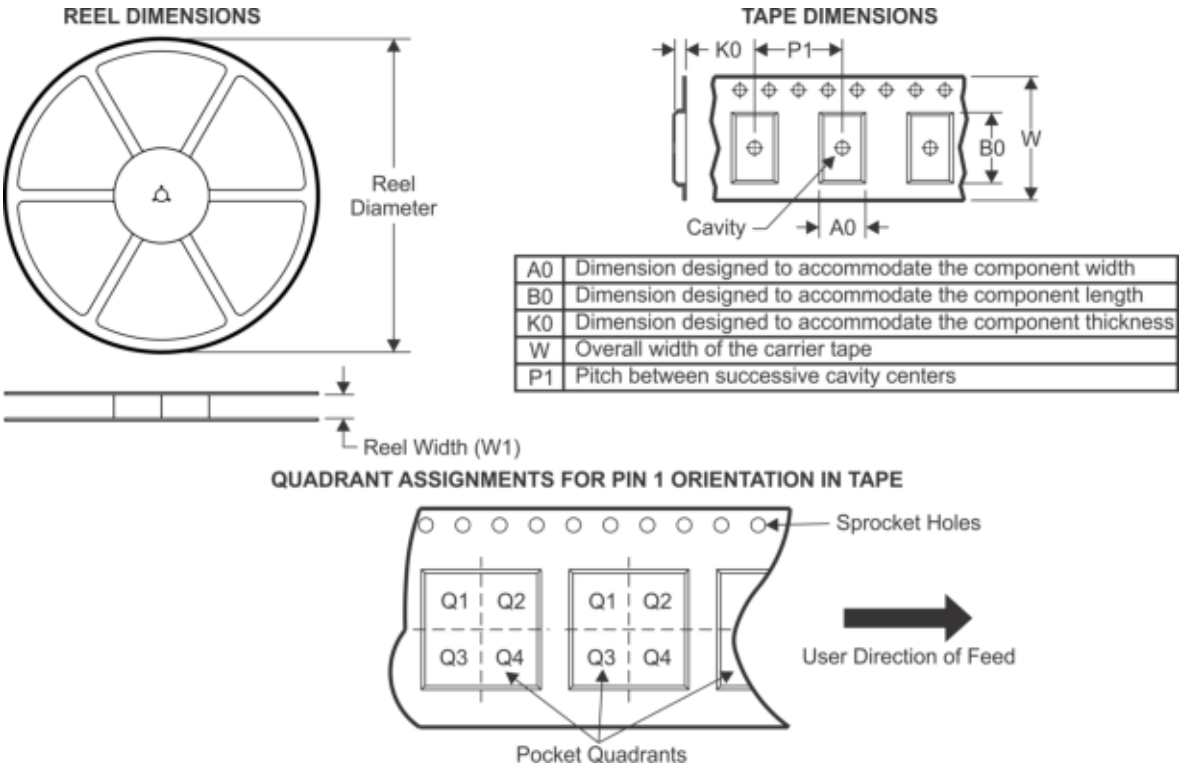
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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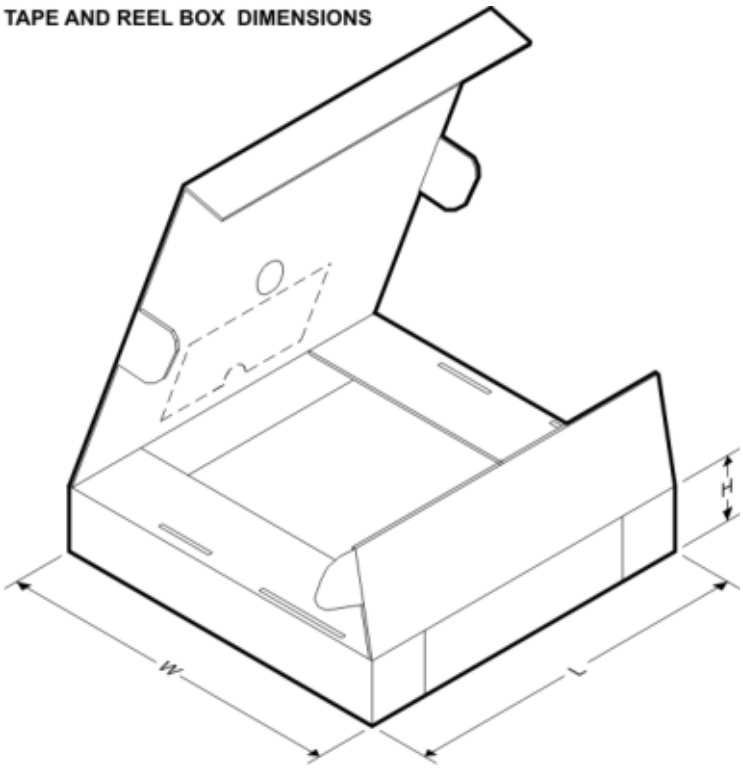



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC6061AIMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6061AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6061IMX | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6061IMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

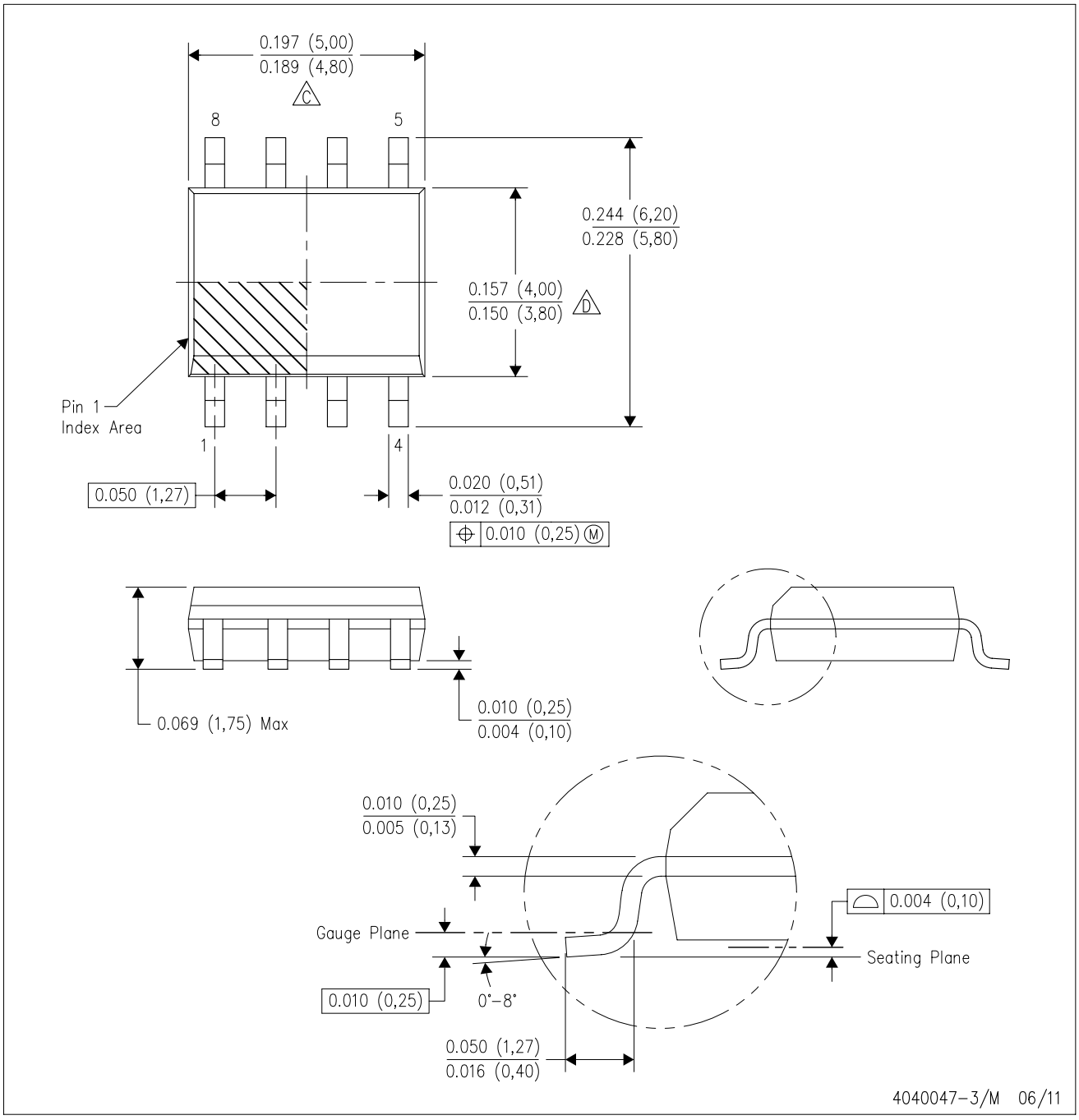
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMC6061AIMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6061AIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6061IMX | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6061IMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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