National Semiconductor

January 2007

LMP8271
High Common Mode, Gain of 20, Bidirectional Precision Voltage Difference Amplifier

General Description

The LMP8271 is a fixed gain differential amplifier with a –2V to 16V input common mode voltage range and a supply voltage range of 4.75V to 5.5V. The LMP8271 is part of the LMP® precision amplifier family which will detect, amplify and filter small differential signals in the presence of high common mode voltages. The gain is fixed at 20 and is adequate to drive an ADC to full scale in most cases. This fixed gain is achieved in two separate stages, a preamplifier with gain of +10 and a second stage amplifier with a gain of +2. The internal signal path is brought out on two pins that provide a connection for a filter network.

The LMP8271 will function over an extended common mode input voltage range making the device suitable for applications with load dump events such as automotive systems.

The mid-rail offset adjustment pin enables the user to utilize this device for bidirectional current sensing. This is achieved by adjusting an externally set voltage reference. Accurate bidirectional load current measurements are achieved when monitoring the output with respect to this reference voltage.

Features

Typical Values, T_A = 25°C

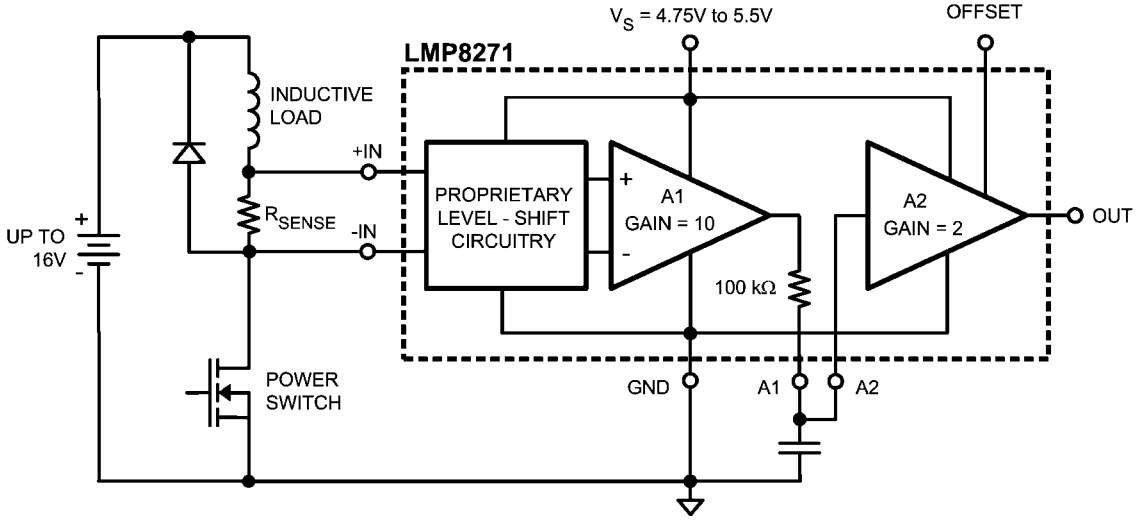
- Bidirectional current sense capability
- Input offset voltage ±1 mV max
- TCV_{OS} ±15 µV/°C max
- CMRR 80 dB min
- Output voltage swing Rail-to-rail
- Bandwidth 80 kHz
- Operating temperature range (ambient) –40°C to 125°C
- Supply voltage 4.75V to 5.5V
- Supply current 1 mA

Applications

- Fuel injection control
- High and low side driver configuration current sensing
- Power management systems

Typical Application

Low Side Current Sensing



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)
- Human Body Model
  - For input pins only: ±4000V
  - For All other pins: ±2000V
- Machine Model: 200V

Supply Voltage (V_S - GND): 5.75V

Common Mode Voltage on +IN and –IN
- Transient (400 ms): –7V to 45V

Storage Temperature Range: –65°C to +150°C

Junction Temperature (Note 3): +150°C max

Soldering Information
- Infrared or Convection (20 sec): 235°C
- Wave Soldering Lead Temp. (10 sec): 260°C

Operating Ratings (Note 1)

Temperature Range

Packaged Devices (Note 3): –40°C to +125°C

Supply Voltage (V_S – GND): 4.75V to 5.5V

Package Thermal Resistance (θ_{JA} (Note 3))
- 8-Pin SOIC: 190°C/W

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_S = 5V, GND = 0, –2V ≤ V_{CM} ≤ 16V, R_L = Open. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_{OS}	Input Offset Voltage	$V_{CM} = V_S/2$			±0.25	±1.0	mV
TC V_{OS}	Input Offset Voltage Drift	$V_{CM} = V_S/2$	25°C ≤ T_A ≤ 125°C		±6	**±15**	µV/°C
			–40°C ≤ T_A ≤ 25°C		±6	**±20**	
A2 I_B	Input Bias Current of A2	(Note 7)				**±20**	nA
I_S	Supply Current				1.0	1.2 **1.4**	mA
R_{CM}	Input Impedance Common Mode			**160**	200	**240**	kΩ
R_{DM}	Input Impedance Differential Mode			**320**	400	**480**	kΩ
CMVR	Input Common-Mode Voltage Range			**–2**		**+16**	V
DC CMRR	DC Common Mode Rejection Ratio	0°C ≤ T_A ≤ 125°C	–2V ≤ V_{CM} ≤ 16V	**80**	103		dB
		–40°C ≤ T_A ≤ 0°C	–2V ≤ V_{CM} ≤ 16V	**77**			
AC CMRR	AC Common Mode Rejection Ratio (Note 8)	–2V ≤ V_{CM} ≤ 16V	f = 1 kHz	80	95		dB
			f = 10 kHz		78		
PSRR	Power Supply Rejection Ratio	4.75V ≤ V_S ≤ 5.5V		**70**	80		dB
$R_{F\text{-}INT}$	Filter Resistor			**97**	100	**103**	kΩ
$TCR_{F\text{-}INT}$	Filter Resistor Drift				20		ppm/°C
	Midscale Offset Scaling Accuracy (Pin 7)					1	%
A_V	Total Gain			19.8	20	20.2	V/V
	Gain Drift				±2	**±25**	ppm/°C
A_{V1}	A1 Gain			9.9	10	10.1	V/V
A_{V2}	A2 Gain			1.98	2	2.02	V/V
A1 V_{OUT}	A1 Output Voltage Swing		VOL		0.004	0.01	V
			VOH	4.80	4.95		
A2 V_{OUT}	A2 Output Voltage Swing (Notes 9, 10)	R_L = 100 kΩ on Output	VOL		0.007	0.02	V
			VOH	4.80	4.99		
		R_L = 10 kΩ on Output	VOL		0.03		V
			VOH		4.95		
SR	Slew Rate (Note 11)				0.7		V/µs
BW	Bandwidth				80		kHz
Noise	0.1 Hz to 10 Hz				5.7		μV_{PP}
	Spectral Density	f = 1 kHz			452		$nV/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the parametric norm at the time of characterization.

Note 6: The V_{OS} maximum limit indicated does not include effects of lifetime drift, see Application Note.

Note 7: Positive current corresponds to current flowing into the device.

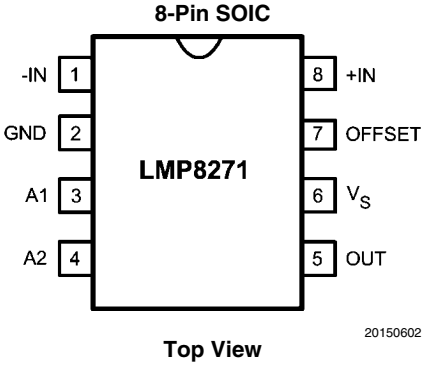
Note 8: AC Common Mode Signal is a $16V_{PP}$ sine-wave (0V to 16V) at the given frequency.

Note 9: For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.

Note 10: For this test input is driven from A1 stage.

Note 11: Slew rate is the average of the rising and falling slew rates.

Connection Diagram



Top View

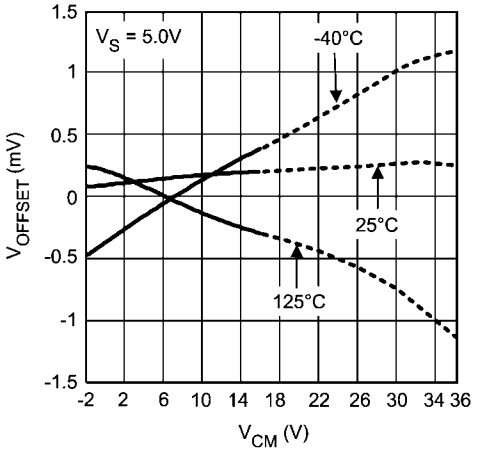
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMP8271MA	LMP8271MA	95 Units/Rail	M08A
	LMP8271MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics

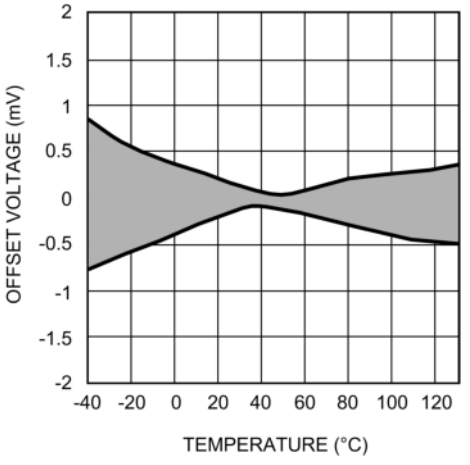
Unless otherwise specified: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2

V_{OS} vs. V_{CM} Over Temperature



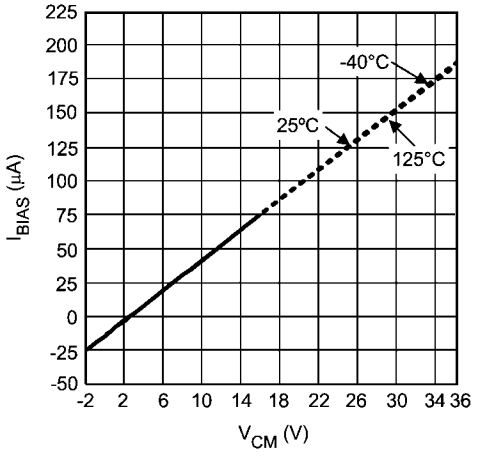
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Typical V_{OS} vs. Temperature



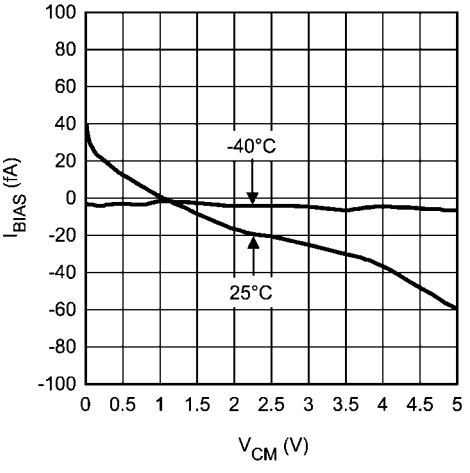
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Input Bias Current Over Temperature (A1 Inputs)



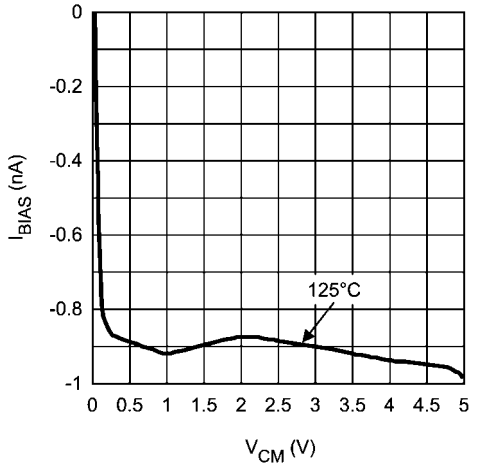
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Input Bias Current Over Temperature (A2 Inputs)



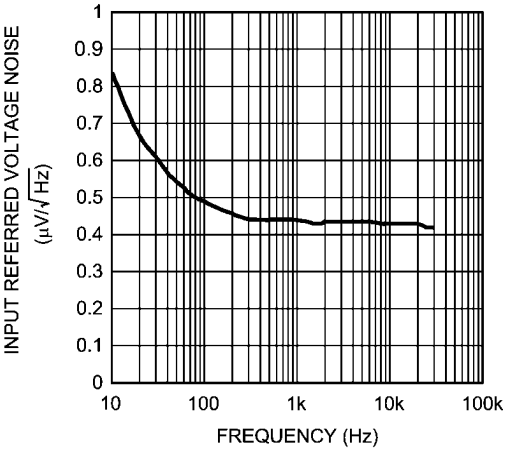
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Input Bias Current Over Temperature (A2 Inputs)



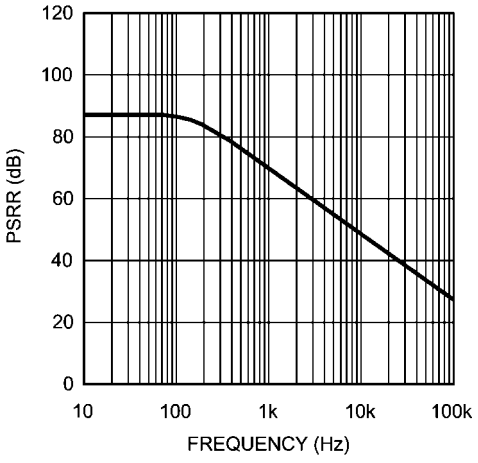
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Input Referred Voltage Noise vs. Frequency



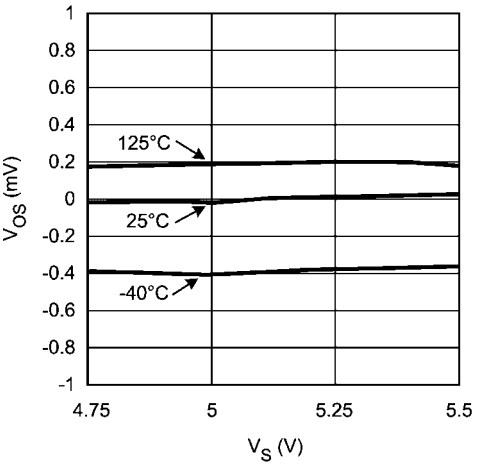
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PSRR vs. Frequency



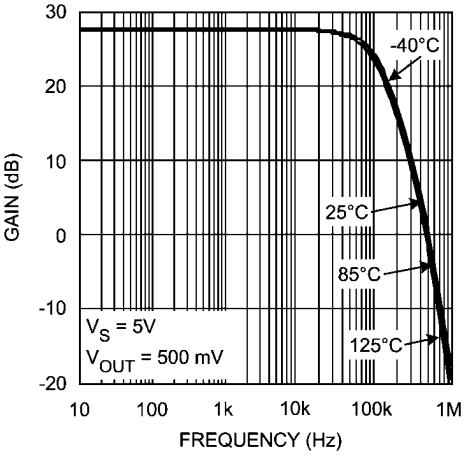
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V_{OS} vs. Supply Voltage



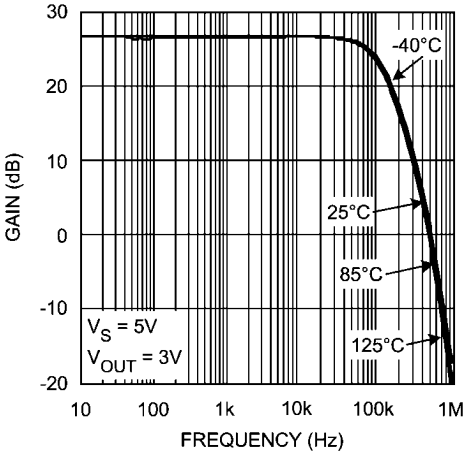
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Gain vs. Frequency Over Temperature



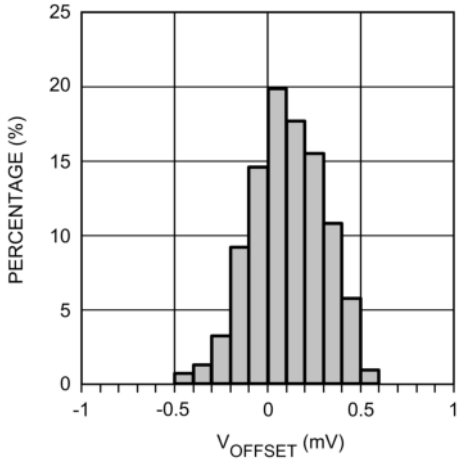
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Gain vs. Frequency Over Temperature



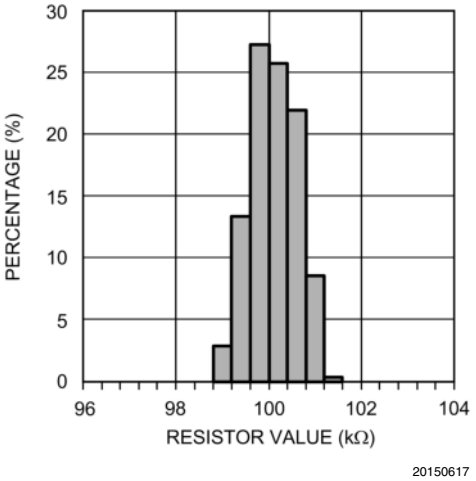
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Offset Voltage Distribution



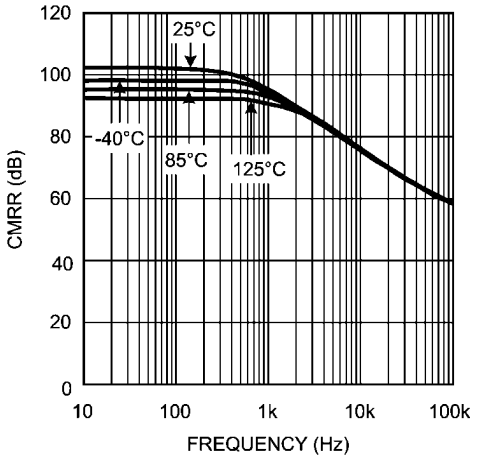
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Filter Resistor



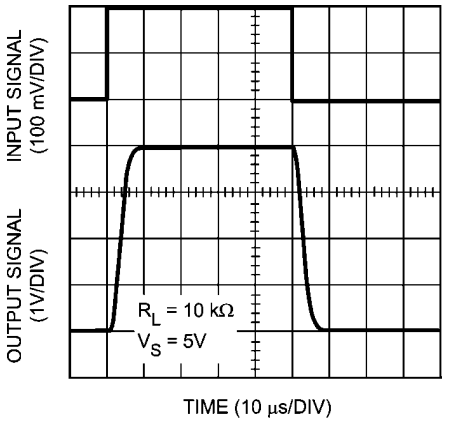
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CMRR vs. Frequency



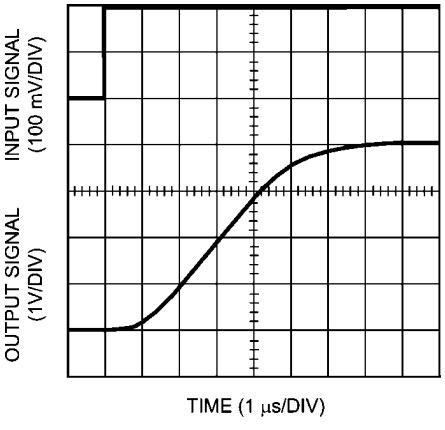
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Step Response



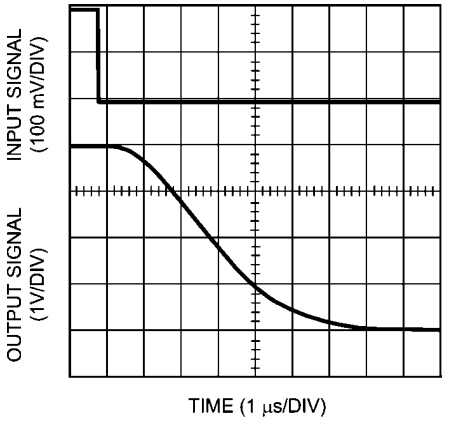
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Settling Time (Rising Edge)



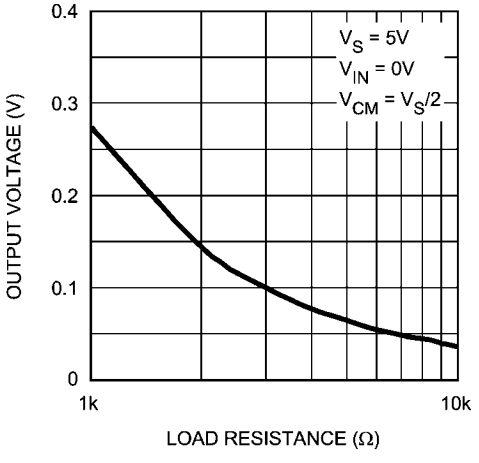
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Settling Time (Falling Edge)



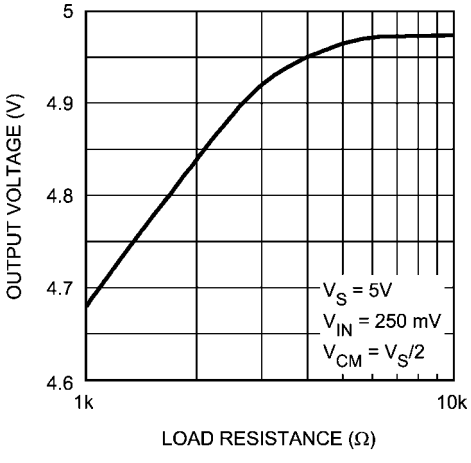
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Output Voltage vs. R_L to V_S



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Output Voltage vs. R_L to GND



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Application Note

LMP8271

The LMP8271 is a single supply amplifier with a fixed gain of 20 and a common mode voltage range of −2V to 16V. The fixed gain is achieved in two separate stages, a preamplifier with gain of +10 and a second stage amplifier with gain of +2. A block diagram of the LMP8271 is shown in .

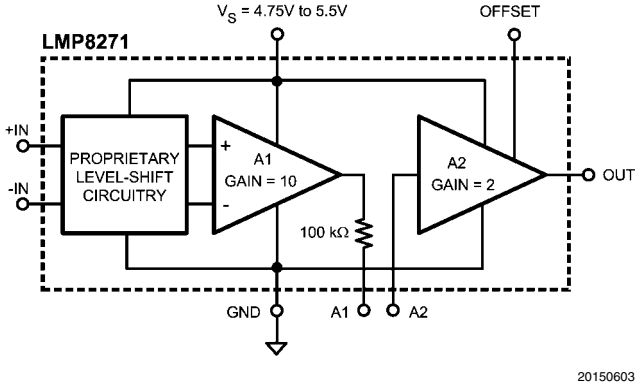


FIGURE 1. LMP8271

The overall offset of the LMP8271 is minimized by trimming amplifier A1. This is done so that the output referred offset of A1 cancels the input referred offset of A2 or $10V_{OS1} = -V_{OS2}$.

Because of this offset voltage relationship, the offset of each individual amplifier stage may be more than the limit specified for the overall system in the datasheet tables. Care must be given when pin 3 and 4, A1 and A2, are connected to each other. If the signal going from A1 to A2 is amplified or attenuated (by use of amplifiers and resistors), the overall LMP8271 offset will be affected as a result. Filtering the signal between A1 and A2 or simply connecting the two pins will not change the offset of the LMP8271.

Referencing the input referred offset voltages of each stage, the following relationship holds:

$$\frac{(10V_{OS1}) + (V_{OS2})}{10} = V_{OS}\,(\text{LMP8271})$$

If the signal on pin 3 is scaled, attenuated or amplified, by a factor **X** then the offset of the overall system will become:

$$\frac{(10V_{OS1}) \times (X) + (V_{OS2})}{10\,(X)} = V_{OS}\,(\text{LMP8271})$$

POWER SUPPLY DECOUPLING

In order to decouple the LMP8271 from AC noise on the power supply, it is recommended to use a 0.1 µF on the supply pin. It is best to use a 0.1 µF capacitor in parallel with a 10 µF capacitor. This will generate an AC path to ground for most frequency ranges and will greatly reduce the noise introduced by the power supply.

LIFETIME DRIFT

Input Offset Voltage is an electrical parameter which may drift over time. This drift, known as lifetime drift, is very common in operational amplifiers; however, its effect is more evident in precision amplifiers. This is due to the very low Input Offset Voltage specifications in these amplifiers.

Numerous reliability tests have been performed to characterize this drift for the LMP8271. Prior to each long term reliability test the Input Offset Voltage of the LMP8271 was measured at room temperature. The LMP8271 was then subjected to a preconditioning sequence consisting of a 16 hour bake at 125°C; an unbiased 168 hour Temperature Humidity Storage Test ,THST, at 85°C and 85% humidity; four passes of infrared reflow with a maximum temperature of 260°C; and finally one hundred 30 min Temperature Cycles ,TMCL, between −65°C and 150°C (15 min at each temperature).

The long term reliability tests include Operating Life Time, OPL, performed at 150°C for an extended period of time; Temperature Humidity Bias Testing, THBT, at 85°C and 85% humidity for an extended period of time and repeated cycles of TMCL.

The Offset Voltage was measured again after each reliability test at room temperature. The Offset Voltage Drift is the difference between the initial measurement, before preconditioning, and the later measurement, post preconditioning and reliability test.

below shows the offset voltage drift after preconditioning and 1000 hours of OPL.

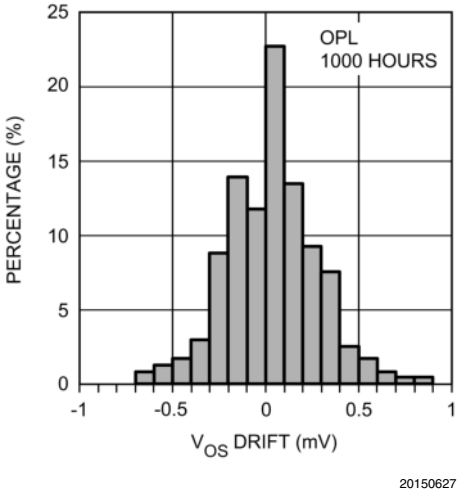


FIGURE 2. OPL Drift Histogram

shows the offset voltage drift after preconditioning and 1000 hours of THBT.

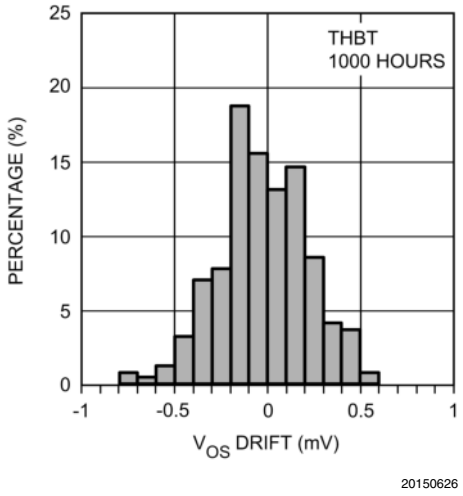


FIGURE 3. THBT Drift Histogram

shows the offset voltage drift after preconditioning and a total of 1000 TMCL cycles.

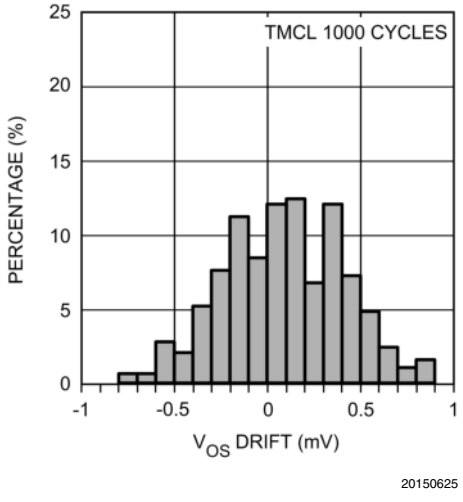


FIGURE 4. TMCL Drift Histogram

SECOND ORDER LOW-PASS FILTER

The LMP8271 can be effectively used to build a second order Sallen-Key low pass filter. The general filter is shown in

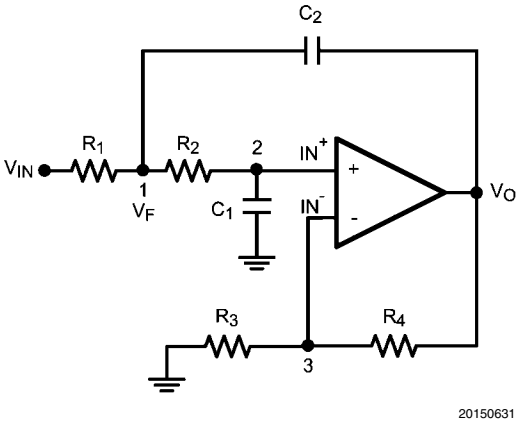


FIGURE 5. Second Order Low-Pass Filter

With the general transfer function:

$$\frac{V_O}{V_{IN}} = \frac{K}{M - KN} \quad (1)$$

Where:

$$M = s^2C_1C_2R_1R_2 + s(R_1C_1+R_1C_2+C_1R_2) + 1$$
$$N = sC_2R_1$$

and

$$\frac{1}{K} = \frac{1}{A_{VOL}} + \frac{R_3}{R_3 + R_4}$$

K represents sum of the DC closed loop gain and the non-ideality behavior of the operational amplifier. Assuming ideal behavior, the equation for K simply reduces to the DC gain, which is set to +2 for the LMP8271.

The LMP8271 can be used to realize this configuration as shown in :

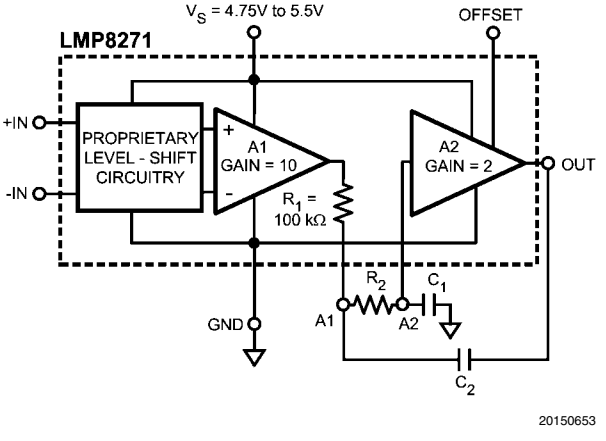


FIGURE 6. Low-Pass Filter With LMP8271

Using , the filter parameters can be calculated as follows:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1+R_2C_1+(1-K)R_1C_2}$$

for the LMP8271, R_1 = 100 kΩ. Setting $R_1 = R_2$ and $C_1 = C_2$ results in a low-pass filter with Q = 1. Since the values of resistors are predetermined, the corner frequency of this implementation of the filter depends on the capacitor values.

MID-RAIL OFFSET ADJUSTMENT PIN

The external mid-rail offset adjustment pin enables the user to utilize the LMP8271 for bidirectional current sensing. If the offset pin, pin 7, is connected to ground then the LMP8271 is capable of sensing positive signals. When the offset pin is connected to V_S then $1/2V_S$ is added to the output and under this condition the amplifier can sense both positive and negative signals. If this offset pin is connected to any voltage between ground and V_S, then the output is increased by a voltage equal to half of that offset. Namely, If the offset is connected to V_X, then the output increases by $1/2V_X$. This relationship is shown in .

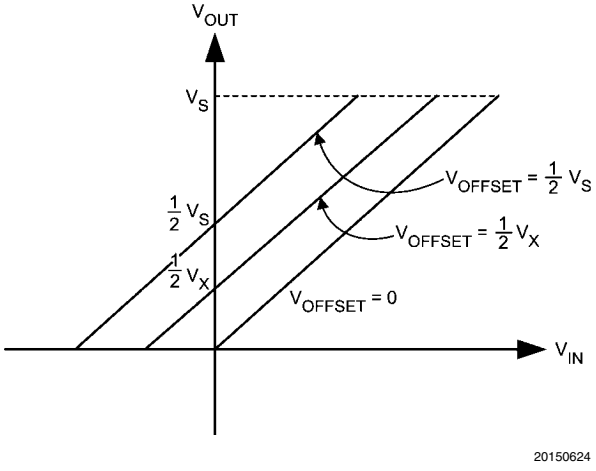


FIGURE 7. Mid-Rail Offset Adjustment Pin Function

Note that the offset pin, pin 7, needs to be connected at all times. If the pin is left floating, the LMP8271 will be operating in an undefined mode. Also pin 7 should be driven from a low impedance source.

In addition to shifting the output of the LMP8271 by $1/2V_X$, the offset voltage applied to the offset adjustment pin shifts the output of the first amplifier by $1/2V_X$. shows a simplified schematic of how this offset adjustment is done. Note that there is a proprietary level shift stage as well as an amplification stage before A1. The combination of these two stages and A1 provide the 10X gain and also shift the output voltage level by half of the offset voltage applied. The output of A1 with respect to the inputs shown (V_{IN}^+ and V_{IN}^-) is:

$V_{OUT}(A1) = 10(V_{IN}^+ - V_{IN}^-) + 1/2\ (V_{OFFSET})$

The output of A2 with respect to its inputs, or the output of A1 is:

$V_{OUT}(A2) = 1/2(V_{OFFSET}) + 2(V_{OUT}(A1) - 1/2\ (V_{OFFSET}))$

Therefore

$V_{OUT}(A2) = 20(V_{IN}^+ - V_{IN}^-) + 1/2\ (V_{OFFSET})$

A2 has a gain of 2X and applying an offset voltage V_X will shift the output voltage level by $1/2V_X$. This shows that half of the voltage applied at the offset pin will be present on the output of both the amplification stages inside the LMP8271.

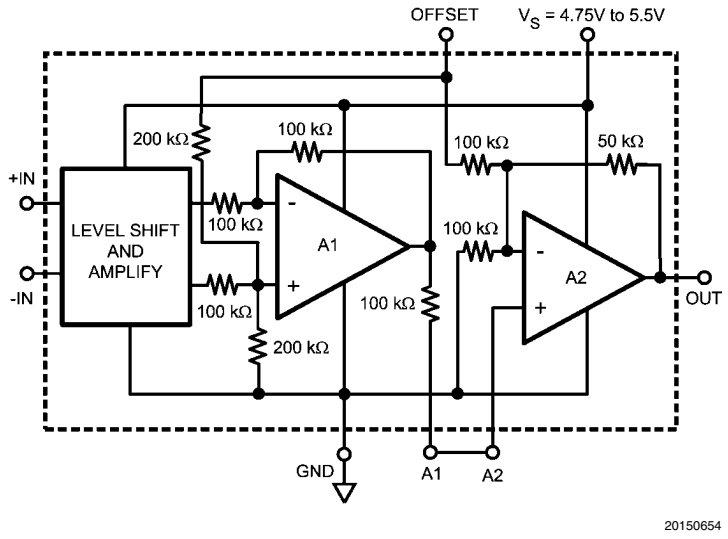


FIGURE 8. Mid-Rail Adjustment Pin Schematic

CURRENT LOOP RECEIVER

Many types of process control instrumentation use 4 to 20 mA transmitters to transmit the sensor's analog value to a central control room. The LMP8271 can be used as a current loop receiver as shown in .

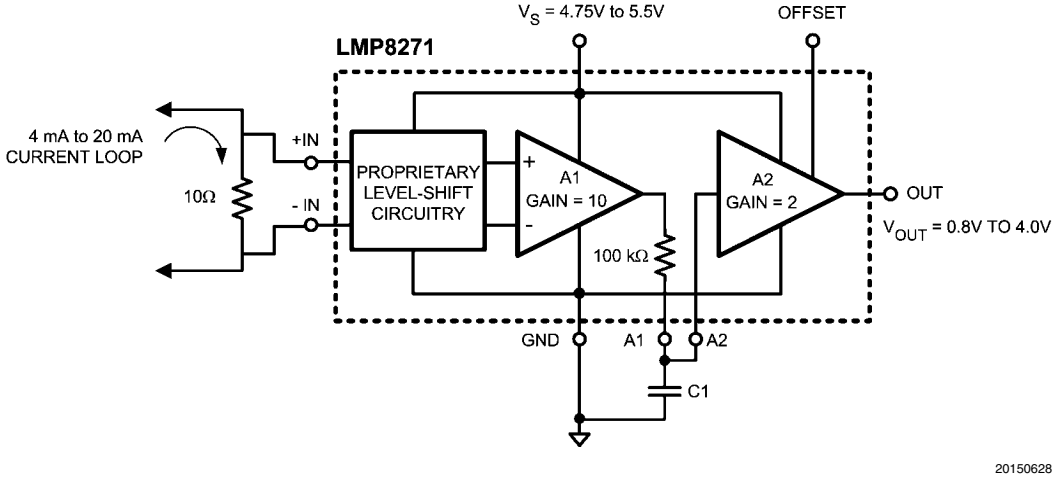


FIGURE 9. Current Loop Receiver

HIGH SIDE CURRENT SENSING

High side current measurement requires a differential amplifier with gain. Here the DC voltage source represents a common mode voltage with the +IN input at the supply voltage and the −IN input very close to the supply voltage. The LMP8271 can be used with a common mode voltage, V_{DC} in this case, of up to 16V.

The LMP8271 can be used for high side current sensing. The large common mode voltage range of this device allows it to sense signals outside of its supply voltage range. Also, the LMP8271 has very high CMRR, which enables it to sense very small signals in the presence of larger common mode signals. The system in couples these two characteristics of the LMP8271 in an automotive application. The signal through R_{S1} is detected and amplified by the LMP8271 in the presence of a common mode signal of up to 16V with the highest accuracy.

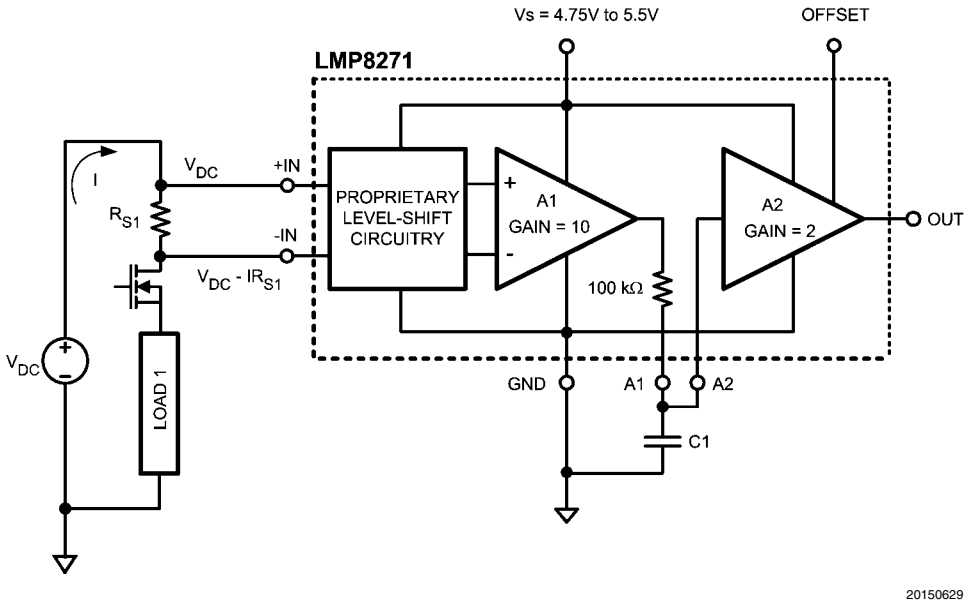


FIGURE 10. High Side Current Sensing

LOW SIDE CURRENT SENSING

Low side current measurements can cause a problem for operational amplifiers by exceeding the negative common mode voltage limit of the device. In , the load current is returning to the power source through a common connection that has a parasitic resistance. The voltage drop across the parasitic resistances can cause the ground connection of the measurement circuits to be at a positive voltage with respect to the common side of the sense resistor. This will result in one or both of the inputs to be negative with respect to the circuit's ground. The LMP8271 has a wide extended common mode voltage range of –2V to 16V and will function in this condition.

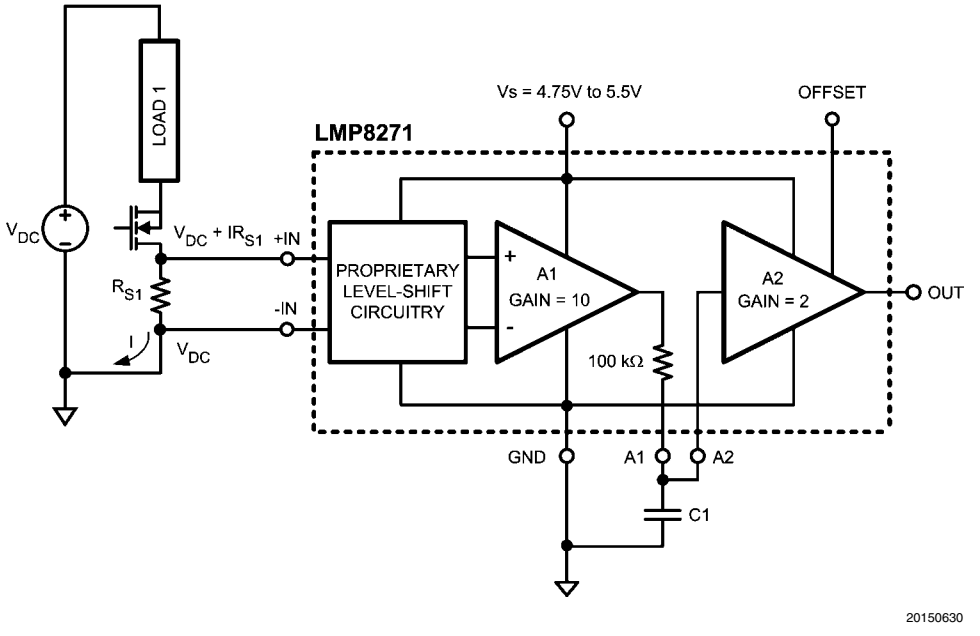


FIGURE 11. Low Side Current Sensing

GAINS OTHER THAN 20

The LMP8271 has an internal gain of +20; however this gain can be modified. The signal path between the two amplifiers is available as external pins.

GAINS LESS THAN 20

shows the configuration used to reduce the LMP8271 gain.

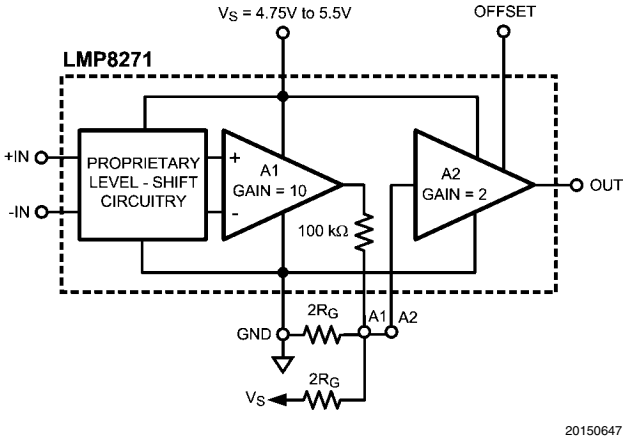


FIGURE 12. Gains Less Than 20

Where:

$$\text{GAIN (NEW)} = \frac{20\ R_G}{R_G + 100\ k\Omega}$$

and

$$R_G = (100\ k\Omega)\ \frac{\text{GAIN (NEW)}}{20 - \text{GAIN (NEW)}}$$

GAINS GREATER THAN 20

A higher gain can be achieved by using positive feedback on the second stage amplifier, A2, of the LMP8271. shows the configuration:

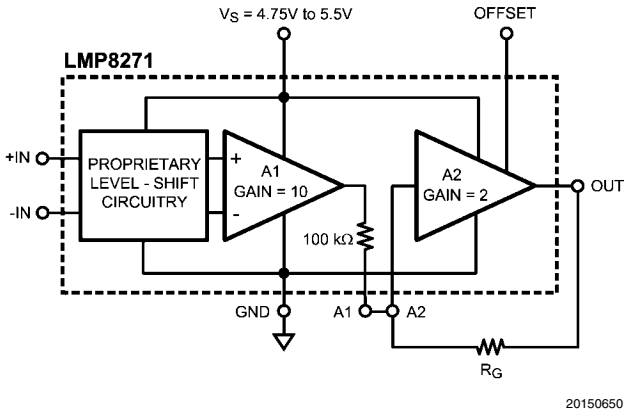


FIGURE 13. Gains Greater Than 20

The total gain is given by:

$$\text{GAIN (NEW)} = \frac{20\ R_G}{R_G - 100\ k\Omega} \quad (2)$$

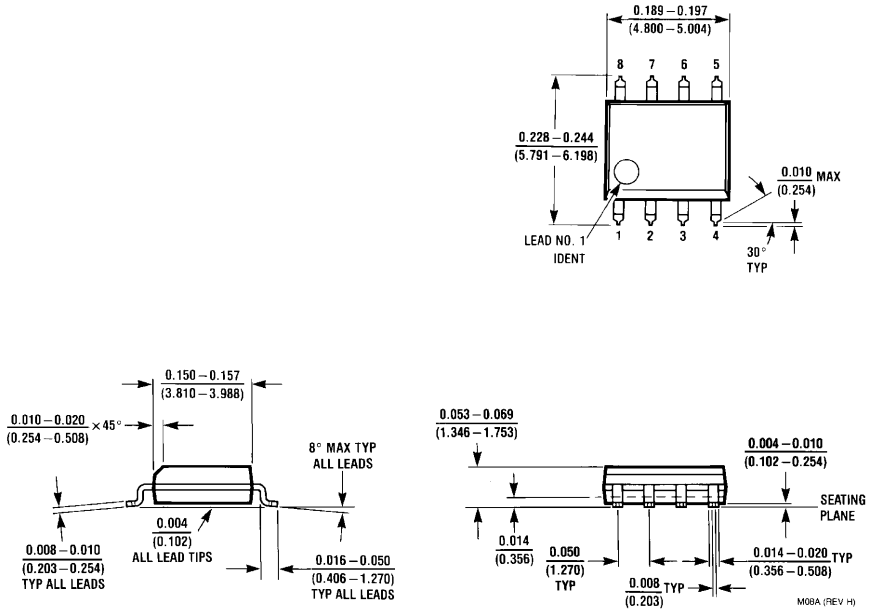
which can be rearranged to calculate R_G:

$$R_G = (100\ k\Omega)\ \frac{\text{GAIN (NEW)}}{\text{GAIN (NEW)} - 20}$$

The inverting gain of the second amplifier is set at 2, giving a total system gain of 20. The non-inverting gain which is achieved through positive feedback can be less than or equal to this gain without any issues. This implies a total system gain of 40 or less is easily achievable. Once the positive gain surpasses the negative gain, the system might oscillate.

As the value of gain resistor, R_G, approaches that of the internal 100 kΩ resistor, maintaining gain accuracy will become more challenging. This is because Gain(new) is inversely proportional to (R_G-100 kΩ), see . As $R_G \rightarrow 100$ kΩ, the denominator of gets smaller. This smaller value will be comparable to the tolerance of the 100 kΩ resistor and R_G and hence the gain will be dominated by accuracy level of these resistors and the gain tolerance will be determined by the tolerance of the external resistor used for R_G and the 3% tolerance of the internal 100 kΩ resistor.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A

Notes

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