PLLatinum™ Low Power Frequency Synthesizer for RF Personal Communications LMX2306 550 MHz, LMX2316 1.2 GHz, LMX2326 2.8 GHz

Check for Samples: LMX2306, LMX2316, LMX2326

FEATURES

- **2.3V to 5.5V Operation**
- **Ultra Low Current Consumption**
- **2.5V V_{CC} JEDEC Standard Compatible**
- **Programmable or Logical Power Down Mode:**
  - **I_{CC} = 1 µA Typical at 3V**
- **Dual Modulus Prescaler:**
  - **LMX2306: 8/9**
  - **LMX2316/26: 32/33**
- **Selectable Charge Pump Tri-state Mode**
- **Selectable FastLock Mode with Timeout Counter**
- **MICROWIRE Interface**
- **Digital Lock Detect**

APPLICATIONS

- **Portable Wireless Communications (PCS/PCN, Cordless)**
- **Wireless Local Area Networks (WLANs)**
- **Cable TV Tuners (CATV)**
- **Pagers**
- **Other Wireless Communication Systems**

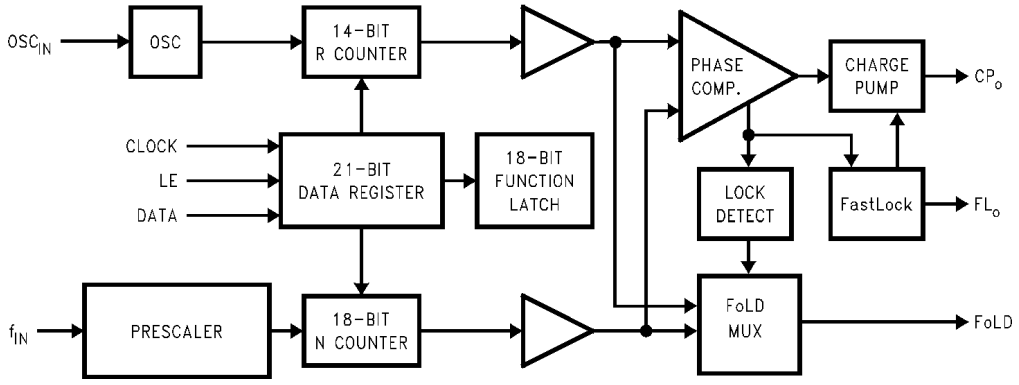
DESCRIPTION

The LMX2306/16/26 are monolithic, integrated frequency synthesizers with prescalers that are designed to be used to generate a very stable low noise signal for controlling the local oscillator of an RF transceiver. They are fabricated using TI's ABiC V silicon BiCMOS 0.5µ process.

The LMX2306 contains a 8/9 dual modulus prescaler while the LMX2316 and the LMX2326 have a 32/33 dual modulus prescaler. The LMX2306/16/26 employ a digital phase locked loop technique. When combined with a high quality reference oscillator and loop filter, the LMX2306/16/26 provide the feedback tuning voltage for a voltage controlled oscillator to generate a low phase noise local oscillator signal. Serial data is transferred into the LMX2306/16/26 via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.3V to 5.5V. The LMX2306/16/26 feature ultra low current consumption; LMX2306 - 1.7 mA at 3V, LMX2316 - 2.5 mA at 3V, and LMX2326 - 4.7 mA at 3V.

The LMX2306/16/26 synthesizers are available in a 16-pin TSSOP surface mount plastic package.

Functional Block Diagram



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Connection Diagrams

LMX2306/16/26

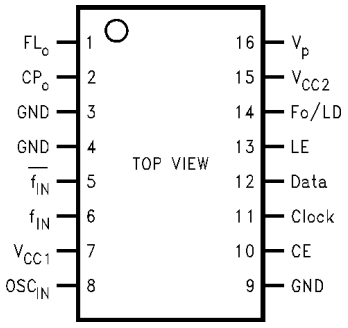


Figure 1. 16-Lead (0.173” Wide) Thin Shrink Small Outline Pkg - TSSOP
See Package Number PW

LMX2306/16/26

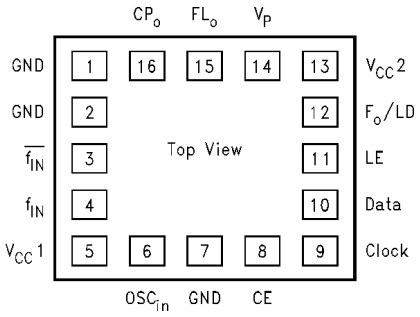


Figure 2. 16-pin Chip Scale Package PLGA
See Package Number NPG

Pin Descriptions

16-Pin TSSOP	16-Pin PLGA	Pin Name	I/O	Description
1	15	FL_o	O	FastLock Output. For connection of parallel resistor to the loop filter. (See FastLock Modes description.)
2	16	CP_o	O	Charge Pump Output. For connection to a loop filter for driving the input of an external VCO.
3	1	GND		Charge Pump Ground.
4	2	GND		Analog Ground.
5	3	$\overline{f_{IN}}$	I	RF Prescaler Complementary Input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The complementary input can be left unbypassed, with some degradation in RF sensitivity.
6	4	f_{IN}	I	RF Prescaler Input. Small signal input from the VCO.
7	5	V_{CC1}		Analog Power Supply Voltage Input. Input may range from 2.3V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. V_{CC1} must equal V_{CC2}.
8	6	OSC_{IN}	I	Oscillator Input. This input is a CMOS input with a threshold of approximately $V_{CC}/2$ and an equivalent 100k input resistance. The oscillator input is driven from a reference oscillator.
9	7	GND		Digital Ground.
10	8	CE	I	Chip Enable. A LOW on CE powers down the device and will tri-state the charge pump output. Taking CE HIGH will power up the device depending on the status of the power down bit F2. (See Powerdown Operation and DEVICE PROGRAMMING AFTER FIRST APPLYING V_{cc}.)
11	9	Clock	I	High Impedance CMOS Clock Input. Data for the various counters is clocked in on the rising edge into the 21-bit shift register.
12	10	Data	I	Binary Serial Data Input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	11	LE	I	Load Enable CMOS Input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 3 appropriate latches (control bit dependent).
14	12	Fo/LD	O	Multiplexed Output of the RF Programmable or Reference Dividers and Lock Detect. CMOS output. (See Table 4.)
15	13	V_{CC2}		Digital Power Supply Voltage Input. Input may range from 2.3V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. V_{CC1} must equal V_{CC2}.
16	14	V_P		Power Supply for Charge Pump. Must be ≥ V_{CC}.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Power Supply Voltage	V_{CC1}	−0.3V to +6.5V
	V_{CC2}	−0.3V to +6.5V
	V_p	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)		−0.3V to V_{CC} + 0.3V
Storage Temperature Range (T_S)		−65°C to +150°C
Lead Temperature (T_L)	(solder, 4 sec.)	+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensured specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.

(2) This device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

Recommended Operating Conditions

		Min	Max	Units
Power Supply Voltage	V_{CC1}	2.3	5.5	V
	V_{CC2}	V_{CC1}	V_{CC1}	V
	V_p	V_{CC}	5.5	V
Operating Temperature (T_A)		−40	+85	°C

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Electrical Characteristics

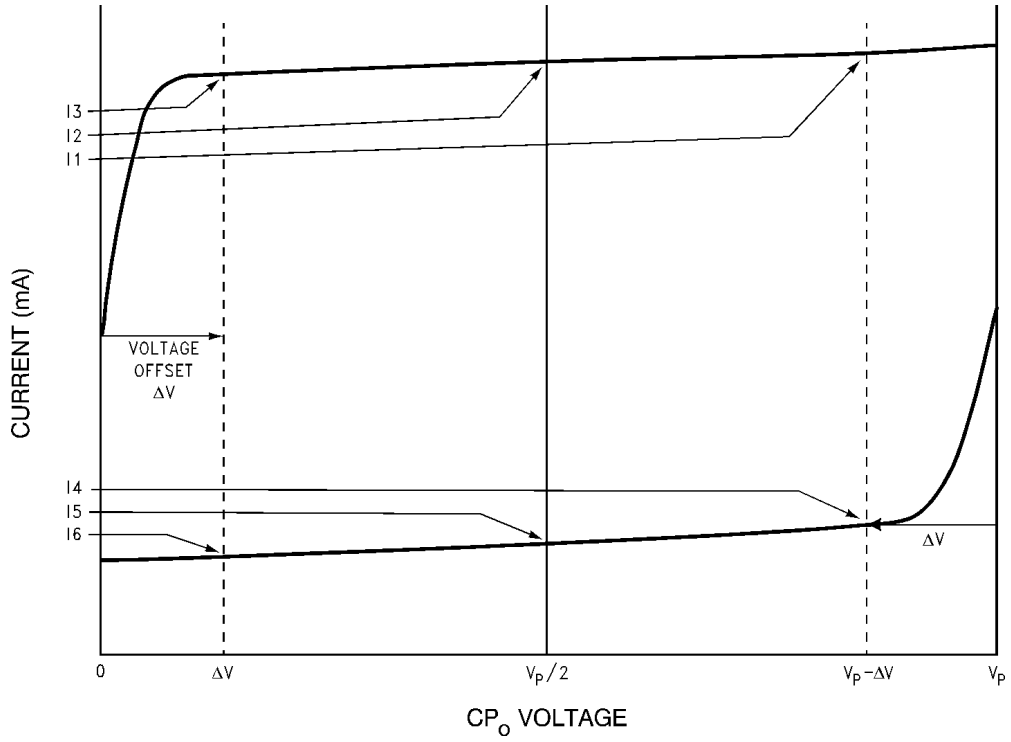
V_{CC} = 3.0V, V_p = 3.0V; −40°C < T_A < 85°C except as specified

Symbol	Parameter		Conditions	Values			Units
				Min	Typ	Max	
I_{CC}	Power Supply Current	LMX2306	V_{CC} = 2.3V to 5.5 V		1.7	3.5	mA
		LMX2316	V_{CC} = 2.3V to 5.5V		2.5	5.0	mA
		LMX2326	V_{CC} = 2.3V to 5.5V		4.7	7.0	mA
$I_{CC-PWDN}$	Powerdown Current		V_{CC} = 3.0V		1		µA
f_{IN}	RF Input Operating Frequency	LMX2306	V_{CC} = 2.3V to 5.5V	25		550	MHz
		LMX2316	V_{CC} = 2.3V to 5.5V	0.1		1.2	GHz
		LMX2326	V_{CC} = 2.3V to 5.5V	0.1		2.1	GHz
			V_{CC} = 3.0V to 5.5V	0.1		2.8	GHz
f_{osc}	Maximum Oscillator Frequency		V_{CC} = 2.3V to 5.5V	5		40	MHz
			V_{CC} = 2.7V to 5.5V	5		100	MHz
fφ	Maximum Phase Detector Frequency					10	MHz
Pf_{IN}	RF Input Sensitivity		V_{CC} = 2.3V to <3.0V	−15		+0	dBm
			V_{CC} = 3.0V to 5.5V	−10		+0	dBm
OSC_{IN}	Oscillator Sensitivity			−5			dBm
V_{IH}	High-Level Input Voltage		See (1)	0.8 × V_{CC}			V
V_{IL}	Low-Level Input Voltage		See (1)			0.2 × V_{CC}	V
I_{IH}	High-Level Input Current		V_{IH} = V_{CC} = 5.5V (1)	−1.0		1.0	µA
I_{IL}	Low-Level Input Current		V_{IL} = 0V, V_{CC} = 5.5V (1)	−1.0		1.0	µA
I_{IH}	Oscillator Input Current		V_{IH} = V_{CC} = 5.5V			100	µA
I_{IL}	Oscillator Input Current		V_{IL} = 0V, V_{CC} = 5.5V	−100			µA
$ICP_{o\text{-source}}$	Charge Pump Output Current		V_{Do} = V_p/2, ICP_o = LOW (2)		−250		µA
$ICP_{o\text{-sink}}$			V_{Do} = V_p/2, ICP_o = LOW (2)		250		µA
$ICP_{o\text{-source}}$			V_{Do} = V_p/2, ICP_o = HIGH (2)		−1.0		mA
$ICP_{o\text{-sink}}$			V_{CPo} = V_p/2, ICP_o = HIGH (2)		1.0		mA
$ICP_{o\text{-Tri}}$	Charge Pump Tri-state Current		0.5 ≤ V_{CPo} ≤ V_p − 0.5 −40°C < T_A < 85°C	−2.5		2.5	nA
$ICP_{o\text{-sink vs}}$ $ICP_{o\text{-source}}$	CP Sink vs Source Mismatch		V_{CPo} = V_p/2 T_A = 25°C		5		%
ICP_o vs V_{Do}	CP Current vs Voltage		0.5 ≤ V_{CPo} ≤ V_p − 0.5 T_A = 25°C		5		%
ICP_o vs T	CP Current vs Temperature		V_{CPo} = V_p/2 −40°C < T_A < 85°C		5		%
V_{OH}	High-Level Output Voltage		I_{OH} = −500 µA	V_{CC} − 0.4			V
V_{OL}	Low-Level Output Voltage		I_{OL} = 500 µA			0.4	V
t_{CS}	Data to Clock Set Up Time		See SERIAL DATA INPUT TIMING	50			ns
t_{CH}	Data to Clock Hold Time		See SERIAL DATA INPUT TIMING	10			ns
t_{CWH}	Clock Pulse Width High		See SERIAL DATA INPUT TIMING	50			ns
t_{CWL}	Clock Pulse Width Low		See SERIAL DATA INPUT TIMING	50			ns
t_{ES}	Clock to Load Enable Set Up Time		See SERIAL DATA INPUT TIMING	50			ns
t_{EW}	Load Enable Pulse Width		See SERIAL DATA INPUT TIMING	50			ns

(1) Except f_{IN} and OSC_{IN}.
(2) See Table 1 for ICP_o description

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Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $VCP_o = V_P - \Delta V$
I2 = Charge Pump Sink Current at $VCP_o = V_P/2$
I3 = Charge Pump Sink Current at $VCP_o = \Delta V$
I4 = Charge Pump Source Current at $VCP_o = V_P - \Delta V$
I5 = Charge Pump Source Current at $VCP_o = V_P/2$
I6 = Charge Pump Source Current at $VCP_o = \Delta V$
ΔV = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to V_{CC} and GND. Typical values are between 0.5V and 1.0V.

Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ICP_o \text{ Vs } VCP_o = \frac{\frac{1}{2}(|I1| - |I3|)}{\frac{1}{2}(|I1| + |I3|)} \times 100\% = \frac{\frac{1}{2}(|I4| - |I6|)}{\frac{1}{2}(|I4| + |I6|)} \times 100\% \quad (1)$$

Charge Pump Output Current Sink Vs Charge Pump Output Current Source Mismatch

$$ICP_o \text{ SINK Vs } ICP_o \text{ SOURCE} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\% \quad (2)$$

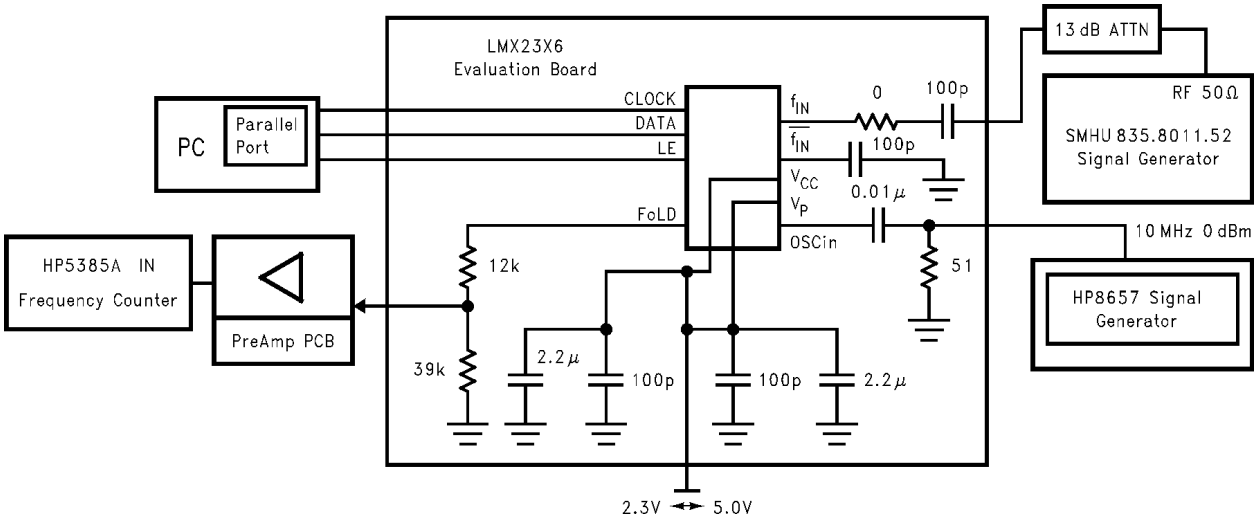
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Charge Pump Output Current Magnitude Variation Vs Temperature

$$ICP_o \text{ Vs } T_A = \frac{|I_2|_{T_A} - |I_2|_{T_A = 25°C}}{|I_2|_{T_A = 25°C}} \times 100\%$$

$$= \frac{|I_5|_{T_A} - |I_5|_{T_A = 25°C}}{|I_5|_{T_A = 25°C}} \times 100\% \quad (3)$$

RF Sensitivity Test Block Diagram



N=10,000 R=50 P=32

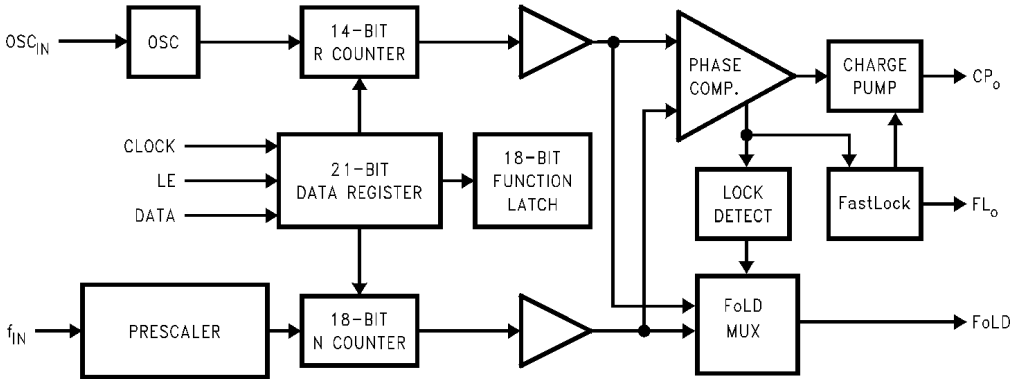
Sensitivity limit is reached when the error of the divided RF output, FoLD, is greater than or equal to 1 Hz.

Functional Description

The simplified block diagram below shows the 21-bit data register, a 14-bit R Counter, an 18-bit N Counter, and a 18-bit Function Latch (intermediate latches are not shown). The data stream is shifted (on the rising edge of LE) into the DATA input, MSB first. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:

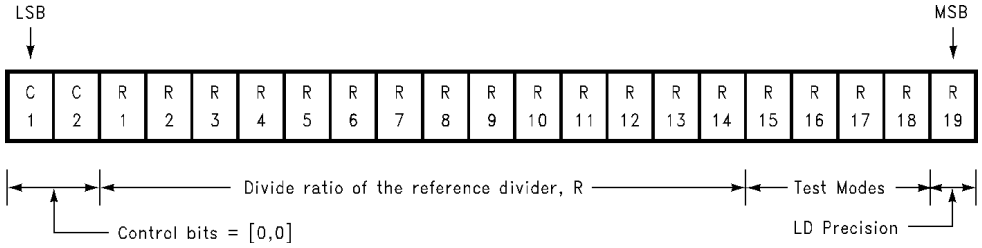
Control		DATA Location
C1	C2	
0	0	R Counter
1	0	N Counter
0	1	Function Latch
1	1	Initialization

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PROGRAMMABLE REFERENCE DIVIDER

If the Control Bits are [C_1, C_2] = [0,0], data is transferred from the 21-bit shift register into a latch that sets the 14-bit R Counter. The 4 bits R15–R18 are for test modes, and should be set to 0 for normal use. The LD precision bit, R19, is described in the Lock Detect Output Characteristics section. Serial data format is shown below.



R15 to R18 are test modes and should be zero for normal operation.
Data is shifted in MSB first.

14-bit Programmable Reference Divider Ratio (R Counter)

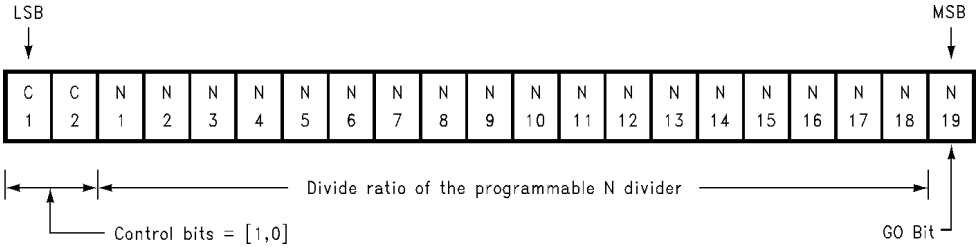
Divide Ratio[2][3]	R[1] 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(1) R1 to R14: These bits select the divide ratio of the programmable reference divider.
(2) Divide ratios less than 3 are prohibited.
(3) Divide ratio: 3 to 16383

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PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 5-bit swallow counter (A counter) and the 13-bit programmable counter (B counter). If the Control Bits are [C_1, C_2] = [1,0], data is transferred from the 21-bit shift register into a 5-bit latch (which sets the Swallow (A) Counter), a 13-bit latch (which sets the 13-bit programmable (B) Counter), and the GO bit (See FastLock Modes section) MSB first. For the LMX2306 the maximum N value is 65535 and the minimum N value is 56. For the LMX2316/26, the maximum N value is 262143 and the minimum N value is 992. Serial data format is shown below.



Data is shifted in MSB first.

5-bit Swallow Counter Divide Ratio (A Counter)

LMX2316/26							LMX2306 (1)					
Divide Ratio (2)	N 5	N 4	N 3	N 2	N 1		Divide Ratio (3)	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0		0	X	X	0	0	0
1	0	0	0	0	1		1	X	X	0	0	1
•	•	•	•	•	•		•	•	•	•	•	•
31	1	1	1	1	1		7	X	X	1	1	1

(1) X denotes a Don't Care condition
(2) Divide ratio: 0 to 31 B ≥ A
(3) Divide ratio: 0 to 7 B ≥ A

13-Bit Programmable Counter Divide Ratio (B Counter)

Divide Ratio (1)	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	N 7	N 6
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

(1) Divide ratio: 3 to 8191 (Divide ratios less than 3 are prohibited) B≥A

Pulse Swallow Function

fvco = [(P x B) + A] x fosc/R

where

- f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
- B: Preset divide ratio of binary 13-bit programmable counter (3 to 8191)
- A:
- Preset divide ratio of binary 5-bit swallow counter (0 ≤ A ≤ 31; A ≤ B for LMX2316/26) or (0 ≤ A ≤ 7, A ≤ B for LMX2306)
- f_{osc}: Output frequency of the external reference frequency oscillator
- R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)
- P: Preset modulus of dual modulus prescaler for the LMX2306; P = 8 for the LMX2316/26; P = 32 (4)

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FUNCTION AND INITIALIZATION LATCHES

Both the function and initialization latches write to the same registers. (See DEVICE PROGRAMMING AFTER FIRST APPLYING V_{cc} section for initialization latch description.)

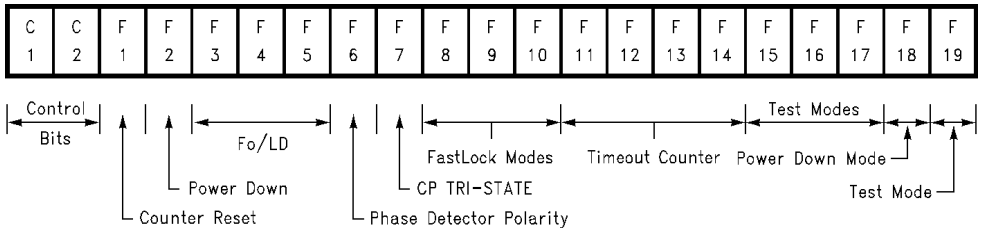


Table 1. Programmable Modes

C1	C2	F1	F2	F3–5	F6	F7	F8
0	1	COUNTER RESET	POWER DOWN	FoLD CONTROL	PD POLARITY	CP TRI-STATE	FASTLOCK ENABLE

F9	F10	F11–14	F15–F17	F18	F19
FAST-LOCK CONTROL	TIMEOUT COUNTER ENABLE	TIMEOUT COUNTER VALUE	TEST MODES	POWER DOWN MODE	TEST MODE

Table 2. Mode Select Truth Table

REGISTER LEVEL	COUNTER RESET	POWER DOWN	PHASE DETECTOR POLARITY	CP TRI-STATE
0	RESET DISABLED	POWERED UP	NEGATIVE	NORMAL OPERATION
1	RESET ENABELED	POWERED DOWN	POSITIVE	TRI-STATE

Function Description

F1. The **Counter Reset** enable mode bit F1, when activated, allows the reset of both N and R counters. Upon powering up, the F1 bit needs to be disabled, then the N counter resumes counting in “close” alignment with the R counter. (The maximum error is one prescalar cycle).

F2. Refer to Powerdown Operation section.

F3–5. Controls output of **FoLD** pin. See FoLD truth table. See Table 4.

F6. Phase Detector Polarity. Depending upon VCO characteristics, F6 bit should be set accordingly. When VCO characteristics are positive F6 should be set HIGH; When VCO characteristics are negative F6 should be set LOW

F7. Charge Pump Tri-state is set using bit F7. For normal operation this bit is set to zero.

F8. When the **FastLock Enable** bit is set the part is forced into one of the four FastLock modes. See description in Table 5, FastLock Decoding.

F9. The **FastLock Control** bit determines the mode of operation when in FastLock (F8 = 1). When not in FastLock mode, FL_o can be used as a general purpose output controlled by this bit. For F9 = 1, FL_o is HIGH and for F9 = 0, FL_o is LOW. See Table 5 for truth table.

F10. Timeout Counter Enable bit is set to 1 to enable the timeout counter. See Table 5 for truth table.

F11–14. FastLock Timeout Counter is set using bits F11-14. Table 6 for counter values.

F15–17. Function bits F15–F17 are for **Test Modes**, and should be set to 0 for normal use.

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F18. Refer to Powerdown Operation section.

F19. Function bit F19 is for a **Test Mode**, and should be set to 0 for normal use.

Powerdown Operation

Bits F[2] and F[18] provide programmable powerdown modes when the CE pin is HIGH. When CE is LOW, the part is always immediately disabled regardless of powerdown bit status. Refer to Table 3.

Synchronous and asynchronous powerdown modes are both available by MICROWIRE selection. Synchronous powerdown occurs if the F[18] bit (Powerdown Mode) is HIGH when F[2] bit (Powerdown) becomes HIGH. Asynchronous powerdown occurs if the F[18] bit is LOW when its F[2] bit becomes HIGH.

In the synchronous powerdown mode (F[18] = HIGH), the powerdown function is gated by the charge pump to prevent unwanted frequency jumps. Once the powerdown program bit F[2] is loaded, the part will go into powerdown mode after the first successive charge pump event.

In the asynchronous powerdown mode (F[18] = LOW), the device powers down immediately after latching LOW data into bit F[2].

The device returns to an actively powered up condition in either synchronous or asynchronous mode immediately upon LE latching LOW data into bit F[2].

Activation of a powerdown condition in either synchronous or asynchronous mode including CE pin activated powerdown has the following effects:

- Removes all active DC current paths.
- Forces the R, N, and timeout counters to their load state conditions.
- Will Tri-state the charge pump.
- Resets the digital lock detect circuitry.
- Debiases the f_{IN} input to a high impedance state.
- Disables the oscillator input buffer circuitry.
- The MICROWIRE control register remains active and capable of loading the data.

Table 3. Power Down Truth Table

CE(Pin 10)	F[2]	F[18]	Mode
LOW	X	X	Asynchronous Power Down
HIGH	0	X	Normal Operation
HIGH	1	0	Asynchronous Power Down
HIGH	1	1	Synchronous Power Down

Table 4. The Fo/LD (pin 14) Output Truth Table

F[3]	F[4]	F[5]	Fo/LD Output State
0	0	0	Tri-state
0	0	1	R Divider Output (fr)
0	1	0	N Divider Output (fp)
0	1	1	Serial Data Output
1	0	0	Digital Lock Detect (See Lock Detect Output Characteristics Section)
1	0	1	n Channel Open Drain Lock Detect (See Lock Detect Output Characteristics Section)
1	1	0	Active HIGH
1	1	1	Active LOW

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Lock Detect Output Characteristics

Output provided to indicate when the VCO frequency is in “lock.” When the loop is locked and the open drain lock detect mode is selected, the pin's output is HIGH, with narrow pulses LOW. When digital lock detect is selected, the output will be HIGH when the absolute phase error is < 15 ns for three or five consecutive phase frequency detector reference cycles, depending on the value of R[19]. Once lock is detected the output stays HIGH unless the absolute phase error exceeds 30 ns for a single reference cycle. Setting the charge pump to tri-state or power down (bits F2, F18) will reset the digital lock detect to the unlocked state. The LD precision bit, R[19], will select five consecutive reference cycles, instead of three, for entering the locked state when R[19] = HIGH.

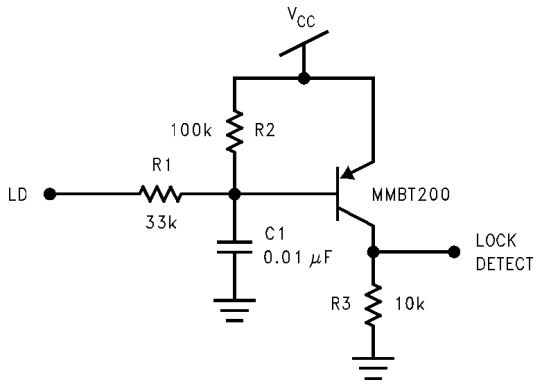


Figure 3. Typical Lock Detect Circuit

Lock Detect Filter Calculation

The component values for the open drain lock detect filter can be determined after assessing the qualifications for an in-lock condition. The in-lock condition can be specified as being a particular number (N) of consecutive reference cycles or duration (D) wherein the phase detector phase error is some factor less than the reference period. In an example where the phase detector reference period is 10 kHz, one might select the threshold for in-lock as occurring when 5 consecutive phase comparisons have elapsed where the phase errors are a 1000 times shorter than the reference period (100 ns). Here, N = 5 and F = 1000.

For the lock detect filter shown in Figure 3, when used in conjunction with a open drain (active sink only) lock detect output, the resistor value for R2 would be chosen to be a factor of F * R1. Thus, if resistor R1 were pulled low for only 1/1000th of the reference cycle period, its “effective” resistance would be on par with R2. The two resistors for that duty cycle condition on average appear to be two 1000× R1 resistors connected across the supply voltage with their common node voltage (Vc) at $V_{CC}/2$. Phase errors larger than 1/1000th of the reference cycle period would drag the average voltage of node Vc below $V_{CC}/2$ indicating an out-of-lock status. If the time constant of R2 * C1 is now calculated to be N * the reference period (500 µs), then the voltage of node Vc would fall below $V_{CC}/2$ only after 5 consecutive phase errors whose average pulse width was greater than 100 ns.

FastLock Modes

FastLock enables the designer to achieve both fast frequency transitions and good phase noise performance by dynamically changing the PLL loop bandwidth. The FastLock modes allow wide band PLL fast locking with seemless transition to a low phase noise narrow band PLL. Consistent gain and phase margins are maintained by simultaneously changing charge pump current magnitude, counter values, and loop filter damping resistor. The four FastLock modes in Table 5 are similar to the technique used in Texas Instruments' LMX 233X series Dual Phase Locked Loops and are selected by F9, F10, and N19 when F8 is HIGH. Modes 1 and 2 change loop bandwidth by a factor of two while modes 3 and 4 change the loop bandwidth by a factor of 4. Modes 1 and 2 increase charge pump magnitude by a factor of 4 and should use R2'=R2 for consistent gain and phase margin. Modes 3 and 4 increase charge pump magnitude and decrease the counter values by a factor of 4. R2' = ⅓ R2 should be used for consistent stability margin in modes 3 and 4. When F8 is LOW, the FastLock modes are disabled, F9 controls only the FL_o output level (FL_o = F9), and N19 determines the charge pump current magnitude (N19=LOW→ICP_o = 250 µA, N19=HIGH→ICP_o = 1 mA).

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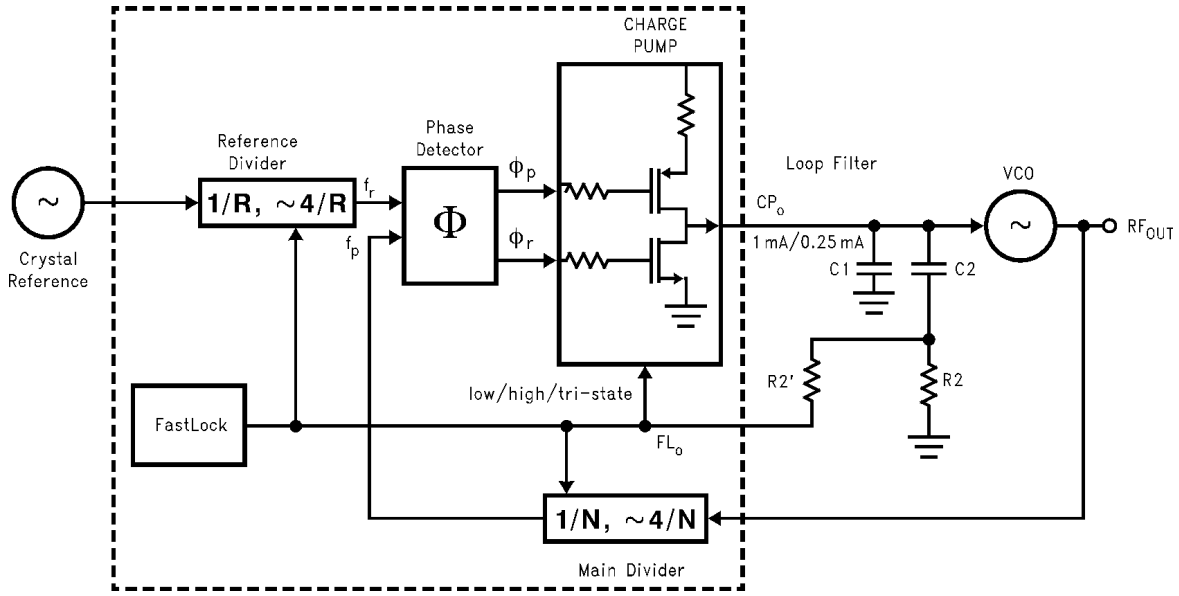


Table 5. FastLock Decoding

FastLock Status	F[8]	F[9]	F[10]	N[19](1)	FastLock State
FastLock Mode #1	1	0	0	1(1)	No Timeout Counter - 1X Divider
FastLock Mode #2	1	0	1	1	Timeout Counter - 1X Divider
FastLock Mode #3	1	1	0	1(1)	No Timeout Counter - 1/4X Divider
FastLock Mode #4	1	1	1	1	Timeout Counter - 1/4X Divider

(1) When the GO bit N[19] is set to one, the part is forced into the high gain mode. When the timeout counter is activated, termination of the counter cycle resets the GO bit to 0. If the timeout counter is not activated, N[19] must be reprogrammed to zero in order to remove the high gain state. See below for descriptions of each individual FastLock mode.

There are two techniques of switching in and out of FastLock. To program the device into any of the FastLock modes, the GO bit N[19] must be set to one to begin FastLock operation. In the first approach, the timeout counter can be used (FastLock 2 and 4) to stay in FastLock mode for a programmable number of phase detector reference cycles (up to 63) and then reset the GO bit automatically. In the second approach (FastLock 1 and 3) without the timeout counter, the PLL will remain in FastLock mode until the user resets the GO bit via the MICROWIRE serial bus. Once the GO bit is set to zero by the timeout counter or by MICROWIRE, the PLL will then return to normal operation. This transition does not effect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless transition between FastLock and standard mode.

FastLock Mode 1 In this mode, the output level of the FL_o is programmed in a low state while the ICP_o is in the 4x state. The device remains in this state until a command is received, resetting the N[19] bit to zero. Programming N[19] to zero will return the device to normal operation*., i.e., ICP_o = 1x and FL_o returned to Tri-state.

FastLock Mode 2 Identical to mode 1, except the switching of the device out of FastLock is controlled by the Timeout counter. The device will remain in FastLock until the timeout counter has counted down the appropriate number of phase detector cycles, at which time the PLL returns to normal operation*.

FastLock Mode 3 This mode is similar to mode 1 in that the output level of the FL_o is low and the ICP_o is switched to the 4x state. Additionally, the R and N divide ratios are reduced by one fourth during the transient, resulting in a 16x improved gain. As in mode 1, the device remains in this state until a MICROWIRE command is received, resetting the N[19] bit to zero and returning the device to normal operation*.

FastLock Mode 4 Identical to mode 3, except the switching of the device out of FastLock is controlled by the Timeout counter. The device will remain in FastLock until the timeout counter has counted down the appropriate number of phase detector cycles, at which time the PLL returns to normal operation*.

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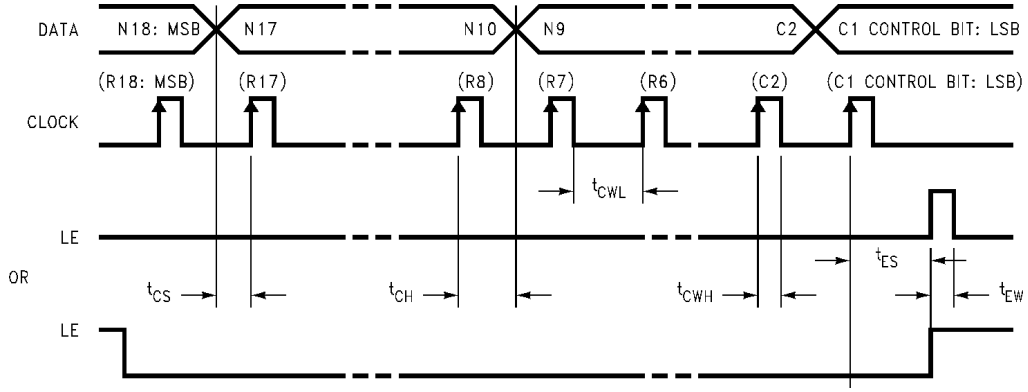
***Normal Operation** FastLock Normal Operation is defined as the device being in low current mode and standard divider values.

Table 6. FastLock Timeout Counter Value Programming

Timeout (# PD Cycles)(1)	3	7	11	15	19	23	27	31	35	•	59	63
F11 **(4)**	0	1	0	1	0	1	0	1	0	•	0	1
F12 **(8)**	0	0	1	1	0	0	1	1	0	•	1	1
F13 **(16)**	0	0	0	0	1	1	1	1	0	•	1	1
F14 **(32)**	0	0	0	0	0	0	0	0	1	•	1	1

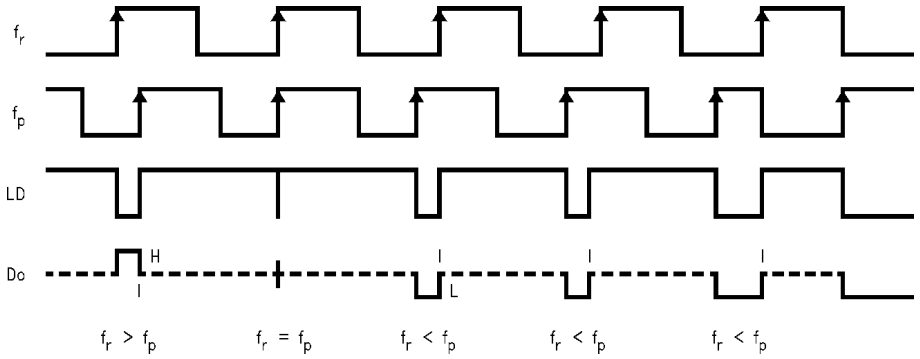
(1) The timeout counter decrements after each phase detector comparison cycle.

SERIAL DATA INPUT TIMING



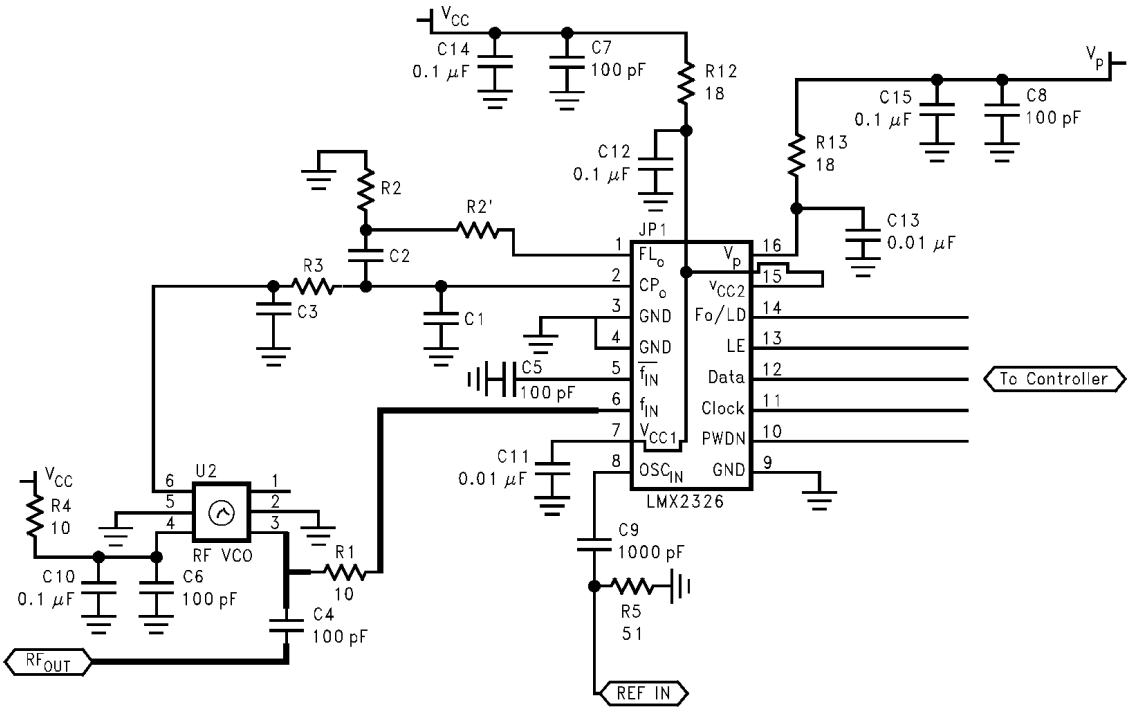
Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.
TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC/2}$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 1.84V @ V_{CC} = 2.3V and 4.4V @ V_{CC} = 5.5V.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



Phase difference detection range: −2π to +2π
The Phase Detector Polarity F[6] = HIGH
The minimum width pump up and pump down current pulses occur at the ICP_o pin when the loop is locked.

TYPICAL APPLICATION EXAMPLE



OPERATIONAL NOTES:

*VCO is assumed AC coupled.

**R1 increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

**50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See Figure 4 below.)

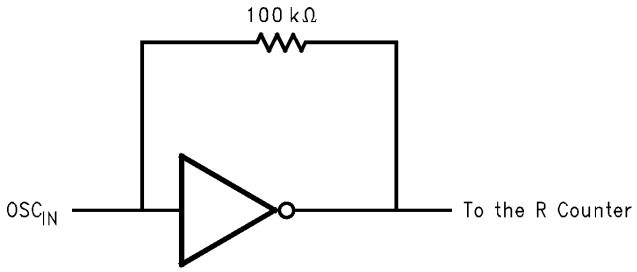


Figure 4.

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APPLICATION INFORMATION

DEVICE PROGRAMMING AFTER FIRST APPLYING V_{cc}

Three MICROWIRE programming methods can be used to change the function latch, R counter latch, and N counter latch contents with close phase alignment of R and N counters to minimize lock up time after the cold power up.

INITIALIZATION SEQUENCE METHOD

Loading the function latch with [C1, C2] = [1, 1] immediately followed by an R counter load, then an N counter load, efficiently programs the MICROWIRE. Loading the function latch with [C1, C2] = [1, 1] programs the same function latch as a load with [C1, C2] = [0, 1] and additionally provides an internal reset pulse described below. This program sequence insures that the counters are at load point when the N counter data is latched in and the part will begin counting in close phase alignment.

The following results from latching the MICROWIRE with an F latch word, [C1, C2] = [1, 1]:

- The function latch contents are loaded.
- An internal pulse resets the R, N, and timeout counters to load state conditions and will tri-state the charge pump. If the function latch is programmed for the synchronous powerdown case; CE = HIGH, F[2] = HIGH, F[18] = HIGH, this internal pulse triggers powerdown. Refer to Powerdown Operation section for a synchronous powerdown description. Note that the prescaler bandgap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N counter data after the initialization word will activate the same internal reset pulse. Successive N counter data loads without an initialization load will not trigger the internal reset pulse.

CE METHOD

Programming the function latch, R counter latch and N counter latch while the part is being held in a powerdown state by CE allows lowest possible power dissipation. After the MICROWIRE contents have been programmed and the part is enabled, the R and N counter contents will resume counting in close phase alignment. Note that after CE transitions from LOW to HIGH, a duration of 1 µs may be required for the prescaler bandgap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the part up and down by pin control in order to check for channel activity. The MICROWIRE does not need to be reprogrammed each time the part is enabled and disabled as long as it has been programmed at least once after V_{CC} was applied.

COUNTER RESET METHOD

This MICROWIRE programming method consists of a function latch load, [C1, C2] = [0, 1], enabling the counter reset bit, F[1]. The R and N counter latches are then loaded followed by a final function latch load that disables the counter reset. This provides the same close phase alignment as the initialization sequence method with direct control over the internal reset. Note that counter reset holds the counters at load point and will tri-state the charge pump, but does not trigger synchronous powerdown. The counter reset method requires an extra function latch load compared to the initialization sequence method.

DEVICE PROGRAMMING

When programming the LMX2306, LMX2316, and LMX2326, first determine the frequencies and mode of operation desired. Data register is programmed with a 21-bit data stream shifted into the R counter, N counter, or the F latch. The Functional Description section shows the bits for the R counter, and the corresponding information for the N counter. The FL_0 programming information is given in the FUNCTION AND INITIALIZATION LATCHES section. Typical numbers for a GSM application example are given. In the example, the RF output is locking at 950 MHz (f_{vco}) with a 200 kHz channel spacing ($f_{comparison}$). The crystal oscillator reference input is 10 MHz (f_{osc}) and the prescaler value (P) is 32. An example of both methods of FastLock will be shown.

The last two bits (control bits C1 and C2) of each bit stream identify which counter or FL_0 mode will be programmed. For example, to program the R counter, C1 and C2 will be 0,0. Immediately proceeding these two bits is the N, R, or F bits providing the divide ratios and FastLock mode information.

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Control Bits		DATA Location
C1	C2	
0	0	R Counter
1	0	N Counter
0	1	Function Latch
1	1	Initialization

For example, to load the N counter, the last two bits C1 and C2 must be 10.

Once the control bits have been determined, the frequency information must be determined. To begin, determine the N and R counter values as follows:

$$N = f_{vco}/f_{comparison} \quad (5)$$

and

$$R = f_{osc}/f_{comparison} \quad (6)$$

For this example R and N are determined as follows:

$$R = 10\ MHz/200\ kHz = 50 \quad (7)$$

and

$$N = 950\ MHz/200\ kHz = 4750 \quad (8)$$

N COUNTER

The calculated value of N, and the value of P are now used to determine the values of A and B where A and B are both integer values:

$$N = P * B + A$$

where

- B is the divisor
- A is the remainder (9)

Therefore:

$$B = div\ (N/P) \quad (10)$$

and

$$A = N - (B * P) \quad (11)$$

For this example, B and A are calculated as follows:

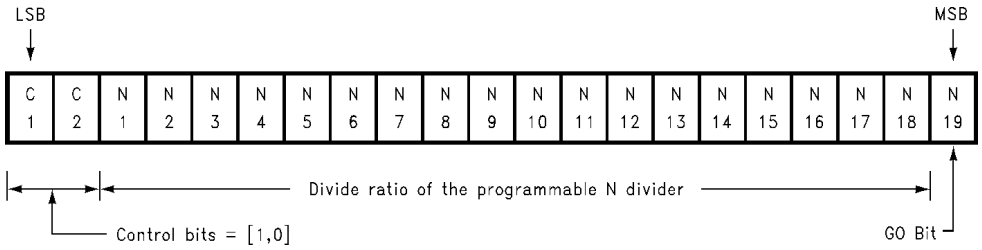
$$B = div\ (4750/32) = 148 = 0000010010100 \quad (12)$$

and

$$A = 4750 - (148 * 32) = 14 = 01110 \quad (13)$$

To load the N counter with these values, the programming bit stream would be as follows. The first bit, the GO bit, (MSB) N[19] is used for FastLock operation and will be discussed in the F LATCH section. The next 13 bits, (N[18]–N[6]) shifted in, are the B counter value, 0000010010100_b*. Bits N[5]–N[1] are the A counter and are 01110_b in this example. The final two bits (the control bits) are 1,0 identifying the N counter. In programming the N counter, the value of B must be greater than or equal to A, and the value of B must be greater than or equal to 3.

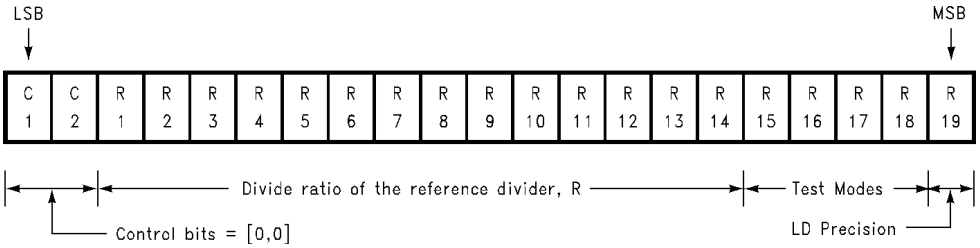
Note: *In programming the counter, data is shifted in MSB first.



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R COUNTER

Programming the R counter is done by shifting in the binary value of R calculated previously (50_d = 110010_b). The first bit shifted in is R[19] the LD precision bit. The next 4 bits (R[18]–R[15]) shifted in, are used for testing and should always be loaded with zeros. The R[14]–R[1] bits are used to program the reference divider ratio and should be 00000000110010_b for this example. The final two bits, C[1] and C[2] denote the R counter and should be 0, 0. The resulting bit stream looks as follows:

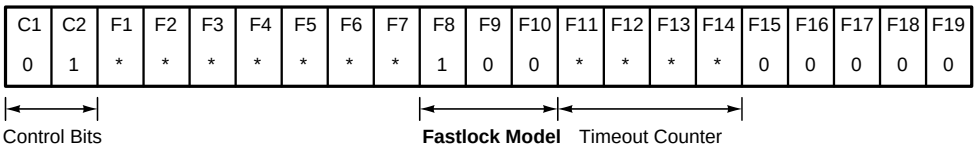


F LATCH

To program the device for any of the FastLock modes, C[1] = 0 and C[2] = 1 which direct data to the F latch. The FUNCTION AND INITIALIZATION LATCHES section discusses the 4 modes of FastLock operation. The user must first determine which FastLock mode will be used. When using any of the FastLock modes, the programmer needs to experimentally determine the length of time to stay in high gain mode. This is done by looking at the transient response and determining the time at which the device has settled to within the appropriate frequency tolerance. FastLock mode should be terminated just prior to “lock” to place the switching phase glitch within the transient settling time. The counter reset mode (F[1] bit) holds both the N and R counters at load point when F[1] = HIGH. Upon setting F[1] = LOW, the N and R counters will resume counting in close phase alignment. Other functions of the F latch such as FoLD output control, Phase detector polarity, and charge pump tri-state are defined in the FUNCTION AND INITIALIZATION LATCHES section also.

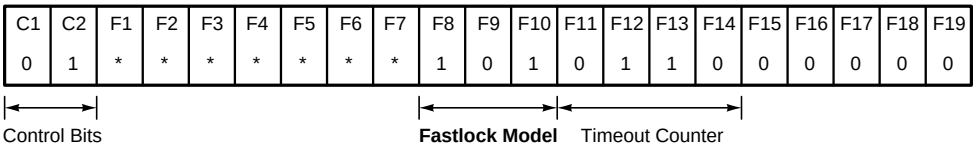
FastLock MODE 1 PROGRAMMING

The F[1]–F[7] bits will be denoted as (*) and are dependent on the desired modes of the applicable functions. To program the device for mode 1 FastLock, the F[8]–F[10] bits are programmed 100, while the N[19] bit is set to 1. The device will stay in the 4X current mode until another N bit stream is sent with the N[19] bit reset to 0. This gives a bit stream as follows:



FastLock MODE 2 PROGRAMMING

Again, the F[1]–F[7] bits will be denoted as don't care (*) but are dependent on the desired modes of the applicable functions. To program the device for mode 2 FastLock, the F[8]–F[10] bits are programmed 101, while the N[19] bit is set to 1. The device will stay in the 4X current mode for the programmed number of phase detector cycles. Bits F[11]–F[14] program this number of cycles and are shown in Table 6. For our example, we will use 27 phase detector cycles, i.e. bits F[11]–F[14] will be 0110_b. After 27 phase detector cycles, the N[19] bit returns to zero, bringing the device back to low current mode. The resulting bit stream is as follows:



*FastLock modes 3 and 4 are programmed in the same manner and give the added 4X gain increase as discussed in FastLock Modes.

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REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	17

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