LP295x-N Series of Adjustable Micropower Voltage Regulators

1 Features

- Input Voltage Range: 2.3 V to 30 V
- 5-V, 3-V, and 3.3-V Output Voltage Versions Available
- High Accuracy Output Voltage
- Ensured 100-mA Output Current
- Extremely Low Quiescent Current
- Low Dropout Voltage
- Extremely Tight Load and Line Regulation
- Very Low Temperature Coefficient
- Use as Regulator or Reference
- Needs Minimum Capacitance for Stability
- Current and Thermal Limiting
- Stable With Low-ESR Output Capacitors (10 mΩ to 6 Ω)
- LP2951-N Versions Only:
  - $\overline{\text{Error}}$ Flag Warns of Output Dropout
  - Logic-Controlled Electronic Shutdown
  - Output Programmable From 1.24 V to 29 V

2 Applications

- High-Efficiency Linear Regulator
- Regulator with Undervoltage Shutdown
- Low Dropout Battery-powered Regulator
- Snap-ON/Snap-OFF Regulator

3 Description

The LP2950-N and LP2951-N are micropower voltage regulators with very low quiescent current (75 µA typical) and very low dropout voltage (typical 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the device increases only slightly in dropout, prolonging battery life.

Careful design of the LP2950-N/LP2951-N has minimized all contributions to the error budget. This includes a tight initial tolerance (0.5% typical), extremely good load and line regulation (0.05% typical) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

One such feature is an $\overline{\text{error}}$ flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5-V, 3-V, or 3.3-V output (depending on the version), or programmed from 1.24 V to 29 V with an external pair of resistors.

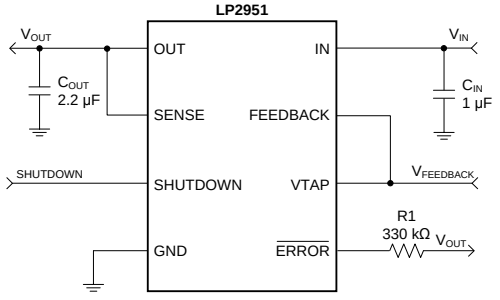
The LP2950-N is available in the surface-mount TO-252 package and in the popular 3-pin TO-92 package for pin-compatibility with older 5-V regulators. The 8-pin LP2951-N is available in plastic, ceramic dual-in-line, WSON, or metal can packages and offers additional system functions.

Device Information[1]

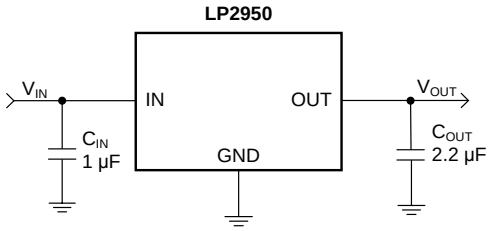
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2950-N	TO-92 (3)	4.30 mm × 4.30 mm
	TO-252 (3)	9.91 mm × 6.58 mm
LP2951-N	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	4.00 mm × 4.00 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

LP2951 Simplified Schematic



LP2950-N Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Voltage Options ... 3
6 Pin Configuration and Functions ... 4
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information: LP2950-N ... 6
7.5 Thermal Information: LP2951-N ... 6
7.6 Electrical Characteristics ... 7
7.7 Typical Characteristics ... 10
8 Detailed Description ... 16
8.1 Overview ... 16
8.2 Functional Block Diagrams ... 16
8.3 Feature Description ... 17
8.4 Device Functional Modes ... 18
9 Application and Implementation ... 19
9.1 Application Information ... 19
9.2 Typical Applications ... 20
10 Power Supply Recommendations ... 32
11 Layout ... 32
11.1 Layout Guidelines ... 32
11.2 Layout Example ... 32
11.3 WSON Mounting ... 33
12 Device and Documentation Support ... 34
12.1 Documentation Support ... 34
12.2 Related Links ... 34
12.3 Community Resources ... 34
12.4 Trademarks ... 34
12.5 Electrostatic Discharge Caution ... 34
12.6 Glossary ... 34
13 Mechanical, Packaging, and Orderable Information ... 34

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (May 2016) to Revision Q — **Page**

- Changed LP2951-N ESD parameter pin references and added SENSE pin row to LP2951-N ESD parameter in *ESD Ratings* table ... 5

Changes from Revision O (December 2014) to Revision P — **Page**

- Added rows to *ESD Ratings* table to differentiate values for pins 3 and 7 of the LP2951-N device ... 5
- Added footnotes 2 and 3 to both *Thermal Information* tables ... 6

Changes from Revision N (May 2013) to Revision O — **Page**

- Added *Device Information* and *ESD Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section; update pin names; change package nomenclature from National to TI ... 1

Changes from Revision M (April 2013) to Revision N — **Page**

- Changed layout of National Data Sheet to TI format ... 1

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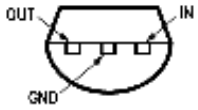
5 Voltage Options

DEVICE NUMBER	PACKAGE	VOLTAGE OPTION (V)
LP2950-N	TO-92 (LP)	3 (±0.5%, ±1 %)
		3.3 (±0.5%, ±1 %)
		5 (±0.5%, ±1 %)
	TO-252 (NDP)	3 (±1 %)
		3.3 (±1%)
		5 (±1%)
LP2951-N	SOIC (D)	3 (±0.5%, ±1%)
		3.3 (±0.5%, ±1%)
		5 (±0.5%, ±1%)
	VSSOP (DGK)	3 (±0.5%, ±1%)
		3.3 (±0.5%, ±1%)
		5 (±0.5%, ±1%)
	WSON (NGT)	3 (±0.5%, ±1%)
		3.3 (±0.5%, ±1%)
		5 (±0.5%, ±1%)
	PDIP (P)	5 (±0.5%, ±1%)

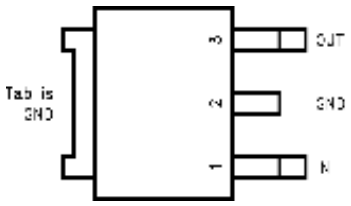
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6 Pin Configuration and Functions

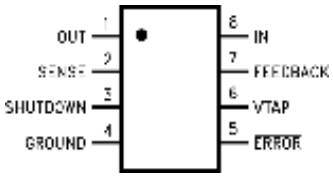
LP Package
3-Pin TO-92
Bottom View



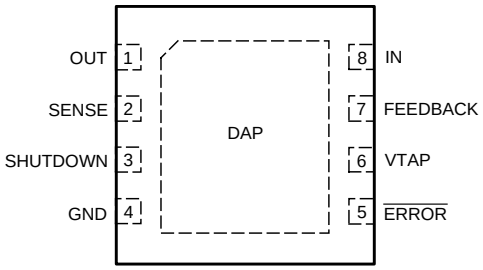
NDP Package
3-Pin TO-252
Front View



P, D, DGK Packages
8-Pin PDIP, SOIC, VSSOP
Top View



NGT Package
8-Pin WSON
Top View



Connect DAP to GND at device pin 4.

Pin Functions: LP2950-N

PIN			I/O	DESCRIPTION
NAME	LP2950			
	LP	NDP		
GND	2	2	—	Ground
IN	3	1	I	Input supply voltage
OUT	1	3	O	Regulated output voltage

Pin Functions: LP2951-N

PIN			I/O	DESCRIPTION
NAME	LP2951			
	D, DGK, P	NGT		
$\overline{\text{ERROR}}$	5	5	O	Error output
FEEDBACK	7	7	I	Voltage feedback input
GROUND	4	4	—	Ground
IN	8	8	I	Input supply voltage
OUT	1	1	O	Regulated output voltage
SENSE	2	2	I	Output voltage sense
SHUTDOWN	3	3	I	Disable device
VTAP	6	6	O	Internal resistor divider

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input supply voltage - SHUTDOWN input voltage error comparator output voltage(3)		–0.3	30	V
FEEDBACK input voltage(3)(4)		–1.5	30	V
Power dissipation			Internally Limited	
Junction temperature, T_J			150	°C
Soldering dwell time, temperature	Wave		4 seconds, 260	°C
	Infrared		10 seconds, 240	°C
	Vapor phase		75 seconds, 219	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) May exceed input supply voltage.
(4) When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

7.2 ESD Ratings

				VALUE	UNIT
LP2950-N					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2500	V
LP2951-N					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	IN, OUT, GND, $\overline{\text{ERROR}}$	±2500	V
			SHUTDOWN	±2000	
			SENSE	±1500	
			VTAP, FEEDBACK	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum input supply voltage			30	V
Junction temperature, T_J(2)	LP2950AC-XX, LP2950C-XX	–40	125	°C
	LP2951	–55	150	°C
	LP2951AC-XX, LP2951C-XX	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The junction-to-ambient thermal resistances are as follows: 157.4°C/W for the TO-92 (LP) package, 51.3°C/W for the TO-252 (NDP) package, 56.3°C/W for the molded PDIP (P), 117.7°C/W for the molded plastic SOIC (D), 171°C/W for the molded plastic VSSOP (DGK). The above thermal resistances for the P, D, and DGK packages apply when the package is soldered directly to the PCB. The value of $R_{\theta JA}$ for the WSON (NGT) package is typically 43.3°C/W but is dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For details of thermal resistance and power dissipation for the WSON package, see *AN-1187 Leadless Leadframe Package (LLP)*.

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7.4 Thermal Information: LP2950-N

THERMAL METRIC[1]		LP2950-N		UNIT
		LP (TO-92)	NDP (TO-252)	
		3 PINS	3 PINS	
$R_{\theta JA}$[2]	Junction-to-ambient thermal resistance, High-K	157.4	51.3[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.2	53.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	153.6	30.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.2	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	n/a	30	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the TO-252 (NDP) package $R_{\theta JA}$ includes twelve (12) thermal vias under the tab per EIA/JEDEC JESD51-5.

7.5 Thermal Information: LP2951-N

THERMAL METRIC[1]		LP2951-N				UNIT
		P (PDIP)	D (SOIC)	DGK (VSSOP)	NGT (WSON)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$[2]	Junction-to-ambient thermal resistance, High K	56.3	117.7	171.0	43.3[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	63.7	62.3	35.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.5	57.9	91.4	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.9	15.9	8.9	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.3	57.5	90.1	20.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	9.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the WSON (NGT) package $R_{\theta JA}$ includes six (6) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

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7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(1)	LP2951(2)			LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
3-V VERSIONS(3)											
Output voltage	T_J = 25°C	2.985	3	3.015	2.985	3	3.015	2.970	3	3.030	V(4)
	−25°C ≤ T_J ≤ 85°C				2.970	3	3.030	2.955	3	3.045	V(5)
	Full operating temperature range	2.964	3	3.036							V(4)
					2.964	3	3.036	2.940	3	3.060	V(5)
Output voltage	100 µA ≤ I_L ≤ 100 mA, 100 µA ≤ I_L ≤ 100 mA, T_J ≤ T_{JMAX}	2.955	3	3.045							V(4)
					2.958	3	3.042	2.928	3	3.072	V(5)
3.3-V VERSIONS(3)											
Output voltage	T_J = 25°C	3.284	3.3	3.317	3.284	3.3	3.317	3.267	3.3	3.333	V(4)
	−25°C ≤ T_J ≤ 85°C		3.3		3.267	3.3	3.333	3.251	3.3	3.350	V(5)
	Full operating temperature range	3.260	3.3	3.340							V(4)
					3.260	3.3	3.340	3.234	3.3	3.366	V(5)
Output voltage	100 µA ≤ I_L ≤ 100 mA, T_J ≤ T_{JMAX}	3.251	3.3	3.350							V(4)
					3.254	3.3	3.346	3.221	3.3	3.379	V(5)
5-V VERSIONS(3)											
Output voltage	T_J = 25°C	4.975	5	5.025	4.975	5	5.025	4.95	5	5.05	V(4)
	−25°C ≤ T_J ≤ 85°C		5		4.95	5	5.05	4.925	5	5.075	V(5)
	Full operating temperature range	4.94	5	5.06							V(4)
					4.94	5	5.06	4.9	5	5.1	V(5)
Output voltage	100 µA ≤ I_L ≤ 100 mA, T_J ≤ T_{JMAX}	4.925	5	5.075							V(4)
					4.925	5	5.075	4.88	5	5.12	V(5)
ALL VOLTAGE OPTIONS											
Output voltage temperature coefficient	See(6), –40°C ≤ T_J ≤ 125°C		20	120							ppm/°C(4)
						20	100		50	150	ppm/°C(5)
Line regulation(7)	(V_ONOM + 1 V) ≤ V_{in} ≤ 30 V(8)		0.03%	0.1%		0.03%	0.11%		0.04%	0.2%	See(4)
	(V_ONOM + 1 V) ≤ V_{in} ≤ 30 V(8), –40°C ≤ T_J ≤ 125°C		0.03%	0.5%							See(4)
						0.03%	0.2%		0.04%	0.4%	(5)
Load regulation(7)	100 µA ≤ I_L ≤ 100 mA		0.04%	0.1%		0.04%	0.1%		0.1%	0.2%	See(4)
	100 µA ≤ I_L ≤ 100 mA, –40°C ≤ T_J ≤ 125°C		0.04%	0.3%							See(4)
						0.04%	0.2%		0.1%	0.3%	See(5)

(1) Unless otherwise noted, all limits apply for T_A = T_J = 25°C as well as specified for V_{IN} = (V_ONOM + 1 V), I_L = 100 µA and C_L = 1 µF for 5-V versions and 2.2 µF for 3-V and 3.3-V versions. Additional conditions for the 8-pin versions are FEEDBACK tied to VTAP, OUTPUT tied to SENSE, and $V_{SHUTDOWN}$ ≤ 0.8 V.
(2) A Military RETS specification is available on request.
(3) All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3-V and 3.3-V versions are designated by the last two digits, but the 5-V version is denoted with no code at this location of the part number (refer to the *Package Option Addendum* at end of data sheet).
(4) Ensured and 100% production tested.
(5) Ensured but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
(6) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(7) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(8) Line regulation for the LP2951-N is tested at 150°C for I_L = 1 mA. For I_L = 100 µA and T_J = 125°C, line regulation is specified by design to 0.2%. See *Typical Characteristics* for line regulation versus temperature and load current.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(1)	LP2951(2)			LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Dropout voltage(9)	I_L = 100 µA		50	80		50	80		50	80	mV(4)
	I_L = 100 µA, –40°C ≤ T_J ≤ 125°C			150							mV(4)
							150			150	mV(5)
	I_L = 100 mA		380	450		380	450		380	450	mV(4)
	I_L = 100 mA, –40°C ≤ T_J ≤ 125°C			600			600			600	mV(4)
							600			600	mV(5)
Ground current	I_L = 100 µA		75	120		75	120		75	120	µA(4)
	I_L = 100 µA, –40°C ≤ T_J ≤ 125°C			140							µA(4)
							140			140	µA(5)
	I_L = 100 mA		8	12		8	12		8	12	mA(4)
	I_L = 100 mA, –40°C ≤ T_J ≤ 125°C			14							mA(4)
							14			14	mA(5)
Dropout ground current	V_{IN} = (V_ONOM − 0.5)V, I_L = 100 µA		110	170		110	170		110	170	µA(4)
	V_{IN} = (V_ONOM − 0.5 V), I_L = 100 µA, –40°C ≤ T_J ≤ 125°C			200			200			200	µA(4)
							200			200	µA(5)
Current limit	V_{OUT} = 0 V		160	200		160	200		160	200	mA(4)
	V_{OUT} = 0 V, –40°C ≤ T_J ≤ 125°C			220							mA(4)
							220			220	mA(5)
Thermal regulation	See(10)		0.05	0.2		0.05	0.2		0.05	0.2	%/W(4)
Output noise 10 Hz to 100 kHz	C_L = 1µF (5 V Only)		430			430			430		$µV_{RMS}$
	C_L = 200 µF		160			160			160		$µV_{RMS}$
	C_L = 3.3 µF (Bypass = 0.01 µF Pins 7 to 1 (LP2951-N)		100			100			100		$µV_{RMS}$
8-PIN VERSIONS ONLY		**LP2951**			**LP2951AC-XX**			**LP2951C-XX**			
Reference voltage		1.22	1.235	1.25	1.22	1.235	1.25	1.21	1.235	1.26	V(4)
	–40°C ≤ T_J ≤ 125°C	1.2		1.26							V(4)
					1.2		1.26 1	1.2		1.27	V(5)
Reference voltage	See(11), –40°C ≤ T_J ≤ 125°C	1.19		1.27							V(4)
					1.19		1.27	1.185		1.285	V(5)
Feedback pin bias current			20	40		20	40		20	40	nA(4)
	–40°C ≤ T_J ≤ 125°C			60							nA (4)
							60			60	nA(5)
Reference voltage temperature coefficient	See(6)		20			20			50		ppm/°C
Feedback pin bias current temperature coefficient			0.1			0.1			0.1		nA/°C

(9) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1-V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2 V (2.3 V over temperature) must be taken into account.

(10) Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30 V (1.25-W pulse) for T = 10 ms.

(11) $V_{REF} \le V_{OUT} \le (V_{IN} - 1\ V)$, 2.3 V ≤ V_{IN} ≤ 30 V, 100 µA ≤ I_L ≤ 100 mA, $T_J \le T_{JMAX}$.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS(1)	LP2951(2)			LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ERROR COMPARATOR											
Output leakage current	V_{OH} = 30 V		0.01	1		0.01	1		0.01	1	µA(4)
	V_{OH} = 30 V, –40°C ≤ T_J ≤ 125°C			2							µA(4)
							2			2	µA(5)
Output low voltage	V_{IN} = (V_ONOM − 0.5 V), I_{OL} = 400 µA		150	250		150	250		150	250	mV(4)
	V_{IN} = (V_ONOM − 0.5 V), I_{OL} = 400 µA, –40°C ≤ T_J ≤ 125°C			400			400			400	mV(4)
							400			400	mV(5)
Upper threshold voltage	See(12)	40	60		40	60		40	60		mV(4)
	See(12), –40°C ≤ T_J ≤ 125°C	25									mV(4)
					25			25			mV(5)
Lower threshold voltage	See(12)		75	95		75	95		75	95	mV(4)
	See(12), –40°C ≤ T_J ≤ 125°C			140							mV(4)
							140			140	mV(5)
Hysteresis	See(12)		15			15			15		mV
SHUTDOWN INPUT											
Input			1.3			1.3			1.3		V
Logic voltage	Low (Regulator ON), –40°C ≤ T_J ≤ 125°C			0.6							V(4)
							0.7			0.7	V(5)
Logic voltage	High (Regulator OFF), –40°C ≤ T_J ≤ 125°C	2									V(4)
					2			2			V(5)
Shutdown pin input current	$V_{shutdown}$ = 2.4 V		30	50		30	50		30	50	µA(4)
	$V_{shutdown}$ = 2.4 V –40°C ≤ T_J ≤ 125°C			100							µA(4)
							100			100	µA(5)
	$V_{shutdown}$ = 30 V		450	600		450	600		450	600	µA(4)
	$V_{shutdown}$ = 30 V, –40°C ≤ T_J ≤ 125°C			750							µA(4)
							750			750	µA(5)
Regulator output current in shutdown	See(13)		3	10		3	10		3	10	µA(4)
	–40°C ≤ T_J ≤ 125°C			20							µA(4)
							20			20	µA(5)

(12) Comparator thresholds are expressed in terms of a voltage differential at the FEEDBACK pin below the nominal reference voltage measured at V_{IN} = ($V_{O(NOM)}$ + 1) V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2) / R2.For example, at a programmed output voltage of 5 V, the $\overline{\text{ERROR}}$ output is specified to go low when the output drops by 95 mV × 5 V / 1.235 V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% ensured.

(13) $V_{SHUTDOWN}$ ≥ 2 V, V_{IN} ≤ 30 V, V_{OUT} = 0, FEEDBACK pin tied to V_{TAP}.

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7.7 Typical Characteristics

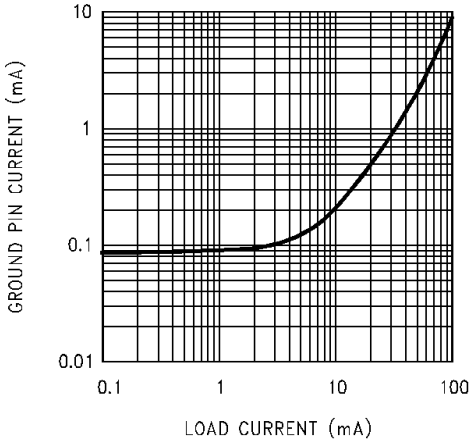


Figure 1. Quiescent Current

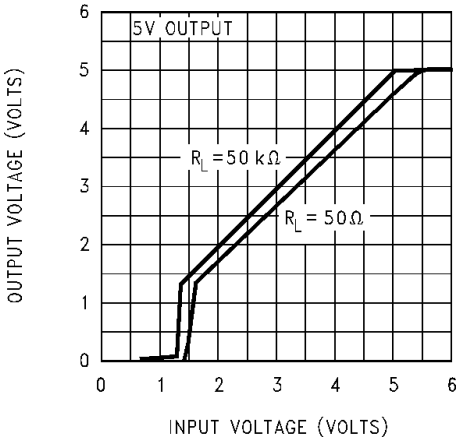


Figure 2. Dropout Characteristics

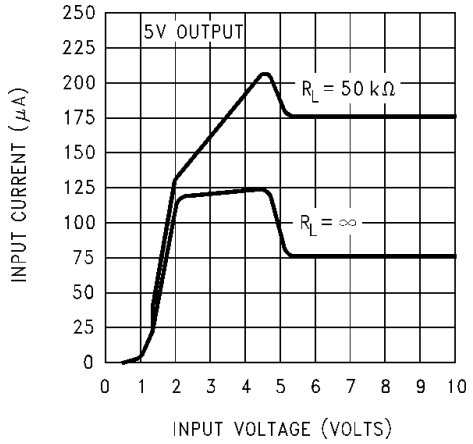


Figure 3. Input Current

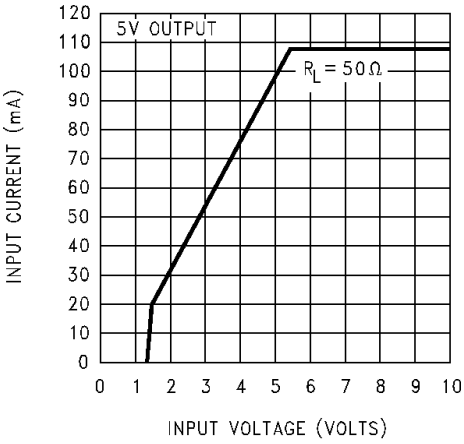


Figure 4. Input Current

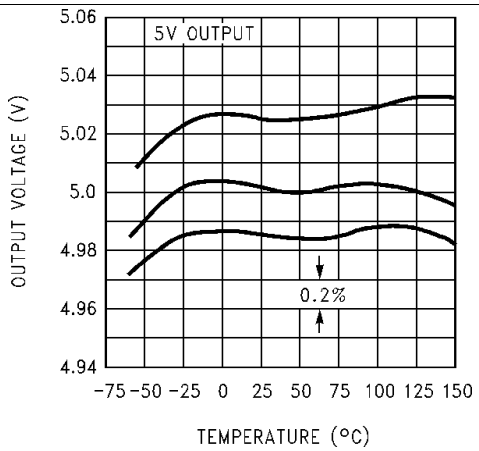


Figure 5. Output Voltage vs. Temperature of 3 Representative Units

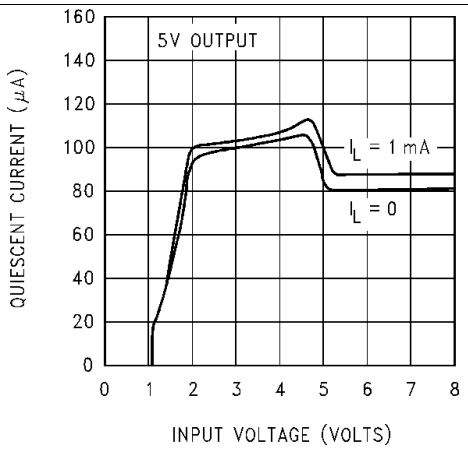


Figure 6. Quiescent Current

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Typical Characteristics (continued)

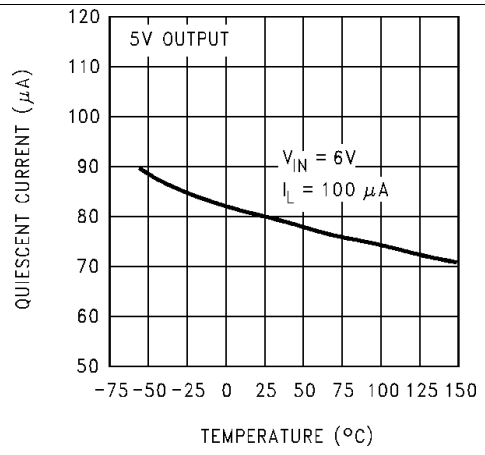


Figure 7. Quiescent Current

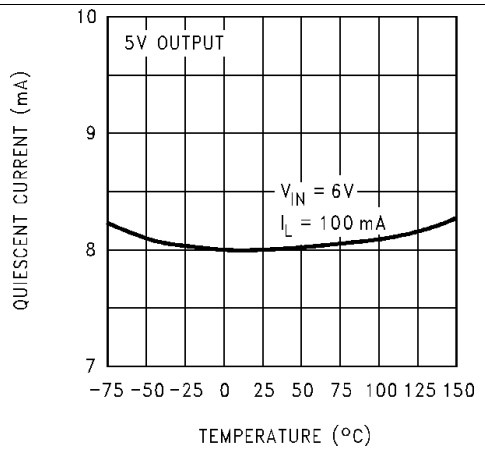


Figure 8. Quiescent Current

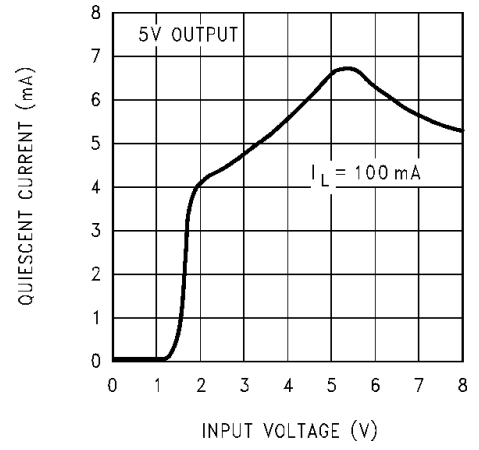


Figure 9. Quiescent Current

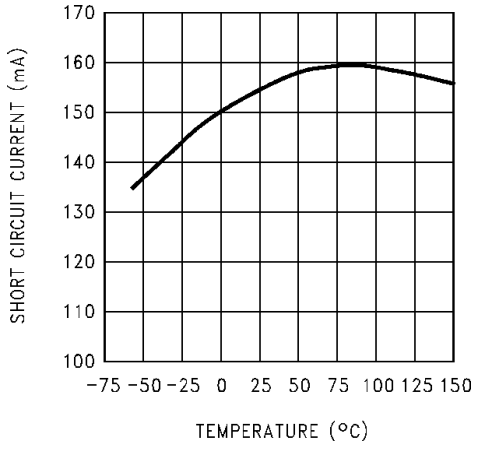


Figure 10. Short Circuit Current

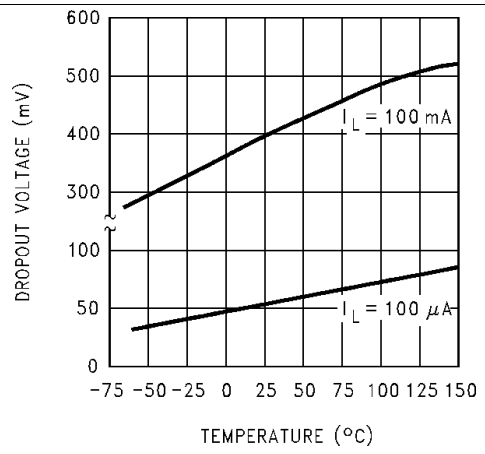


Figure 11. Dropout Voltage

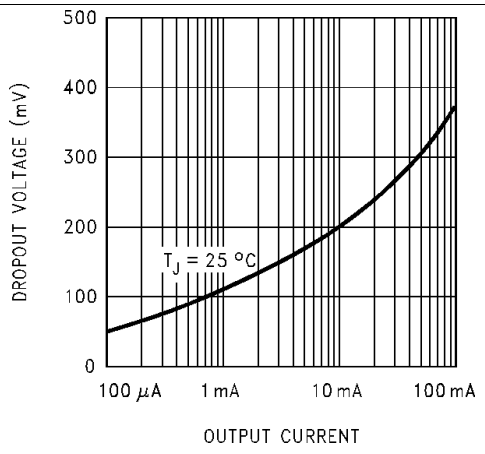


Figure 12. Dropout Voltage

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Typical Characteristics (continued)

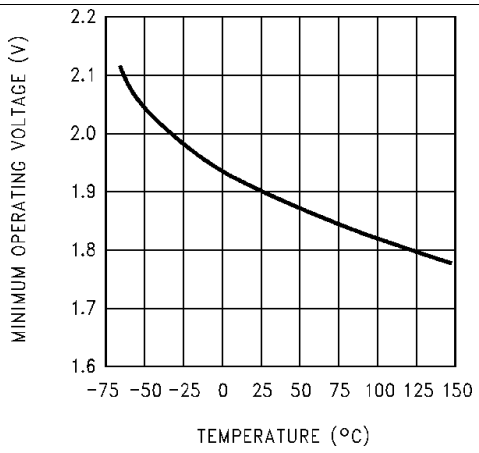


Figure 13. LP2951-N Minimum Operating Voltage

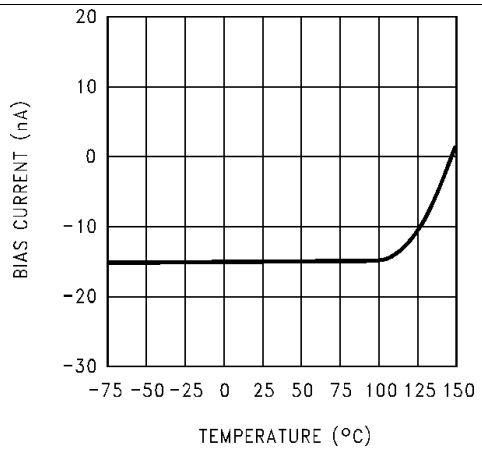


Figure 14. LP2951-N Feedback Bias Current

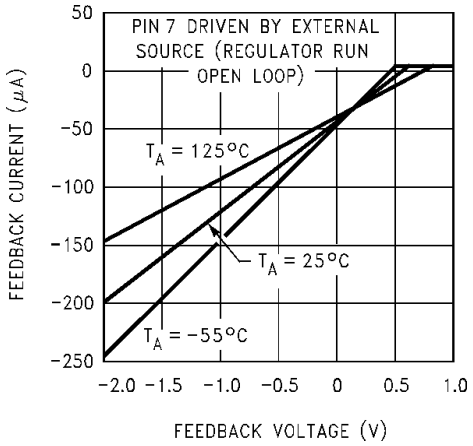


Figure 15. LP2951-N Feedback Pin Current

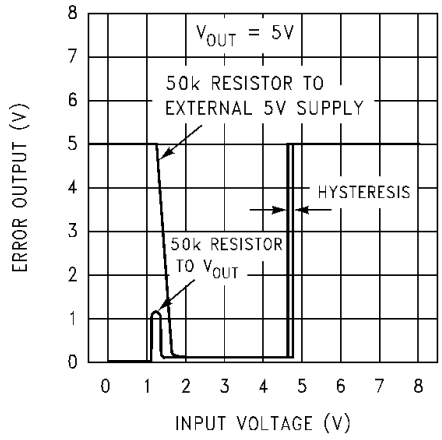


Figure 16. LP2951-N Error Comparator Output

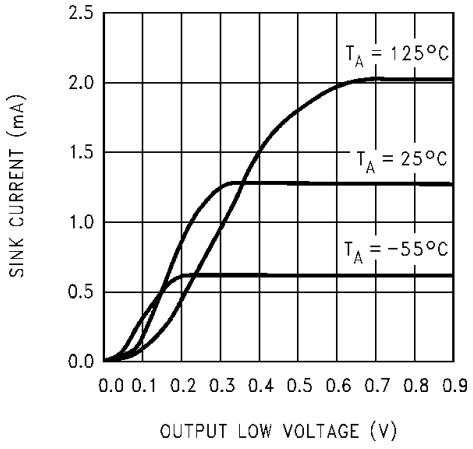


Figure 17. LP2951-N Comparator Sink Current

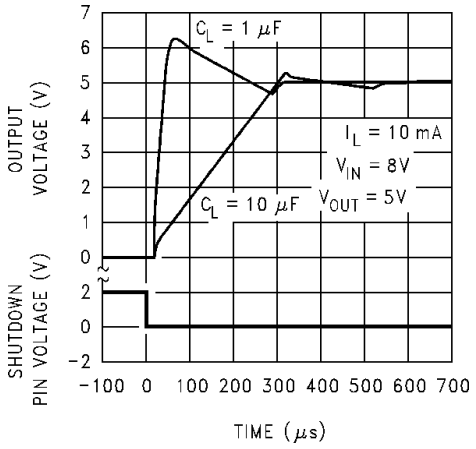


Figure 18. LP2951-N Enable Transient

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Typical Characteristics (continued)

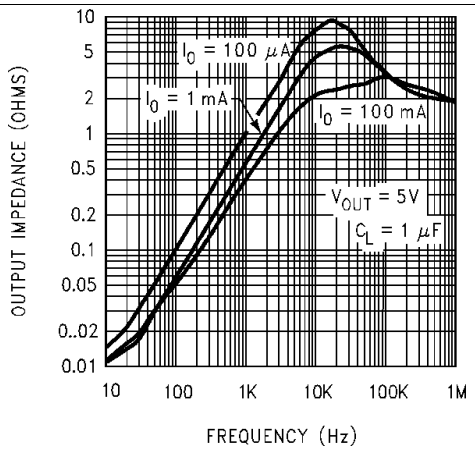


Figure 19. Output Impedance

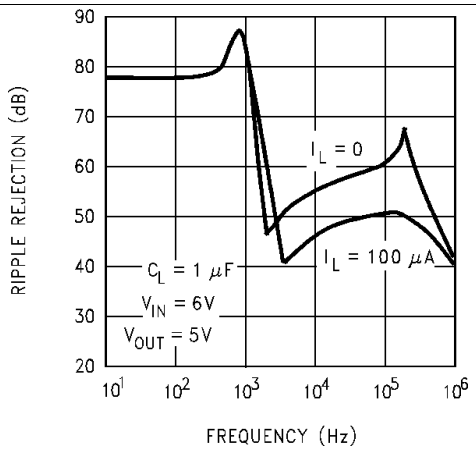


Figure 20. Ripple Rejection

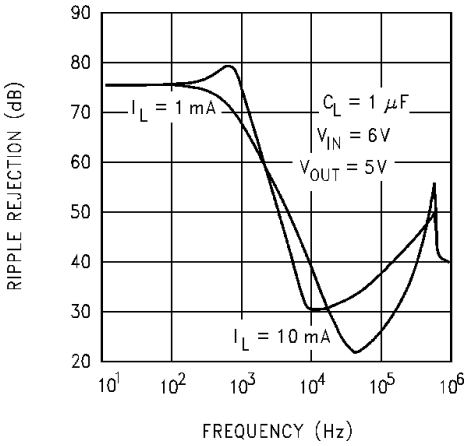


Figure 21. Ripple Rejection

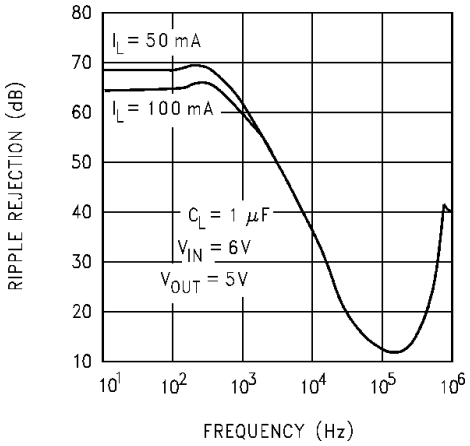


Figure 22. Ripple Rejection

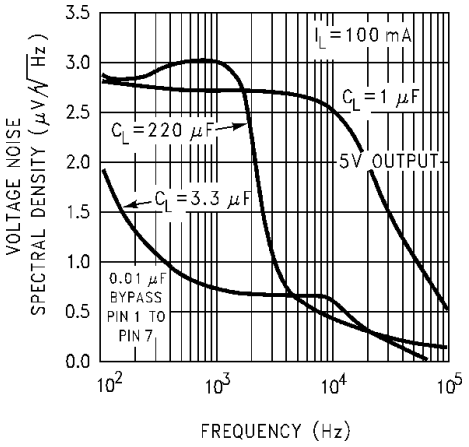


Figure 23. LP2951-N Output Noise

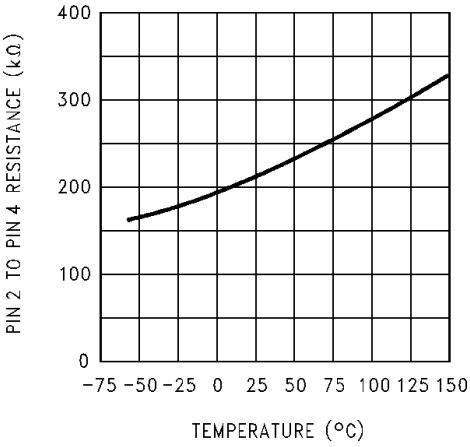


Figure 24. LP2951-N Divider Resistance

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Typical Characteristics (continued)

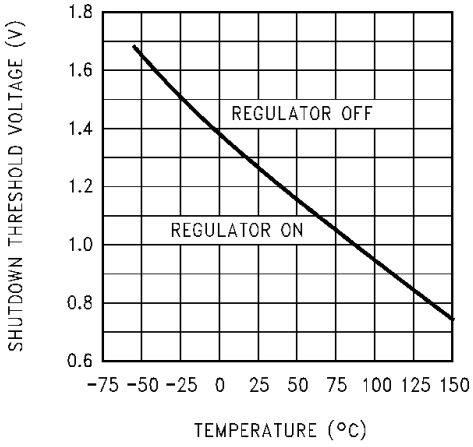


Figure 25. Shutdown Threshold Voltage

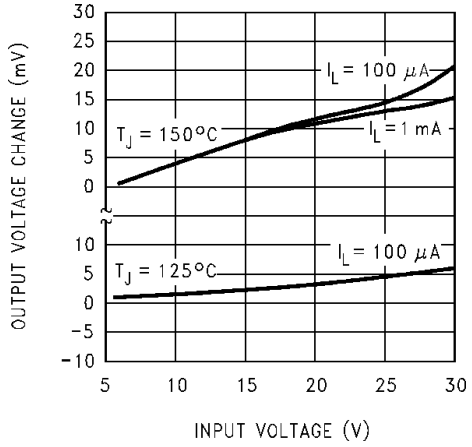


Figure 26. Line Regulation

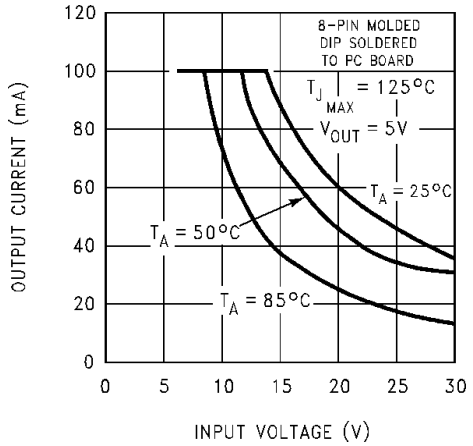


Figure 27. LP2951-N Maximum Rated Output Current

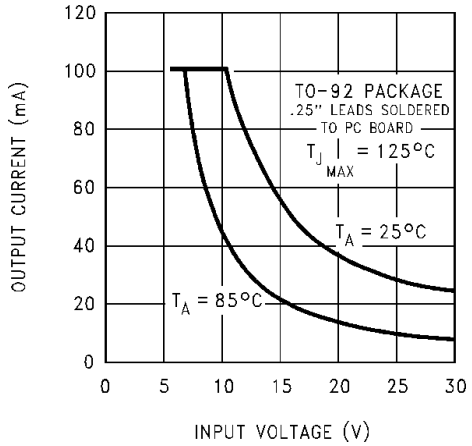


Figure 28. LP2950-N Maximum Rated Output Current

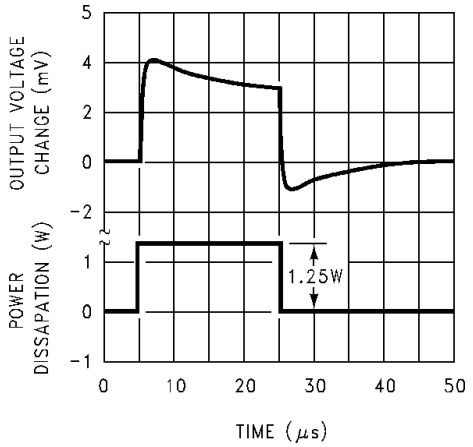


Figure 29. Thermal Response

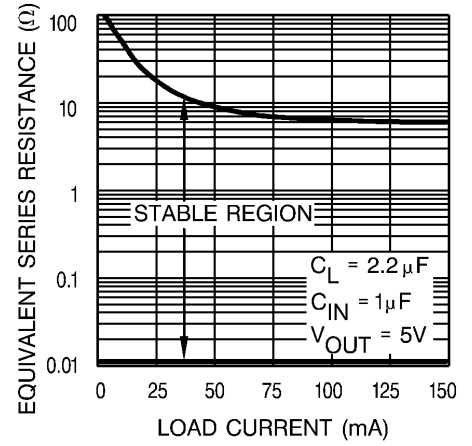


Figure 30. Output Capacitor ESR Range

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Typical Characteristics (continued)

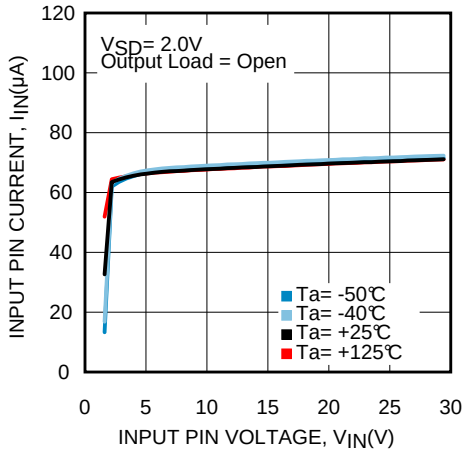


Figure 31. LP2951-N Input Pin Current vs Input Voltage

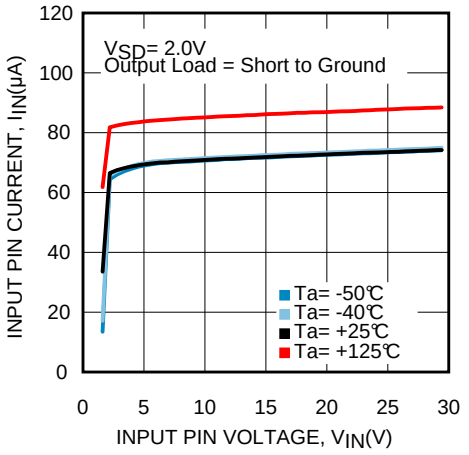


Figure 32. LP2951-N Input Pin Current vs Input Voltage

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8 Detailed Description

8.1 Overview

The LP2950-N and LP2951-N are very high accuracy micro power voltage regulators with low quiescent current (75 µA typical) and low dropout voltage (typical 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems.

The LP2950-N and LP2951-N block diagram contains several features, including:

- Very high accuracy 1.23-V reference;
- Fixed 5-V, 3-V, and 3.3-V versions; and
- Internal protection circuitry, such as foldback current limit, and thermal shutdown.

The LP2951-N VERSIONS ONLY:

- Fixed 5-V, 3-V, and 3.3-V versions and programmable output version from 1.24 V to 29 V with an external pair of resistors;
- Shutdown input, allowing turn off the regulator when the SHUTDOWN pin is pulled low; and
- Error flag output, which may be used for a power-on reset.

8.2 Functional Block Diagrams

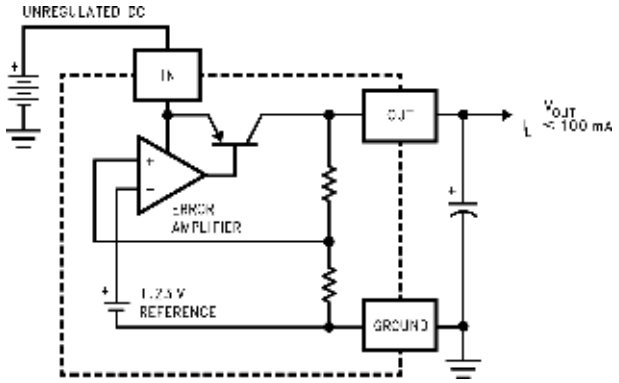


Figure 33. LP2950-N Functional Block Diagram

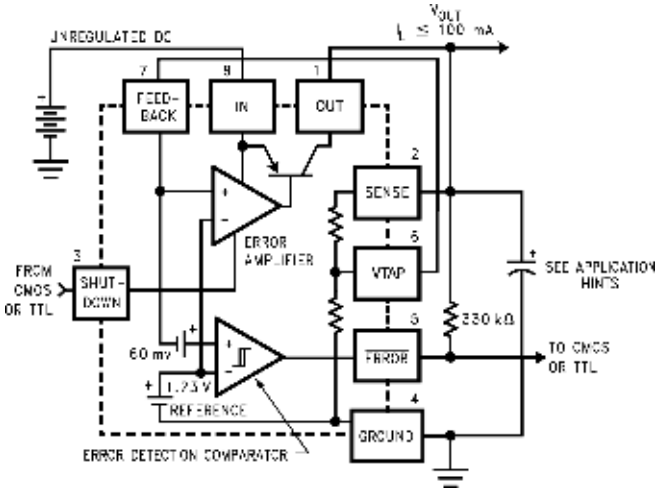


Figure 34. LP2951-N Functional Block Diagram

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8.3 Feature Description

8.3.1 Fixed Voltage Options and Programmable Voltage Version

The LP2950-N and LP2951-N provide 3 fixed output options: 3 V, 3.3 V, and 5 V. Please consult factory for custom voltages. In order to meet different application requirements, LP2951-N can also be used as a programmable voltage regulator, with an external resistors network; please refer to *Application and Implementation* for more details.

8.3.2 High Accuracy Output Voltage

With special carful design to minimize all contributions to the output voltage error, the LP2950-N/LP2951-N distinguished itself as a very high output voltage accuracy micro power LDO. This includes a tight initial tolerance (0.5% typical), extremely good load and line regulation (.05% typical) and a very low output voltage temperature coefficient, making the part an ideal a low-power voltage reference.

8.3.3 Low Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary.

8.3.4 Shutdown Mode

When the SHUTDOWN pin is pulled to high level, LP2951-N enters shutdown mode and a very low quiescent current is consumed. This function is designed for the application which needs a shutdown mode to effectively enhance battery life cycle.

8.3.5 Error Detection Comparator Output

The LP2951-N generates a logic low output whenever its output falls out of regulation by more than approximately 5%. Please refer to *Application and Implementation* for more details.

8.3.6 Internal Protection Circuitry

8.3.6.1 Short-Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output. A fold back feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the fold back current limit, the device may not start up correctly.

8.3.6.2 Thermal Protection

The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the device is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

8.3.7 Enhanced Stability

The LP2950-N and LP2951-N is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 6 mΩ. For output capacitor requirement, please refer to *Application and Implementation*.

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8.4 Device Functional Modes

8.4.1 Operation with 30 V ≥ V_{IN} > $V_{OUT(TARGET)}$ + 1 V

The device operate if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 1 V. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

8.4.2 Operation with Shutdown Control

If the voltage on the SHUTDOWN pin is higher than 1.3 V, the device is disabled. Decreasing shutdown below 0.7 V initiates the start-up sequence of the device.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP2950-N and LP2951-N are linear voltage regulator operating from 2.3 V to 30 V on the input and regulates voltages between 1.24 V to 29 V with 0.5% accuracy and 160 mA maximum outputs current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2950-N and LP2951-N is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very low dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, PSRR, or any other transient specification is required, the design becomes more challenging.

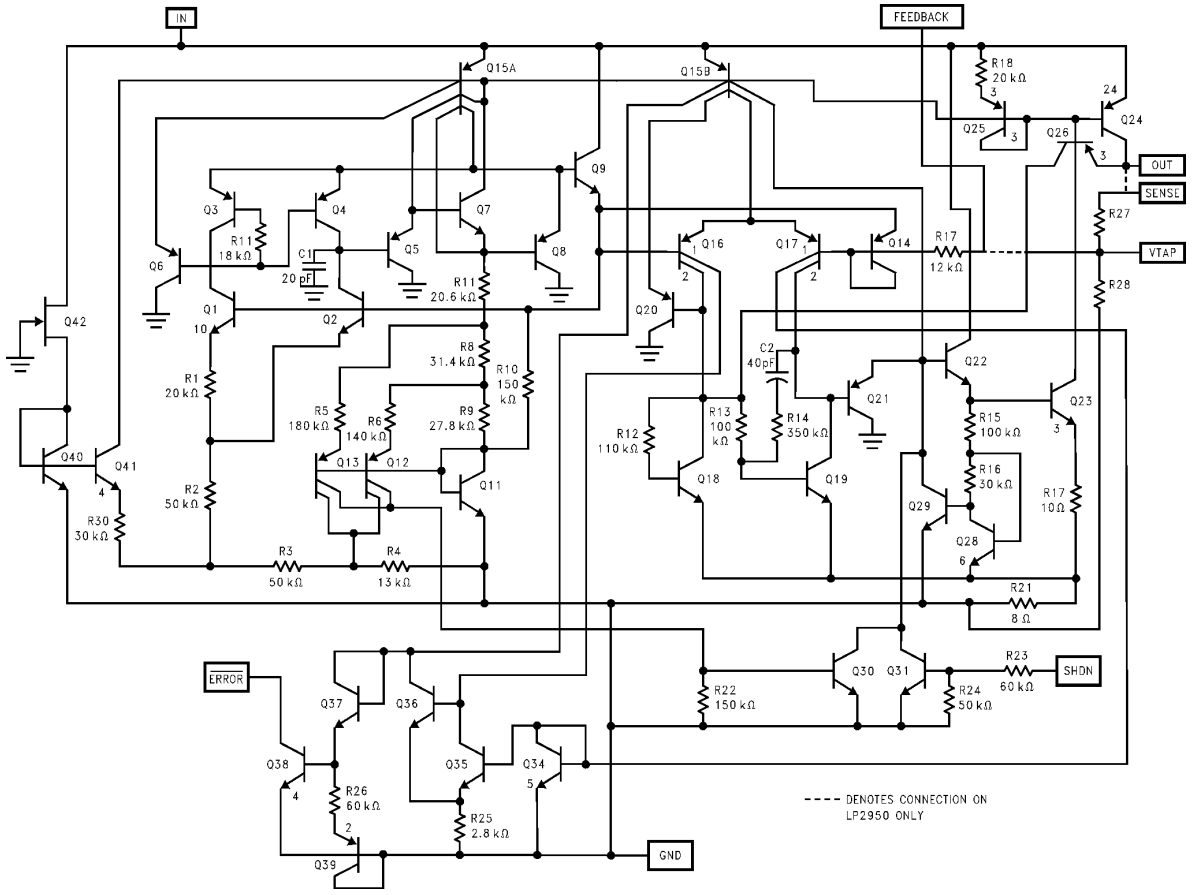


Figure 35. Schematic Diagram

9.2 Typical Applications

9.2.1 1-A Regulator with 1.2-V Dropout

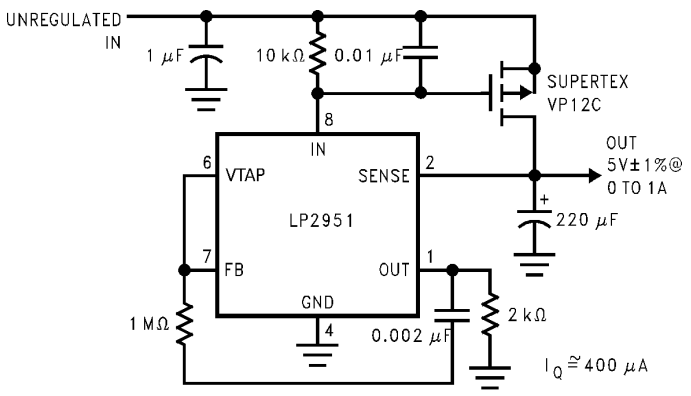


Figure 36. 1-A Regulator with 1.2-V Dropout

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	DESIGN REQUIREMENT
Input voltage	6.5 V, ±10%, provided by the DC-DC converter switching at 1 MHz
Output voltage	5 V, ±1%
Output current	100 mA (maximum), 1 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 200 μV_{RMS}
PSRR at 1 KHz	> 50 dB

9.2.1.2 Detailed Design Procedure

At 100-mA loading, the dropout of the LP2950-N/LP2951-N has 600 mV maximum dropout over temperature, thus an 1500-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2950-N/LP2951-N in this configuration is V_{OUT} / V_{IN} = 76.9%. To achieve the smallest form factor, the TO-92 package is selected. Input and output capacitors are selected in accordance with the Capacitor Recommendation section. Ceramic capacitances of 1 µF for the input and one 2.2-µF capacitors for the output are selected. With an efficiency of 73.3% and a 100-mA maximum load, the internal power dissipation is 150 mW, which corresponds to a 18.9°C junction temperature rise for the TO-92 package. With an 85°C maximum ambient temperature, the junction temperature is at 103.9°C. To minimize noise, a bypass capacitance (C_{BYPASS}) of 0.01-µF is selected between pin 7 to pin 1 for LP2951-N.

9.2.1.2.1 Output Capacitor Requirements

A 1-µF (or greater) capacitor is required between the output and ground for stability at output voltages of 5 V or higher. At lower output voltages, more capacitance is required (2.2 µF or more is recommended for 3-V and 3.3-V versions). Without this capacitor the device oscillates. Most types of tantalum or aluminum electrolytic work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

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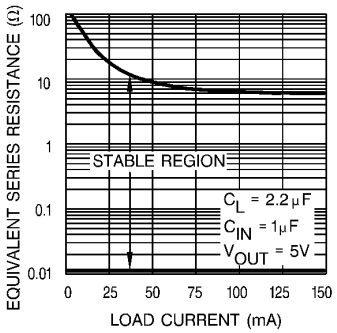


Figure 37. Output Capacitor ESR Range

The reason for the lower ESR limit is that the loop compensation of the feedback loop relies on the capacitance value and the ESR value of the output capacitor to provide the zero that gives added phase lead (See Figure 37).

$$f_Z = (1 / (2 \times \pi \times C_{OUT} \times ESR)) \quad (1)$$

Using the 2.2 µF value from the *Output Capacitor ESR Range* curve (Figure 37), a useful range for f_Z can be estimated:

$$f_{Z(MIN)} = (1 / (2 \times \pi \times 2.2\ \mu F \times 5\ \Omega)) = 14.5\ kHz \quad (2)$$

$$f_{Z(MAX)} = (1 / (2 \times \pi \times 2.2\ \mu F \times 0.05\ \Omega)) = 318\ kHz \quad (3)$$

For ceramic capacitors, the low ESR produces a zero at a frequency that is too high to be useful, so meaningful phase lead does not occur. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance about 0.1 Ω to 2 Ω) to simulate the needed ESR. Only X5R, X7R, or better, MLCC types should be used, and should have a DC voltage rating at least twice the $V_{OUT(NOM)}$ value.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 µF for currents below 10 mA or 0.1 µF for currents below 1 mA. Using the adjustable versions at voltages below 5 V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100-mA load at 1.23 V output (output shorted to Feedback) a 3.3-µF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950-N remains stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951-N versions with external resistors, a minimum load of 1 µA is recommended.

Applications having conditions that may drive the LP2950-N/51 into nonlinear operation require special consideration. Nonlinear operation occurs when the output voltage is held low enough to force the output stage into output current limiting while trying to pull the output voltage up to the regulated value. The internal loop response time controls how long it takes for the device to regain linear operation when the output has returned to the normal operating range. There are three significant nonlinear conditions that need to be considered, all can force the output stage into output current limiting mode, all can cause the output voltage to over-shoot with low value output capacitors when the condition is removed, and the recommended generic solution is to set the output capacitor to a value not less than 10 µF. Although the 10 µF value for C_{OUT} may not eliminate the output voltage over-shoot in all cases, it should lower it to acceptable levels (< 10% of $V_{OUT(NOM)}$) in the majority of cases. In all three of these conditions, applications with lighter load currents are more susceptible to output voltage over-shoot than applications with higher load currents.

1. At power-up, with the input voltage rising faster than output stage can charge the output capacitor.

   $V_{IN}\ t_{RISE(MIN)} > ((C_{OUT} / 100\ mA) \times \Delta V_{IN})$

   where

   - $\Delta V_{IN} = V_{OUT(NOM)} + 1\ V$ (4)

2. Recovery from an output short circuit to ground condition.

   $$C_{OUT(MIN)} \approx (160\ mA - I_{LOAD(NOM)}) / ((V_{OUT(NOM)}/10)/25\ \mu s)) \quad (5)$$

3. Toggling the LP2951-N SHUTDOWN pin from high (OFF) to low (ON).

   $$C_{OUT(MIN)} \approx (160\ mA - I_{LOAD(NOM)}) / ((V_{OUT(NOM)}/10)/25\ \mu s)) \quad (6)$$

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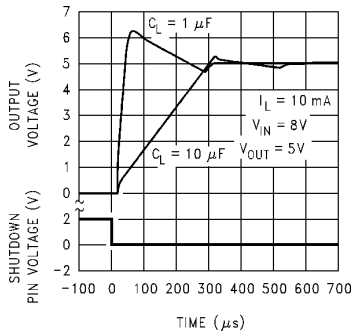


Figure 38. LP2951-N Enable Transient

9.2.1.2.2 Input Capacitor Requirements

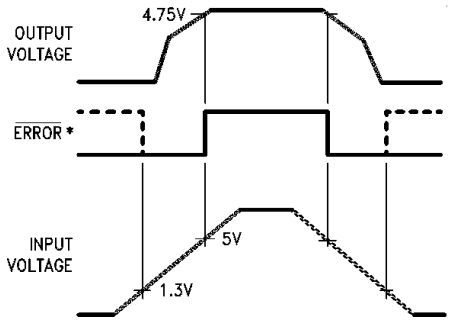
A minimum 1 µF tantalum, ceramic or aluminum electrolytic capacitor should be placed from the LP2950-N/LP2951-N input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

9.2.1.2.3 Error Detection Comparator Output

The comparator produces a logic low output whenever the LP2951-N output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains “5% below normal” regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75 V for a 5-V output or 11.4 V for a 12-V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 39 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951-N input is ramped up and down. For 5 V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3-V input. It goes high at about 5-V input (the input voltage at which V_{OUT} = 4.75 V). Because the LP2951-N dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5 V) varies with the load current. The **output** voltage trip point (approx. 4.75 V) does not vary with load.

The error comparator has an open-collector output which requires an external pull up resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100 k to 1 MΩ. The resistor is not required if this output is unused.



*When $V_{IN} \leq 1.3$ V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pullup voltage. Using V_{OUT} as the pullup voltage (see Figure 40), rather than an external 5-V source, keeps the error flag voltage under 1.2 V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

Figure 39. $\overline{\text{ERROR}}$ Output Timing

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9.2.1.2.4 Programming the Output Voltage (LP2951-N)

The LP2951-N may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the FEEDBACK and VTAP pins together. Alternatively, it may be programmed for any output voltage between its 1.235-V reference and its 30-V maximum rating. As seen in Figure 40, an external pair of resistors is required.

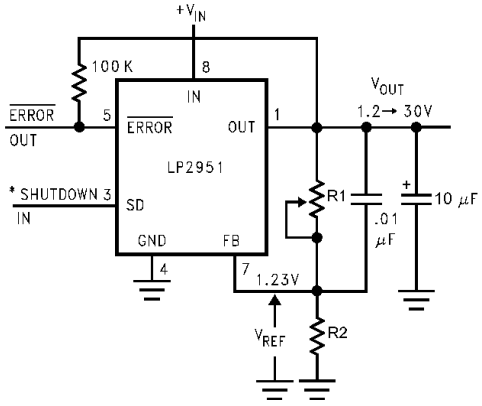
The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1 \quad (7)$$

where

- V_{REF} is the nominal 1.235-V reference voltage and I_{FB} is the FEEDBACK pin bias current, nominally –20 nA

The minimum recommended load current of 1 µA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} produces a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100 kΩ reduces this error to 0.17% while increasing the resistor program current to 12 µA. Because the LP2951-N typically draws 60 µA at no load with pin 2 open-circuited, this is a small price to pay.



$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

*Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.
Note: Pins 2 and 6 are left open.

Figure 40. Adjustable Regulator

Stray capacitance to the LP2951-N FEEDBACK pin can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100-pF capacitor between the OUT pin and the FEEDBACK pin, and increasing the output capacitor to at least 3.3 µF, fixes this problem.

9.2.1.2.5 Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3-lead LP2950-N but is relatively inefficient, as increasing the capacitor from 1 µF to 220 µF only decreases the noise from 430 μV_{RMS} to 160 μV_{RMS} for a 100-kHz bandwidth at 5-V output.

Noise can be reduced fourfold by a bypass capacitor across R1, because it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz} \quad (8)$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 µV rms for a 100-kHz bandwidth at 5-V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

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9.2.1.3 Application Curves

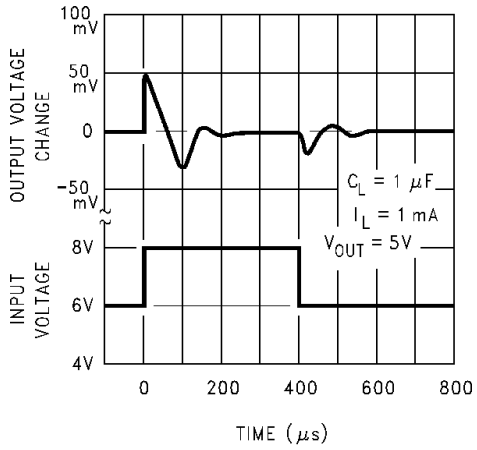


Figure 41. Line Transient Response

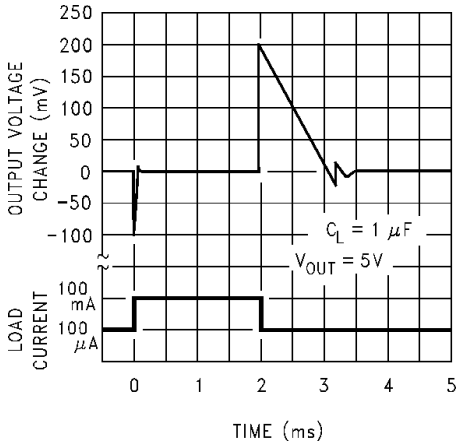


Figure 42. Load Transient Response

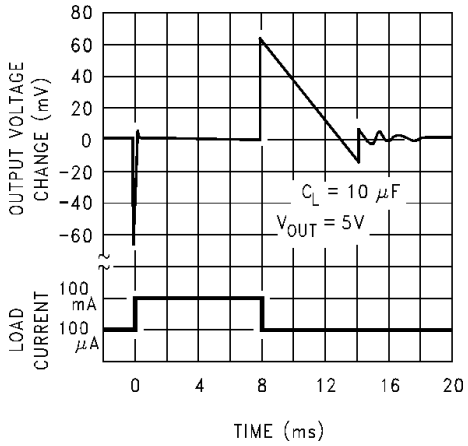


Figure 43. Load Transient Response

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9.2.2 300-mA Regulator with 0.75-V Dropout

In Figure 44, by paralleling the LP2951 together with 2x2N5432 (150-mA N channel JFET), a user can get a higher output current capability around 300 mA.

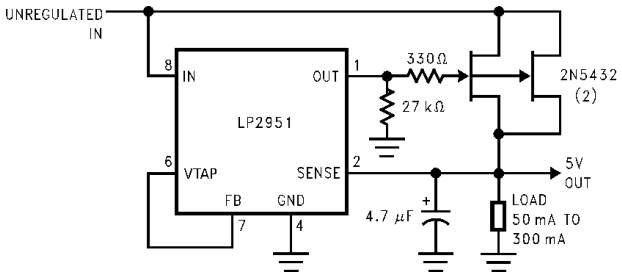
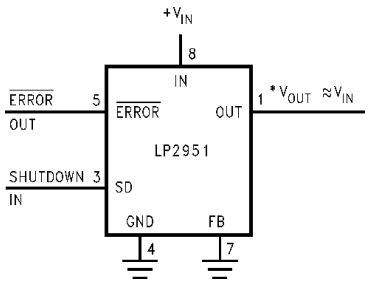


Figure 44. 300-mA Regulator with 0.75-V Dropout

9.2.3 Wide Input Voltage Range Current Limiter

The LP2951 can be used as a 160-mA current limiter as Figure 45. When FB is connected to ground, the pass element is fully turned on and out voltage will be close to input voltage. Input-output voltage ranges from 40 mV to 400 mV, depending on load current.



*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Figure 45. Wide Input Voltage Range Current Limiter

9.2.4 Low Drift Current Source

The LP2951 can be used as a low drift current source as Figure 46 shows. By connected V_{out} to FB, V_{out} will regulated at 1.235 V, and current consumption at R is I_L = 1.23/R.

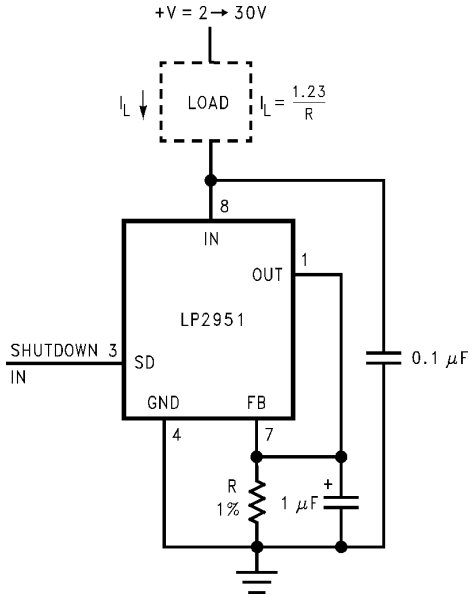
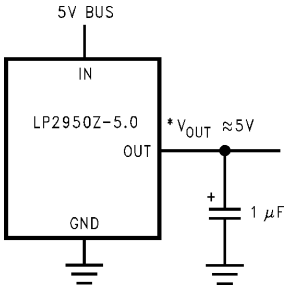


Figure 46. Low Drift Current Source

9.2.5 5-V Current Limiter

The LP2950 internal current limit function can be leveraged to build 5-V current limiter as Figure 47 shows. The minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.



*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Figure 47. 5-V Current Limiter

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9.2.6 Regulator with Early Warning and Auxiliary Output

The LP2951 can be used to build a Regulator with early warning and auxiliary output as Figure 48 shows. it has below features:

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output
- Operation: V_{OUT} of regulator 1 is programmed one diode drop above 5 V. Its error flag becomes active when $V_{IN} \leq 5.7$ V. When V_{IN} drops below 5.3 V, the error flag of regulator 2 becomes active and via Q1 latches the main output off. When V_{IN} again exceeds 5.7 V regulator 1 is back in regulation and the early warning signal rises, unlatching regulator 2 via D3.

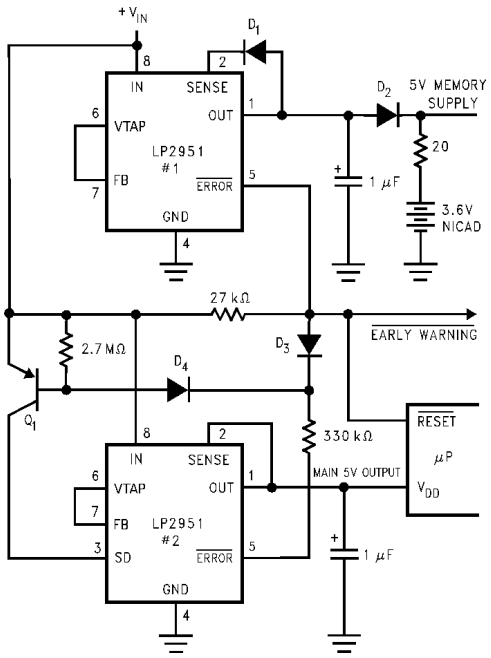


Figure 48. Regulator With Early Warning and Auxiliary Output

9.2.7 Latch Off When Error Flag Occurs

As Figure 49 presents, a latch off when error flag occurs circuit works in below two mode:

When output is within ±95% of V_{OUT} option, the error flag pin keep output high, which turns off PNP bipolar and pulls SD pin to low, then the LP2951 keeps output regulated voltage.

When output drop to less than 95% of V_{OUT} option, it triggers error flag output a low voltage, which turns on PNP bipolar and pulls SD pin to high, then the device enters shutdown mode and turns off output voltage. During a shutdown sequence, the $\overline{\text{ERROR}}$ pin continues output low, and the LP2951 device latches in shutdown mode.

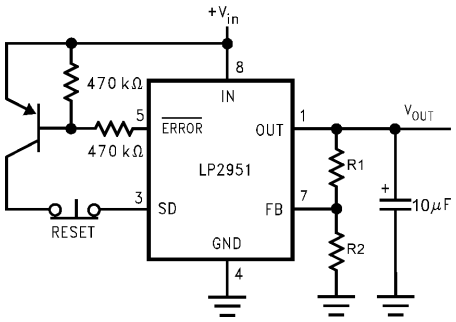


Figure 49. Latch Off When Error Flag Occurs

9.2.8 2-A Low Dropout Regulator

As Figure 50 shows, the 2-A low dropout regulator has below features:

$$V_{out} = 1.23V\left(1 + \frac{R_1}{R_2}\right)$$

For 5 V_{OUT}, use internal resistors. Wire pin 6 to pin 7 and wire pin 2 to + V_{OUT} bus.

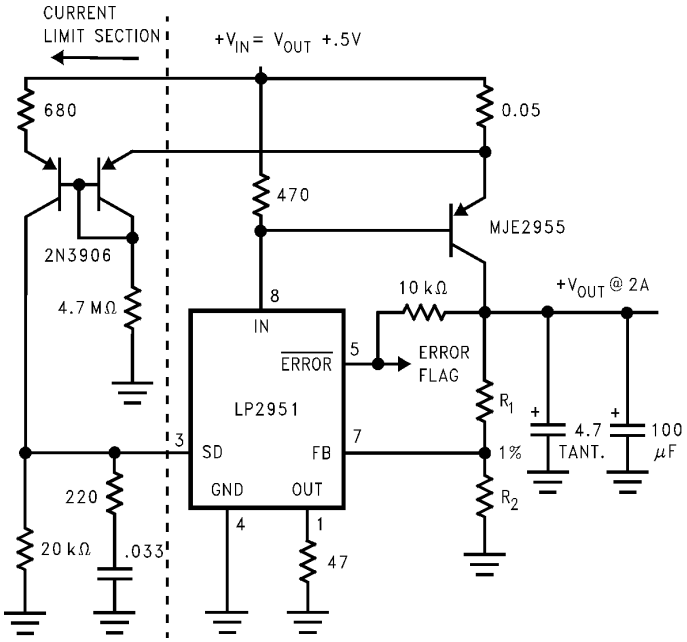


Figure 50. 2-A Low Dropout Regulator

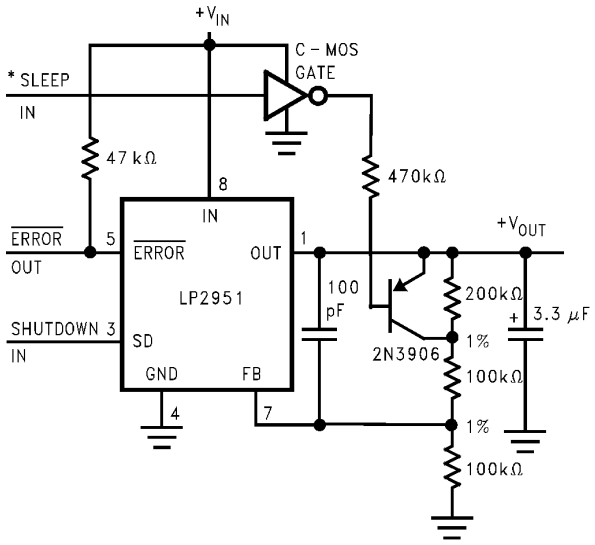
9.2.9 5-V Regulator with 2.5-V Sleep Function

In Figure 51, the 5-V regulator with 2.5-V sleep function works in below mode:

When sleep input is low, C-MOS output a high voltage and 2N3906 is off, then V_{out} = (1 + 300 KΩ/100 KΩ) × V_{FB} ≈ 5 V

when sleep input is high, C-MOS output a low voltage, turns on 2N3906, then 200-KΩ resistor is bypassed from circuit, and V_{OUT} = (1+100 KΩ/100 KΩ) × V_{FB} ≈ 2.5 V.

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*High input lowers V_{out} to 2.5 V.

Figure 51. 5-V Regulator with 2.5-V Sleep Function

9.2.10 Open Circuit Detector for 4 → 20-mA Current Loop

Figure 52 shows the open circuit detector for 4 → 20-mA current loop. The circuit outputs a high level while input current is less than 3.5 mA.

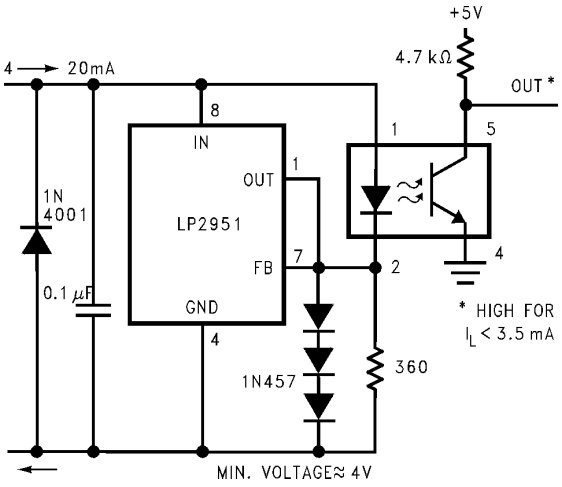
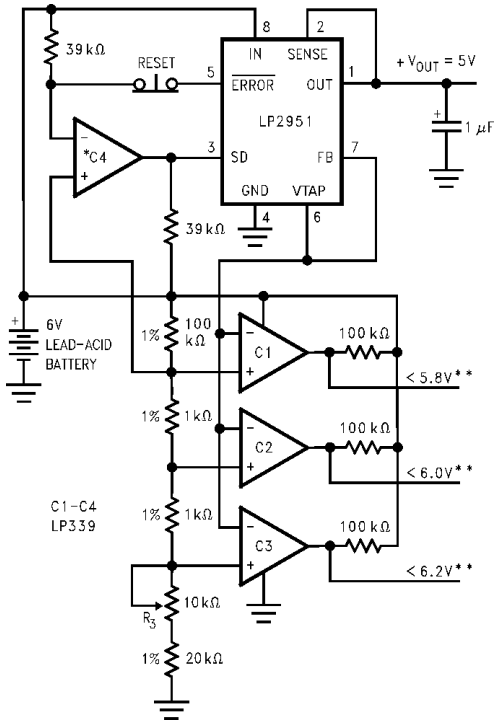


Figure 52. Open Circuit Detector for 4 → 20-mA Current Loop

9.2.11 Regulator with State-of-Charge Indicator

In Figure 53, the LP339, a quad comparator, is used to indicate battery voltage state. The comparator's negative input voltage is equal to the LP2951 1.235-V feedback voltage. By adjusting R3, we can adjust positive input voltage of C1~C3 to target value.



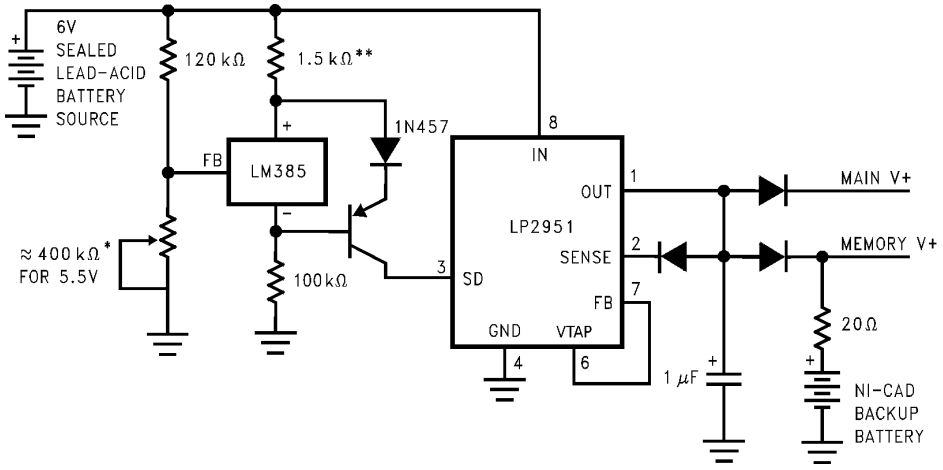
*Optional latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6 V.
**Outputs go low when V_{IN} drops below designated thresholds.

Figure 53. Regulator with State-of-Charge Indicator

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9.2.12 Low Battery Disconnect

In Figure 54, a band-gap voltage reference LM385 is used to generate shutdown signal, when V_{in} < 5.5 V, the LP2951 turns off and turns on again when V_{IN} > 6 V.



For values shown, regulator shuts down when V_{in} < 5.5 V and turns on again at 6 V. Current drain in disconnected mode is approximately 150 μA.
*Sets disconnect voltage.
**Sets disconnect hysteresis.

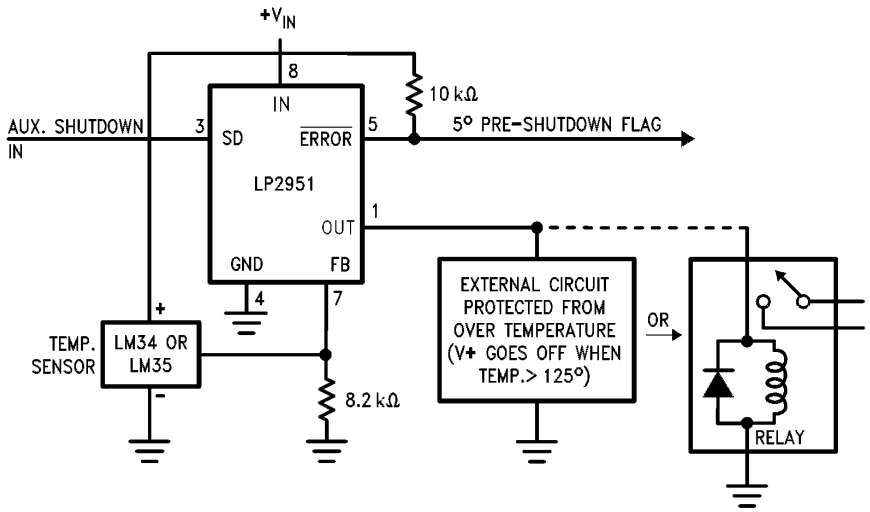
Figure 54. Low Battery Disconnect

9.2.13 System Overtemperature Protection Circuit

In Figure 55, temperature sensors LM34/35's output voltage is linearly proportional to the Celsius (Centigrade) temperature.

At room temperature, LM34/35's output voltage is lower than 1.235-V feedback voltage, the internal pass transistor fully turns on, and the LP2951 output voltage is close to V_{IN}.

When ambient temperature raise higher than protection target, LM34/35's output voltage is higher than 1.235-V feedback voltage, the internal pass transistor turns off, and the LP2951 output goes off.



LM34 for 125°F shutdown
LM35 for 125°C shutdown

Figure 55. System Overtemperature Protection Circuit

10 Power Supply Recommendations

The LP2950-N and LP2951-N are designed to operate from an input voltage supply range between 2.3 V and 30 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

11.2 Layout Example

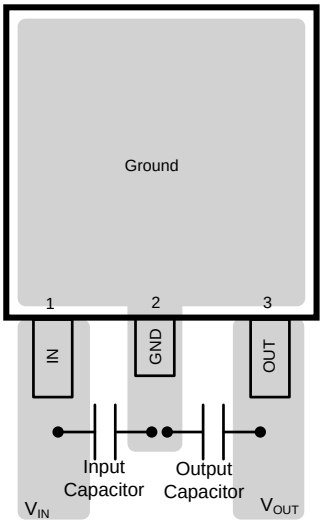


Figure 56. LP2950 Board Layout

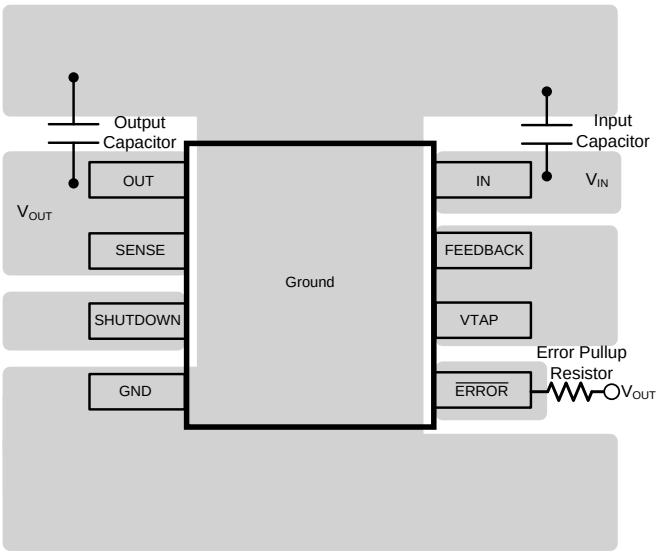


Figure 57. LP2951 VSSOP Board Layout

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Layout Example (continued)

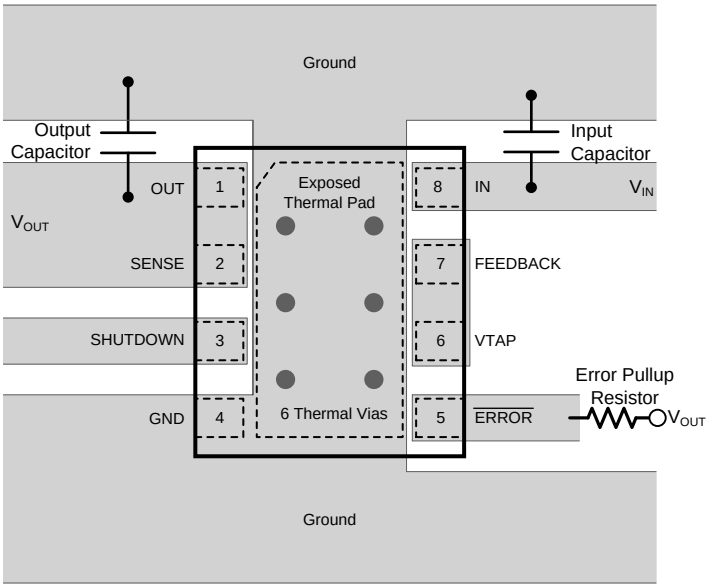


Figure 58. LP2951 WSON Board Layout

11.3 WSON Mounting

The NGT (no pullback) 8-lead WSON package requires specific mounting techniques which are detailed in *AN-1187 Leadless Leadframe Package (LLP)*. Referring to the PCB Design Recommendations section, note that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, TI recommends that the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

For the LP2951-N in the NGT 8-lead WSON package, the junction-to-case thermal rating, $R_{\theta JC}$, is 35°C/W, where the case is the bottom of the package at the center of the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the eight pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 4 (that is, GND). Alternately, but not recommended, the DAP may be left floating (that is, no electrical connection). The DAP must not be connected to any potential other than ground.

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

AN-1187 Leadless Leadframe Package (LLP)

12.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP2950-N	Click here	Click here	Click here	Click here	Click here
LP2951-N	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2950ACZ-3.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950A CZ3.0	Samples
LP2950ACZ-3.3/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950A CZ3.3	Samples
LP2950ACZ-5.0/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950A CZ5.0	Samples
LP2950ACZ-5.0/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950A CZ5.0	Samples
LP2950ACZ-5.0/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950A CZ5.0	Samples
LP2950ACZ-5.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950A CZ5.0	Samples
LP2950CDT-3.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.0	Samples
LP2950CDT-3.3	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP2950 CDT-3.3	
LP2950CDT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.3	Samples
LP2950CDT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-5.0	Samples
LP2950CDTX-3.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.0	Samples
LP2950CDTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-3.3	Samples
LP2950CDTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP2950 CDT-5.0	Samples
LP2950CZ-3.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950 CZ3.0	Samples
LP2950CZ-3.3/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950 CZ3.3	Samples
LP2950CZ-3.3/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950 CZ3.3	Samples
LP2950CZ-5.0/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950 CZ5.0	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2950CZ-5.0/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950 CZ5.0	Samples
LP2950CZ-5.0/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type		2950 CZ5.0	Samples
LP2950CZ-5.0/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	2950 CZ5.0	Samples
LP2951ACM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951 ACMC	
LP2951ACM-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951A CM30C	Samples
LP2951ACM-3.3	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951A CM33C	
LP2951ACM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951A (CM33>D, CM33C)	Samples
LP2951ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951 ACM>D	Samples
LP2951ACMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0DA	
LP2951ACMM-3.0	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0BA	
LP2951ACMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BA	Samples
LP2951ACMM-3.3	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0CA	
LP2951ACMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CA	Samples
LP2951ACMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DA	Samples
LP2951ACMMX-3.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BA	Samples
LP2951ACMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CA	Samples
LP2951ACMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DA	Samples
LP2951ACMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	2951 (ACM>D, ACMC)	
LP2951ACMX-3.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951A CM30C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951ACMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951A (CM33>D, CM33C)	Samples
LP2951ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951 (ACM>D, ACMC)	Samples
LP2951ACN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP 2951ACN	Samples
LP2951ACSD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	2951AC	Samples
LP2951ACSDX-3.3/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	51AC33	Samples
LP2951ACSDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951AC	Samples
LP2951CM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2951 CMC	
LP2951CM-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M30C	Samples
LP2951CM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M33>D	Samples
LP2951CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951 (CM>D, CMC)	Samples
LP2951CMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L0DB	
LP2951CMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BB	Samples
LP2951CMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CB	Samples
LP2951CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DB	Samples
LP2951CMMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	L0DB	
LP2951CMMX-3.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0BB	Samples
LP2951CMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CB	Samples
LP2951CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0DB	Samples
LP2951CMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	2951 (CM>D, CMC)	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951CMX-3.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951C M30C	Samples
LP2951CMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951C (M33>D, M33C)	Samples
LP2951CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2951 CM>D	Samples
LP2951CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP 2951CN	Samples
LP2951CSD-3.0/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	51AC30B	Samples
LP2951CSD-3.3/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC33B	Samples
LP2951CSD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	2951ACB	Samples
LP2951CSDX-3.3/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	51AC33B	Samples
LP2951CSDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	2951ACB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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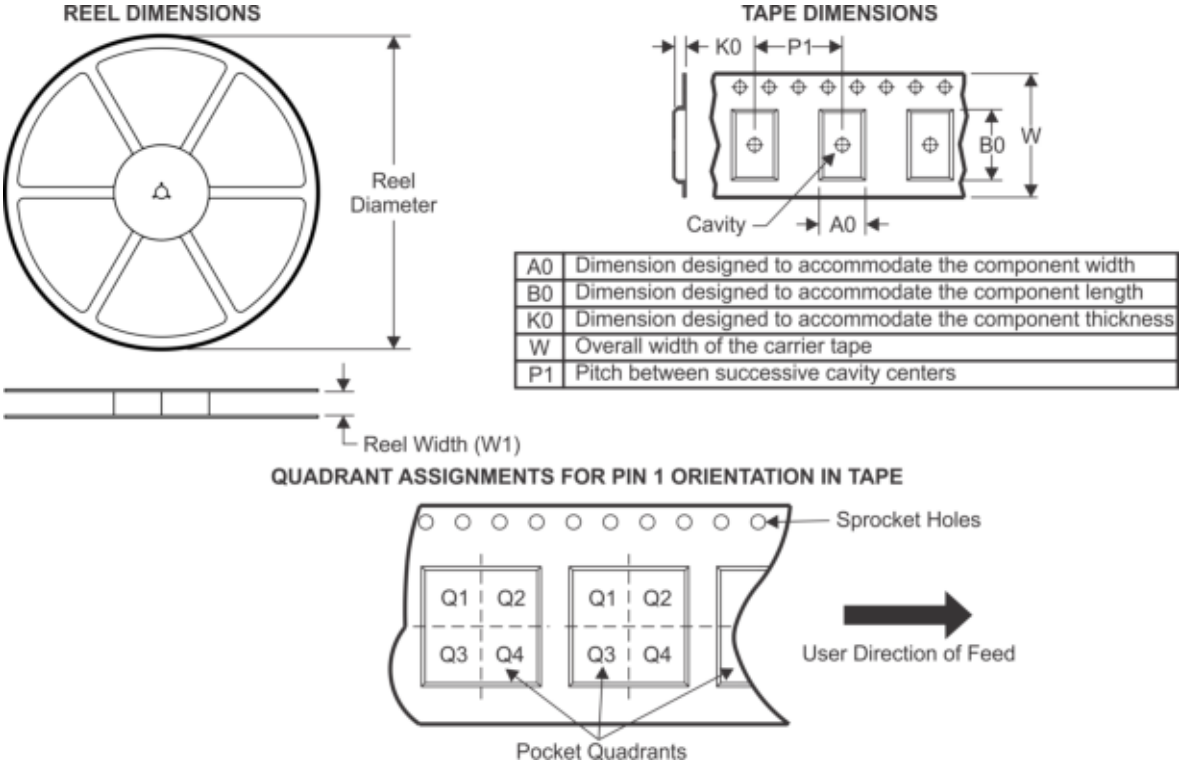
OTHER QUALIFIED VERSIONS OF LP2951-N :

- Automotive: LP2951-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



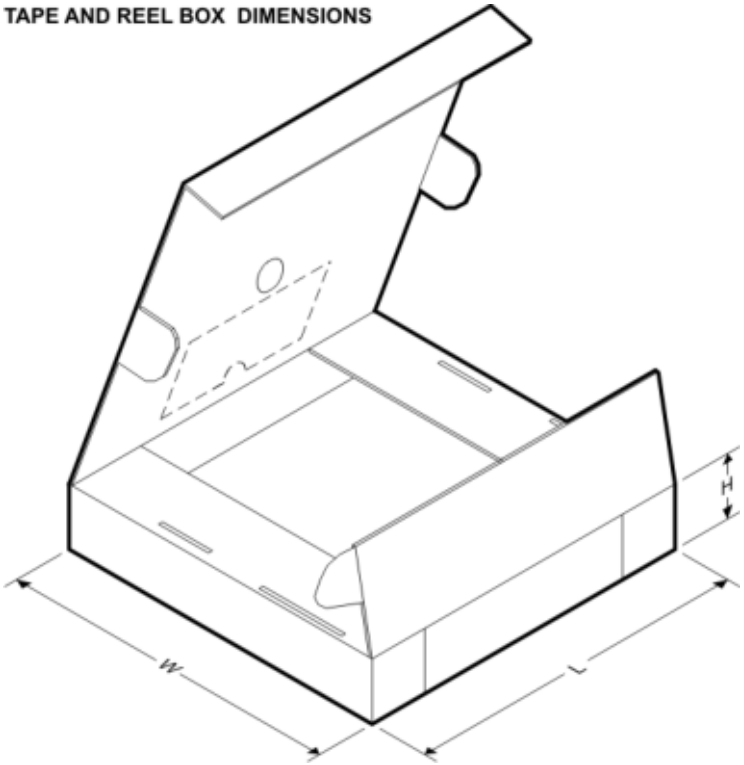
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2950CDTX-3.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2950CDTX-3.3/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2950CDTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP2951ACMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951ACSD/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2951ACSDX-3.3/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951ACSDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2951CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2951CSD-3.0/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LP2951CSD-3.3/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951CSD/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LP2951CSDX-3.3/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2951CSDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

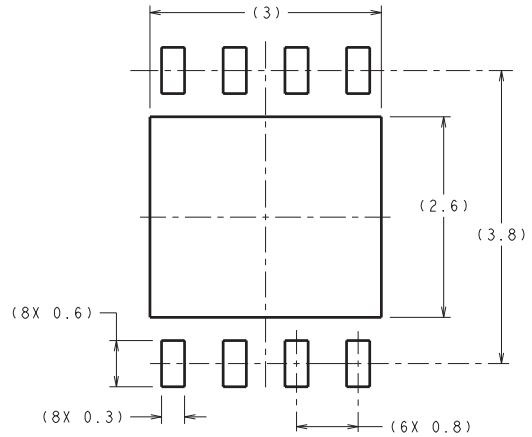
TAPE AND REEL BOX DIMENSIONS



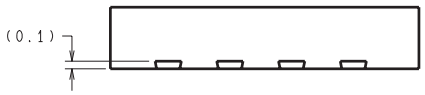
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2950CDTX-3.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP2950CDTX-3.3/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP2950CDTX-5.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP2951ACMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.0	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.3	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951ACMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951ACSD/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0
LP2951ACSDX-3.3/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LP2951ACSDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LP2951CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2951CMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2951CMX	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2951CSD-3.0/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0
LP2951CSD-3.3/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LP2951CSD/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0
LP2951CSDX-3.3/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LP2951CSDX/NOPB	WSON	NGT	8	4500	346.0	346.0	35.0

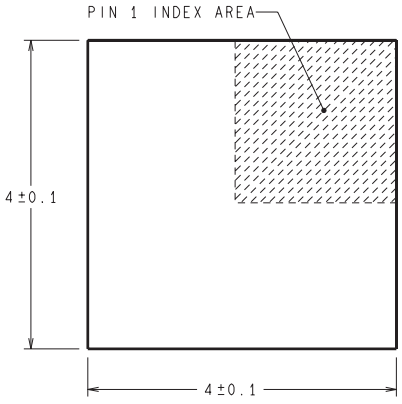
NGT0008A

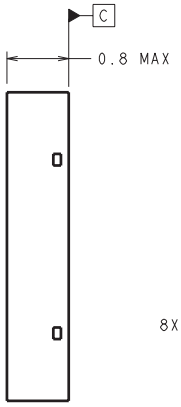


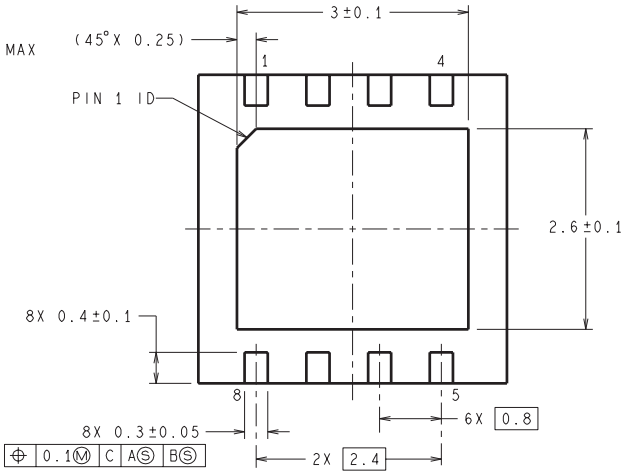
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN







SDC08A (Rev A)

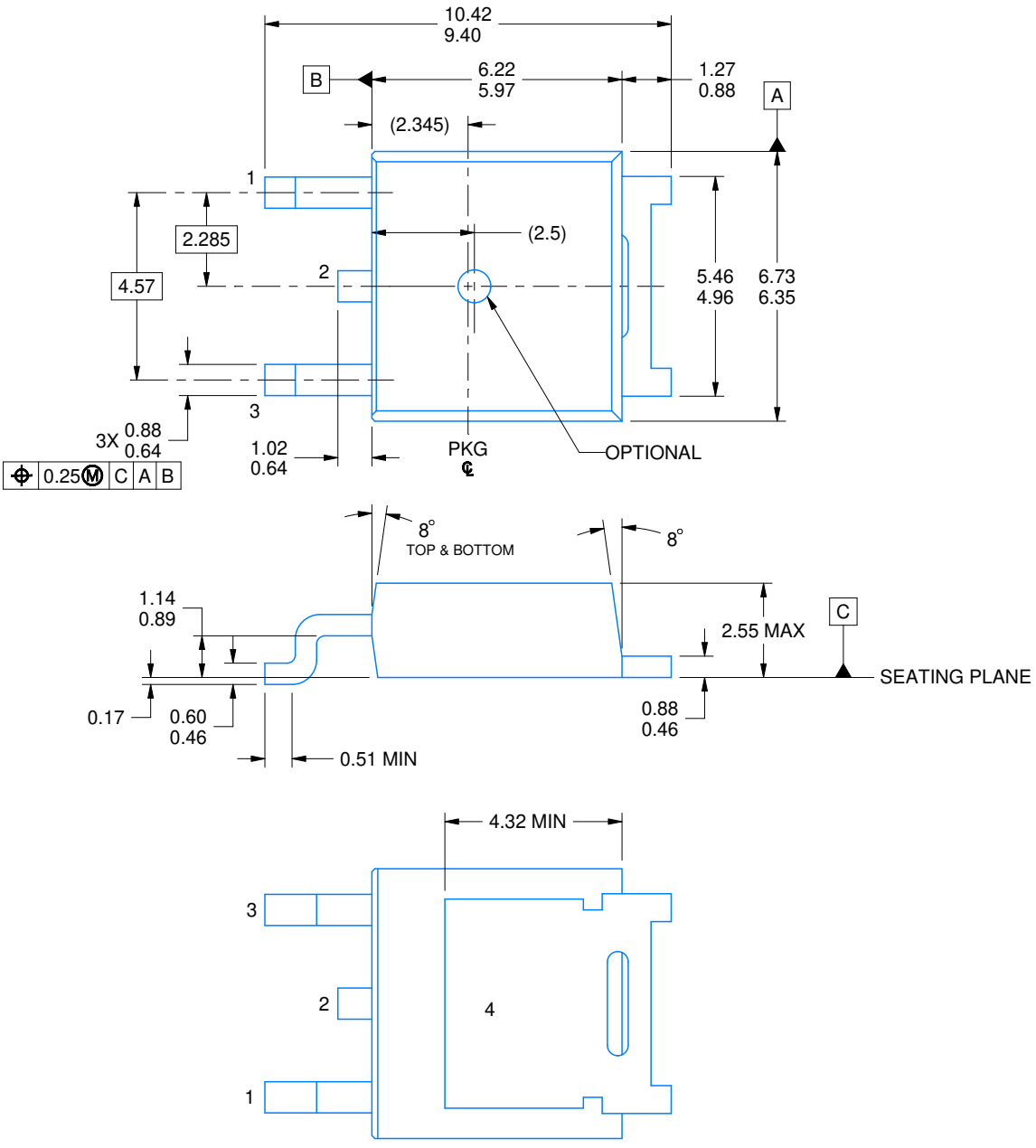
NDP0003B



PACKAGE OUTLINE

TO-252 - 2.55 mm max height

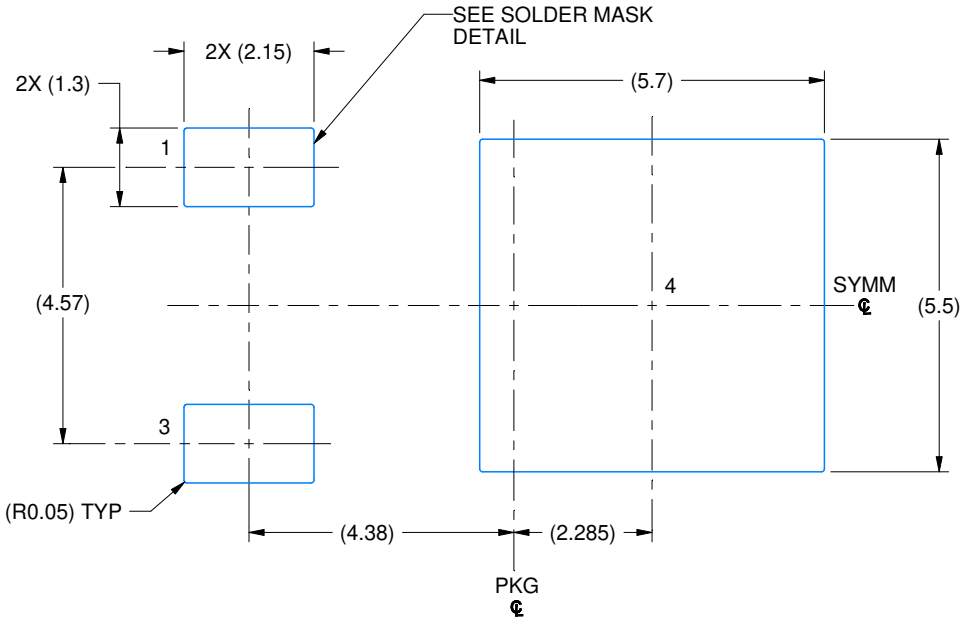
TRANSISTOR OUTLINE



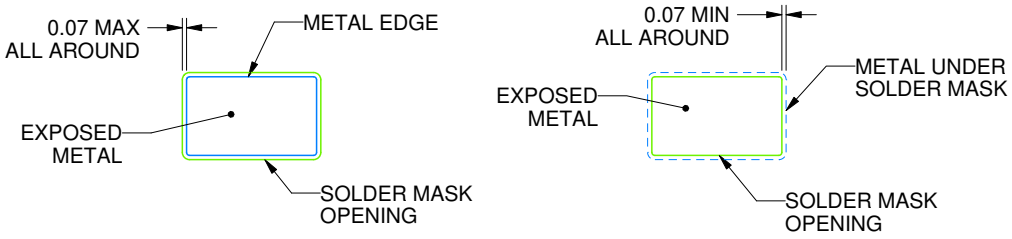
4219870/A 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

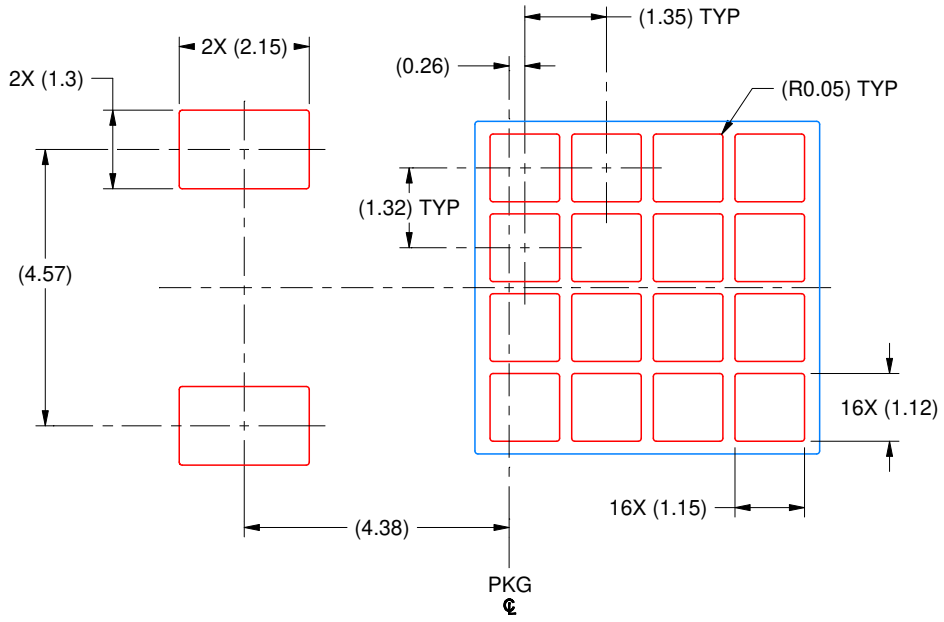


SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



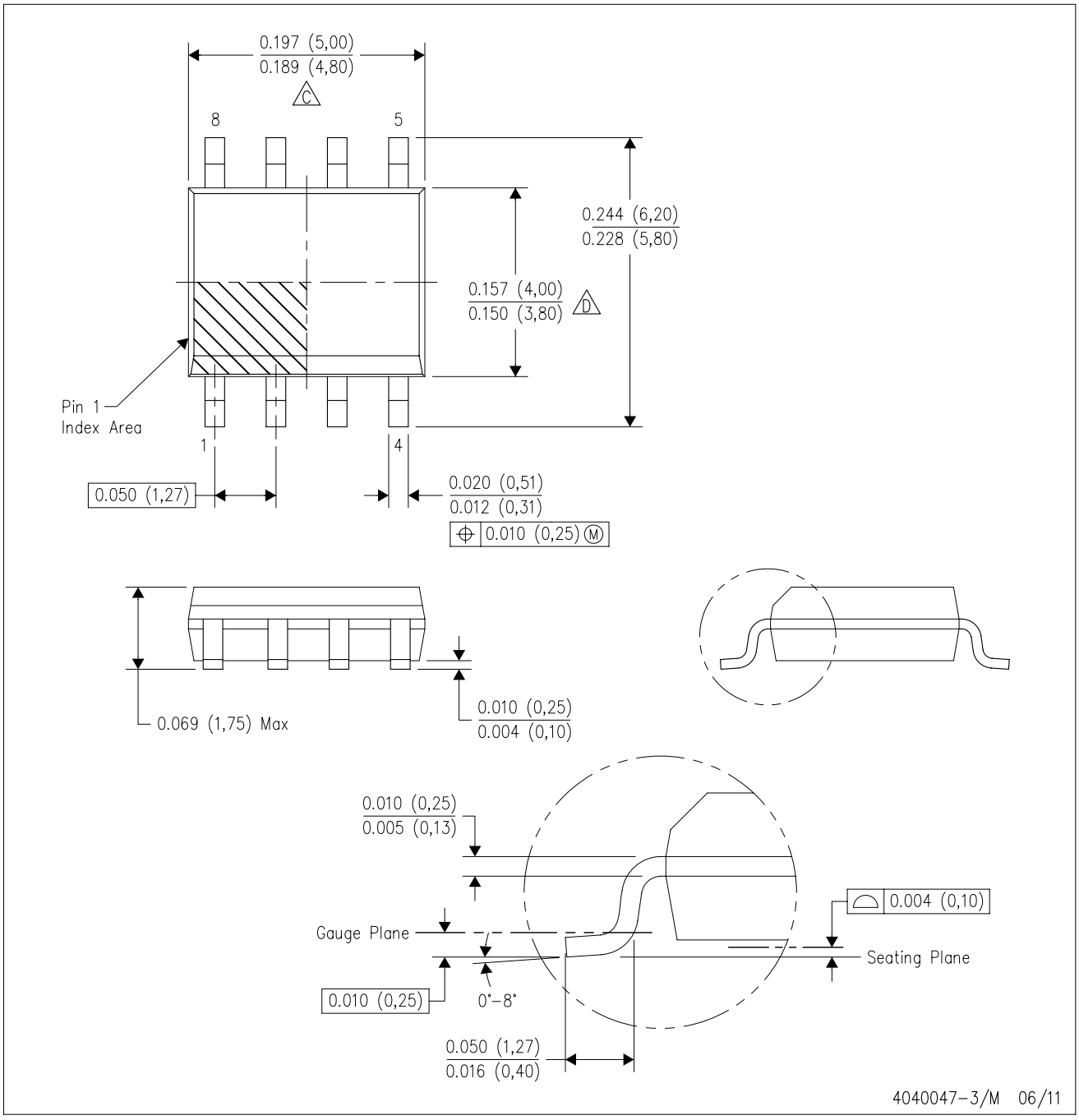
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A 03/2018

NOTES: (continued)

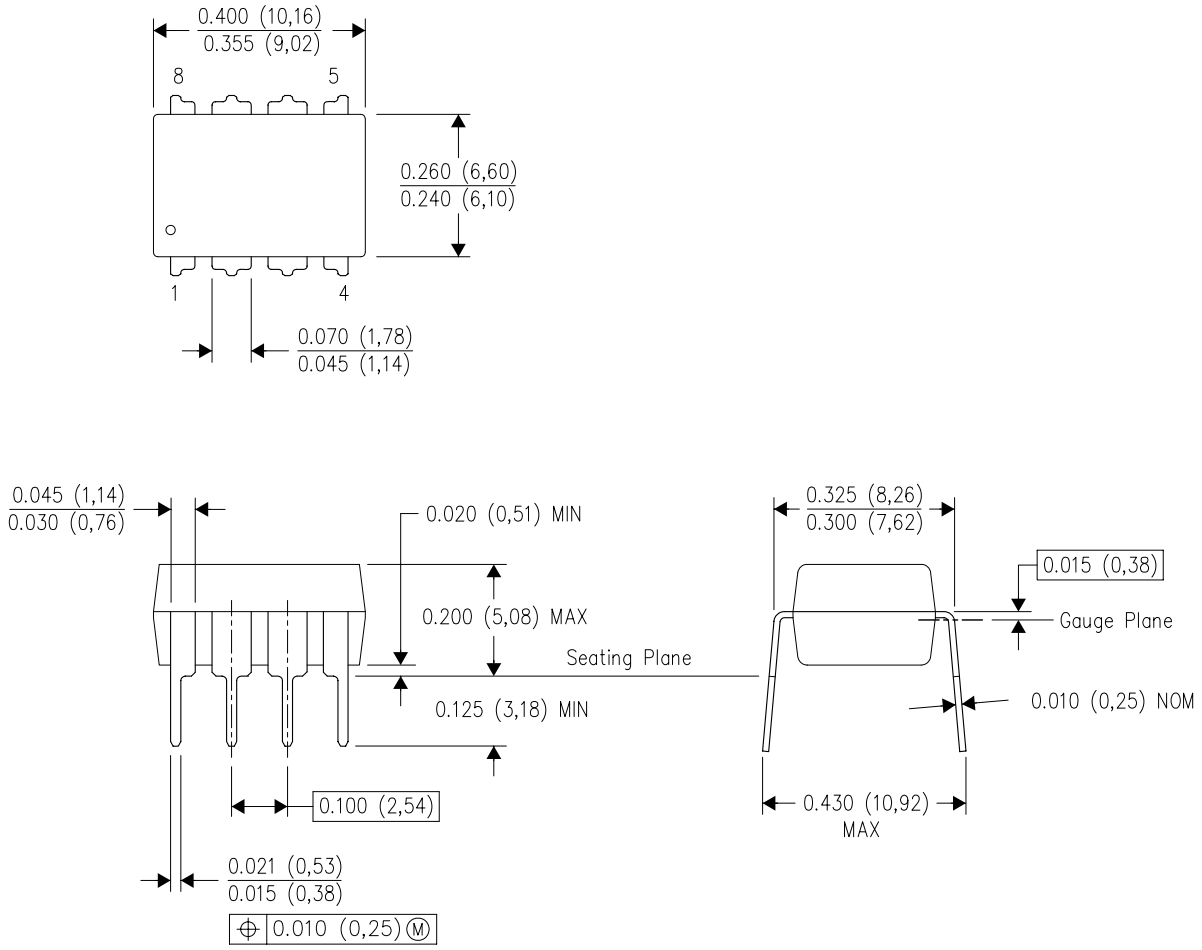
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



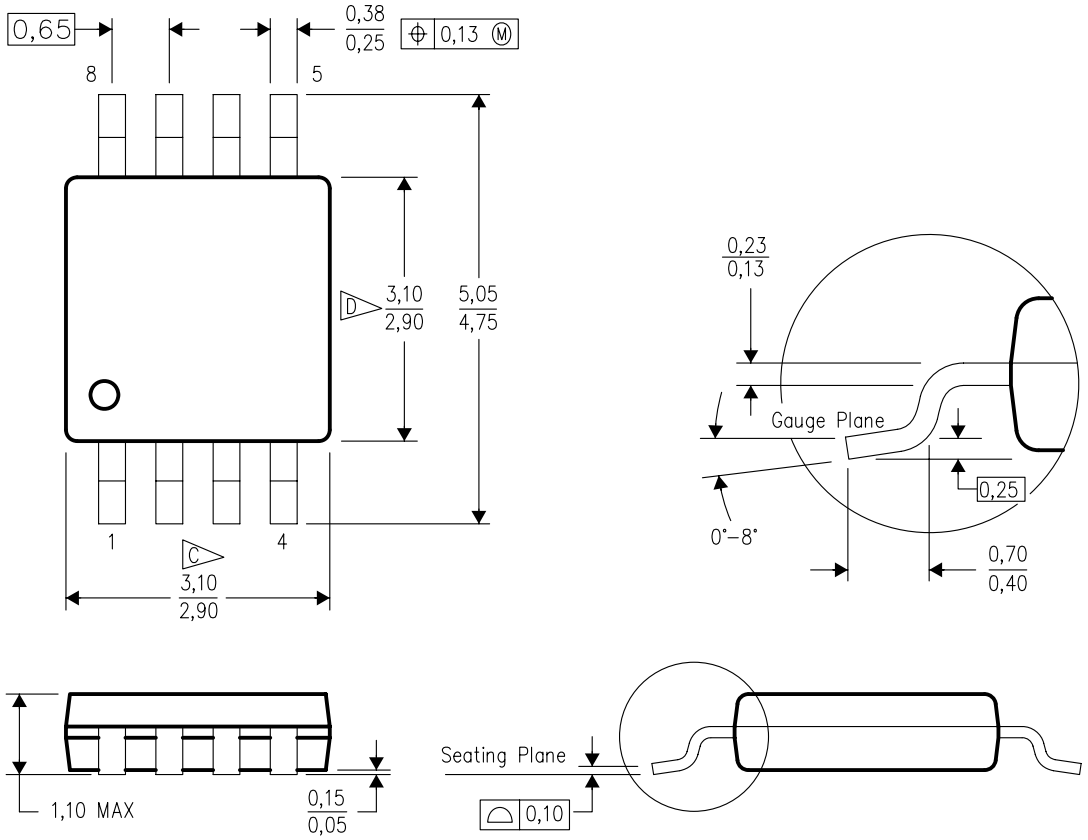
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

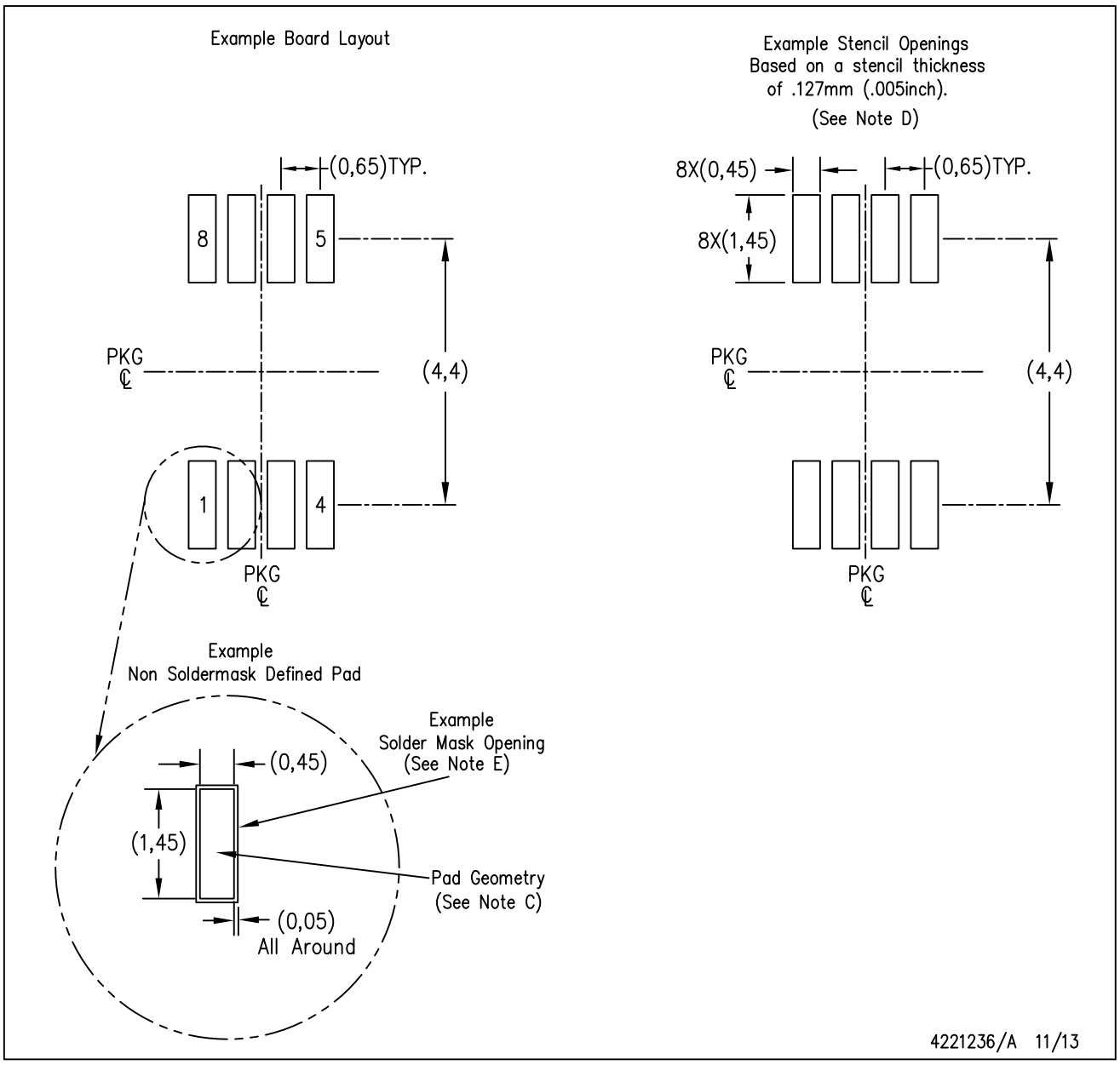
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

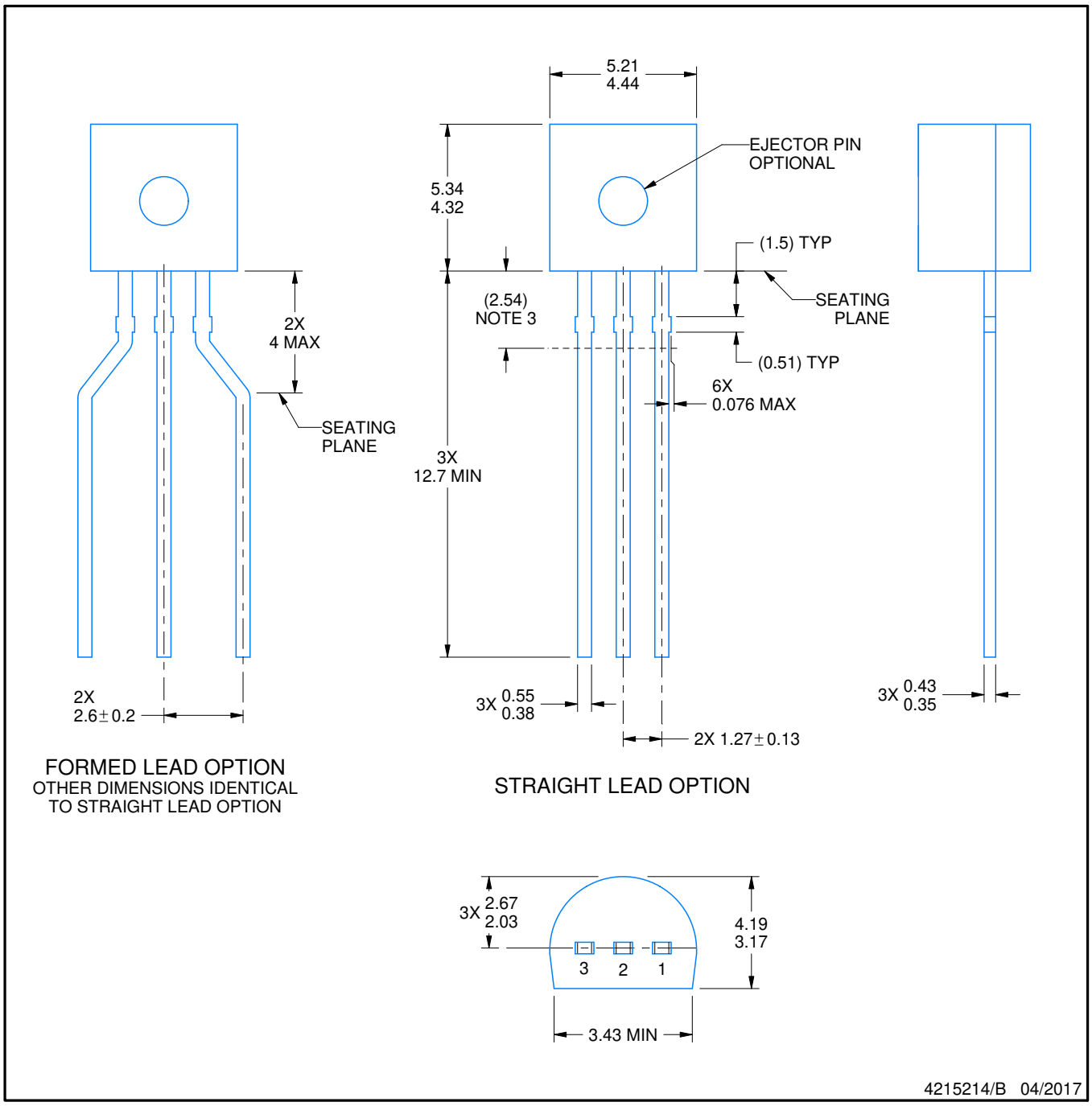




PACKAGE OUTLINE

TO-92 - 5.34 mm max height

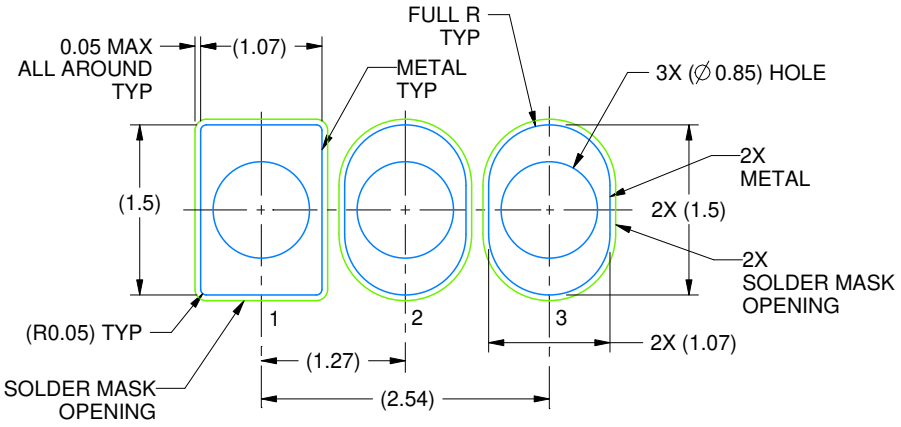
TO-92



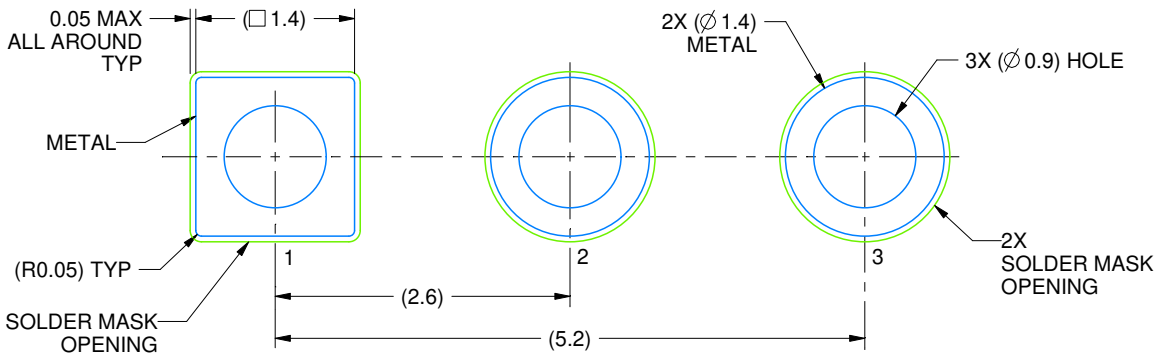
4215214/B 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



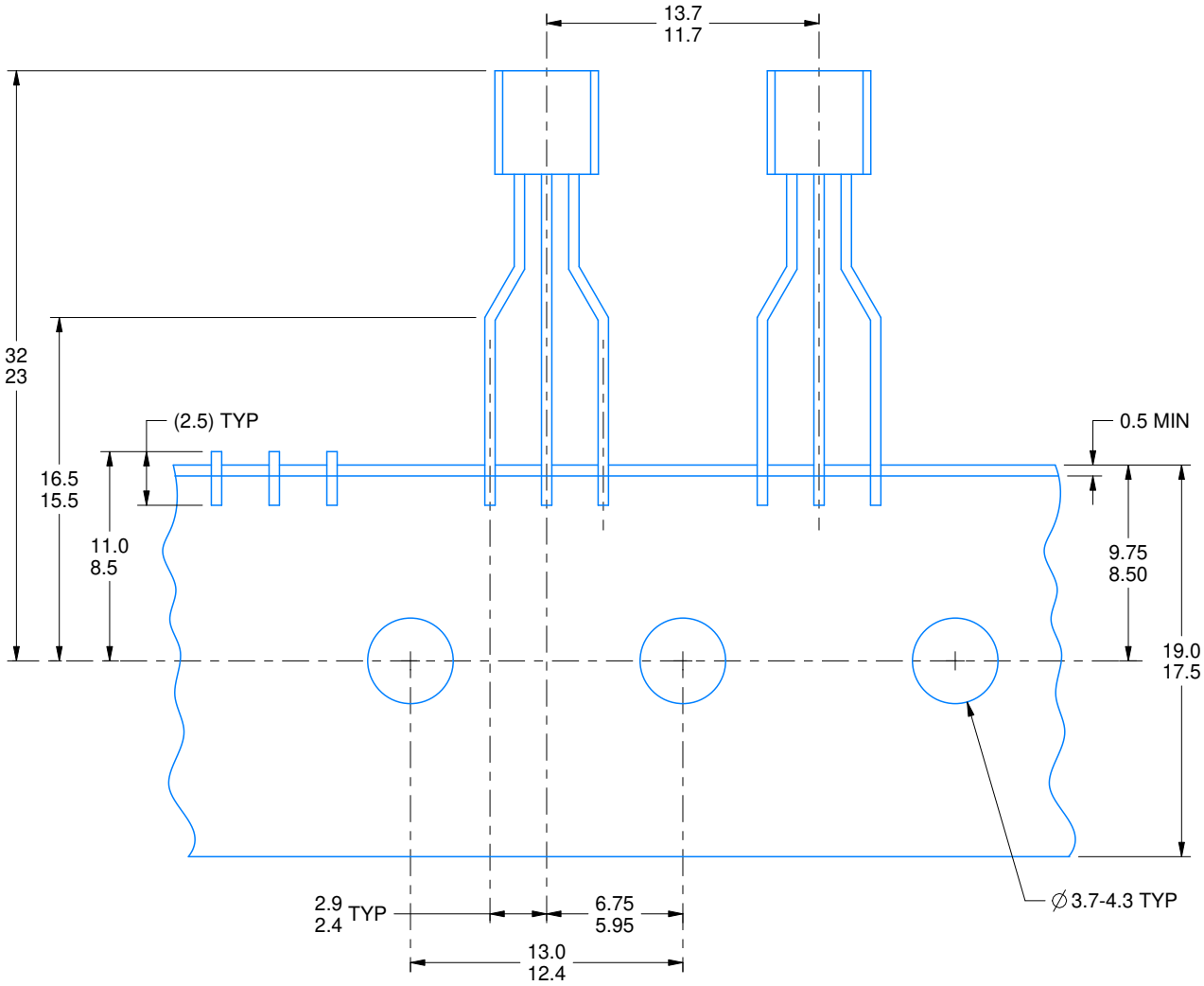
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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