LP3927

LP3927 Cellular/PCS System Power Management IC



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National Semiconductor

LP3927
Cellular/PCS System Power Management IC

General Description

The LP3927 system power management IC is designed for cellular/PCS handsets as well as other portable systems that require intelligent power management. Each device contains five low-dropout linear regulators (LDO's), a reset timer, a power-up control logic, a general-purpose open drain output that can be used to light LEDs, and a CMOS rail-to-rail input/output operational amplifier.

Each linear regulator features an extremely low dropout voltage of 100 mV (typ) at maximum output current. LDO1 and LDO2 are powered on and off by either the KYBD or the $\overline{\text{VEXT}}$ pin. LDO3, LDO4 and LDO5 each have its independent enable pin. LDO1 and LDO4 are rated at 150 mA each, LDO2 and LDO5 are rated at 200 mA each and LDO3 is rated at 100 mA. All LDO's are optimized for low noise and high isolation.

The open drain output current sink can be programmed up to 150 mA by using an external low cost resistor.

A single supply, low voltage operational amplifier has rail to rail input and output with 600 kHz of gain-bandwidth product.

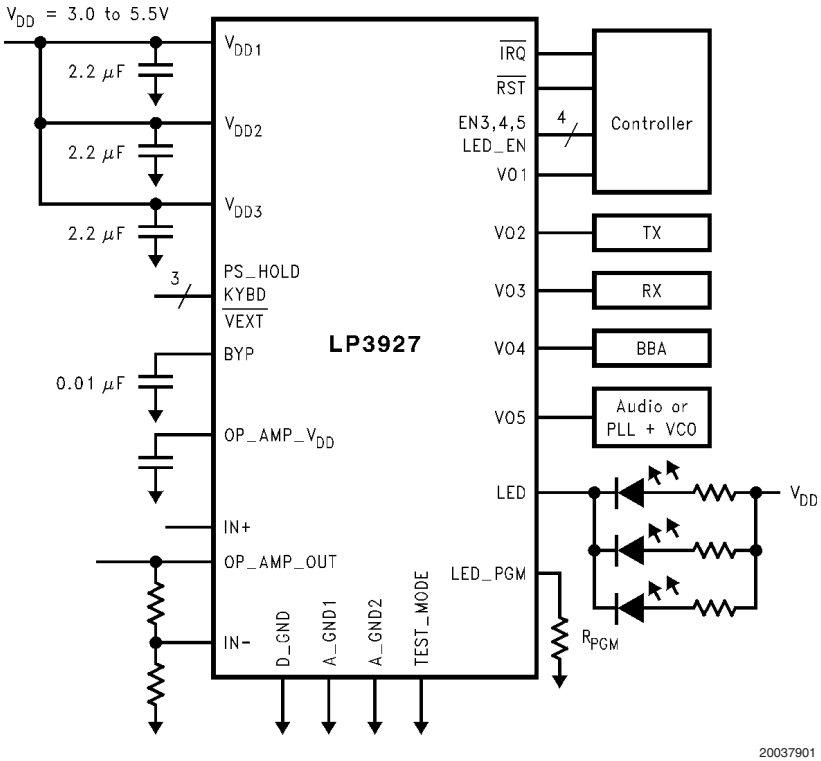
Key Specifications

- 3.0V to 5.5V Input Voltage Range
- Two 200 mA, Two 150 mA and One 100 mA LDO's
- 100 mV typ Dropout Voltage @ I_{MAX}
- 150 mA General-Purpose Open-drain programmable current sink for back light LED
- Low Voltage Rail to Rail Input/Output Operational Amplifier
- 28 pin LLP package

Applications

- Cellular/PCS handsets
- PDA's, Palmtops, and portable terminals
- Single–Cell Li+ Systems
- 2- or 3- Cell NiMH, NiCd or Alkaline System

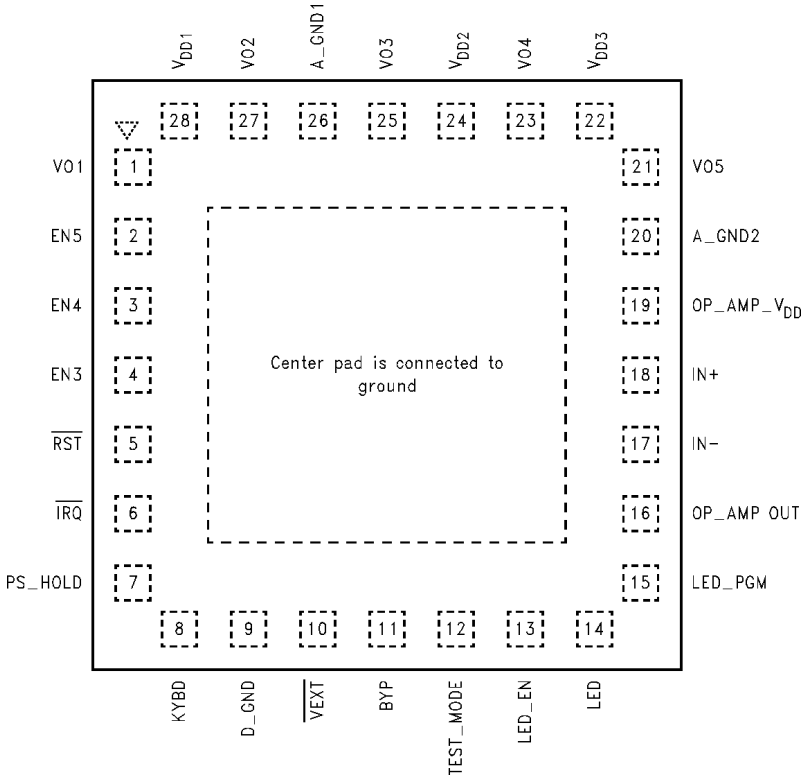
Typical Application Circuit



V_{DD1}, V_{DD2} and V_{DD3} must be tied together externally. Collectively called V_{DD}.

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LP3927 Pin Out Diagram (Top View)



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Output Current Rating and Voltage Options

	I_{MAX} (mA)	Voltage Options (V)
LDO1	150	1.8, 1.9, 2.5, 2.6*, 2.7
LDO2	200	1.8, 2.85*, 2.9, 3.0
LDO3	100	2.7, 2.8, 2.9*, 3.0
LDO4	150	2.7, 2.8, 2.9*, 3.0
LDO5	200	2.7, 2.8, 2.9, 3.0*

	I_{MAX} (mA)	Voltage Options (V)
LDO1	150	1.85*, 1.9, 2.5, 2.6, 2.7
LDO2	200	1.8, 2.85*, 2.9, 3.0
LDO3	100	2.7, 2.85*, 2.9, 3.0
LDO4	150	2.6*, 2.85, 2.9, 3.0
LDO5	200	2.7, 2.85*, 2.9, 3.0

	I_{MAX} (mA)	Voltage Options (V)
LDO1	150	1.85*, 1.9, 2.5, 2.6, 2.7
LDO2	200	1.8, 2.85, 2.9, 3.0*
LDO3	100	2.7, 2.85, 2.9, 3.0*
LDO4	150	2.6, 2.85, 2.9, 3.0*
LDO5	200	2.7, 2.85, 2.9, 3.0*

* denotes the voltage options that are available currently. For other options, please contact the National Semiconductor factory sales office/distributors for availability and specifications.
Voltage options in the two tables cannot be mixed and matched.

Ordering Information

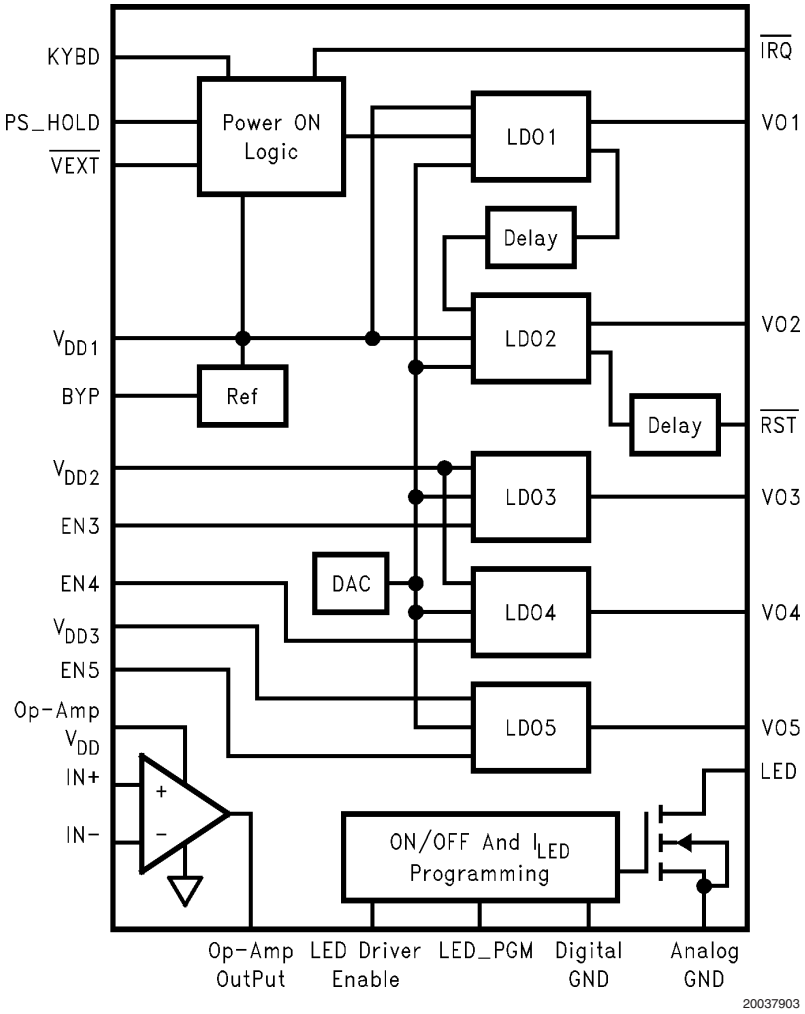
LP3927 Supplied as 1000 Units, tape and reel	LP3927 Supplied as 4500 Units, tape and reel	Standard LDO delay	Optional LDO delay	VO1 (V)	VO2 (V)	VO3 (V)	VO4 (V)	VO5 (V)	TOP MARKING
LP3927ILQ-AH	LP3927ILQX-AH		X	2.6	2.85	2.9	2.9	3.0	3927AH
LP3927ILQ-AJ	LP3927ILQX-AJ	X							3927AJ
LP3927ILQ-AP	LP3927ILQX-AP	X		1.85	2.85	2.85	2.6	2.85	3927AP
LP3927ILQ-AZ	LP3927ILQX-AZ	X		1.85	3.00	3.00	3.00	3.00	3927AZ

For LDO delay options, please refer to Electrical Characteristics Table.

Pin Descriptions

Pin	Name	Functional Description
1	VO1	150 mA, LDO1 output pin.
2	EN5	LDO5 enable input.
3	EN4	LDO4 enable input.
4	EN3	LDO3 enable input.
5	$\overline{RST}$	Externally pulled high, open drain output to processor/memory reset.
6	$\overline{IRQ}$	Externally pulled high, open drain output to processor interrupt indicating KYBD has gone high.
7	PS_HOLD	Input from the processor to the LP3927. A HIGH indicates a steady supply of power is granted. Refer to "Application Hints" section for more detail.
8	KYBD	An active high input signal indicating the keyboard “On/Off” button has been asserted. Refer to "Application Hints" section for more detail.
9	D_GND	Digital ground, used primarily for the digital and DAC circuits.
10	$\overline{VEXT}$	Active low input indicating a battery charger insertion Refer to "Application Hints" section for more detail.
11	BYP	Reference bypass pin.
12	TEST_MODE	Pin used for production testing, factory use only. This pin should be grounded in applications.
13	LED_EN	LED driver enable input.
14	LED	LED driver, drain connection of the LED drive MOSFET.
15	LED_PGM	LED drive current programming pin.
16	OP_AMP_OUT	Operational amplifier output pin.
17	IN–	– input of the Op-Amp.
18	IN+	+ input of the Op-Amp.
19	OP_AMP_V_{DD}	Power supply pin for Op-Amp.
20	A_GND2	Ground for analog.
21	VO5	200 mA, LDO5 output pin.
22	V_{DD3}	Input power pin for LDO5. V_{DD1}, V_{DD2} and V_{DD3} must be tied together externally.
23	VO4	150 mA, LDO4 output pin.
24	V_{DD2}	Input power pin for LDO3 and LDO4. V_{DD1}, V_{DD2} and V_{DD3} must be tied together externally.
25	VO3	100 mA, LDO3 output pin.
26	A_GND1	Ground for analog.
27	VO2	200 mA, LDO2 output pin.
28	V_{DD1}	Input power pin for LDO1 and LDO2. V_{DD1}, V_{DD2} and V_{DD3} must be tied together externally.

Functional Block Diagram



Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

All pins except LED_PGM, BYP, op amp's inputs & output	–0.3V to 6.0V
OP_AMP_OUT, IN-, IN+	-0.3V to 5.5V
GND to GND SLUG	±0.3V
Junction Temperature	150˚C
Storage Information	–65˚C to 150˚C
Soldering Temperature	
Pad Temperature	235˚C
Maximum Power Dissipation (Note 3)	2.6W
ESD (Note 4):	
KYBD	4 kV
All other pins	2 kV

Operating Ratings (Notes 1, 2)

V_{DD1}, V_{DD2}, V_{DD3}, KYBD, OP_AMP_V_{DD}	3.0V to 5.5V
EN3, EN4, EN5	–0.3V to (V_{DD} + 0.3V)
C_{OUT}:	
Capacitance	1.0 µF to 20.0 µF
ESR	0.005Ω to 0.5Ω
Junction Temperature	–40˚C to 125˚C
Operating Temperature	–40˚C to 85˚C
Thermal Resistance (Note 5)	
θ_{JA} (LLP28)	30.8˚C/W
Maximum Power Dissipation (Note 6)	1.78W

Electrical Characteristics, LDO's

Unless otherwise noted, $V_{DD} = V_{OUT(target)} + 0.7V$, C_{IN} (V_{DD1}, V_{DD2}, V_{DD3}) = 4.7 µF, C_{OUT} (VO1 to VO5) = 2.2 µF, C_{byp} = 0.1 µF. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, –40˚C to +85˚C. (Notes 7, 8)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{DD}	Input Voltage Range	V_{DD1}, V_{DD2}, V_{DD3},KYBD	3.7	3	5.5	V
ΔV_{OUT}	Output Voltage Tolerance	$I_{OUT} = I_{MAX}/2$, V_{DD} = 3.7V		**–2**	**+2**	%
	Load Regulation	I_{OUT} = 100 µA to I_{MAX}, V_{DD} = 3.7V		**–2**	**+2**	%
	Line Regulation	$V_{DD} = V_{OUT(target)}$ +0.7V to 5.5V, $I_{OUT} = I_{MAX}/2$		**–40**	**+40**	mV
	Total Accuracy Error			**–3.5**	**+3.5**	%
$V_{IN} - V_{OUT}$	Dropout Voltage	$I_{OUT} = I_{MAX}$ (Note 9)	100		170 **200**	mV
e_N	Output Noise Voltage	I_{OUT} = 100 µA, 10 Hz ≤ f ≤ 100 kHz	27			μV_{rms}
PSRR	Power Supply Ripple Rejection Ratio	C_{IN} = 2.2µF, $I_{OUT} = I_{MAX}$, f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	 45 45 30 10			dB
	Cross Talk	(Note 10)	30			dB
I_Q	Quiescent Current	I_{OUT} = 0, PS_HOLD = KYBD = 0 $\overline{VEXT} = V_{DD}$			5 **8**	µA
I_{GND}	Ground Current	$I_{OUT1} = I_{OUT2}$ = 1 mA, LDO3, LDO4, LDO5 OFF	100		**200**	µA
		I_{OUT1}, I_{OUT2}, I_{OUT3}, I_{OUT4}, $I_{OUT5} = I_{MAX}$	400		**950**	
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0V	400			% of I_{MAX}
C_{OUT}	Output Capacitor	Capacitance		**1**	**20**	µF
		ESR		**5**	**500**	mΩ
R_{SHUNT}	$V_{O2} - V_{O5}$ Output Shunt Resistor		70		**200**	Ω

Electrical Characteristics, Digital Interface

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{OL}	Logic Low Output	$\overline{RST}$ and $\overline{IRQ}$ I_{LOAD} = 250 µA			**150**	mV
V_{IH}	Logic High Input	KYBD and $\overline{VEXT}$		0.7 V_{DD}		V
		EN3–5, PS_HOLD		1.4		
		LED_EN for AH and AJ options		0.85V_{DD}		
		LED_EN for AP and AZ options		2.0		
V_{IL}	Logic Low Input	KYBD and $\overline{VEXT}$			0.2 V_{DD}	V
		EN3–5, PS_HOLD			0.4	
		LED_EN for AH and AJ options			0.2 V_{DD}	
		LED_EN for AP and AZ options			0.4	
$I_{LEAKAGE}$	Input Leakage Current	$\overline{VEXT}$, PS_HOLD, $\overline{IRQ}$, KYBD, EN3–5, 0V ≤ V_{DD} ≤ 5.5V		**–10**	**+10**	µA

Electrical Characteristics, Error Flag

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{Th-H}	Error Flag High	V_{o1} and V_{o2} Outputs (Note 11)	95	92	98	% V_{OUT}
V_{Th-L}	Error Flag Low		90	89	92	
$t_{DELAY-H}$		(Note 12)	6	0	10	µs
$t_{DELAY-L}$			6	0	10	µs
	Keyboard Debounce Delay	(Note 13)	32	16	64	ms
	$\overline{VEXT}$ Debounce Delay	(Note 13)	32	16	64	ms
R_{DELAY}	$\overline{RST}$ Reset Delay	(Note 14)	20	10	40	ms
t_{DELAY}	LDO Delay, standard	(Note 15)	125	0	250	µs
	LDO Delay, optional		10	5	20	ms
$t_{Hold-UP}$	PS_HOLD Input	(Note 16)	500	250	1000	ms

Electrical Characteristics, Backlight LED Driver

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{LED}	Drive Current	V_{LED} = 1V, R_{PGM} = 130kΩ	150	125	175	mA

Electrical Characteristics, Operational Amplifier

Unless otherwise noted, $V_{OP_AMP_VDD}$ = 3.3V, V_{CM} = V_{OUT} = $V_{OP_AMP_VDD}$/2 and R_{LOAD} > 1 MΩ. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, –40˚C to +85˚C. (Note 7)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{DD}	OP_AMP_V_{DD}		3.3	3	5.5	V
V_{OS}	Input Offset Voltage		1.2		10	mV
TC V_{OS}	Offset Voltage Drift		10			µV/˚C
I_B	Input Bias Current		0.2			nA
I_{OS}	Input Offset Current		0.1			nA
R_{IN}	Input Resistance		>1			GΩ
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 2.7V	70			dB
PSRR	Power Supply Rejection Ratio	$V_{OP_AMP_VDD}$ = 2.7V to 3.3V , V_{CM} = 0	60			dB

Electrical Characteristics, Operational Amplifier (Continued)

Unless otherwise noted, $V_{OP_AMP_VDD}$ = 3.3V, $V_{CM} = V_{OUT} = V_{OP_AMP_VDD}/2$ and R_{LOAD} > 1 MΩ. Typical values and limits appearing in normal type apply for T_J = 25˚C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, –40˚C to +85˚C. (Note 7)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
C_{IN}	Common-Mode Input Capacitor		3			pF
V_{OUT}	Output Swing	R_{LOAD} = 2 kΩ			**0.5**	V
				3.1		
I_S	Supply Current	$V_{OP_AMP_VDD}$ = 3.0V	0.5		**1.4**	mA
SR	Slew Rate		0.7			V/µs
GBW	Gain-Bandwidth Product		0.6			MHz

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula

$$P = (T_J - T_A)/\theta_{JA}, \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 2.6W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150˚C, for T_J, 70˚C for T_A, and 30.8˚C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70˚C. Less power can be dissipated safely at ambient temperatures above 70˚C. The Absolute Maximum power dissipation can be increased by 32.5 mW for each degree below 70˚C, and it must be derated by 32.5 mW for each degree above 70˚C.

Note 4: The human-body model is used. The human-body model is 100 pF discharged through 1.5 kΩ.

Note 5: This figure is taken from a thermal modeling result. The test board is a 4 layer FR-4 board measuring 101mm x 101mm x 1.6mm with a 3 x 3 array of thermal vias. The ground plane on the board is 50mm x 50mm. Ambient temperature in simulation is 22˚C, still air. Power dissipation is 1W.

Note 6: Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 1.78W rating appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125˚C, for T_J, 70˚C for T_A, and 30.8˚C/W for θ_{JA} into (1) above. More power can be dissipated at ambient temperatures below 70˚C. Less power can be dissipated at ambient temperatures above 70˚C. The maximum power dissipation for operation can be increased by 32.5 mW for each degree below 70˚C, and it must be derated by 32.5 mW for each degree above 70˚C.

Note 7: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested or guaranteed through statistical analysis. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 8: The target output voltage, which is labeled $V_{OUT(target)}$, is the desired or ideal output voltage.

Note 9: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

Note 10: Pulsing the load of LDO X from 100µA to Imax and measuring its effects at the output of LDO Y. LDO Y enabled but under no load.

Note 11: The error flags are internal to the chip. There is no external access to the signals. LDO1 error flag and the LDO2 error flag will go HIGH when the respective LDO reaches its V_{Th-H} value. The error flags will go LOW when the respective LDO reaches its V_{Th-L} value.

Note 12: The $t_{DELAY-H}$ is the delay between LDO1 reaching its V_{Th-H} and its error flag going HIGH. The $t_{DELAY-L}$ is the delay between LDO1 reaching its V_{Th-L} and its error flag going LOW. Same delays apply to LDO2 and its error flag.

Note 13: Refer to Timing Diagram.

Note 14: The delay between LDO2 error flag HIGH and $\overline{RST}$ signal HIGH in the power up sequence. In the power down sequence, it is the delay between $\overline{RST}$ signal LOW and LDO2 disabled.

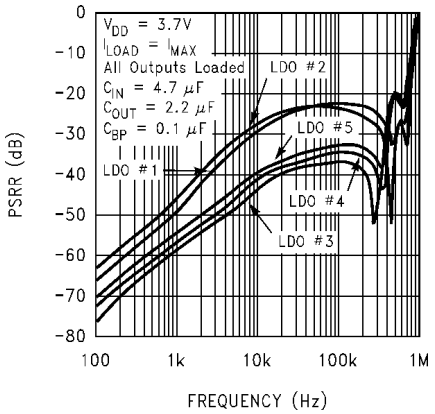
Note 15: The delay between LDO1 error flag HIGH and LDO2 enable in power up sequence. In the power down sequence, it is the delay between LDO2 error flag LOW and LDO1 disable. For the optional LDO delay, please contact the factory for availability.

Note 16: Time between $\overline{RST}$ high and PS_HOLD going high.

Typical Performance Characteristics

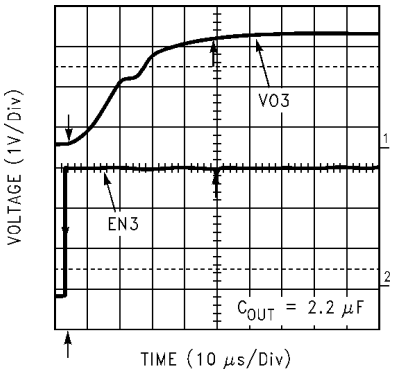
Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{BYP} = 0.01 µF, $V_{DD} = V_{OUT} + 0.2V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{DD}.

PSRR vs Frequency



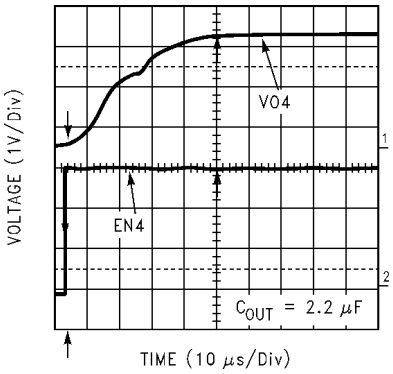
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LDO3 Enable Response (Cout=2.2µF)



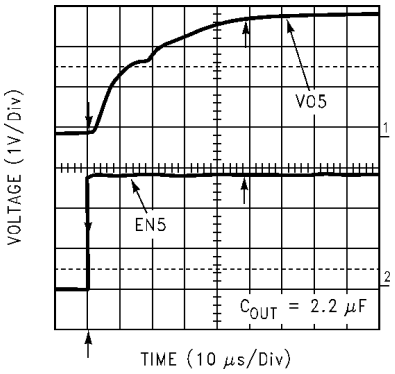
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LDO4 Enable Response (Cout=2.2µF)



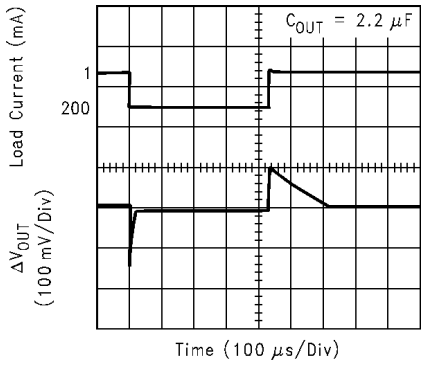
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LDO5 Enable Response (Cout=2.2µF)



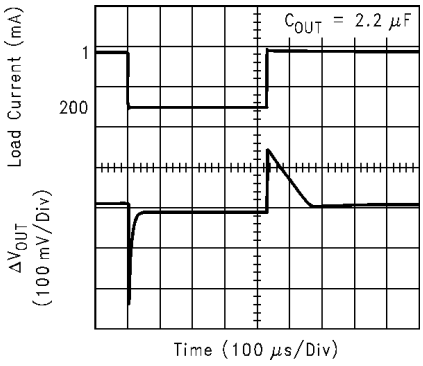
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LDO2 (1.8V Option) Load Transient



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LDO2 (2.85V Option) Load Transient

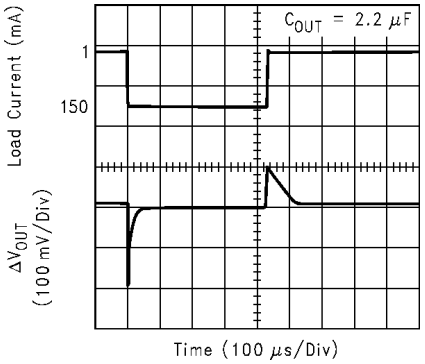


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Typical Performance Characteristics

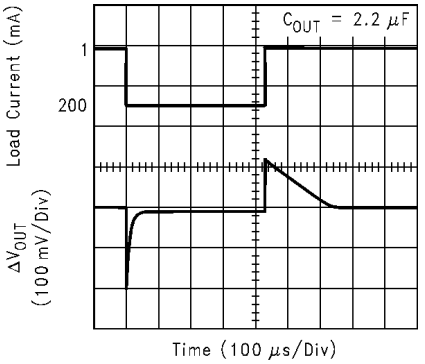
Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{BYP} = 0.01 µF, $V_{DD} = V_{OUT} + 0.2V$, $T_A = 25^{\circ}C$, Enable pin is tied to V_{DD}. (Continued)

LDO4 (2.8V Option) Load Transient



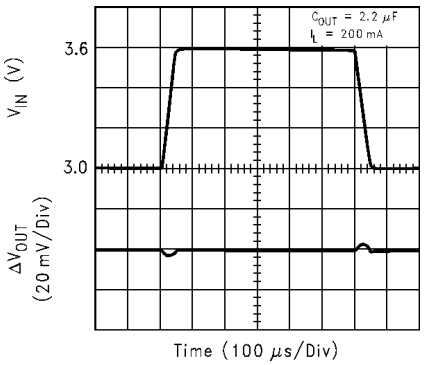
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LDO5 (3.0V Option) Load Transient



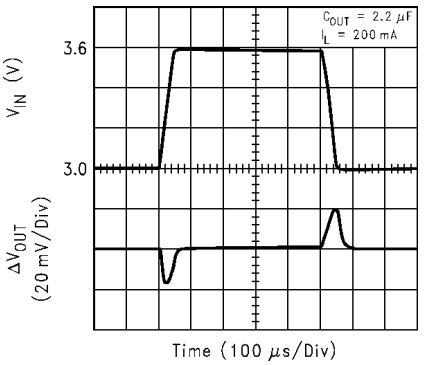
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LDO2 (1.8V Option) Line Transient



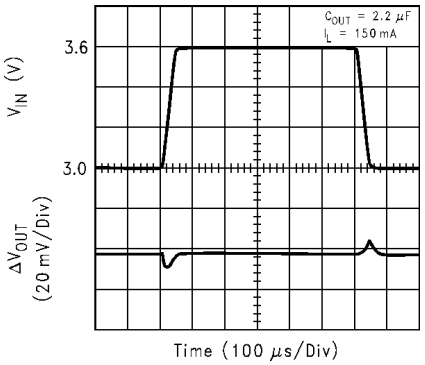
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LDO2 (2.85V Option) Line Transient



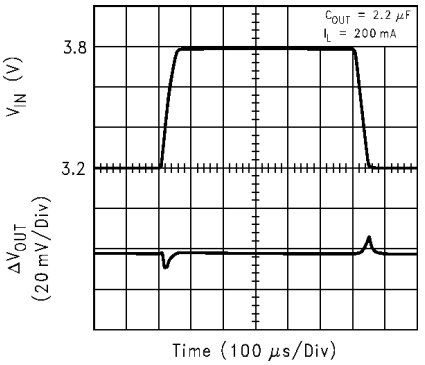
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LDO4 (2.8V Option) Line Transient



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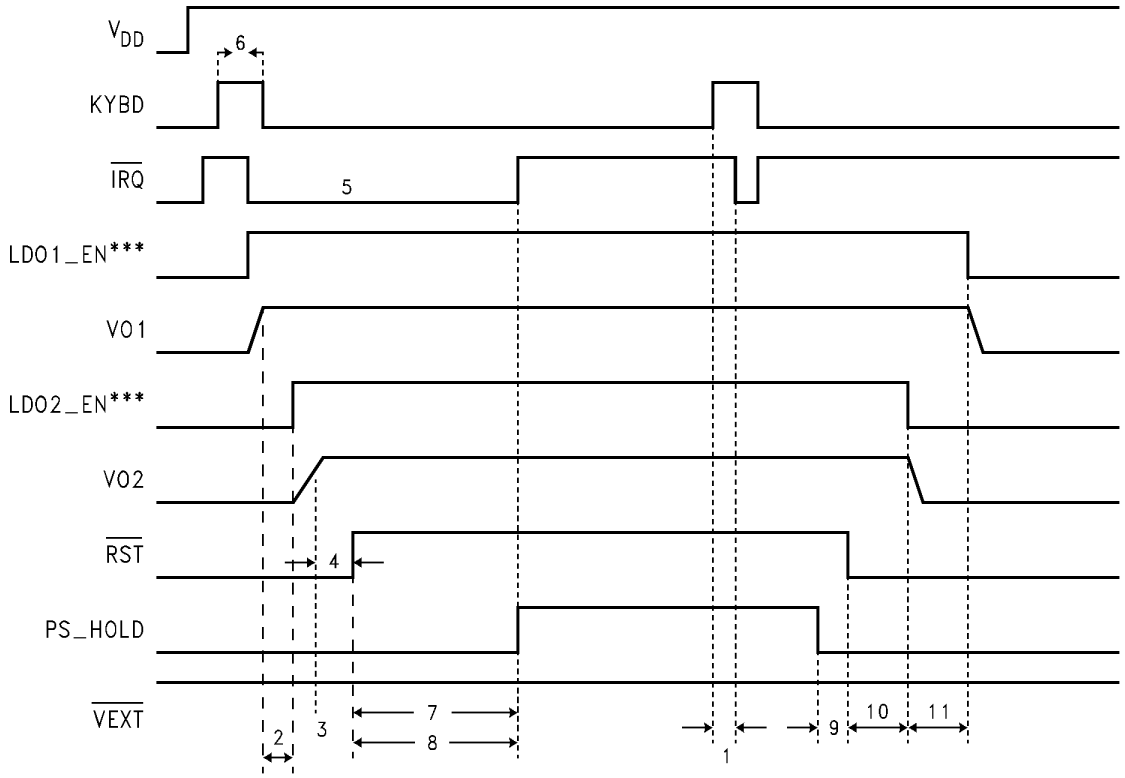
LDO5 (3.0V Option) Line Transient



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Timing Diagrams

Keyboard Start-Up/Shut-Down



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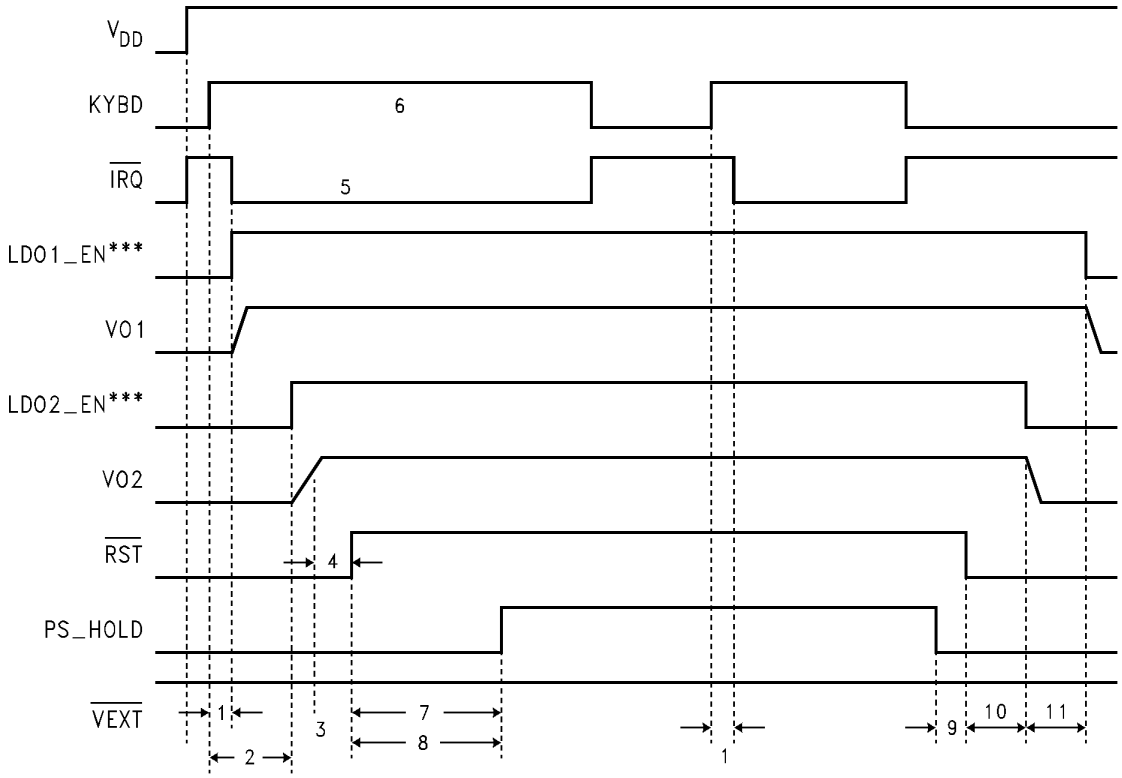
Note: Diagram indicates Open Drain $\overline{IRQ}$ tied to V_{DD}.

*** = Internal signal

1. Keyboard de-bounce delay, 32 msec typ.
2. Delay between LDO1 reaching 95% of its output voltage and LDO2 enable, 125 µsec typical.
3. Both LDO1 and LDO2 outputs reach 95% of respective output voltage, start $\overline{RST}$ timer.
4. $\overline{RST}$ delay, 20 msec typical.
5. $\overline{IRQ}$ is active low.
6. Keyboard press must be greater than 32 msec.
7. PS_HOLD timer begins upon $\overline{RST}$ going high.
8. Maximum of 500 msec period from $\overline{RST}$ going high to PS_HOLD going high.
9. Response time from PS_HOLD going low to $\overline{RST}$ going low.
10. Delay between $\overline{RST}$ high-low transition to LDO2 disable.
11. Delay between LDO2 disable and LDO1 disable.

Timing Diagrams (Continued)

Keyboard Held at Start-Up/Shut-Down



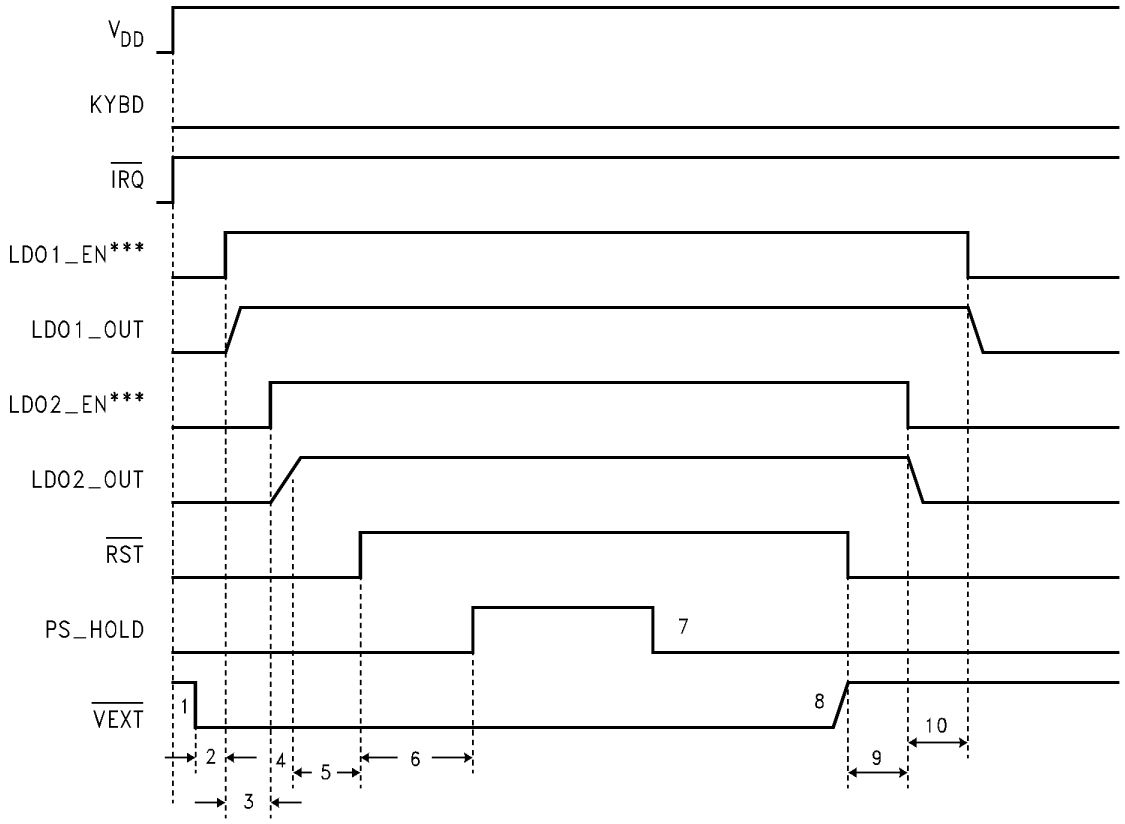
Note: Diagram indicates Open Drain $\overline{IRQ}$ tied to V_{DD}.

*** = Internal signal

1. Keyboard de-bounce delay, 32msec typ.
2. Delay between LDO1 reaching 95% of its output voltage and LDO2 enable.
3. Both LDO1 and LDO2 outputs reach 95% of the respective output voltage, start $\overline{RST}$ timer.
4. Reset delay.
5. $\overline{IRQ}$ is active low.
6. Keyboard press must be greater than 32 msec.
7. PS_HOLD timer begins upon $\overline{RST}$ going high.
8. Maximum of 500 msec period from $\overline{RST}$ going high to PS_HOLD going high.
9. Response time from PS_HOLD going low to $\overline{RST}$ going low.
10. Delay between $\overline{RST}$ high-low transition to LDO2 disable.
11. Delay between LDO2 disable and LDO1 disable.

Timing Diagrams (Continued)

VEXT Detect Start-Up/Shut Down



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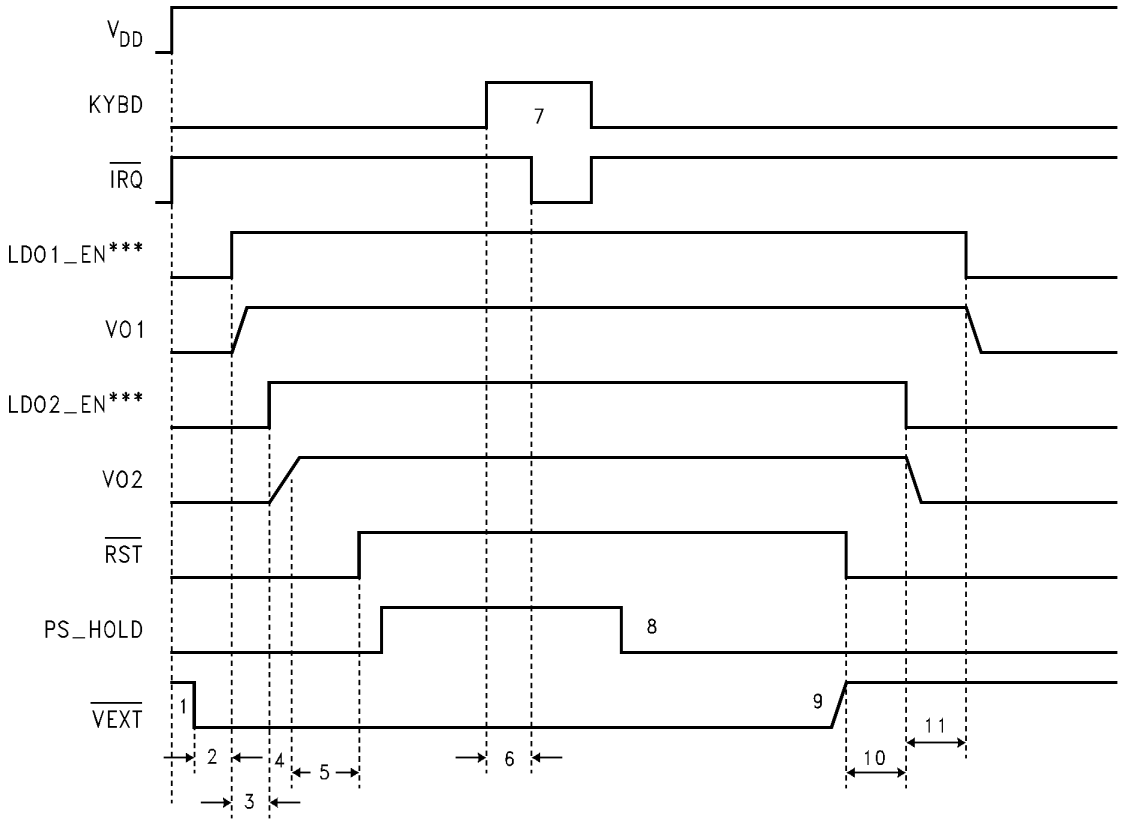
Note: Diagram indicates Open Drain $\overline{IRQ}$ tied to V_{DD}.

*** = Internal signal

1. $\overline{VEXT}$ goes active low.
2. $\overline{VEXT}$ 32 msec de-bounce period.
3. Delay between LDO1 and LDO2 enables.
4. Both LDO1 and LDO2 outputs reach 95% of respective output voltage, start Reset timer.
5. Reset delay.
6. Period between Reset and PS_HOLD going high is not relevant since $\overline{VEXT}$ is low
7. PS_HOLD goes low but LDOs continue to run since $\overline{VEXT}$ is low.
8. PS_HOLD is low and $\overline{VEXT}$ goes high, $\overline{RST}$ pin goes low.
9. Delay between $\overline{RST}$ going low and LDO2 disabled.
10. Delay between LDO2 and LDO1 disabled.

Timing Diagrams (Continued)

VEXT Detect W/Keyboard Interrupts



Note: Diagram indicates Open Drain $\overline{IRQ}$ tied to V_{DD}.

*** = Internal signal

1. $\overline{VEXT}$ goes active low.
2. $\overline{VEXT}$ 32 msec de-bounce period.
3. Delay between LDO1 and LDO2 enable.
4. Both LDO1 and LDO2 outputs reach 95% of respective output voltage, start Reset timer.
5. Reset delay.
6. Keyboard de-bounce delay.
7. Keyboard pulse must be a minimum of 32 msec.
8. PS_HOLD may go low after Key press, but LDOs stay on since $\overline{VEXT}$ is low.
9. $\overline{VEXT}$ goes high, begin shutdown since PS_HOLD is low.
10. Delay between $\overline{RST}$ going low and LDO2 disabled.
11. Delay between LDO2 disable and LDO1 disabled.

Application Hints

LP3927 FUNCTION DESCRIPTION

The LP3927 is designed for cellular/PCS handsets. The LDOs power the microprocessor, RF and digital sections of the phone. When a KYBD debounce of longer than 32 ms is detected by the LP3927, the $\overline{IRQ}$ signal is asserted and sent to the microprocessor. In addition, the KYBD signal turns on LDO1. When LDO1 reaches 95% of its output voltage option, a 125 µs delay (standard LDO delay. The optional LDO delay has a 10msec delay) takes place, and LDO2 turns on. When LDO2 reaches 95% of its output voltage option, $\overline{RST}$ goes high after a 20 ms delay. At this point, the microprocessor comes out of reset and the LP3927 starts the PS_HOLD timer. If PS_HOLD goes high before 500 ms, $\overline{IRQ}$ is de-asserted. If PS_HOLD stays low for longer than 500 ms, $\overline{IRQ}$ will still de-assert, but $\overline{RST}$ will also be asserted, and the part will power down.

The power down sequence is the exact reverse of the power up sequence. PS_HOLD from the microprocessor goes low, indicating a request to turn the part off. This causes $\overline{RST}$ to go low. LDO2 will be turned off after a 20 ms delay. When LDO2 drops to 90% of its output voltage option, LDO1 will start to turn off after a 125 µs (or a 10msec) delay. Another KYBD debounce after power up does not necessary mean power down.

Whenever LDO1 or LDO2 falls under 90% of the output voltage option, $\overline{RST}$ immediately goes low to bring PS_HOLD low in order to turn the part off.

Plugging the charger into the cell phone will cause an external signal $\overline{VEXT}$ to toggle from high to low. The LP3927 will respond differently to this signal depending on the scenario:

Case 1: If a charger is plugged into the cell phone after the phone is already on, the $\overline{VEXT}$ signal go from high to low. The LP3927 will acknowledge this signal but all other signals remain unchanged.

Case 2: If a charger is plugged into the phone while the phone is off, $\overline{VEXT}$ signal goes from high to low and the LP3927 will proceed to turn LDO1 on after a 32 ms delay, and the identical power-up sequence follows. This case bypasses the power-up initiated by KYBD and $\overline{IRQ}$. KYBD remains low and $\overline{IRQ}$ remains high at all time during power-up.

When the charger is plugged in, the phone cannot be turned off unless both $\overline{VEXT}$ goes high and PS_HOLD goes low.

LDOs

The LP3927 contains five LDOs. LDO1 and 2 are powered by the V_{DD1} line; LDO3 and 4 are powered by the V_{DD2} line; and LDO5 is powered by the V_{DD3} line. V_{DD1}, V_{DD2} and V_{DD3} must be tied together externally. All five LDOs accept an input voltage from 3.0V to 5.5V. This accommodates the full usable range of a single Li-On battery.

LDO1 and 4 each provide 150 mA of current. LDO2 and 5 each provide 200 mA of current. LDO3 provides 100 mA of current. The output of each LDO can be programmed to different voltage levels at the factory. Refer to “Output Current Rating and Voltage Options” Table for more details.

LDO INPUT CAPACITOR

An input capacitance of ≈ 2.2 µF is required between each V_{DD} input pins and ground. (The amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the inputs.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and termperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≈ 1 µF over the entire operating temperature range.

LDO OUTPUT CAPACITOR

The LDOs are designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (X7R, X5R, Z5U, or Y5V) in 1 µF to 20 µF range with 5 mΩ to 500 mΩ ESR range is suitable in the LP3927 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost.

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 mΩ to 500 mΩ).

LED CURRENT DRIVER

The LED pin on the LP3927 is an open-drain output that can provide up to 150 mA to drive backlight LEDs. It is turned on when the LED_EN pin is pulled high, and off when the LED_EN pin is pulled low. The external resistor R_{PGM} connected to the LED_PGM pin programs the output current of LED. A 130 kΩ resistor sets the output current to 150 mA. An ***approximated*** equation between R_{PGM} and I_{LED} is:

$$ILED = \frac{19235}{R_{PGM}}$$

OPERATIONAL AMPLIFIER

The LP3927 has an internal op amp with rail-to-rail input and output and a 600 kHz of gain-bandwidth product.

LEADLESS LEADFRAME PACKAGE (LLP)

The LP3927 is packaged in a 28-lead LLP package for enhanced thermal performance. The 28-lead LLP measures 5 mm x 5 mm x 0.75 mm. Its small size and low profile is ideal for handset applications and other portable applications that require power management.

THERMAL PERFORMANCE

The LLP package is designed for enhanced thermal performance because of the exposed die attach pad at the bottom center of the package. It brings advantage to thermal performance by creating a very direct path for thermal dissipation. Compared to the traditional leaded packages where the die attach pad is embedded inside the mold compound, the LLP reduces a layer in the thermal path.

The thermal advantage of the LLP package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board and thermal vias are planted underneath the thermal land. Based on a LLP thermal mea-

Application Hints (Continued)

surement, junction to ambient thermal resistance (θ_{JA}) can be improved by as much as two times if a LLP is soldered on the board with thermal land and thermal vias than if not.

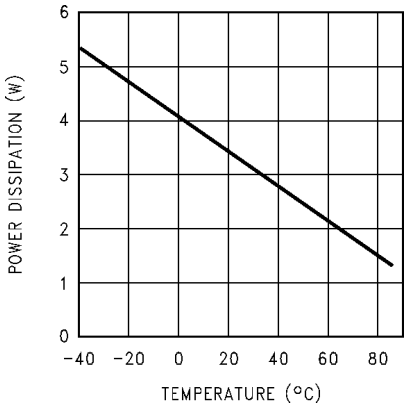
Consider the following equation:

$$P = \frac{(T_J - T_A)}{\theta_{JA}}$$

Where P is the power dissipated, T_J is the maximum junction temperature of the die, T_A is the ambient temperature, and θ_{JA} is the thermal resistance of the package. T_J is specified at 150˚C.

According to the above equation, in the case where the LP3927 is dissipating 3W of power, T_A is limited to 32.6˚C when T_J of 125˚C and θ_{JA} of 30.8˚C/W are used in the equation. In order to operate at a higher ambient temperature, power dissipation has to be reduced. A curve of maximum power dissipation vs ambient temperature is provided below.

Power Dissipation vs Ambient Temperature (θ_{JA}=30.8˚C/W)



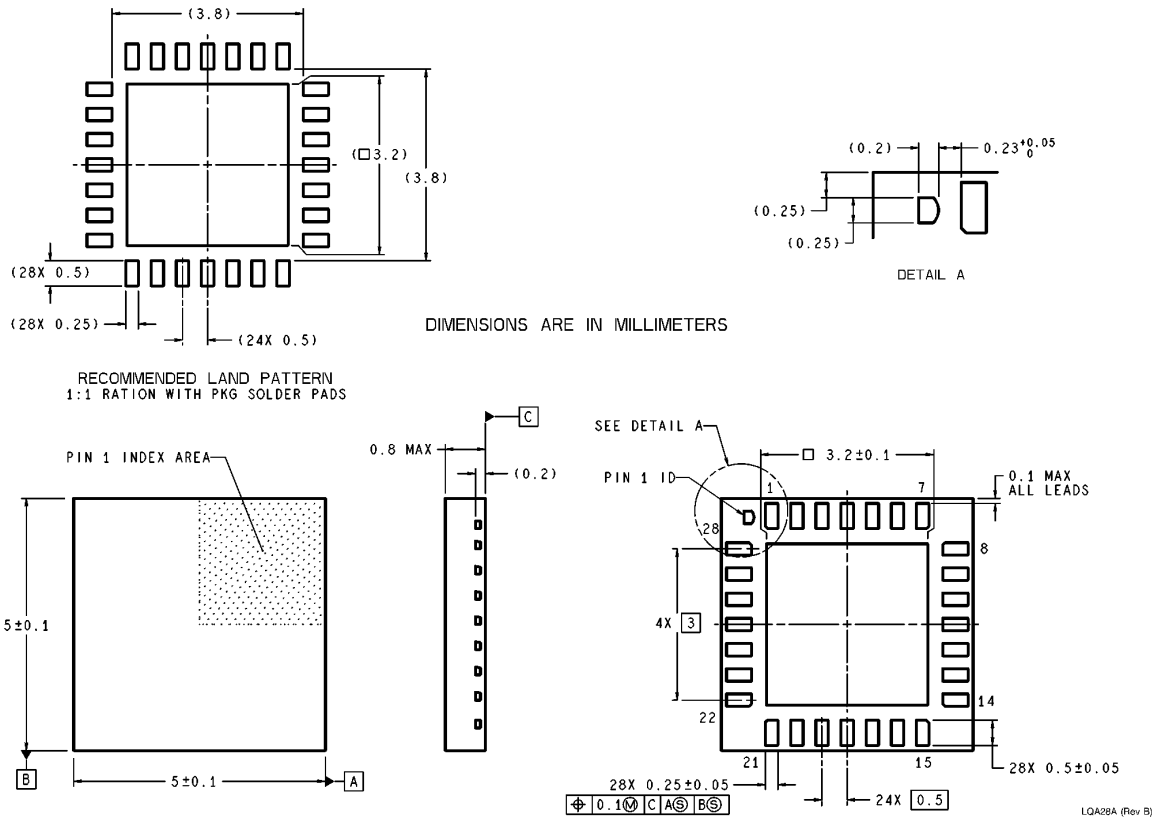
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LAYOUT CONSIDERATION

The LP3927 has an exposed die attach pad located at the bottom center of the LLP package. It is imperative to create a thermal land on the PCB board when designing a PCB layout for the LLP package. The thermal land helps to conduct heat away from the die, and the land should be the same dimension as the exposed pad on the bottom of the LLP (1:1 ratio). The land should be on both the top and the bottom layer of the PCB board. In addition, thermal vias should be added inside the thermal land to conduct more heat away from the surface of the PCB to the ground plane. Typical pitch and outer diameter for these thermal vias are 1.27 mm and 0.33 mm respectively. Typical copper via barrel plating is 1 oz. although thicker copper may be used to improve thermal performance. The LP3927 bottom pad is connected to ground. Therefore, the thermal land and vias on the PCB board need to be connected to ground.

For more information on board layout techniques, refer to Application Note 1187 “Leadless Leadframe Package (LLP).” The application note also discusses package handling, solder stencil, and assembly process.

Physical Dimensions inches (millimeters) unless otherwise noted



28 Lead LLP Package
NS Package Number lqa28A

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