LPC47N217N

56-Pin Super I/O with LPC Interface

PRODUCT FEATURES

Data Brief

- 3.3 Volt Operation (5V tolerant)
- Programmable Wakeup Event Interface (IO_PME# Pin)
- SMI Support (IO_SMI# Pin)
- GPIOs (13)
- Two IRQ Input Pins
- XNOR Chain
- PC2001
- ACPI 2.0 Compliant
- 56-pin QFN Lead-free RoHS Compliant package
- Intelligent Auto Power Management
- Serial Port
  - One Full Function Serial Port
  - High Speed 16C550A Compatible UART with Send/Receive 16-Byte FIFO
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - Multiple Base I/O Address options and 15 IRQ Options
- Multi-Mode Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 15 IRQ and 3 DMA Options
- LPC Bus Host Interface
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI CLKRUN# Support
  - Power Management Event (IO_PME#) Interface Pin

ORDER NUMBER(S):

LPC47N217N-ABZJ for 56-pin QFN Lead-free ROHS Compliant package

LPC47N217N-ABZJ-TR for 56-pin QFN Lead-free ROHS Compliant package (tape and reel)

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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General Description

The SMSC LPC47N217N is a 3.3V PC 99, PC2001, and ACPI 2.0 compliant Super I/O Controller. The LPC47N217N implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part also includes 13 GPIO pins.

The LPC47N217N incorporates a 16C550A compatible UART and one Multi-Mode parallel port with ChiProtect™ circuitry plus EPP and ECP support. The LPC47N217N is easy to use and offers lower system cost and reduced board area.

The LPC47N217N offers a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI CLKRUN# support, relocatable configuration ports, and three DMA channel options.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect™ circuitry prevents damage caused by an attached powered printer when the LPC47N217N is not powered.

The LPC47N217N features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the parallel port and UART.

The LPC47N217N supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows operating systems, PC99, and PC2001. The I/O Address, DMA Channel, and Hardware IRQ of each device in the LPC47N217N may be reprogrammed through the internal configuration registers. There are multiple I/O address location options, a Serialized IRQ interface, and three DMA channels.

Block Diagram

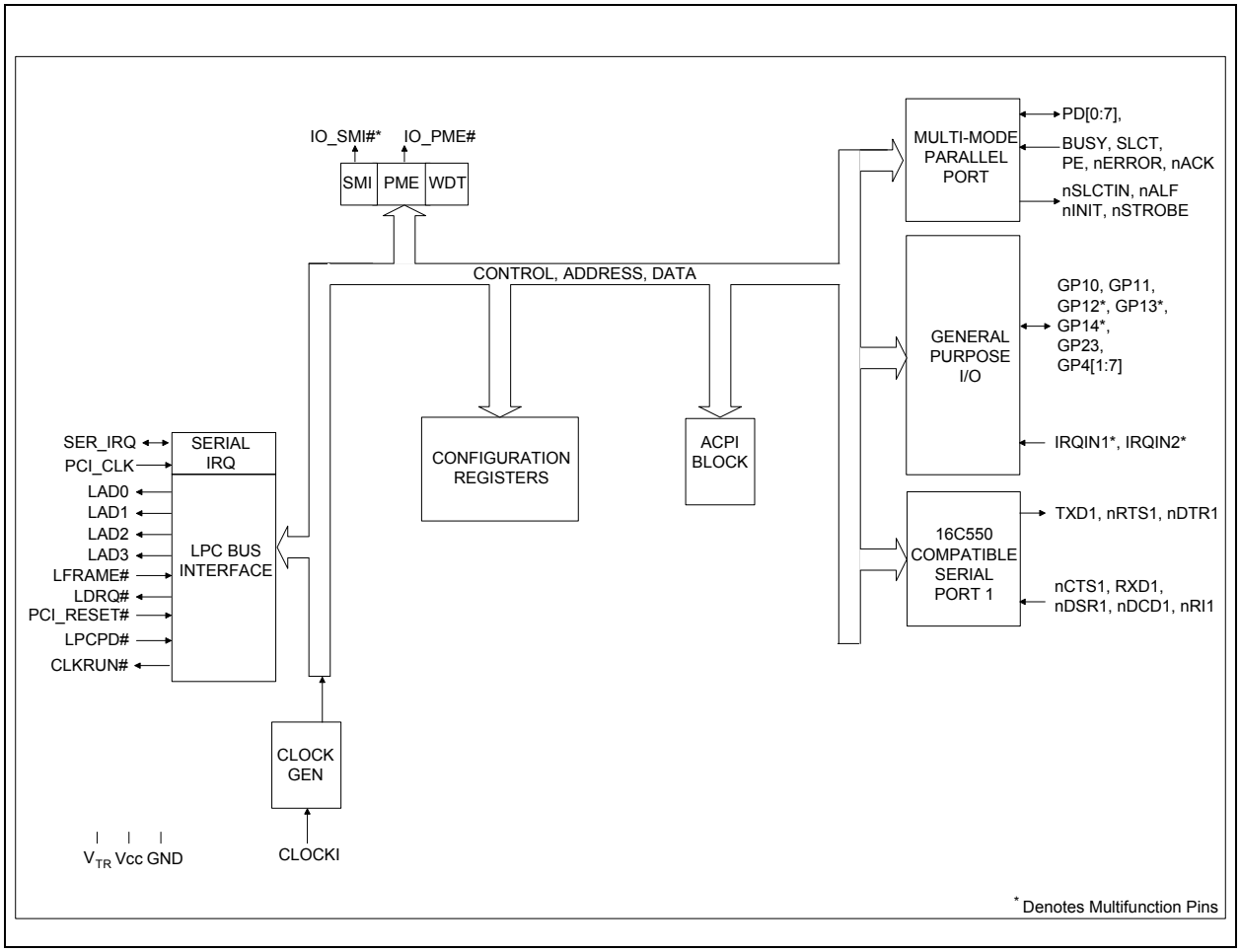
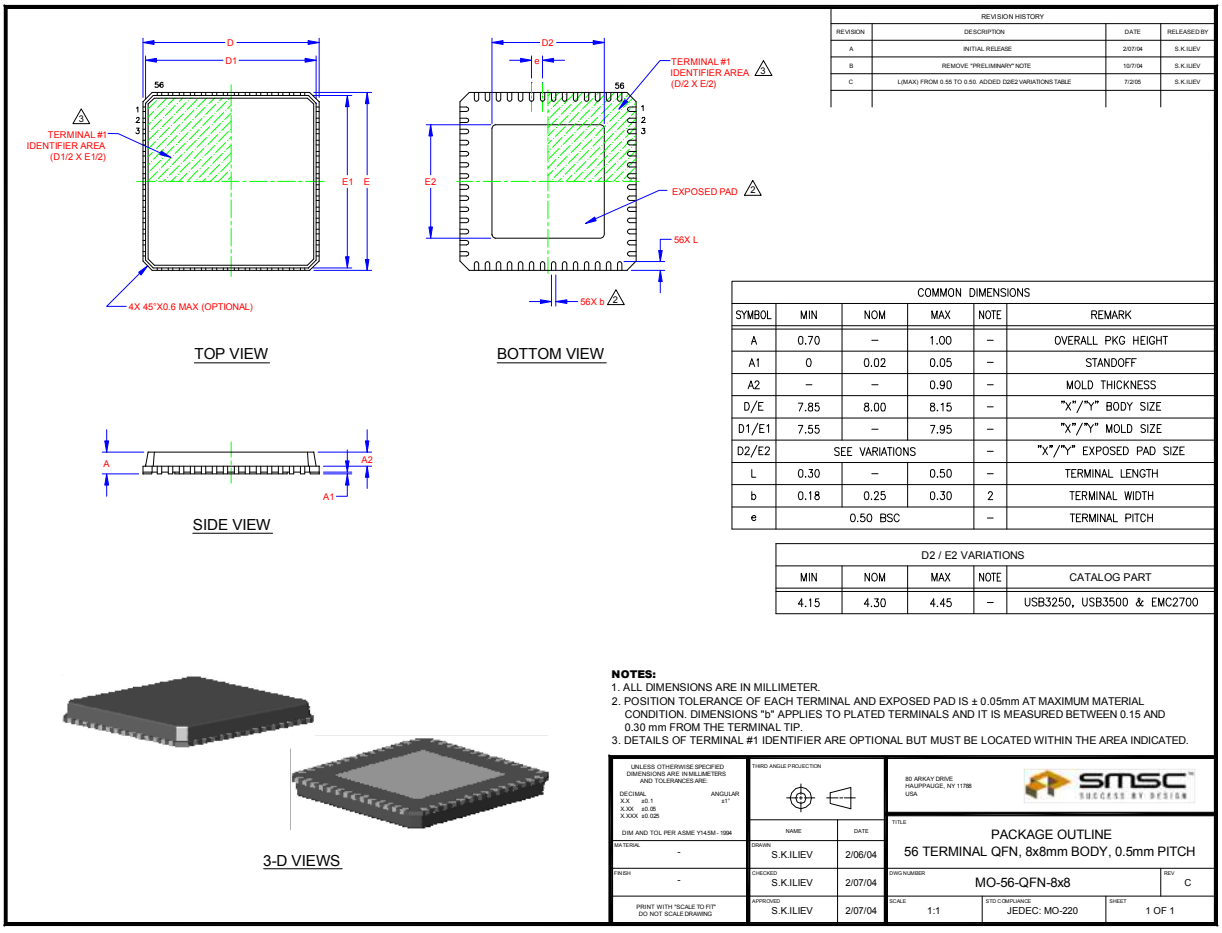


Figure 1 LPC47N217N Block Diagram

PRODUCT PREVIEW

Package Outline



REVISION HISTORY

REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	2/07/04	S.K.ILIEV
B	REMOVE "PRELIMINARY" NOTE	10/7/04	S.K.ILIEV
C	L(MAX) FROM 0.55 TO 0.50. ADDED D2/E2 VARIATIONS TABLE	7/2/05	S.K.ILIEV

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	–	1.00	–	OVERALL PKG HEIGHT
A1	0	0.02	0.05	–	STANDOFF
A2	–	–	0.90	–	MOLD THICKNESS
D/E	7.85	8.00	8.15	–	"X"/"Y" BODY SIZE
D1/E1	7.55	–	7.95	–	"X"/"Y" MOLD SIZE
D2/E2	SEE VARIATIONS			–	"X"/"Y" EXPOSED PAD SIZE
L	0.30	–	0.50	–	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			–	TERMINAL PITCH

D2 / E2 VARIATIONS

MIN	NOM	MAX	NOTE	CATALOG PART
4.15	4.30	4.45	–	USB3250, USB3500 & EMC2700

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025; ANGULAR ±1°
DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL: -
FINISH: -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	S.K.ILIEV	2/06/04
CHECKED	S.K.ILIEV	2/07/04
APPROVED	S.K.ILIEV	2/07/04

80 ARKAY DRIVE
HAUPPAUGE, NY 11788
USA

TITLE: PACKAGE OUTLINE
56 TERMINAL QFN, 8x8mm BODY, 0.5mm PITCH

DWG NUMBER: MO-56-QFN-8x8 REV: C
SCALE: 1:1
STD COMPLIANCE: JEDEC: MO-220
SHEET: 1 OF 1

Figure 2 LPC47N217N 56-Pin QFN Package, 8x8mm Body, 0.5mm Pitch

PRODUCT PREVIEW