LSF0102-Q100

2-bit bidirectional multi-voltage level translator; open-drain; push-pull

Rev. 4 — 24 June 2024 Product data sheet

1. General description

The LSF0102-Q100 is a 2 channel bidirectional multi-voltage level translator for open-drain and push-pull applications. It supports up to 100 MHz up translation and ≥100 MHz down translation at ≤ 30 pF capacitive load. There is no need for a direction pin which minimizes system effort. The LSF0102-Q100 supports 5 V tolerant I/O pins for compatibility with TTL levels in a variety of applications. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +125 °C
- Bidirectional voltage translation with no direction pin
- Up translation
  - ≤ 100 MHz; C_L = 30 pF
  - ≤ 50 MHz; C_L = 50 pF
- Down translation
  - ≥ 100 MHz; C_L = 30 pF
  - ≥ 50 MHz; C_L = 50 pF
- Hot insertion
- Bidirectional voltage level translation between:
  - 0.95 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.8 V and 2.5 V, 3.3 V and 5.0 V
  - 2.5 V and 3.3 V and 5.0 V
  - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I/O pins to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O pins for EN = Low.
- Flow-through pinout for easy PCB trace routing.
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
LSF0102DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
LSF0102DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

5. Marking

Table 2. Marking

Type number	Marking code[1]
LSF0102DP-Q100	h2
LSF0102DC-Q100	h2

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

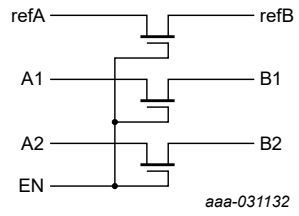
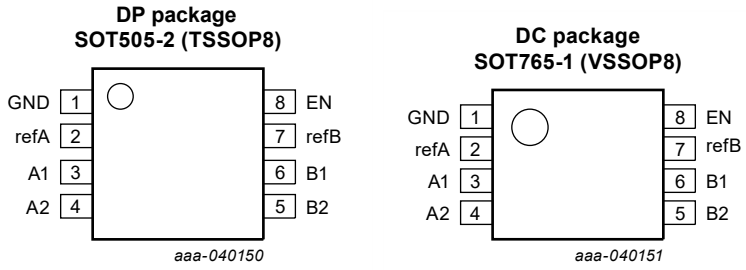


Fig. 1. Logic symbol

7. Pinning information

7.1. Pinning LSF0102



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7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1	ground (0 V)
refA	2	reference voltage A
A1	3	data input/output A
A2	4	data input/output A
B2	5	data input/output B
B1	6	data input/output B
refB	7	reference voltage B
EN	8	enable input (active HIGH)

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN	**An, Bn channel**
H	An = Bn
L	Z

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	pins refA, refB, An, Bn and EN	[1]	-0.5	+7.0	V
$I_{I/O}$	input/ouput current	pins refA, refB, An and Bn; continuous channel current		-	+128	mA
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins refA, refB, An, Bn and EN	0.0	5.0	V
$I_{I/O}$	input/ouput current	pins refA, refB, An and Bn; continuous channel current	-	+64	mA
T_{amb}	ambient temperature		-40	+125	°C

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11. Static characteristics

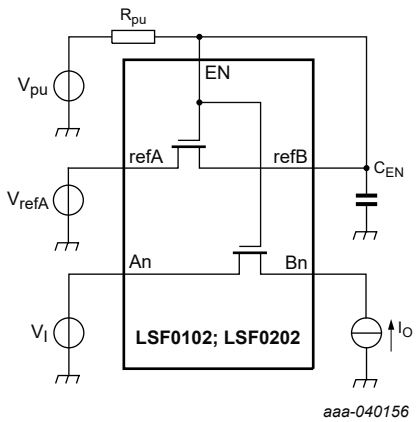
Table 7. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
V_{IK}	input clamping voltage	V_{EN} = 0 V; I_I = -18 mA	-1.2	-	-	V
I_I	leakage current	pins An, Bn, refA, refB and EN; V_I = GND to 5.0 V	-	1	5	µA
C_I	input capacitance	pins refA, refB and EN; V_I = 0 V or 3 V	-	6	-	pF
$C_{io(off)}$	OFF-state input/output capacitance	pins An, Bn; V_O = 0 V or 3 V; V_{EN} = 0.0 V	-	3	6.0	pF
$C_{io(on)}$	ON-state input/output capacitance	pins An, Bn; V_O = 0 V or 3 V; V_{EN} = 3.0 V	-	6	12.5	pF
R_{ON}	ON resistance	see Fig. 2 [2]				
		V_I = 0 V; V_{pu} = 5.0 V; I_O = 64 mA				
		V_{refA} = 3.3 V	-	3	-	Ω
		V_{refA} = 1.8 V	-	4	-	Ω
		V_{refA} = 1.0 V	-	7	-	Ω
		V_I = 0 V; V_{pu} = 5.0 V; I_O = 32mA				
		V_{refA} = 1.8 V	-	4	-	Ω
		V_{refA} = 2.5 V	-	3	-	Ω
		V_I = 1.8 V; V_{pu} = 5.0 V; I_O = 15 mA				
		V_{refA} = 3.3 V	-	4	-	Ω
		V_I = 1.0 V; V_{pu} = 3.3 V; I_O = 10 mA				
		V_{refA} = 1.8 V	-	7	-	Ω
		V_I = 0 V; V_{pu} = 3.3 V; I_O = 10 mA				
		V_{refA} = 1.0 V	-	5	-	Ω
		V_I = 0 V; V_{pu} = 1.8 V; I_O = 10 mA				
		V_{refA} = 1.0 V	-	6	-	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Measured by the voltage drop between the An and Bn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) pins.



R_{pu} = 200 kΩ; C_{EN} = 100 nF (The An and Bn pins may be exchanged.)

Fig. 2. Test circuit for measuring R_{ON}

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12. Dynamic characteristics

Table 8. Switching characteristics

GND = 0 V; for waveform see Fig. 3; for test circuit see Fig. 4

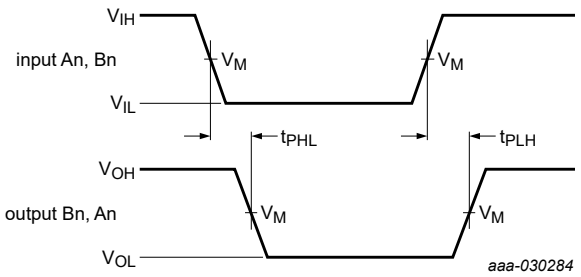
Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Translating down						
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An;				
		$V_{IH} = V_{pu} = V_{refA} + 1\ V$				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.35	-	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	0.8	-	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	1.2	-	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.3	-	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.7	-	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	1.1	-	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An;				
		$V_{IH} = V_{pu} = V_{refA} + 1\ V$				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.5	-	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	1.0	-	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	1.3	-	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.4	-	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.8	-	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	1.2	-	ns
Translating up						
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An;				
		$V_{IH} = V_{refA}$; $V_{EXT} = V_{pu} = V_{refA} + 1\ V$				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.5	-	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	0.9	-	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	1.1	-	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.4	-	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.8	-	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	1.0	-	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An;				
		$V_{IH} = V_{refA}$; $V_{EXT} = V_{pu} = V_{refA} + 1\ V$				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.6	-	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	1.1	-	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	1.3	-	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.4	-	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.9	-	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	1.0	-	ns

[1] All typical values are measured at T_{amb} = 25 °C.

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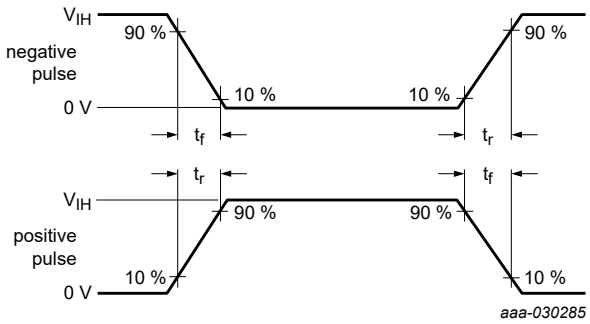
12.1. Waveforms and test circuit



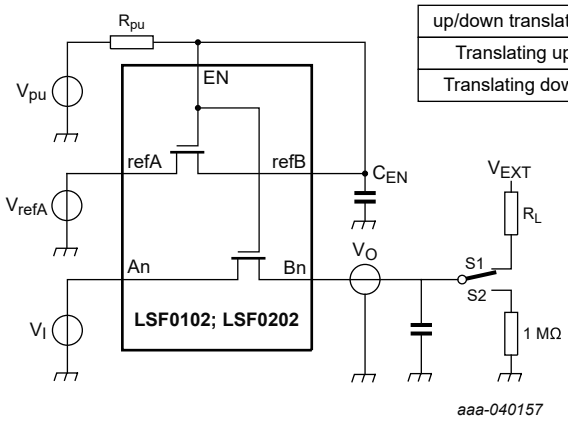
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. The data input (An, Bn) to output (Bn, An) propagation delay times



V_I source waveform



up/down translating	switch
Translating up	S1
Translating down	S2

Test circuit

Test data is given in Table 9. The An and Bn pins may be exchanged.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω.

Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance; C_{EN} = Decoupling capacitance; R_{pu} = Pull-up resistance; R_L = Load resistance; S1/S2 = Test selection switch

Fig. 4. Test circuit for measuring switching times

Table 9. Test data

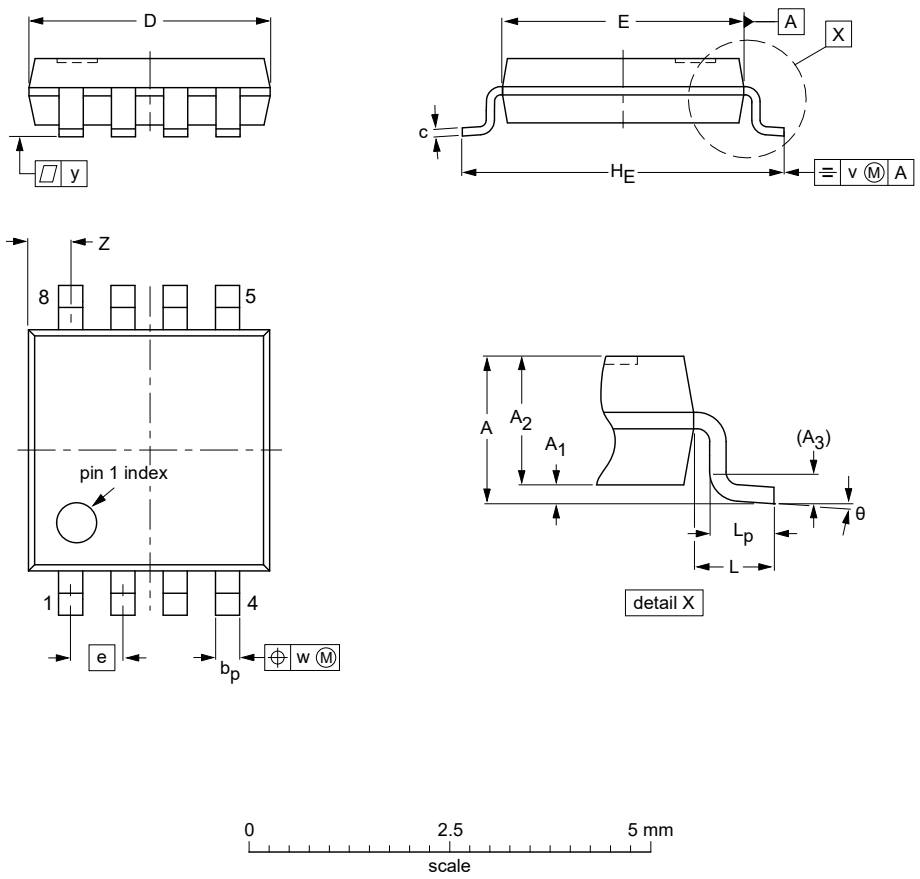
Input		Output	Load			
t_r, t_f	V_M	V_M	C_L	C_{EN} [1]	R_L [1]	R_{pu}
≤ 2 ns	$0.5V_{refA}$	$0.5V_{refA}$	15 pF, 30 pF, 50 pF	100 nF	300 Ω	200 kΩ

[1] All typical values are measured at T_{amb} = 25 °C.

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13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

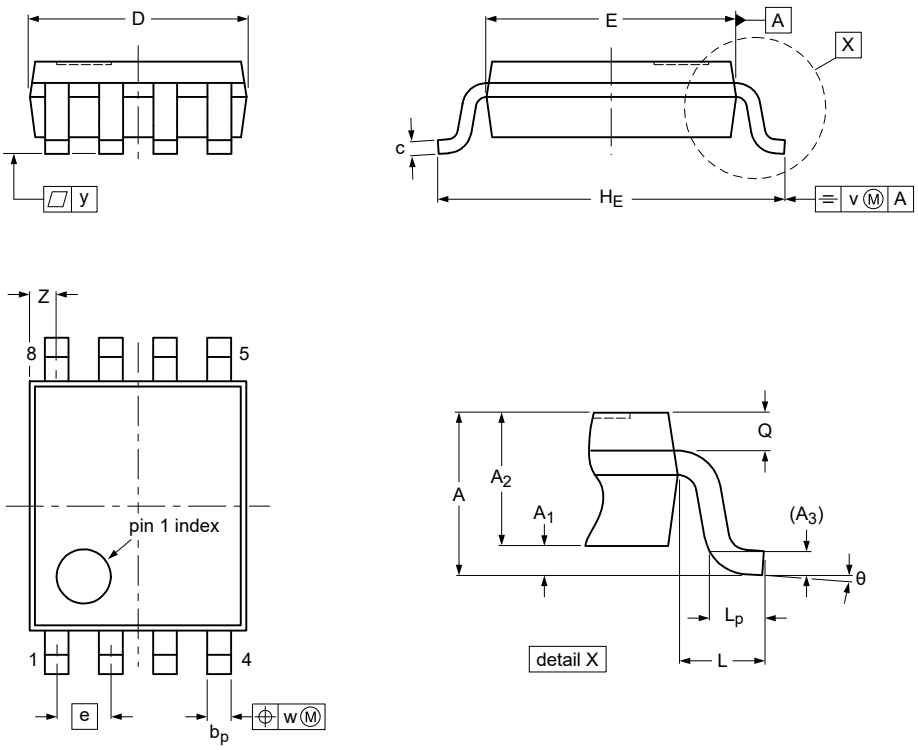
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 5. Package outline SOT505-2 (TSSOP8)

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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	max	1	0.15	0.85	0.12	0.27	0.23	2.1	2.4	0.5	3.2	0.4	0.40	0.21	0.2	0.08	0.1	0.4	8°
	nom																		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 6. Package outline SOT765-1 (VSSOP8)

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14. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^2c	Inter-Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
MDIO	Management Data Input/Output
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition
PMBus	Power Management Bus
SDIO	Secure Digital Input/Output
SMBus	System Management Bus
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LSF0102_Q100 v.4	20240624	Product data sheet	-	LSF0102_Q100 v.3
Modifications:	• Section 7: pin configuration drawings updated.			
LSF0102_Q100 v.3	20231128	Product data sheet	-	LSF0102_Q100 v.2
Modifications:	• Section 2: up- and down-translation typo corrected.			
LSF0102_Q100 v.2	20200904	Product data sheet	-	LSF0102_Q100 v.1
Modifications:	• Type number LSF0102DC-Q100 (SOT765-1/VSSOP8) added.			
LSF0102_Q100 v.1	20200611	Product data sheet	-	-

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16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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