High Voltage Synchronous N-Channel MOSFET Driver

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
- **Bootstrap Supply Voltage to 114V**
- **Wide V_{CC} Voltage: 7.2V to 13.5V**
- **Adaptive Shoot-Through Protection**
- **2.5A Peak TG Pull-Up Current**
- **3A Peak BG Pull-Up Current**
- **1.2Ω TG Driver Pull-Down**
- **0.55Ω BG Driver Pull-Down**
- **5ns TG Fall Time Driving 1nF Load**
- **8ns TG Rise Time Driving 1nF Load**
- **3ns BG Fall Time Driving 1nF Load**
- **6ns BG Rise Time Driving 1nF Load**
- Drives Both High and Low Side N-Channel MOSFETs
- Undervoltage Lockout
- Thermally Enhanced 8-Lead MSOP Package

APPLICATIONS

- Distributed Power Architectures
- Automotive Power Supplies
- High Density Power Modules
- Telecommunications

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DESCRIPTION

The LTC®4444 is a high frequency high voltage gate driver that drives two N-channel MOSFETs in a synchronous DC/DC converter with supply voltages up to 100V. This powerful driver reduces switching losses in MOSFETs with high gate capacitance.

The LTC4444 is configured for two supply-independent inputs. The high side input logic signal is internally level-shifted to the bootstrapped supply, which may function at up to 114V above ground.

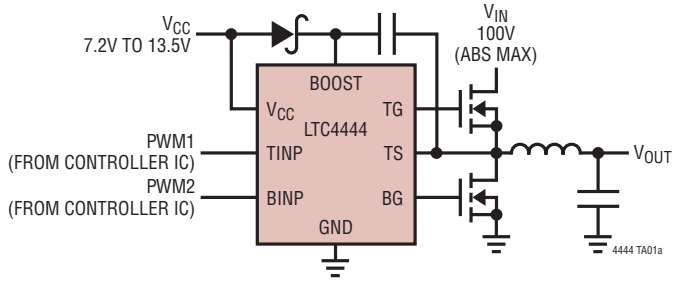
The LTC4444 contains undervoltage lockout circuits that disable the external MOSFETs when activated. Adaptive shoot-through protection prevents both MOSFETs from conducting simultaneously.

For a similar driver in this product family, please refer to the chart below.

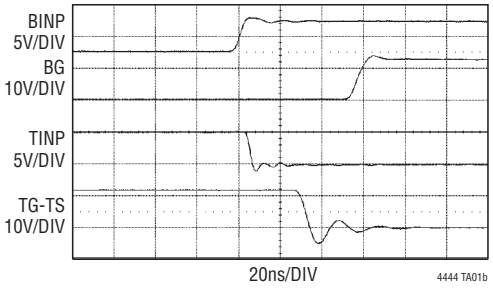
PARAMETER	LTC4444	LTC4446	LTC4444-5
Shoot-Through Protection	Yes	No	Yes
Absolute Max TS	100V	100V	100V
MOSFET Gate Drive	7.2V to 13.5V	7.2V to 13.5V	4.5V to 13.5V
V_{CC} UV^+	6.6V	6.6V	4V
V_{CC} UV^-	6.15V	6.15V	3.55V

TYPICAL APPLICATION

High Input Voltage Buck Converter



LTC4444 Driving a 1000pF Capacitive Load



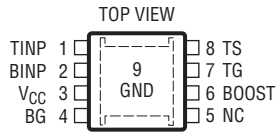
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} ..... –0.3V to 14V
- BOOST – TS ..... –0.3V to 14V

TINP Voltage ..... –2V to 14V
BINP Voltage ..... –2V to 14V
BOOST Voltage ..... –0.3V to 114V
TS Voltage ..... –5V to 100V
Operating Junction Temperature Range
(Notes 2, 3) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W (NOTE 4)
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4444EMS8E#PBF	LTC4444EMS8E#TRPBF	LTDBF	8-Lead Plastic MSOP	–40°C to 125°C
LTC4444IMS8E#PBF	LTC4444IMS8E#TRPBF	LTDBF	8-Lead Plastic MSOP	–40°C to 125°C
LTC4444HMS8E#PBF	LTC4444HMS8E#TRPBF	LTDBF	8-Lead Plastic MSOP	–40°C to 150°C
LTC4444MPMS8E#PBF	LTC4444MPMS8E#TRPBF	LTDBF	8-Lead Plastic MSOP	–55°C to 150°C
AUTOMOTIVE PRODUCTS**				
LTC4444EMS8E#WPBF	LTC4444EMS8E#WTRPBF	LTDBF	8-Lead Plastic MSOP	–40°C to 125°C
LTC4444IMS8E#WPBF	LTC4444IMS8E#WTRPBF	LTDBF	8-Lead Plastic MSOP	–40°C to 125°C
LTC4444HMS8E#WPBF	LTC4444HMS8E#WTRPBF	LTDBF	8-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BOOST} = 12V, V_{TS} = GND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver Supply, V_{CC}							
V_{CC}	Operating Voltage			7.2		13.5	V
I_{VCC}	DC Supply Current	TINP = BINP = 0V			350	550	µA
UVLO	Undervoltage Lockout Threshold	V_{CC} Rising V_{CC} Falling Hysteresis	● ●	6.00 5.60	6.60 6.15 450	7.20 6.70	V V mV
Bootstrapped Supply (BOOST – TS)							
I_{BOOST}	DC Supply Current	TINP = BINP = 0V			0.1	2	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BOOST} = 12V, V_{TS} = GND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Signal (TINP, BINP)							
$V_{IH(BG)}$	BG Turn-On Input Threshold	BINP Ramping High	●	2.25	2.75	3.25	V
$V_{IL(BG)}$	BG Turn-Off Input Threshold	BINP Ramping Low	●	1.85	2.3	2.75	V
$V_{IH(TG)}$	TG Turn-On Input Threshold	TINP Ramping High	●	2.25	2.75	3.25	V
$V_{IL(TG)}$	TG Turn-Off Input Threshold	TINP Ramping Low	●	1.85	2.3	2.75	V
$I_{TINP(BINP)}$	Input Pin Bias Current				±0.01	±2	µA
High Side Gate Driver Output (TG)							
$V_{OH(TG)}$	TG High Output Voltage	I_{TG} = –10mA, $V_{OH(TG)}$ = V_{BOOST} – V_{TG}			0.7		V
$V_{OL(TG)}$	TG Low Output Voltage	I_{TG} = 100mA, $V_{OL(TG)}$ = V_{TG} –V_{TS}	●		120	250	mV
$I_{PU(TG)}$	TG Peak Pull-Up Current		●	1.7	2.5		A
$R_{DS(TG)}$	TG Pull-Down Resistance		●		1.2	2.5	Ω
Low Side Gate Driver Output (BG)							
$V_{OH(BG)}$	BG High Output Voltage	I_{BG} = –10mA, $V_{OH(BG)}$ = V_{CC} – V_{BG}			0.7		V
$V_{OL(BG)}$	BG Low Output Voltage	I_{BG} = 100mA	●		55	125	mV
$I_{PU(BG)}$	BG Peak Pull-Up Current		●	2	3		A
$R_{DS(BG)}$	BG Pull-Down Resistance		●		0.55	1.25	Ω
Switching Time [BINP (TINP) is Tied to Ground While TINP (BINP) is Switching. Refer to Timing Diagrams]							
$t_{PLH(TG)}$	TG Low-High Propagation Delay		●		25	50	ns
$t_{PHL(TG)}$	TG High-Low Propagation Delay		●		22	45	ns
$t_{PLH(BG)}$	BG Low-High Propagation Delay		●		19	40	ns
$t_{PHL(BG)}$	BG High-Low Propagation Delay		●		14	35	ns
$t_{r(TG)}$	TG Output Rise Time	10% – 90%, C_L = 1nF 10% – 90%, C_L = 10nF			8 80		ns ns
$t_{f(TG)}$	TG Output Fall Time	10% – 90%, C_L = 1nF 10% – 90%, C_L = 10nF			5 50		ns ns
$t_{r(BG)}$	BG Output Rise Time	10% – 90%, C_L = 1nF 10% – 90%, C_L = 10nF			6 60		ns ns
$t_{f(BG)}$	BG Output Fall Time	10% – 90%, C_L = 1nF 10% – 90%, C_L = 10nF			3 30		ns ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4444 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4444E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4444I is guaranteed over the –40°C to 125°C operating temperature range, the LTC4444H is guaranteed over the –40°C to 150°C operating temperature range and the LTC4444MP is tested and guaranteed over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

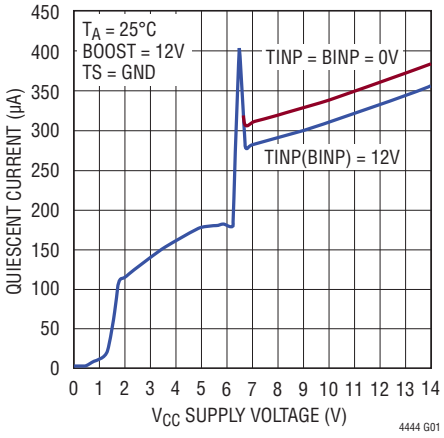
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

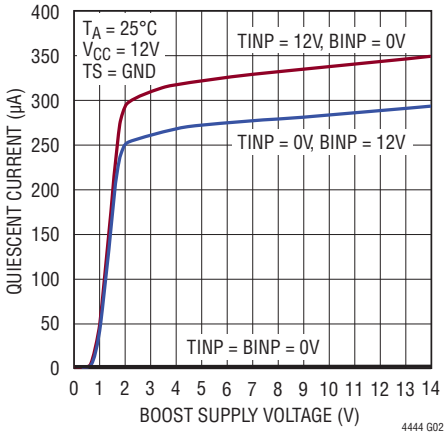
Note 4: Failure to solder the exposed back side of the MS8E package to the PC board will result in a thermal resistance much higher than 40°C/W.

TYPICAL PERFORMANCE CHARACTERISTICS

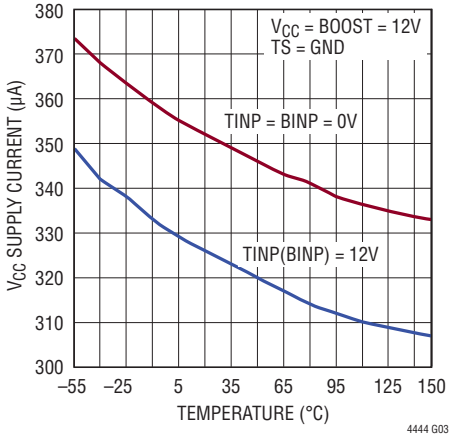
V_{CC} Supply Quiescent Current vs Voltage



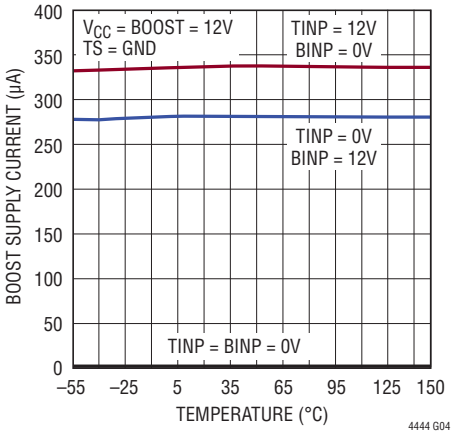
BOOST-TS Supply Quiescent Current vs Voltage



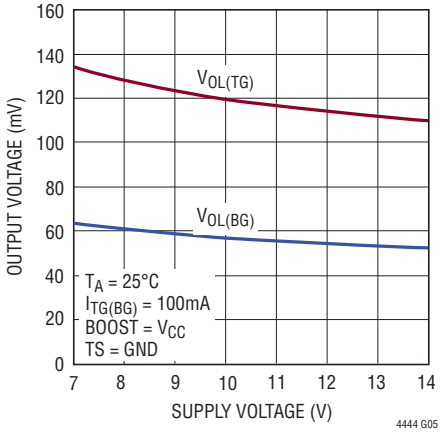
V_{CC} Supply Current vs Temperature



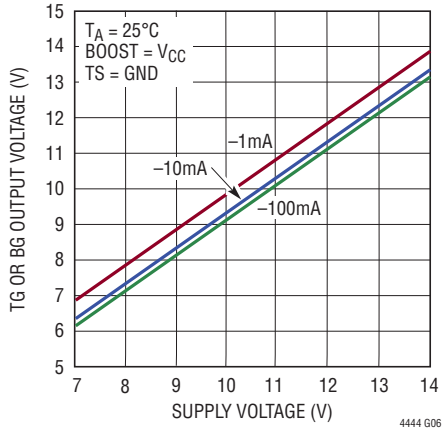
Boost Supply Current vs Temperature



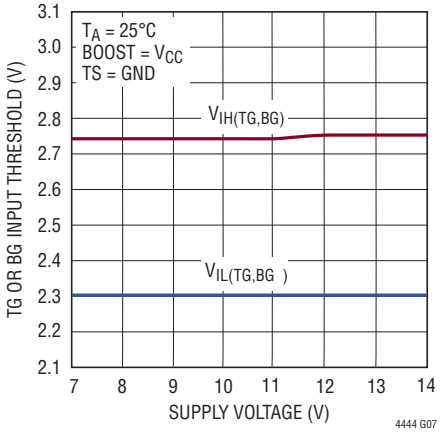
Output Low Voltage (V_{OL}) vs Supply Voltage



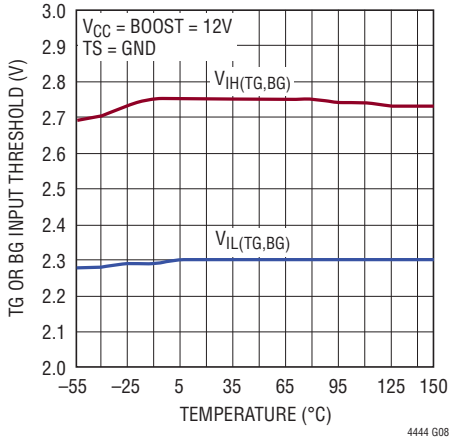
Output High Voltage (V_{OH}) vs Supply Voltage



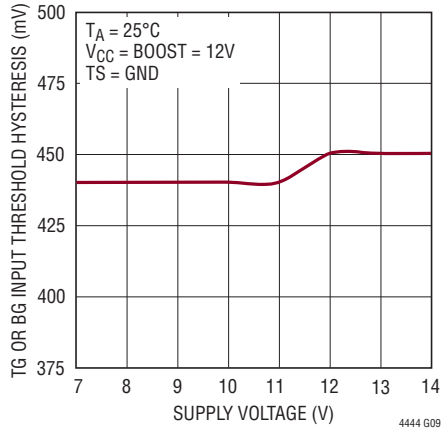
Input Thresholds (TINP, BINP) vs Supply Voltage



Input Thresholds (TINP, BINP) vs Temperature

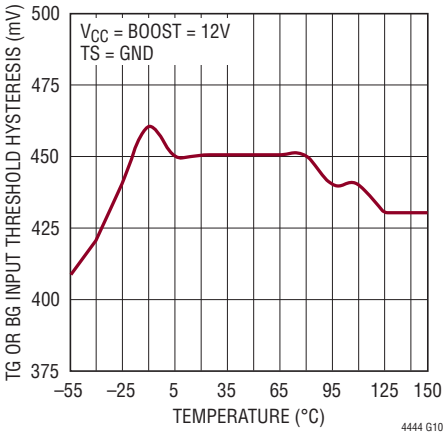


Input Thresholds (TINP, BINP) Hysteresis vs Voltage

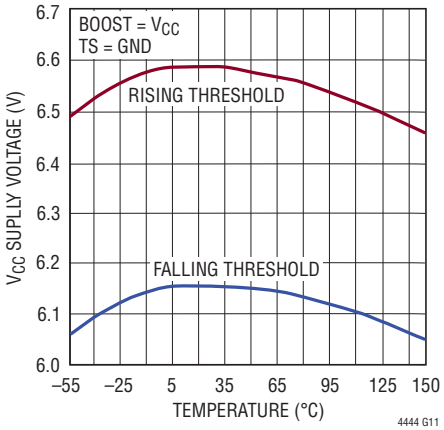


TYPICAL PERFORMANCE CHARACTERISTICS

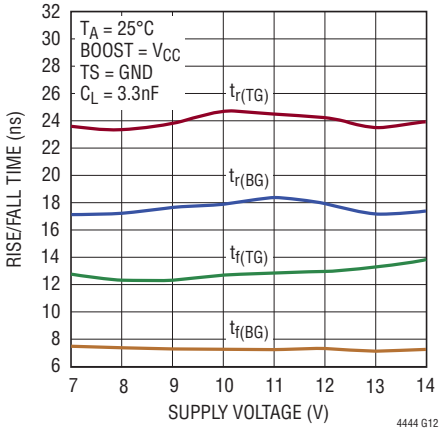
Input Thresholds (TINP, BINP) Hysteresis vs Temperature



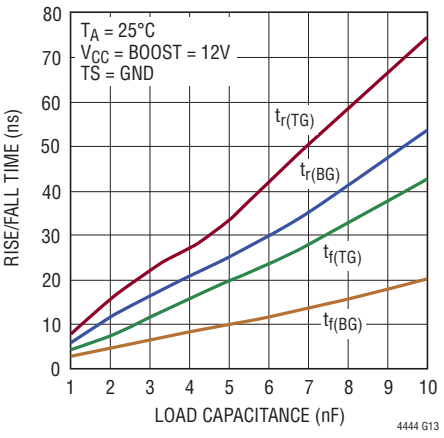
V_{CC} Undervoltage Lockout Thresholds vs Temperature



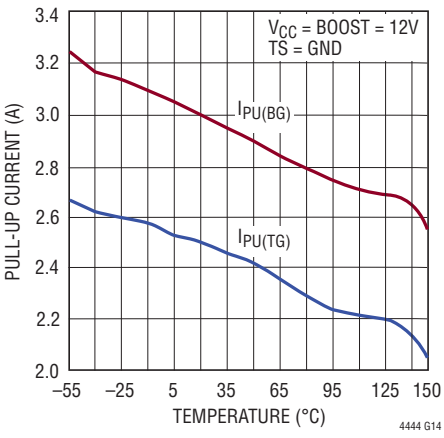
Rise and Fall Time vs V_{CC} Supply Voltage



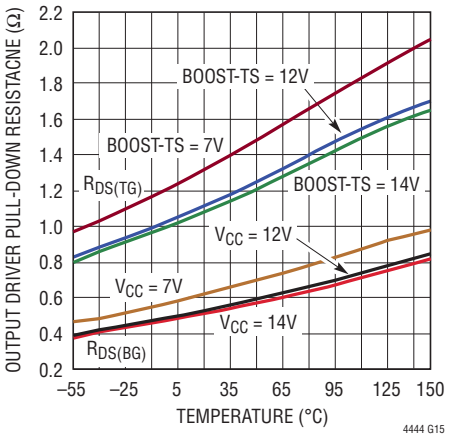
Rise and Fall Time vs Load Capacitance



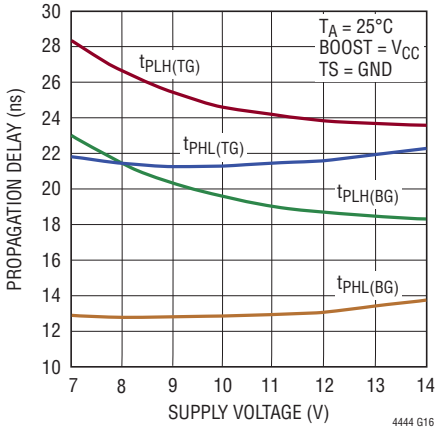
Peak Driver (TG, BG) Pull-Up Current vs Temperature



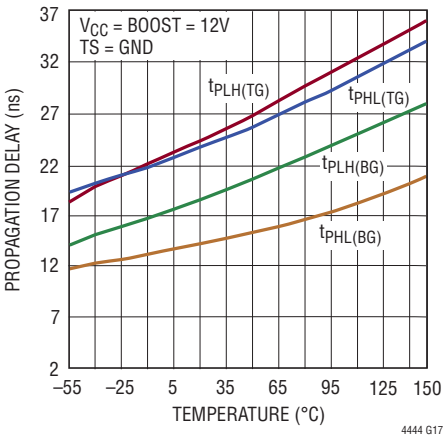
Output Driver Pull-Down Resistance vs Temperature



Propagation Delay vs V_{CC} Supply Voltage

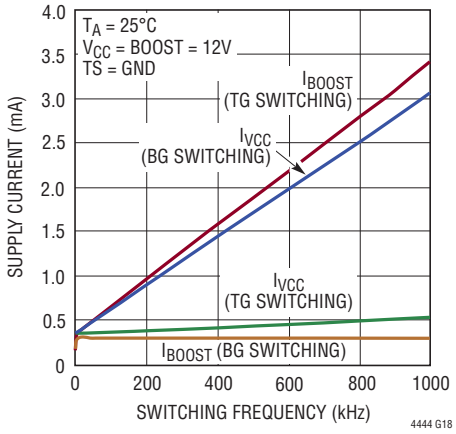


Propagation Delay vs Temperature

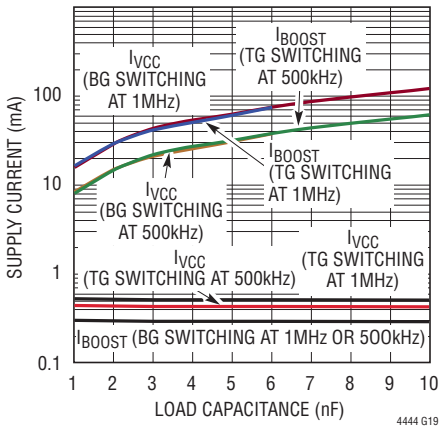


TYPICAL PERFORMANCE CHARACTERISTICS

Switching Supply Current vs Input Frequency



Switching Supply Current vs Load Capacitance



PIN FUNCTIONS

TINP (Pin 1): High Side Input Signal. Input referenced to GND. This input controls the high side driver output (TG).

BINP (Pin 2): Low Side Input Signal. This input controls the low side driver output (BG).

V_{CC} (Pin 3): Supply. This pin powers input buffers, logic and the low side gate driver output directly and the high side gate driver output through an external diode connected between this pin and BOOST (Pin 6). A low ESR ceramic bypass capacitor should be tied between this pin and GND (Pin 9).

BG (Pin 4): Low Side Gate Driver Output (Bottom Gate). This pin swings between V_{CC} and GND.

NC (Pin 5): No Connect. No connection required.

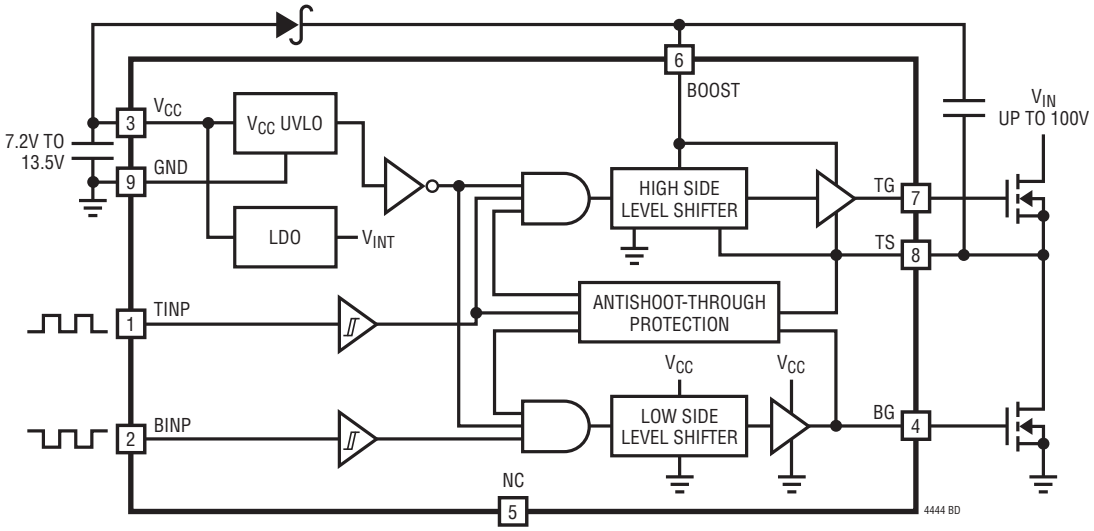
BOOST (Pin 6): High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 8). Normally, a bootstrap diode is connected between V_{CC} (Pin 3) and this pin. Voltage swing at this pin is from $V_{CC} – V_D$ to $V_{IN} + V_{CC} – V_D$, where V_D is the forward voltage drop of the bootstrap diode.

TG (Pin 7): High Side Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

TS (Pin 8): High Side MOSFET Source Connection (Top Source).

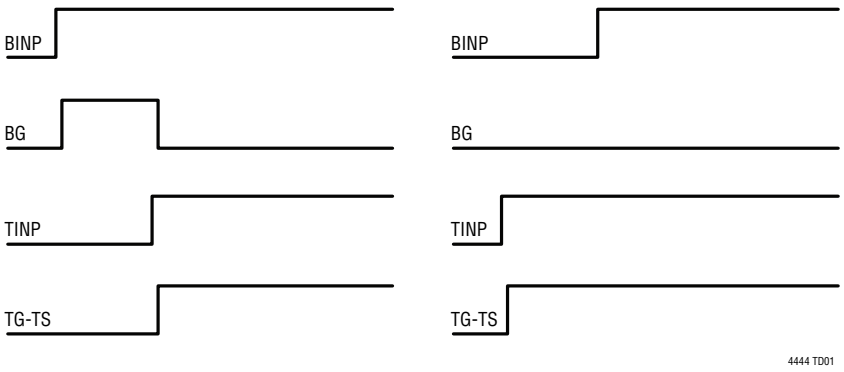
GND (Exposed Pad Pin 9): Ground. Must be soldered to PCB ground for optimal thermal performance.

BLOCK DIAGRAM

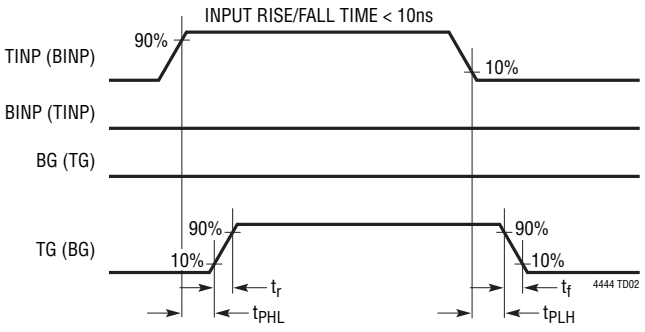


TIMING DIAGRAMS

Adaptive Shoot-Through Protection



Switching Time



OPERATION

Overview

The LTC4444 receives ground-referenced, low voltage digital input signals to drive two N-channel power MOSFETs in a synchronous buck power supply configuration. The gate of the low side MOSFET is driven either to V_{CC} or GND, depending on the state of the input. Similarly, the gate of the high side MOSFET is driven to either BOOST or TS by a supply bootstrapped off of the switching node (TS).

Input Stage

The LTC4444 employs CMOS compatible input thresholds that allow a low voltage digital signal to drive standard power MOSFETs. The LTC4444 contains an internal voltage regulator that biases both input buffers for high side and low side inputs, allowing the input thresholds (V_{IH} = 2.75V, V_{IL} = 2.3V) to be independent of variations in V_{CC}. The 450mV hysteresis between V_{IH} and V_{IL} eliminates false triggering due to noise during switching transitions. However, care should be taken to keep both input pins (TINP and BINP) from any noise pickup, especially in high frequency, high voltage applications. The LTC4444 input buffers have high input impedance and draw negligible input current, simplifying the drive circuitry required for the inputs.

Output Stage

A simplified version of the LTC4444's output stage is shown in Figure 1. The pull-up devices on the BG and TG outputs are NPN bipolar junction transistors (Q1 and Q2). The BG and TG outputs are pulled up to within an NPN V_{BE} (~0.7V) of their positive rails (V_{CC} and BOOST, respectively). Both BG and TG have N-channel MOSFET pull-down devices (M1 and M2) which pull BG and TG down to their negative rails, GND and TS. The large voltage swing of the BG and TG output pins is important in driving external power MOSFETs, whose $R_{DS(ON)}$ is inversely proportional to the gate overdrive voltage ($V_{GS} - V_{TH}$).

Rise/Fall Time

The LTC4444's rise and fall times are determined by the peak current capabilities of Q1 and M1. The predriver that drives Q1 and M1 uses a nonoverlapping transition scheme to minimize cross-conduction currents. M1 is fully turned off before Q1 is turned on and vice versa.

Since the power MOSFET generally accounts for the majority of the power loss in a converter, it is important to quickly turn it on or off, thereby minimizing the transition time in its linear region. An additional benefit of a strong pull-down on the driver outputs is the prevention

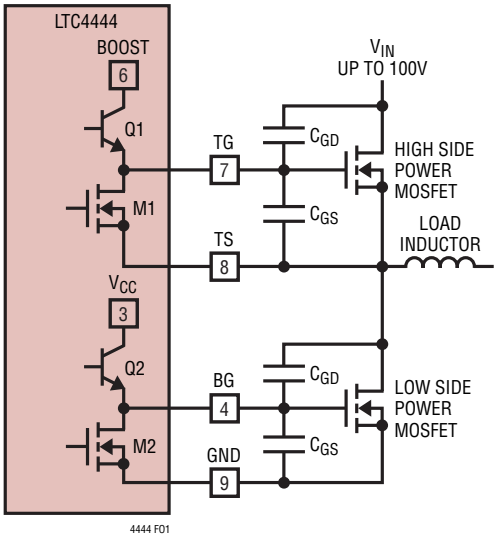


Figure 1. Capacitance Seen by BG and TG During Switching

OPERATION

of cross- conduction current. For example, when BG turns the low side (synchronous) power MOSFET off and TG turns the high side power MOSFET on, the voltage on the TS pin will rise to V_{IN} very rapidly. This high frequency positive voltage transient will couple through the C_{GD} capacitance of the low side power MOSFET to the BG pin. If there is an insufficient pull-down on the BG pin, the voltage on the BG pin can rise above the threshold voltage of the low side power MOSFET, momentarily turning it back on. With both the high side and low side MOSFETs conducting, significant cross-conduction current will flow through the MOSFETs from V_{IN} to ground and will cause substantial power loss. A similar effect occurs on TG due to the C_{GS} and C_{GD} capacitances of the high side MOSFET.

The powerful output driver of the LTC4444 reduces the switching losses of the power MOSFET, which increase with transition time. The LTC4444's high side driver is capable of driving a 1nF load with 8ns rise and 5ns fall times using a bootstrapped supply voltage $V_{BOOST-TS}$ of 12V while its low side driver is capable of driving a 1nF load with 6ns rise and 3ns fall times using a supply voltage V_{CC} of 12V.

Undervoltage Lockout (UVLO)

The LTC4444 contains an undervoltage lockout detector that monitors V_{CC} supply. When V_{CC} falls below 6.15V, the output pins BG and TG are pulled down to GND and TS, respectively. This turns off both external MOSFETs. When V_{CC} has adequate supply voltage, normal operation will resume.

Adaptive Shoot-Through Protection

Internal adaptive shoot-through protection circuitry monitors the voltages on the external MOSFETs to ensure that they do not conduct simultaneously. This feature improves efficiency by eliminating cross-conduction current from flowing from the V_{IN} supply through both of the MOSFETs to ground during a switch transition. If both TINP and BINP are high at the same time, BG will be kept off and TG will be turned on (refer to the Timing Diagrams). If BG is still high when TINP turns on, TG will not be turned on until BG goes low.

When TINP turns off, the adaptive shoot-through protection circuitry monitors the level of the TS pin. BG can be turned on if the TS pin goes low. If the TS pin stays high, BG will be turned on 150ns after TINP turns off.

APPLICATIONS INFORMATION

Power Dissipation

To ensure proper operation and long-term reliability, the LTC4444 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + P_D (\theta_{JA})$$

where:

T_J = Junction temperature

T_A = Ambient temperature

P_D = Power dissipation

θ_{JA} = Junction-to-ambient thermal resistance

Power dissipation consists of standby and switching power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

P_{DC} = Quiescent power loss

P_{AC} = Internal switching loss at input frequency, f_{IN}

P_{QG} = Loss due turning on and off the external MOSFET with gate charge QG at frequency f_{IN}

The LTC4444 consumes very little quiescent current. The DC power loss at V_{CC} = 12V and $V_{BOOST-TS}$ = 12V is only (350µA)(12V) = 4.2mW.

APPLICATIONS INFORMATION

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal node capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads C_{LOAD} on TG and BG at switching frequency f_{IN}, the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f)[(V_{BOOST-TS})^2 + (V_{CC})^2]$$

In a typical synchronous buck configuration, $V_{BOOST-TS}$ is equal to $V_{CC} – V_D$, where V_D is the forward voltage drop across the diode between V_{CC} and BOOST. If this drop is small relative to V_{CC}, the load losses can be approximated as:

$$P_{CLOAD} = 2(C_{LOAD})(f_{IN})(V_{CC})^2$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge, QG. The QG value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's QG vs V_{GS} curves. For identical MOSFETs on TG and BG:

$$P_{QG} = 2(V_{CC})(Q_G)(f_{IN})$$

To avoid damage due to power dissipation, the LTC4444 includes a temperature monitor that will pull BG and TG low if the junction temperature rises above 160°C. Normal operation will resume when the junction temperature cools to less than 135°C.

Bypassing and Grounding

The LTC4444 requires proper bypassing on the V_{CC} and $V_{BOOST-TS}$ supplies due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing.

To obtain the optimum performance from the LTC4444:

A. Mount the bypass capacitors as close as possible between the V_{CC} and GND pins and the BOOST and TS pins. The leads should be shortened as much as possible to reduce lead inductance.

B. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC4444 switches greater than 3A peak currents and any significant ground drop will degrade signal integrity.

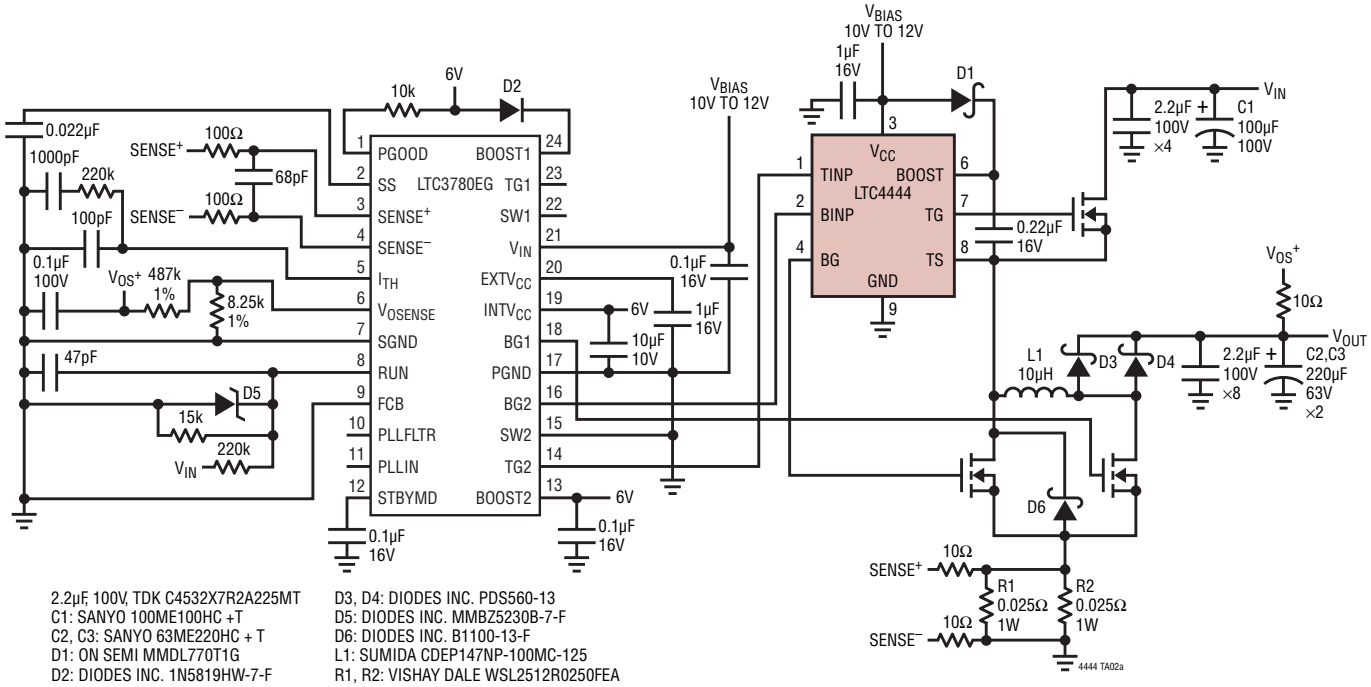
C. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.

D. Keep the copper trace between the driver output pin and the load short and wide.

E. Be sure to solder the Exposed Pad on the back side of the LTC4444 package to the board. Correctly soldered to a 2500mm^2 double sided 1oz copper board, the LTC4444 has a thermal resistance of approximately 40°C/W for the MS8E package. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than 40°C/W.

TYPICAL APPLICATION

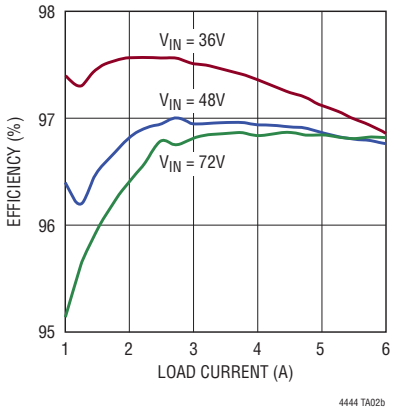
LTC3780 High Efficiency 36V to 72V V_{IN} to 48V/6A Buck-Boost DC/DC Converter



2.2µF, 100V, TDK C4532X7R2A225MT
C1: SANYO 100ME100HC +T
C2, C3: SANYO 63ME220HC + T
D1: ON SEMI MMDL770T1G
D2: DIODES INC. 1N5819HW-7-F

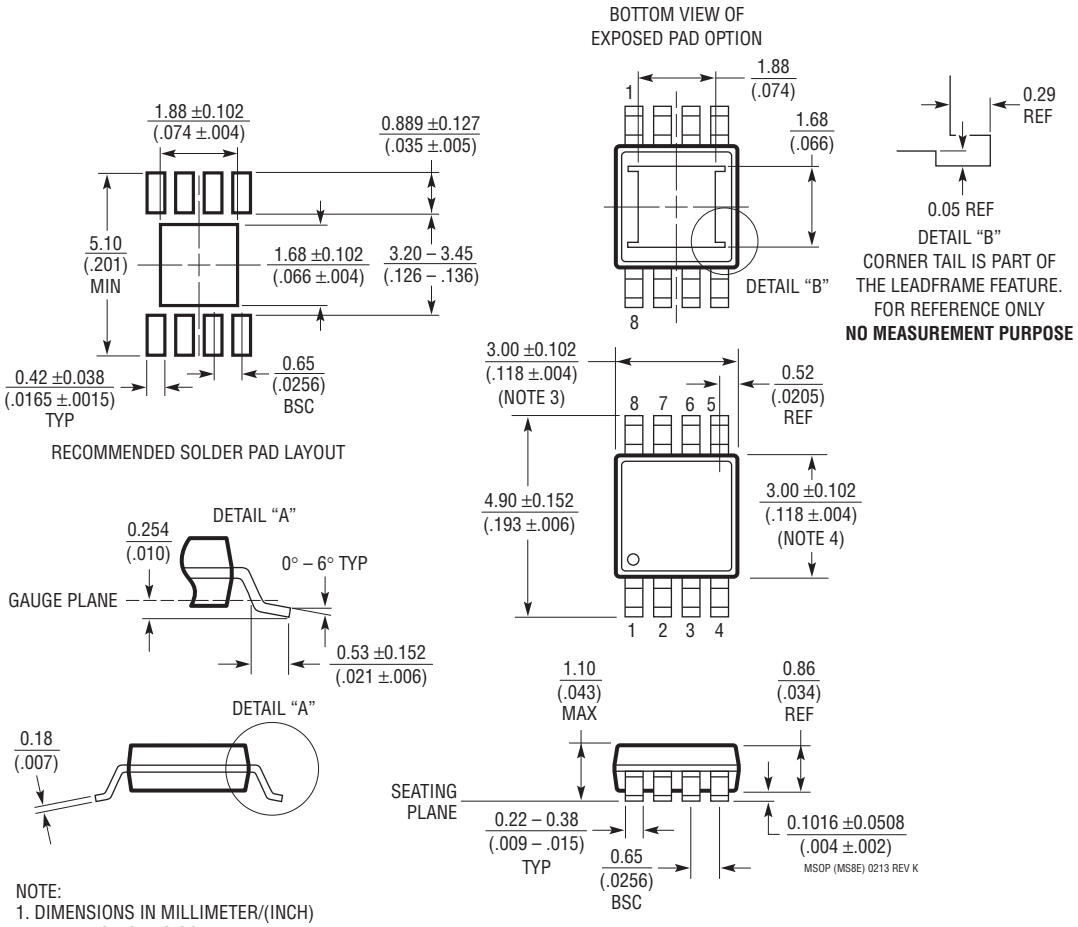
D3, D4: DIODES INC. PDS560-13
D5: DIODES INC. MMBZ5230B-7-F
D6: DIODES INC. B1100-13-F
L1: SUMIDA CDEP147NP-100MC-125
R1, R2: VISHAY DALE WSL2512R0250FEA

Efficiency



PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

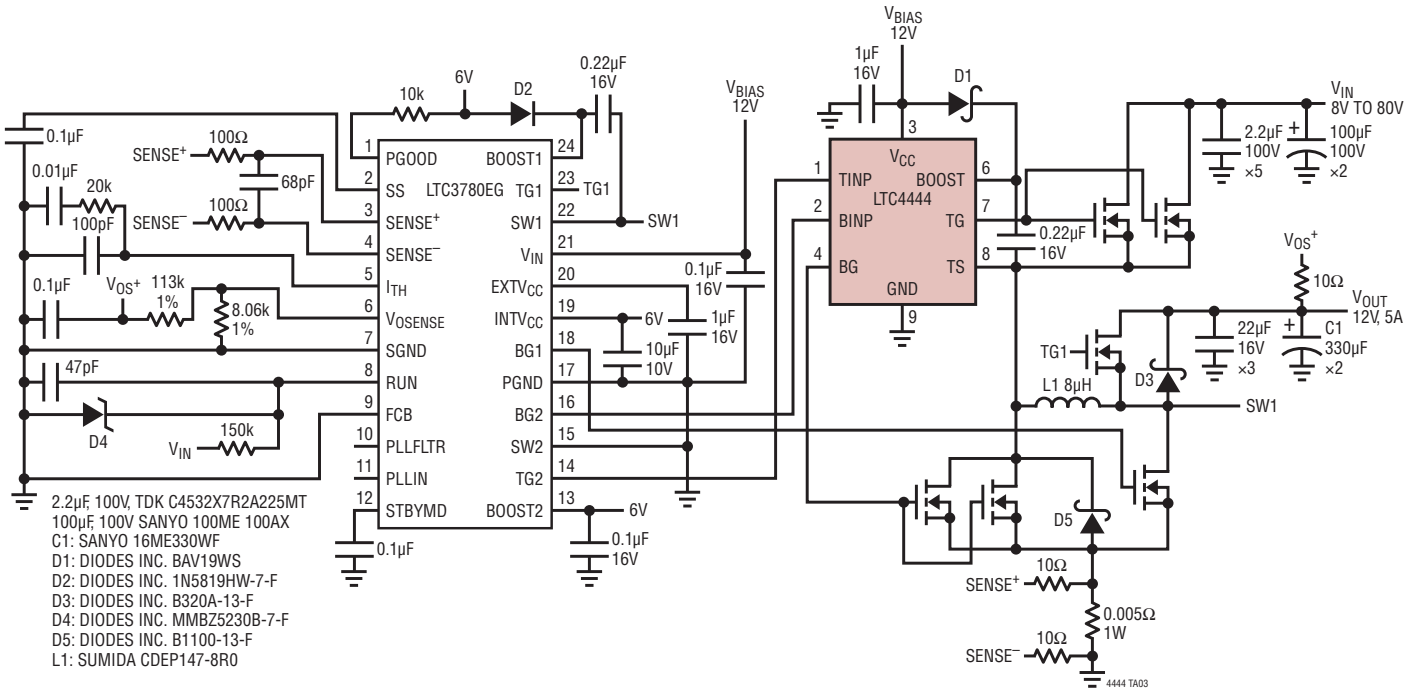
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/10	MP-grade part added. Reflected throughout the data sheet.	1 to 14
B	01/11	H-grade part added. Reflected throughout the data sheet.	1 to 14
C	12/18	Added AEC-Q100 approval and product information.	1 and 2

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TYPICAL APPLICATION

LTC3780 High Efficiency 8V to 80V V_{IN} to 12V/5A Buck-Boost DC/DC Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4446	High Voltage Synchronous N-Channel MOSFET Driver without Shoot-Through Protection	Up to 100V Supply Voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 3A Peak Pull-Up/ 0.55Ω Peak Pull-Down
LTC4440/LTC4440-5	High Speed, High Voltage, High Side Gate Driver	Up to 80V Supply Voltage, 8V ≤ V_{CC} ≤ 15V, 2.4A Peak Pull-Up/ 1.5Ω Peak Pull-Down
LTC4442	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 6V ≤ V_{CC} ≤ 9.5V, 3.2A Peak Pull-Up/ 4.5A Peak Pull-Down
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 4.5V ≤ V_{CC} ≤ 6.5V, 3.2A Peak Pull-Up/ 4.5A Peak Pull-Down
LTC4441/LTC4441-1	N-Channel MOSFET Gate Driver	Up to 25V Supply Voltage, 5V ≤ V_{CC} ≤ 25V, 6A Peak Output Current
LTC1154	High Side Micropower MOSFET Driver	Up to 18V Supply Voltage, 85µA Quiescent Current, H-Grade Available

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