105V, 2.3A Low EMI Synchronous Step-Down Regulator

FEATURES

- **Wide V_{IN} Range: 4.4V to 105V (110V Abs Max)**
- **Ultralow EMI/EMC Emissions: CISPR25 Compliant**
- **2µA I_Q When Regulating $48V_{IN}$ to $3.3V_{OUT}$**
- **Fast and Accurate Output Current Programming and Monitoring with No External R_{SENSE}**
- **Brick Wall Current Limit**
- **Low Minimum On-Time: 40ns**
- **Wide V_{OUT} Range: 1V to V_{IN}**
- **100% Maximum Duty Cycle Operation**
- Programmable Fixed Frequency: 200kHz to 2MHz
- Eight, Pin-Selectable Fixed (1.2V to 15V) or Adjustable Output Voltages
- Selectable Pulse-Skipping or Low Ripple Burst Mode® Operation at Light Loads
- PLL Synchronization to External Clock
- $EXTV_{CC}$ LDO Powers Chip from V_{OUT} = 3.3V to 40V
- OPTI-LOOP® or Fixed Internal Compensation
- Input and Output Overvoltage Protection
- Thermally Enhanced (5mm × 6mm) QFN Package

APPLICATIONS

- Battery Chargers and CC/CV Supplies
- Automotive and Military Systems
- Industrial, Avionics and Heavy Equipment
- Medical Instruments and Telecommunication Systems

DESCRIPTION

The LTC®7103 is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing a constant frequency, average current mode control architecture. It operates from an input voltage range of 4.4V to 105V and provides an adjustable regulated output voltage from 1V to V_{IN} while delivering up to 2.3A of output current.

The LTC7103 features high frequency operation and a low minimum on-time that reduce inductor size and enable constant-frequency operation even at very high step-down ratios. In addition, the LTC7103 achieves the lowest possible dropout voltage with 100% maximum duty cycle operation. During light load operation, converter efficiency and output ripple can be optimized by selecting Burst Mode or pulse-skipping operation.

The LTC7103 includes accurate, high speed average current programming and monitoring without the need for an external sense resistor. Additional features include a bypass LDO to maximize efficiency, fixed or adjustable output voltage and loop compensation, and a wide array of protection features to enhance reliability.

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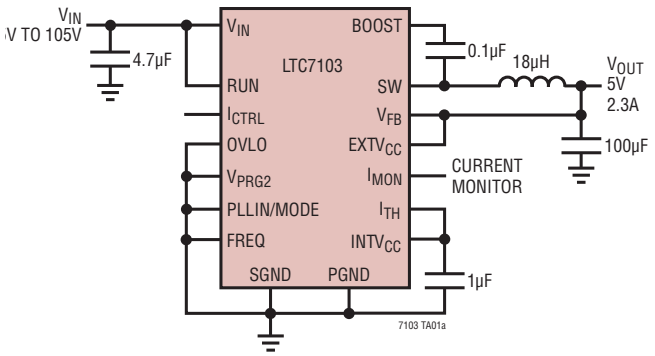
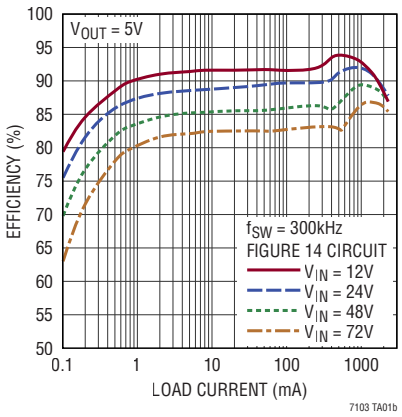
TYPICAL APPLICATION

5V to 105V Input to 5V/2.3A Output Step-Down Regulator



Efficiency vs Load Current



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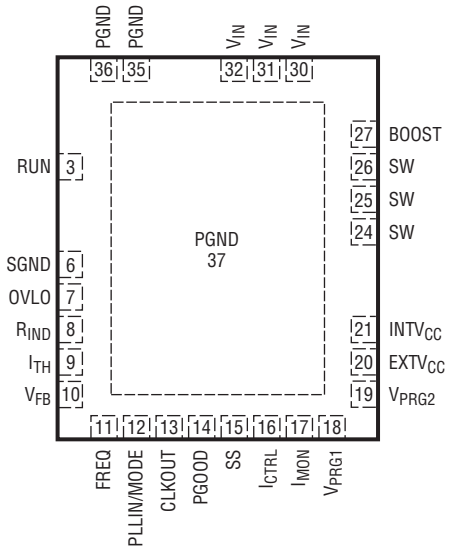
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Supply Voltage.....–0.3V to 110V
$INTV_{CC}$, (BOOST-SW) Voltages..... –0.3V to 6V
BOOST Voltage .....–0.3V to 110V
RUN Voltage.....–0.3V to 110V
V_{FB}, PGOOD Voltages ..... –0.3V to 16V
$EXTV_{CC}$ Voltage .....–0.3V to 41V
R_{IND}, V_{PRG1}, V_{PRG2} Voltages.....–0.3V to $INTV_{CC}$
I_{CTRL}, SS Voltages .....–0.3V to $INTV_{CC}$
FREQ, I_{TH}, PLLIN/MODE, OVLO Voltages..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3, 4)
LTC7103E, LTC7103I..... –40°C to 125°C
LTC7103H ..... –40°C to 150°C
LTC7103MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHE36(26) PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 37) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7103EUHE#PBF	LTC7103EUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LTC7103IUHE#PBF	LTC7103IUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LTC7103HUHE#PBF	LTC7103HUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 150°C
LTC7103MPUHE#PBF	LTC7103MPUHE#TRPBF	7103	36-Lead (5mm × 6mm) Plastic QFN	–55°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Regulator and Voltage Loop							
V_{IN}	Operating Input Voltage Range			4.4		105	V
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout	V_{IN} Rising V_{IN} Falling	● ●	4.36 4.11	4.50 4.25	4.64 4.39	V V
V_{OUT}	Operating Output Voltage Range	(Note 9)		1.0		105	V
I_Q	V_{IN} Input DC Supply Current	(Note 8)					
	Pulse-Skipping Mode	V_{FB} = 1.04V, $EXTV_{CC}$ = 3.4V V_{FB} = 1.04V, $EXTV_{CC}$ = 0V			200 4.4		µA mA
	Sleep Mode	V_{FB} = 1.04V, $EXTV_{CC}$ = 5V V_{FB} = 1.04V, $EXTV_{CC}$ = 0V			1.0 9.0		µA µA
	Shutdown	RUN = 0V			0.7	8.0	µA
	V_{IN} Input Current In Regulation	Figure 14 Circuit, V_{IN} = 48V, I_{OUT} = 500µA Figure 16 Circuit, V_{IN} = 48V, I_{OUT} = 0µA			64 2	75	µA µA
V_{FB}	Regulated Feedback Voltage	(Note 5) I_{TH} Voltage = 0.5V to 1.2V, V_{IN} = 4.5V to 105V V_{PRG1} = V_{PRG2} = FLOAT V_{PRG1} = V_{PRG2} = $INTV_{CC}$ V_{PRG1} = FLOAT, V_{PRG2} = $INTV_{CC}$ V_{PRG1} = V_{PRG2} = SGND V_{PRG1} = SGND, V_{PRG2} = FLOAT V_{PRG1} = SGND, V_{PRG2} = $INTV_{CC}$ V_{PRG1} = FLOAT, V_{PRG2} = SGND V_{PRG1} = $INTV_{CC}$, V_{PRG2} = FLOAT V_{PRG1} = $INTV_{CC}$, V_{PRG2} = SGND	 ● ● ● ● ● ● ● ● ●	 0.990 1.182 1.770 2.455 3.234 3.528 4.900 11.75 14.70	 1.000 1.200 1.800 2.500 3.300 3.600 5.000 12.00 15.00	 1.010 1.218 1.827 2.537 3.350 3.654 5.075 12.24 15.30	 V V V V V V V V V
	Feedback Input Bias Current	V_{PRG1} = V_{PRG2} = FLOAT V_{PRG1} or V_{PRG2} Tied to SGND or $INTV_{CC}$			±2 1.25	±10 1.6	nA µA
g_m	Error Amplifier g_m	I_{TH} = 1V, Sink/Source = 5µA (Note 5)			1.52		mS
$t_{ON,MIN}$	Minimum Controllable ON-Time	(Note 7)	●		40	60	ns
$R_{DS(ON)TOP}$	Top Switch On-Resistance				265		mΩ
$R_{DS(ON)BOT}$	Bottom Switch On-Resistance				142		mΩ
Current Control and Monitoring							
$I_{LIM(AVG)}$	Average Output Current Limit	(Note 6) I_{CTRL} = FLOAT I_{CTRL} = 0.58V		 2.25 0.36	 2.50 0.5	 2.75 0.64	 A A
I_{PK}	Top Switch Peak Current Limit	I_{CTRL} = FLOAT I_{CTRL} = 0.58V		3.32 1.56	3.70 1.70	4.30 2.09	A A
V_{IMON}	Current Monitor Output Voltage	(Note 6) I_{SW} = 2A I_{SW} = 0.5A		 1.04 0.54	 1.12 0.58	 1.19 0.63	 V V
	I_{CTRL} Pin Pull-Up Current	V_{ICTRL} = 1V	●	18	20	22	µA
Start-Up and Shutdown							
I_{SS}	Soft-Start Charge Current	SS = 0V	●	8	11	14	µA
$t_{SS(INT)}$	Internal Soft-Start Ramp Time	SS = FLOAT			1.2		ms
$V_{FB(OV)}$	Feedback Overvoltage Protection	Relative to Regulated V_{FB}		7	10	13	%
$V_{RUN(ON)}$	RUN Pin ON Threshold	V_{RUN} Rising V_{RUN} Falling	● ●	1.16 1.06	1.21 1.11	1.26 1.16	V V
	RUN Pin Hysteresis				100		mV
	RUN Pin Leakage Current	RUN = 1.5V		–10	0	10	nA
$V_{OV(R)}$	OVLO Pin Rising Threshold	V_{OVLO} Rising	●	1.16	1.21	1.26	V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	OVLO Pin Hysteresis				65		mV
	OVLO Pin Leakage Current	OVLO = 1.5V		–10	0	10	nA
Bias Regulators and Housekeeping							
	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising $INTV_{CC}$ Falling			3.00 2.80		V V
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Rising $EXTV_{CC}$ Falling	● ●	3.04 2.95	3.10 3.00	3.17 3.07	V V
	Regulated $INTV_{CC}$ Voltage from V_{IN}			3.37	3.5	3.6	V
	Regulated $INTV_{CC}$ Voltage from $EXTV_{CC}$			3.37	3.5	3.6	V
Oscillator and Phase-Locked Loop							
	Programmable Frequency Accuracy	R_{FREQ} = 12.5k (200kHz) to 57.5k (2MHz) PLLIN/MODE = 0V	●	–15		15	%
f_{LOW}	Low Preset Frequency	V_{FREQ} = 0V; PLLIN/MODE = 0V	●	270	300	330	kHz
f_{HIGH}	High Preset Frequency	V_{FREQ} = $INTV_{CC}$; PLLIN/MODE = 0V	●	0.9	1.0	1.1	MHz
	Synchronizable Frequency	PLLIN/MODE = External Clock	●	200		2000	kHz
	PLLIN/MODE Input High Level for Clocking	PLLIN/MODE = External Clock	●	2.0			V
	PLLIN/MODE Input Low Level for Clocking	PLLIN/MODE = External Clock	●			0.8	V
PGOOD Output							
	PGOOD Voltage Low	I_{PGOOD} = 1mA			0.3	0.5	V
	PGOOD Leakage Current	V_{PGOOD} = 12V		–1		1	µA
	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage					
		V_{FB} Ramping Positive		7	10	13	%
		Hysteresis			2.5		%
		V_{FB} Ramping Negative		–13	–10	–7	%
		Hysteresis			2.5		%
T_{PG}	Delay for Reporting a Fault				24		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7103E is guaranteed to meet specifications from 0°C to 85°C with specifications over the –40°C to 125°C operating junction temperature range assured by design, characterization and correlation with statistical process controls. The LTC7103I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC7103H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC7103MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$$

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device. The overtemperature protection level is not production tested.

Note 5: The LTC7103 is tested in a feedback loop that servos V_{FB} to a voltage near the internal reference voltage to obtain the specified I_{TH} voltage.

Note 6: The Average Output Current Limit, the Top Switch Peak Current Limit and the Current Monitor Output Voltage are measured in a test circuit that simulates operation in a typical application.

Note 7: The minimum controllable on-time is measured in a test mode. (See Minimum ON-Time Considerations in the Applications Information section.)

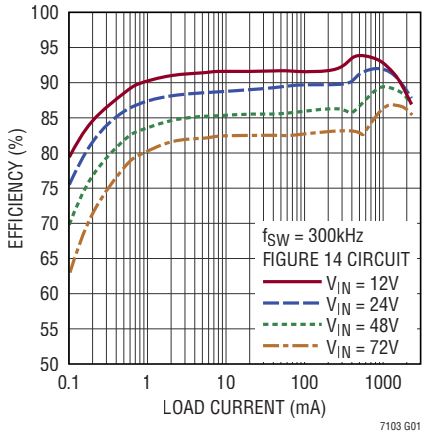
Note 8: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 9: See Operating at V_{OUT} > 6V in the Applications Information section for details about additional design constraints that may apply.

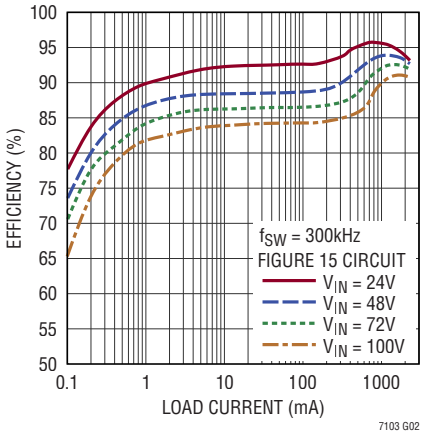
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

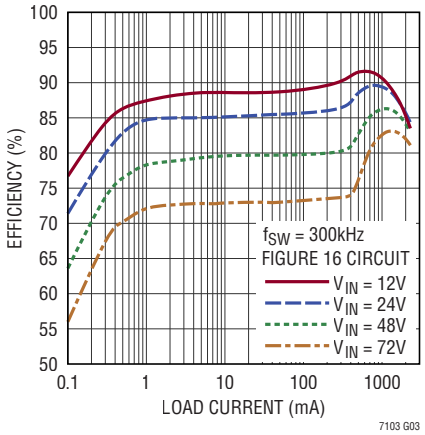
Burst Mode Efficiency at $5V_{OUT}$



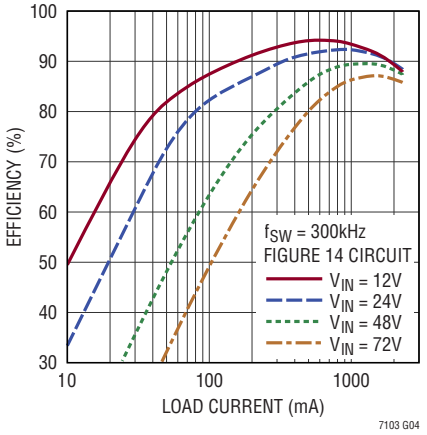
Burst Mode Efficiency at $12V_{OUT}$



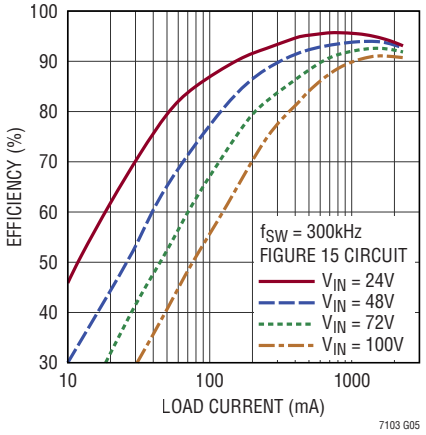
Burst Mode Efficiency at $3.3V_{OUT}$



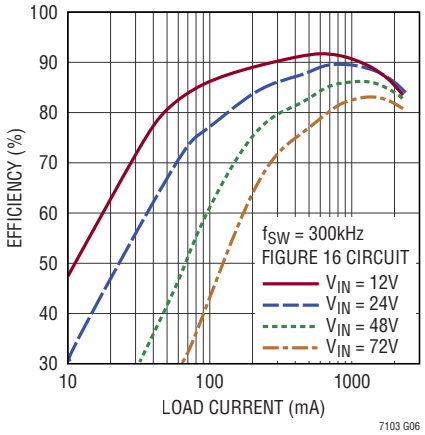
Pulse-Skipping Mode Efficiency at $5V_{OUT}$



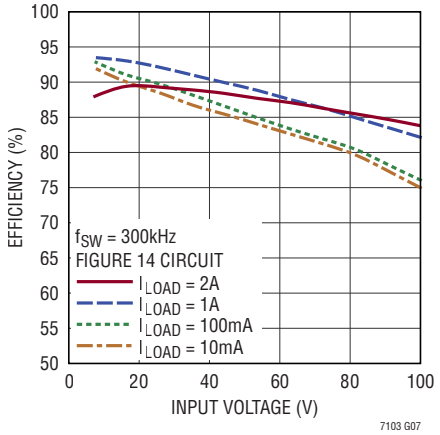
Pulse-Skipping Mode Efficiency at $12V_{OUT}$



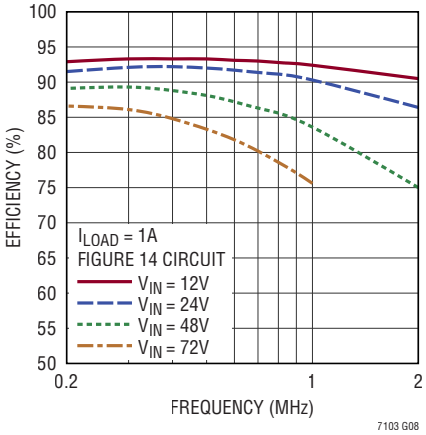
Pulse-Skipping Mode Efficiency at $3.3V_{OUT}$



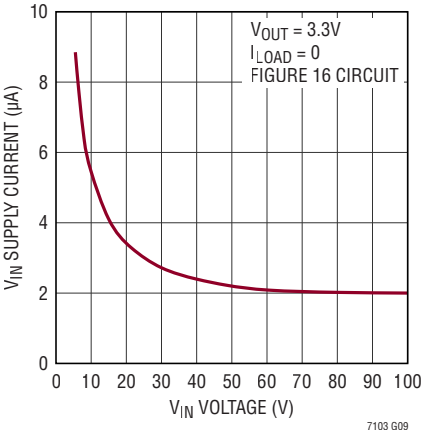
Efficiency vs Input Voltage V_{OUT} = 5V, Burst Mode Operation



Efficiency vs Frequency at 1A



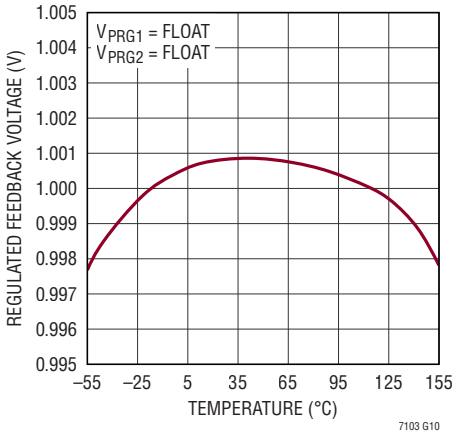
V_{IN} Input Current in Regulation vs Input Voltage



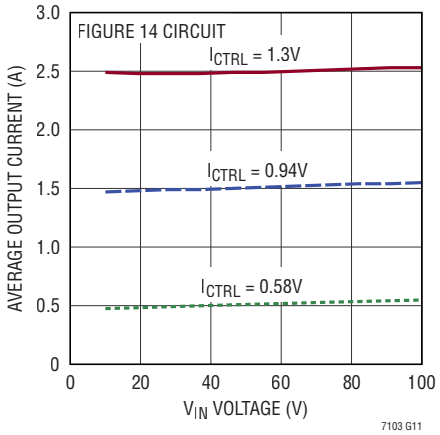
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

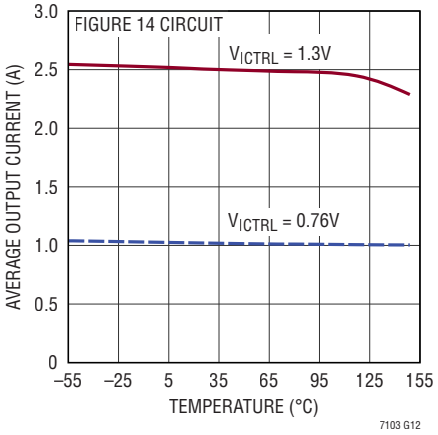
Regulated Feedback Voltage vs Temperature



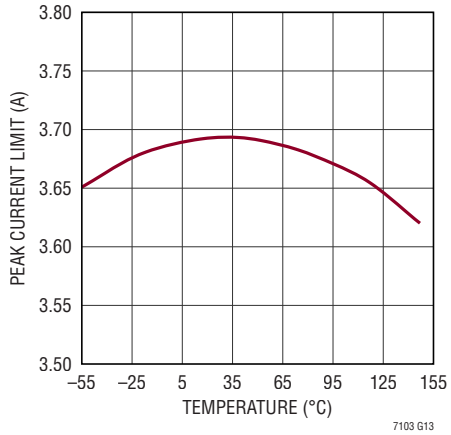
Average Output Current vs V_{IN}, I_{CTRL}



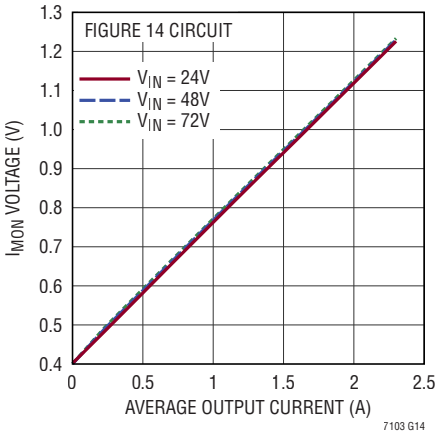
Average Output Current vs Temperature



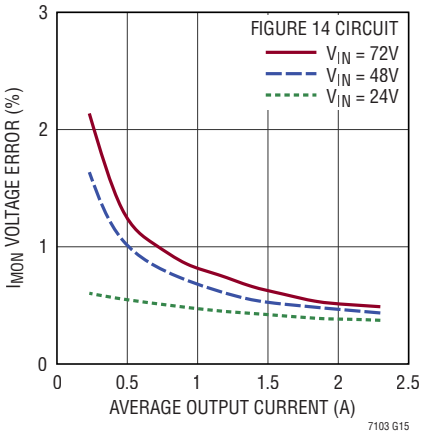
Peak Current Limit vs Temperature



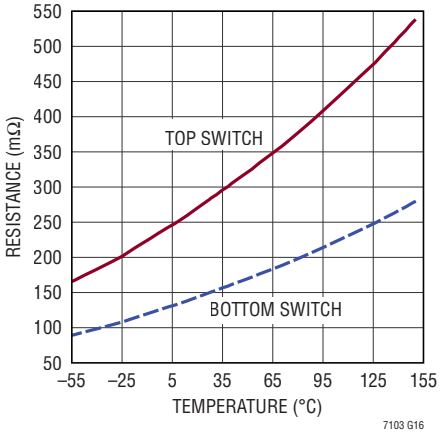
Output Current Monitor vs Average Output Current



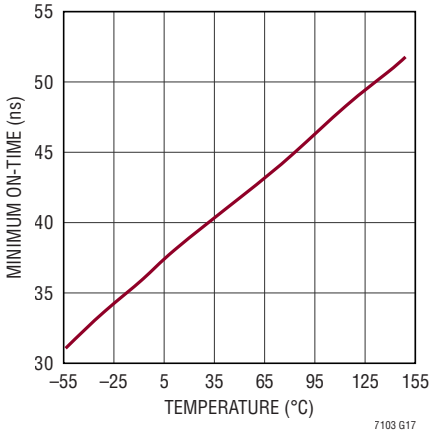
Output Current Monitor Error vs Average Output Current



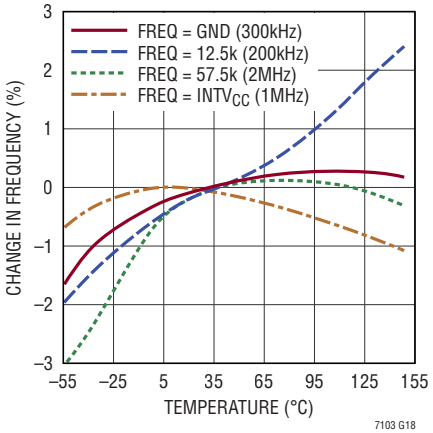
Top and Bottom Switch Resistance vs Temperature



Minimum On-Time vs Temperature



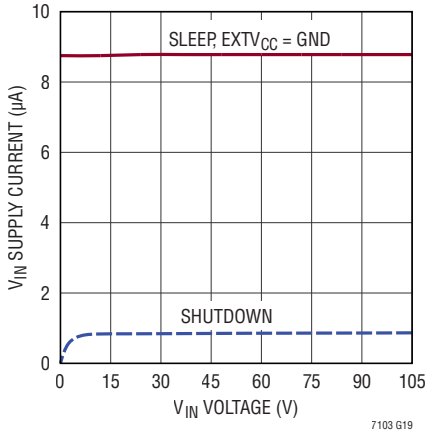
Oscillator Frequency vs Temperature



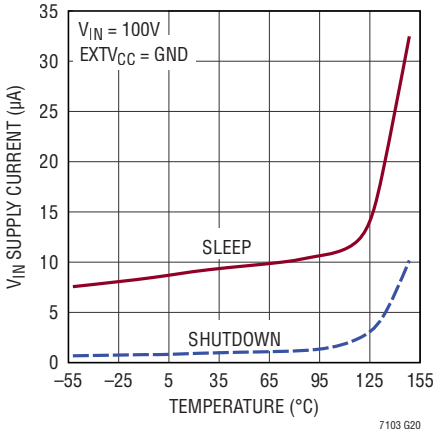
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

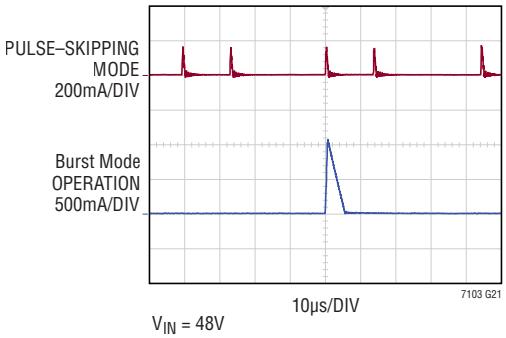
Quiescent Input Current vs Input Voltage



V_{IN} Quiescent Current vs Temperature

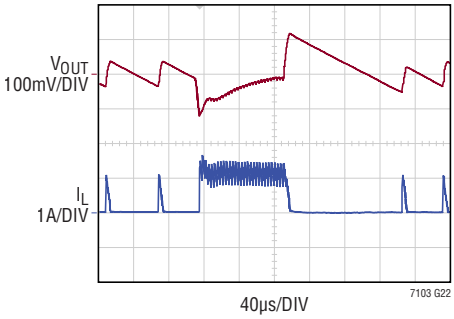


Inductor Current at Light Load



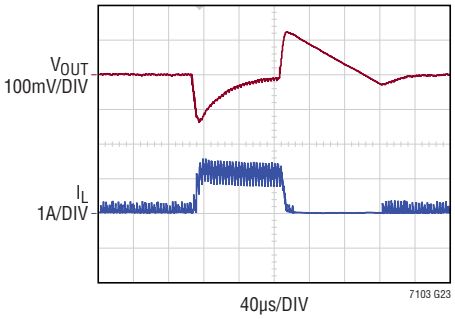
V_{IN} = 48V
I_{LOAD} = 200µA
FIGURE 14 CIRCUIT

Load Step Burst Mode Operation



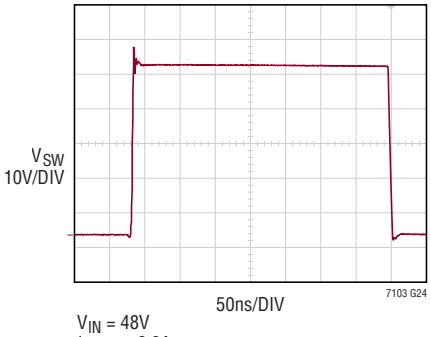
LOAD STEP = 50mA TO 1A
V_{IN} = 48V
FIGURE 14 CIRCUIT

Load Step Pulse-Skipping Mode



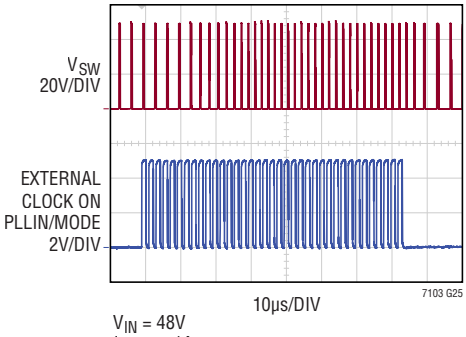
LOAD STEP = 50mA TO 1A
V_{IN} = 48V
FIGURE 14 CIRCUIT

SW Node Waveform at Full Load



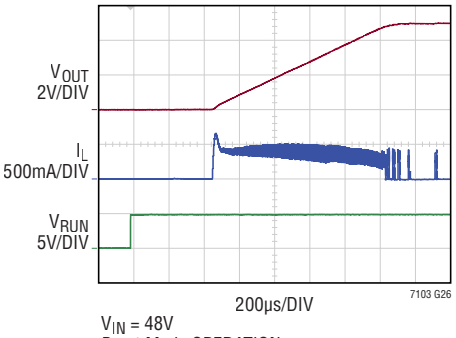
V_{IN} = 48V
I_{LOAD} = 2.3A
FIGURE 14 CIRCUIT

Synchronization to External Clock



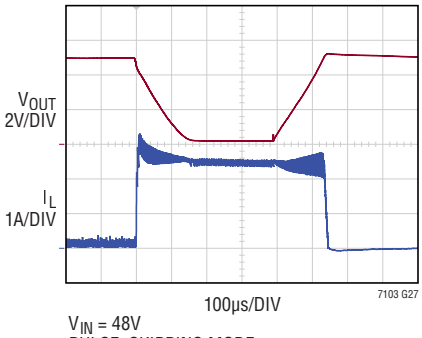
V_{IN} = 48V
I_{LOAD} = 1A
FIGURE 14 CIRCUIT

Start-Up from Shutdown



V_{IN} = 48V
Burst Mode OPERATION
FIGURE 14 CIRCUIT

Short-Circuit and Recovery

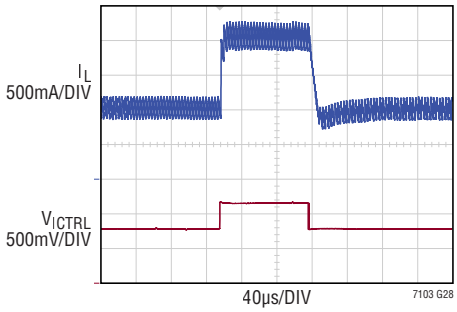


V_{IN} = 48V
PULSE–SKIPPING MODE
FIGURE 14 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

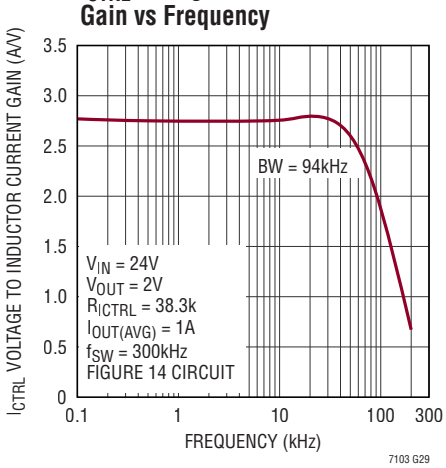
T_A = 25°C, unless otherwise noted.

Output Current Programming Current Loop Step Response



V_{ICTRL} = 0.76V TO 1.12V PULSE
V_{IN} = 48V, V_{OUT} = 2V
FIGURE 14 CIRCUIT

I_{CTRL} Voltage to Inductor Current Gain vs Frequency



Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

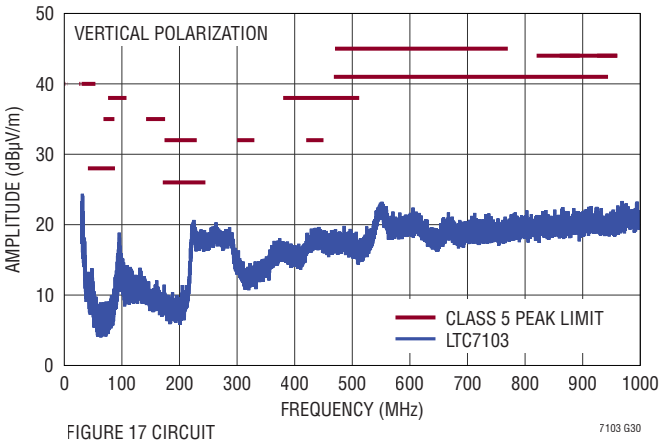


FIGURE 17 CIRCUIT
$48V_{IN}$ TO $5V_{OUT}$ AT 2A
f_{SW} = 400kHz

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

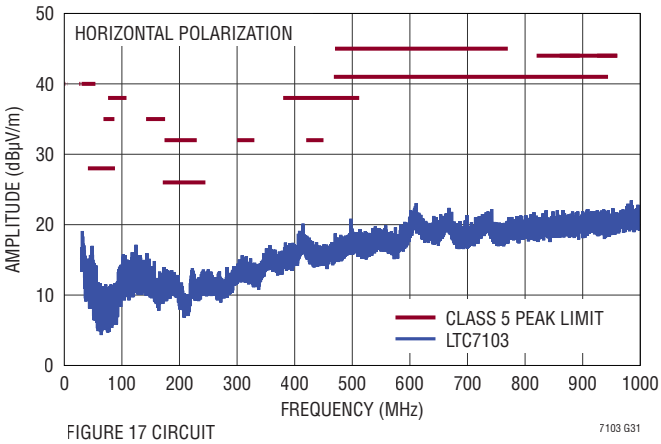


FIGURE 17 CIRCUIT
$48V_{IN}$ TO $5V_{OUT}$ AT 2A
f_{SW} = 400kHz

PIN FUNCTIONS

RUN (Pin 3): Run Control Input. Holding this pin below 1.1V shuts off the switching regulator. Holding this pin below 0.7V reduces the quiescent current to approximately 0.7µA. Place a resistor divider between V_{IN} and this pin to use as an undervoltage lockout. Tie this pin to V_{IN} to always enable the LTC7103.

SGND (Pin 6): Signal Ground.

OVLO (Pin 7): Overvoltage Shutdown Input. If the voltage on this pin exceeds 1.21V, then the switching regulator is shut down and the SS pin is internally grounded. Tie this pin to SGND to allow operation with V_{IN} up to 105V.

R_{IND} (Pin 8): Sets the current used to create an internal ramp that replicates the inductor current up-slope for low duty cycle operation. This pin generates a voltage that varies with the switching frequency. Place a resistor to SGND on this pin equal to 1/(7.5 • L) to set the internal ramp current. This pin can be left floating if fixed output voltage mode is selected using the V_{PRG1} and V_{PRG2} pins. If V_{PRG1} and V_{PRG2} are both floating, then a resistor from R_{IND} to SGND must be used.

I_{TH} (Pin 9): Error Amplifier Output and Switching Regulator Compensation Point. Place compensation components between the I_{TH} pin and SGND. Tie this pin to $INTV_{CC}$ for fixed internal compensation.

V_{FB} (Pin 10): Regulator Feedback Input. When set to adjustable mode, use an external resistor divider between the regulator output voltage and the V_{FB} pin. For fixed output voltage mode, tie V_{FB} directly to the regulator output.

FREQ (Pin 11): The frequency control pin for the internal VCO. Connect this pin to SGND for 300kHz operation or to $INTV_{CC}$ for 1MHz operation. Place a resistor to SGND on this pin to set the operating frequency between 200kHz and 2MHz. Minimize the capacitance on this pin if Burst Mode operation is used. This pin sources 40µA.

PLLIN/MODE (Pin 12): External Synchronization Input to Phase Detector and Burst Mode Control Input. When an external clock is applied to this pin, the phase-locked loop will force the rising edge of the SW signal to be synchronized with the rising edge of the external clock, and the LTC7103 operates in pulse-skipping mode. When not synchronizing to an external clock, this input determines how the LTC7103 operates at light loads. Tie this pin to SGND or float to select Burst Mode operation or tie this pin to $INTV_{CC}$ through a 100k resistor to select pulse-skipping operation. This pin sinks 10µA to SGND. Do not tie this pin directly to $INTV_{CC}$.

CLKOUT (Pin 13): Output clock signal available to synchronize additional regulators for parallel operation. The rising edge of CLKOUT is 180° out of phase with respect to the rising edge of the SW pin. The output level swings from SGND to $INTV_{CC}$.

PGOOD (Pin 14): Open-Drain Power Good Output. The V_{FB} pin is monitored to ensure that the output is in regulation. When the output is not in regulation, the PGOOD pin is pulled low.

SS (Pin 15): Soft-Start and Regulator Timeout Input. The voltage on the SS pin limits the regulated output voltage when the SS voltage is less than 1V. An internal 11µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Leave this pin floating to use the internal 1.2ms soft-start ramp. The SS pin also serves as a timeout to disable switching if the $EXTV_{CC}$ voltage is too low. To disable the regulator timeout feature, tie a 75k resistor between SS and $INTV_{CC}$. See Soft-Start and LDO Regulator Timeout in the Applications Information section.

I_{CTRL} (Pin 16): Programs the Average Output Current in Constant Current Mode. The voltage on this pin determines the maximum I_{TH} voltage, which in turn sets the average output current in constant-current mode. The peak current limit tracks 1.2A above the average current limit set point. Tie this pin to a voltage between 0.4V and 1.3V to program the average output current to a value between 0A and 2.5A. An internal 20µA pull-up on this pin allows a single resistor to SGND to be used to set the voltage. Float this pin to set the average output current to 2.5A and the peak current limit to 3.7A.

PIN FUNCTIONS

I_{MON} (Pin 17): Average Output Current Monitor. This pin generates a voltage between 0.4V and 1.3V that corresponds to an average output current between 0A and 2.5A.

V_{PRG1}, V_{PRG2} (Pins 18,19): Output Voltage Programming Pins. These pins set the regulator to adjustable output mode or to fixed output mode. Floating both pins allows the output to be programmed through the V_{FB} pin using external resistors, regulating V_{FB} to the 1V reference. Tying one of these pins to SGND or $INTV_{CC}$ while the other is tied to SGND, $INTV_{CC}$ or floating programs the output to one of eight fixed output voltages. See Output Voltage Programming in the Applications Information section.

$EXTV_{CC}$ (Pin 20): External Power Input to an Internal LDO that Generates $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power from $EXTV_{CC}$, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is between 3.1V and 40V. If $EXTV_{CC}$ is not used, the regulator timeout feature must be disabled by tying a 75k resistor between SS and $INTV_{CC}$. See $INTV_{CC}$ Regulations in the Applications Information section.

$INTV_{CC}$ (Pin 21): Output of the Internal LDO regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to PGND with a 1µF to 4.7µF ceramic capacitor.

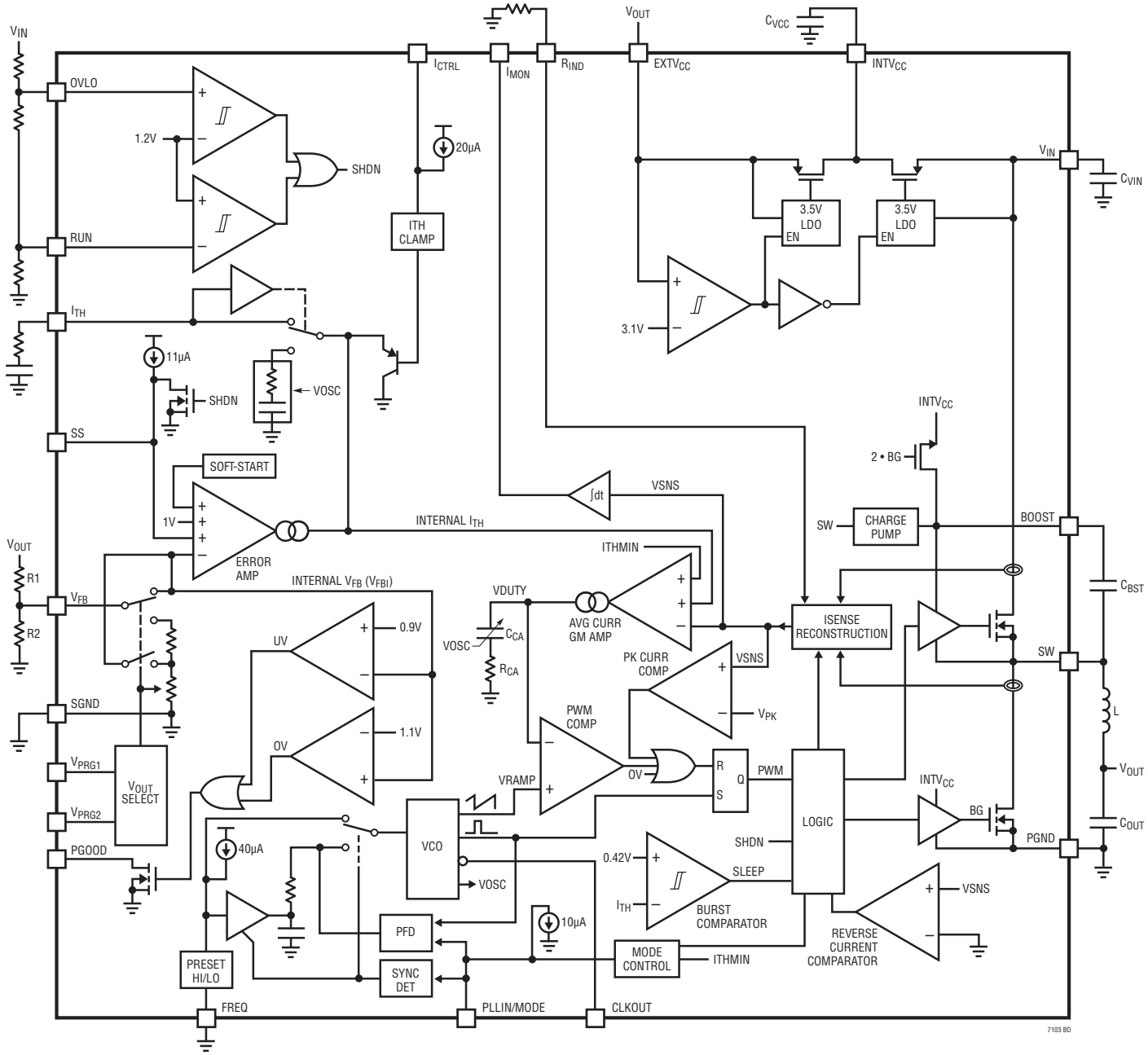
SW (Pins 24, 25, 26): SW Node connection from the internal MOSFET power switches to the output inductor.

BOOST (Pin 27): Bootstrapped Supply to the High Side Floating Gate Driver. Connect a 0.1µF ceramic capacitor between the BOOST and SW pins.

V_{IN} (Pins 30, 31, 32): Power Input Supply. This is the power input to the integrated high side MOSFET switch as well as the input to the internal LDO that generates $INTV_{CC}$ voltage. Decouple this pin with a capacitor to PGND.

PGND/Exposed Pad (Pin 35, 36, 37): Power Ground. Connect to power ground plane. The exposed pad must be connected to PCB ground for rated electrical and thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC7103 is a high efficiency, monolithic, synchronous step-down DC/DC converter utilizing a constant frequency, average current mode control architecture. Average current mode control enables fast and precise control of the output current without the need for an external sense resistor or current sense amplifier. Instead, the inductor current is sensed internally by losslessly monitoring the top and bottom power switch currents. The LTC7103 also contains a unique circuit that replicates the inductor current immediately after the top switch turn-on and combines this with the sensed switch currents to fully reconstruct the inductor current signal internally. This technique allows for direct control and monitoring of the average output current as well as clean operation at very low duty cycles.

During normal operation, the internal top power switch (N-channel MOSFET) is turned on at the beginning of each clock cycle, causing the inductor current to increase. The sensed inductor current is then delivered to the average current amplifier, whose output (VDUTY) is compared with a saw-tooth ramp (VRAMP). When the VRAMP voltage exceeds the VDUTY voltage, the PWM comparator trips and turns off the top power MOSFET.

After the top power MOSFET turns off, the synchronous power switch (N-channel MOSFET) turns on, causing the inductor current to decrease. The bottom switch stays on until the beginning of the next clock cycle, unless the reverse current limit (0A) is reached and the reverse current comparator trips.

In closed-loop operation, the average current amplifier creates an average current loop that forces the average sensed current signal to be equal to the internal I_{TH} voltage. Note that the DC gain and compensation of this average current loop is automatically adjusted to maintain an optimum current-loop response. The error amplifier adjusts the I_{TH} voltage by comparing the divided-down output voltage (V_{FBI}) with a 1.0V reference voltage. If the load current changes, the error amplifier adjusts the average inductor current as needed to keep the output voltage in regulation.

The LTC7103 has been optimized to provide the fastest possible average current loop. To achieve this, the filter on the average current amplifier output (C_{CA}, R_{CA}) is set to provide high DC gain (provided by integrator capacitor C_{CA}) while allowing the inductor current signal to pass through unfiltered. This is accomplished by resistor R_{CA}, which introduces a zero that is well below the switching frequency. The resulting typical PWM comparator waveforms are shown in Figure 1. Note that the VDUTY signal is an inverted reflection of the inductor current signal, which is essential for obtaining a high speed average current loop.

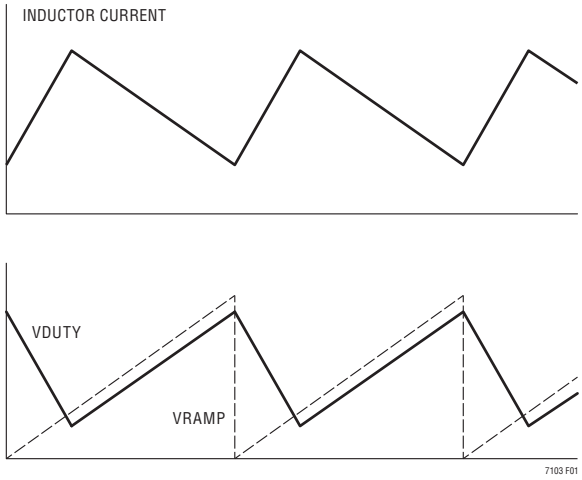


Figure 1. Typical Current Loop Operating Waveforms

Voltage loop compensation can be set externally using the I_{TH} pin, taking advantage of OPTI-LOOP compensation to optimize the loop response. The compensation of the voltage loop is essentially the same as for peak current mode control. Alternatively, the I_{TH} pin can be tied to $INTV_{CC}$ to select internal voltage loop compensation. When internal voltage loop compensation is selected, the LTC7103 automatically adjusts the internal compensation based on switching frequency to maintain a fast and stable voltage loop.

Power and Bias Supplies (V_{IN}, SW, BOOST, $INTV_{CC}$, $EXTV_{CC}$ Pins)

The V_{IN} pins on the LTC7103 are used to supply voltage to the drain terminal of the internal high side N-channel MOSFET. These pins also supply bias voltage for an internal

OPERATION

LDO regulator (the V_{IN} LDO) that generates 3.5V at $INTV_{CC}$. The voltage on $INTV_{CC}$ in turn is used for internal chip bias as well as gate drive for the bottom power MOSFETs. The gate drive for the top power MOSFET is supplied by a floating supply (C_{BST}) between the BOOST and SW pins, which is charged by an internal synchronous diode from $INTV_{CC}$. In addition, an internal charge pump allows for 100% duty cycle operation by maintaining the BOOST to SW voltage when the top MOSFET is on continuously.

To improve efficiency and limit power dissipation in the V_{IN} LDO regulator, a second LDO regulator (the $EXTV_{CC}$ LDO) allows the $INTV_{CC}$ voltage to be derived from the lower-voltage $EXTV_{CC}$ pin. In most applications, the $EXTV_{CC}$ pin is simply tied directly to the regulated output voltage of the DC/DC converter to enable operation in a high efficiency, bootstrapped configuration. In order to ensure that the power dissipation on the internal V_{IN} LDO is limited to a safe level, the LTC7103 incorporates a special regulator timeout feature into the soft-start pin.

Start-Up and Shutdown (RUN, SS, OVLO Pins)

When the RUN pin is below 0.7V, the LTC7103 enters a low current shutdown state, reducing the DC supply current to 0.7µA. When the RUN pin is above 0.7V and the V_{IN} pin is above than the internal undervoltage threshold ($V_{IN(UVLO)}$) of 4.55V, the $INTV_{CC}$ LDO regulators are enabled. However, switching is inhibited until the RUN pin is greater than $V_{RUN(ON)}$ = 1.21V. This allows the RUN pin to be used to implement a V_{IN} undervoltage lockout function so that the power supply will not operate below a user-adjustable level. In addition, switching is also inhibited if the voltage on the OVLO pin exceeds $V_{OV(R)}$ = 1.21V. This feature can be used to implement an input overvoltage lockout function to prevent power supply operation during an overvoltage condition on the input supply.

When appropriate voltages are present on the V_{IN}, RUN and OVLO pins, the LTC7103 will begin switching and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 1.2ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The 11µA current that is sourced from the SS pin will create a smooth voltage ramp on the capacitor. If this external ramp rate is slower than the internal 1.2ms soft-start, then the output voltage will be limited by the ramp rate on the SS pin instead. Once both the external and internal soft-start ramps have exceeded 1V, the output voltage will be in regulation. The internal and external soft-start functions are reset during initial start-up and after an undervoltage or overvoltage condition on the input supply.

The soft-start pin is also used to implement a regulator timeout feature. This feature limits die temperature rise due to power dissipation in the internal V_{IN} LDO regulator by disabling the top and bottom power MOSFETs after a timeout, if $EXTV_{CC}$ voltage is not present. This is useful, for example, if $EXTV_{CC}$ is tied to the output of the DC/DC converter, but the converter output gets shorted to ground. During start-up, a regulator timeout begins after both the internal and external soft-start ramps have exceeded 1V, and $EXTV_{CC} < 3V$. If this condition persists for a period of time (approximately 1.4 times the normal soft-start time), then a regulator timeout fault occurs and all switching stops. After a long restart delay (approximately 46 times the normal soft-start time), a restart is initiated. If the regulator timeout feature is not needed, the SS pin should be tied to $INTV_{CC}$ through a 75k resistor. See Soft-Start and LDO Regulator Timeout in the Applications Section for more information.

Output Voltage Programming (V_{PRG1}, V_{PRG2}, V_{FB} Pins)

The V_{PRG1} and V_{PRG2} pins provide a great deal of flexibility in programming the output voltage of the power supply. Floating both pins selects adjustable V_{OUT} mode. In this mode, the output is programmed using external resistors on the V_{FB} pin, and the V_{FB} voltage is regulated to the 1V reference. If one of the pins is tied either to SGND or $INTV_{CC}$, then fixed output voltage mode is selected. In this mode, precision internal resistor dividers are used to program the output voltage to one of eight fixed voltage levels. See Output Voltage Programming in the Applications Information Section.

Inductor Current Replication (R_{IND} Pin)

The LTC7103 contains a unique circuit that replicates the inductor current immediately after the top switch turn-on and combines this with the sensed switch currents to fully reconstruct the inductor current signal internally.

OPERATION

This technique allows for direct control and monitoring of the average output current as well as clean operation at very short top switch on-times. In order to replicate the inductor current, the LTC7103 needs to know the approximate value of the inductor. This is achieved by placing a resistor on the R_{IND} pin that is equal to 1/(7.5 • L). The LTC7103 uses the current in the R_{IND} resistor in conjunction with the voltage on the V_{IN} and SW pins to generate a replicated inductor current signal. In addition, the R_{IND} pin current is also used in conjunction with the voltages on V_{IN} and SW to set the DC gain of the average current amplifier. This is done to maintain optimum current loop performance over all operating conditions.

Note that if fixed output voltage mode is selected using the V_{PRG1} and V_{PRG2} pins, then the R_{IND} pin can be left floating. In this case, the LTC7103 will assume a particular inductor value based on output voltage and switching frequency. See Inductor Value and R_{IND} Resistor Selection in the Applications Information section.

Light Load Operation: Burst and Pulse-Skipping Modes (PLLIN/MODE Pin)

The LTC7103 can be set to enter high efficiency Burst Mode operation or constant frequency pulse-skipping mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground. To select pulse-skipping mode, tie the PLLIN/MODE pin to $INTV_{CC}$ through a 100k resistor.

When the LTC7103 is set for Burst Mode operation, the minimum output current is set to approximately 200mA even though the voltage on the I_{TH} pin might indicate a lower value. If the average inductor current is higher than the load current, the error amplifier will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.4V, the internal sleep signal goes high (enabling sleep mode) and both MOSFETs are turned off. The I_{TH} pin is then disconnected from the output of the error amplifier and parked at 0.43V.

In sleep mode, much of the internal circuitry is turned off, reducing the total quiescent current that the LTC7103 draws to 9µA.When $EXTV_{CC}$ is present, the majority of this quiescent current (8µA) is drawn from the $EXTV_{CC}$ supply and only 1µA is drawn from the V_{IN} supply. This dramatically reduces the sleep mode V_{IN} supply current in bootstrapped applications where $EXTV_{CC}$ is tied to V_{OUT} and $V_{IN} >> V_{OUT}$. In sleep mode, the load current is supplied by the output capacitor. As the output voltage V_{OUT} decreases, the error amplifier output begins to rise. When the V_{OUT} voltage drops enough, the I_{TH} pin is reconnected to the output of the error amplifier, the sleep signal goes low, and normal operation is resumed by turning on the top MOSFET on the next cycle of the internal oscillator.

When the LTC7103 is set for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the converter operates with discontinuous inductor current (DCM).

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC7103 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation.

When operating with discontinuous inductor current (DCM) in either burst or pulse-skipping mode, the LTC7103 smoothly transitions from average current to peak current control. This feature eases compensation of the voltage loop in light load DCM operation by removing the pole associated with the average current loop.

OPERATION

To avoid spurious changes in the operating mode, the LTC7103 incorporates a 20µs delay before changing from one mode to another. This is particularly helpful since the PLLIN/MODE pin can be used to select an initial operating mode, and subsequently be used to receive an external clock for synchronization. The 20µs delay avoids changes in mode while the synchronizing signal is recognized. When synchronized, the LTC7103 operates in pulse-skipping mode.

Frequency Selection and Phase-Locked Loop (FREQ, PLLIN/MODE Pins)

The switching frequency of the LTC7103 can be selected using the FREQ pin, which can be tied to SGND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to SGND selects 300kHz while tying FREQ to $INTV_{CC}$ selects 1MHz. Placing a resistor between FREQ and SGND sends the FREQ pin voltage into the input of the voltage controlled oscillator (VCO), allowing the frequency to be programmed between 200kHz and 2MHz.

A phase-locked loop (PLL) is available on the LTC7103 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC7103's phase detector (PFD) and low pass filter adjust the voltage of the VCO input to align the turn-on of the top MOSFET to the rising edge of the synchronizing signal.

When an external clock is detected, the PFD low pass filter is quickly prebiased to the operating frequency set by the FREQ pin before the PLL is allowed to take over the VCO. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the top MOSFET turn-on. The ability to prebias the loop filter allows the PLL to lock in rapidly without deviating far from the desired frequency.

The typical capture range of the phase-locked loop is from approximately 160kHz to 2.3MHz, with a guarantee over all manufacturing variations to be between 200kHz and 2MHz. In other words, the LTC7103's PLL is guaranteed to lock to an external clock source whose frequency is between 200kHz and 2MHz.

After the PLL has locked to an external clock, if the external clock is stopped, the LTC7103 will immediately detect this condition and prevent the PFD from adjusting the loop, so that the internal oscillator continues operating at the external clock frequency. After approximately 9µs, the LTC7103 will detect a loss of SYNC, and the oscillator operating frequency returns to the level set by the FREQ pin. This feature prevents the oscillator frequency from dipping momentarily when the external clock is stopped, and enables smooth transitions into and out of synchronization.

The typical input clock thresholds on the PLLIN/MODE pin are 1.5V rising and 1.1V falling, and this input is TTL compatible.

The CLKOUT pin supplies a reference clock that is helpful for synchronizing other switching circuits to the LTC7103 switching frequency. The output high level of this signal is equal to $INTV_{CC}$ (3.5V typical), and the rising edge of the CLKOUT signal is 180° out of phase with respect to the top MOSFET turn-on. This makes it easy to synchronize two LTC7103 converters and operate them out of phase to minimize input current, or to use two LTC7103's together for a higher current, 2-Phase converter. See 2-Phase Operation in the Applications Information section.

Setting and Monitoring Output Current (I_{CTRL}, I_{MON} Pins)

Because the LTC7103 utilizes average current mode control, in which the I_{TH} voltage is proportional to average output current, the setting and monitoring of the average output current is straight-forward.

The average output current limit is set using the I_{CTRL} pin, whose voltage directly clamps the I_{TH} voltage to a maximum level. Tie this pin to a voltage between 0.4V and 1.3V to program the average output current to a value between 0A and 2.5A. An internal 20µA pull-up on this pin allows a single resistor to SGND to be used to set the voltage. This pin can be floated to set the average output current to 2.5A and the peak current limit to 3.7A.

By maintaining a fast and optimized current loop over all operating conditions, the LTC7103 responds to changes in the I_{CTRL} pin voltage with the greatest possible speed. This is orders of magnitude faster than most competing solutions, where a slow, average current loop is placed

OPERATION

outside of the voltage regulation loop. By placing the average current loop inside of the voltage regulation loop, the LTC7103 allows for current programming on a nearly cycle-by-cycle basis.

The average output current can be monitored at the I_{MON} pin. The reconstructed inductor current signal (V_{SNS}) is run through a low pass filter (f_c = 10kHz), buffered, and then delivered to the I_{MON} pin. The voltage on the I_{MON} normally varies between 0.4V and 1.3V, corresponding to an average output current between 0A and 2.5A. The I_{MON} voltage may momentarily be less than 0.4V or greater than 1.3V, but eventually is limited to these levels by the average current loop. During SLEEP, this pin is held at 0.4V.

Short-Circuit Protection and Minimum On-Time

The architecture of the LTC7103 provides inherent protection against short-circuit conditions, without the need for folding back either the output current or the oscillator frequency. This is made possible because the PWM comparator is continuously receiving inductor current information from the average current amplifier. This results in automatic cycle skipping under short-circuit conditions if the minimum on-time of the top switch is too long to maintain control of the inductor current at the full switching frequency. Because a given switching cycle is skipped only as needed to satisfy the high speed average current loop, this creates a brick-wall style current limit without any foldback or hiccups in the operation down to V_{OUT} = 0V. Figure 2 illustrates the typical operation of this brick-wall current limit.

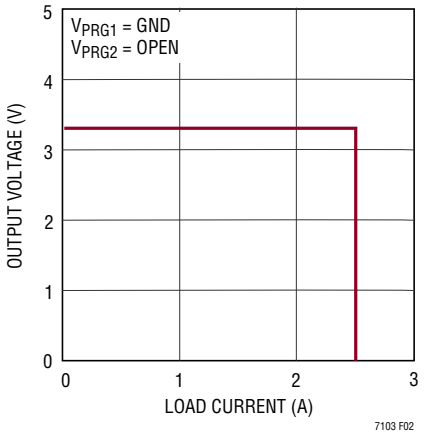


Figure 2. Typical Current Limit Operation

While the average current loop is extremely fast, a failsafe peak current limit (I_{PK}) comparator has also been incorporated to ensure that the inductor current cannot exceed a safe level even momentarily. The peak current limit is internally set to 1.2A above the average current limit, and tracks with the average current limit set by the voltage on the I_{CTRL} pin. In practice, this peak current limit comparator is only needed when there is an abnormal voltage on the average current amplifier output filter and a short-circuit is simultaneously applied. In this case, the peak current limit comparator may be needed for a few cycles while the average current amplifier filter settles.

When operating at a high step-down ratio from V_{IN} to V_{OUT}, care should be taken to choose a switching frequency that is low enough to avoid operation at minimum on-time. However, in the event that a high step-down ratio requires the minimum on-time to be exceeded, the LTC7103 architecture offers inherent protection against output overvoltage. Once again, the PWM comparator will automatically cause the skipping of a cycle as needed to maintain regulation of the output voltage. While this avoids output overvoltage, operation in this mode is undesirable as it increases inductor current ripple.

In addition to this inherent protection, a separate output overvoltage comparator monitors the V_{FB} voltage and prevents top MOSFET turn-on if an overvoltage condition is present (V_{FB} exceeds $V_{FB(OV)}$).

Boost Supply and Dropout Operation

By making use of an internal charge pump, the LTC7103 is capable of operating at 100% duty cycle, providing the lowest possible dropout voltage and zero switching noise while in dropout. This charge pump delivers the small current required to maintain the static gate voltage on the top MOSFET switch when operating in dropout. When not operating in dropout, the gate drive voltage required for switching the top MOSFET switch is supplied by the charge pump formed by the BOOST capacitor (C_{BST}), the bottom MOSFET switch, and an internal switch from $INTV_{CC}$ to BOOST. As dropout is approached, the on-time

OPERATION

of the bottom MOSFET switch is lengthened as needed to maintain an adequate supply to the floating gate driver between BOOST and SW.

Power Good (PGOOD Pin)

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the internal feedback voltage (V_{FBI}) is not within ±10% of the 1V reference voltage. The PGOOD pin is also pulled low when the RUN pin is low (shutdown). When V_{FBI} is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 16V. There is a 20µs delay (T_{PG}) before the PGOOD pin goes low in response to the V_{FBI} voltage going outside of the ±10% window.

Overtemperature and Overvoltage Protection

In addition to the OVLO pin, which provides a user-adjustable protection against V_{IN} overvoltage, the LTC7103 contains an internal V_{IN} overvoltage shutdown feature. If the V_{IN} pin voltage exceeds 118.5V rising (112V falling), then the top and bottom MOSFETs are held off and all switching stops. Likewise, if the internal die temperature exceeds 171°C rising (155°C falling), then the LTC7103 disables switching as well as the LDO regulators until the temperature drops. Note that the internal overvoltage and overtemperature protection features are activated outside of the absolute maximum range of operation, and therefore should not be relied upon operationally. These features are only intended as a secondary failsafe to improve overall system reliability and safety.

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A general LTC7103 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and begins with the selection of the operating frequency and light load operating mode. Next, the inductor L is chosen, which also determines the value of resistor R_{IND}. After the inductor is chosen, the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the boost capacitor C_{BST}, can be selected. Next, either a fixed output voltage or feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as V_{IN} undervoltage/overvoltage lock-out, external soft-start, LDO regulator timeout, external loop compensation, average output current monitor and limit, and PGOOD.

Setting the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

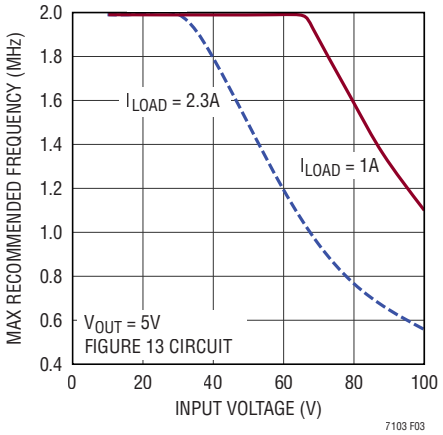

Figure 3. Maximum Recommended Frequency vs Input Voltage

For most LTC7103 applications, a good balance between size and efficiency is achieved with a switching frequency between 300kHz and 750kHz. Operating at higher switching frequencies up to 2MHz is readily possible, but switching losses generally limit the input voltage to lower levels. This is illustrated in Figure 3, which shows the maximum recommended switching frequency versus input voltage at 1A and 2.3A loads for the application circuit of Figure 14. These lines correspond to a power loss of 2.5W in the LTC7103, which will result in a junction temperature rise of approximately 85°C without air flow. See Efficiency Considerations and Thermal Considerations sections for more information on calculating the power loss and temperature rise.

An additional constraint on operating frequency is the minimum controllable on-time of the LTC7103. While the architecture of the LTC7103 inherently maintains output voltage regulation even if the minimum on-time is exceeded, cycle-skipping will result in increased inductor current ripple. To avoid this, chose a switching frequency such that:

$$f < \frac{V_{OUT}}{V_{IN(MAX)} \bullet t_{ON(MIN)}}$$

When operating at V_{OUT} > 6V, additional constraints on the switching frequency may also apply. See Operating at V_{OUT} > 6V section for more information.

The switching frequency is set using the FREQ and/or PLLIN/MODE pins as shown in Table 1.

Table 1. Frequency Setting

FREQ PIN	PLLIN/MODE PIN	FREQUENCY(F)
SGND	DC Voltage	300kHz
$INTV_{CC}$	DC Voltage	1MHz
R = (f/40 + 7.5k) to SGND	DC Voltage	200kHz to 2MHz
Any of the Above	External Clock	Phase-Locked to External Clock (200kHz to 2MHz)

Tying the FREQ pin to SGND selects 300kHz while tying FREQ to $INTV_{CC}$ selects 1MHz. Since the FREQ pin sources 40µA, placing a resistor between FREQ and SGND allows the frequency to be programmed anywhere between 200kHz and 2MHz. Choose a FREQ pin resistor such that:

$$R_{FREQ} = \frac{f}{40} + 7.5k$$

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A phase-locked loop (PLL) is also available on the LTC7103 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. Once synchronized, the turn-on of the top MOSFET is aligned to the rising edge of the synchronizing signal. See Phase-Locked Loop and Frequency Synchronization section for details.

Setting the Light-Load Operating Mode

The LTC7103 can be set to enter high efficiency Burst Mode operation or constant frequency pulse-skipping mode at light load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground. To select pulse-skipping mode, tie the PLLIN/MODE pin to $INTV_{CC}$ through a 100k resistor. When synchronized, the LTC7103 operates in pulse-skipping mode. Table 2 summarizes the use of the PLLIN/MODE pin to select light-load operating mode.

Table 2. Mode Selection

PLLIN/MODE PIN	LIGHT-LOAD OPERATING MODE
SGND	Burst Mode Operation
R = 100k to $INTV_{CC}$	Pulse-Skipping Mode
External Clock	Pulse-Skipping Mode

In general, the requirements of each application will dictate the appropriate choice for light-load operating mode.

In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the converter operates in discontinuous operation. In addition, when the average output current falls below approximately 200mA, the inductor current will begin bursting at frequencies lower than the switching frequency, and entering a low current SLEEP mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light loads.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple and EMI.

In some applications, it may be desirable to change light-load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high efficiency Burst Mode operation by keeping the PLLIN/MODE pin set to 0V. When the system wakes, one might send an external clock to PLLIN/MODE, to switch to pulse-skipping mode. Such on-the-fly mode changes can allow an individual application to benefit from the advantages of each light-load operating mode.

Inductor Value Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For proper operation, always use an inductor value that is greater than:

$$L_{MIN} > 520nH \bullet V_{OUT}$$

Note that in applications with $V_{OUT} > 6V$, additional constraints on the inductance value may also apply. See Operating at $V_{OUT} > 6V$ section for more information.

A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors, but results in greater core loss in the inductor, greater ESR loss in the output capacitor, and larger output ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point for setting the ripple current is approximately $0.75A_{P-P}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee the ripple

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current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The LTC7103 contains a fast, average current limit loop that limits the DC output current to a value determined by the voltage on the I_{CTRL} pin. (See Average Output Current Limit and Monitor section for details.) However, some applications may experience inductor current transients that are limited by the peak current limit comparator, which tracks nominally 1.2A above the average current limit set point. To avoid saturation, choose an inductor with a saturation current I_{SAT} such that:

$$I_{SAT} > \frac{V_{ICTRL} - 0.4}{0.36} + 1.5A$$

This enables the use of an inductor with a current rating that fits the needs of a given application. If the average output current limit is set to the default value of 2.5A, then an inductor with I_{SAT} > 4A is required. However, if the average current limit is set to 1.5A (V_{ITCRL} = 0.94V), then an inductor with I_{SAT} > 3A may be used. Note that if there is a varying voltage on the I_{CTRL} pin, always use the highest value present on I_{CTRL} when calculating the required inductor saturation current. See Average Output Current Limit and Monitor section for details on setting the average current limit.

If fixed V_{OUT} operation is selected using the V_{PRG1} and V_{PRG2} pins, the R_{IND} pin can be left floating, but only if the inductance value is chosen according to Table 3. Since the R_{IND} pin resistor indicates the inductance value being used, the LTC7103 will automatically assume an inductance value as shown in Table 3 when this pin is left floating. These inductance values will provide an inductor ripple current that is approximately 30% to 40% of the full load current. If the nominal value of the inductance used differs by more than 10% from the values specified in Table 3, a resistor must be placed on the R_{IND} pin to indicate this value.

Table 3. Required Inductor Values with R_{IND} Pin Floating

	REQUIRED INDUCTANCE VALUE (R_{IND} = FLOAT)		
FIXED V_{OUT}	f = 300kHz	f = 1MHz	f = ADJ
1.2V	3.9µH	1.2µH	L = 1.1/f
1.8V	5.6µH	1.8µH	L = 1.7/f
2.5V	8.2µH	2.5µH	L = 2.5/f
3.3V	12µH	3.3µH	L = 3.6/f
3.6V	12µH	3.3µH	L = 3.6/f
5V	18µH	5.6µH	L = 5.4/f
12V	47µH	15µH	L = 14/f
15V	47µH	15µH	L = 14/f

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value but is very dependent on the inductance selected. As the inductance increases, core loss decreases. Unfortunately, increased inductance requires more turns of wire leading to increased copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate hard, meaning the inductance collapses abruptly when the peak design current is exceeded. This collapse will result in an abrupt increase in inductor ripple current, so it is important to ensure the core will not saturate.

R_{IND} Resistor Selection

The resistor on the R_{IND} pin is used to indicate to the LTC7103 what inductance value is being used. This is required for the internal reconstruction of the inductor current waveform and to set the DC gain of the current loop. Once the inductor value is selected, the R_{IND} pin resistor is chosen according to:

$$R_{IND} = \frac{1}{7.5 \bullet L}$$

If fixed V_{OUT} operation is selected using the V_{PRG1} and V_{PRG2} pins, the R_{IND} pin can be left floating, but only if the inductance value is chosen according to Table 3. Do

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not leave the R_{IND} pin floating when adjustable V_{OUT} mode is selected. If the R_{IND} pin is left floating and adjustable V_{OUT} mode selected (V_{PRG1} and V_{PRG2} are both floating), the LTC7103 will detect this as a fault condition and will not operate.

The allowable current range on the R_{IND} pin is between 8µA and 220µA, which means that:

$$1.1 \le f \bullet L \le 30$$

Since f ≥ 200kHz, this sets a maximum inductance value of 150µH. In practice, the above constraint does not normally affect the choice of inductor value.

C_{IN} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the drain of the top power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of:

$$I_{RMS} = \frac{I_{OUT(MAX)}}{2}$$

Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7103, ceramic capacitors can also be used for C_{IN}. In many applications, an X7R capacitor of 4.7µF or greater is a suitable choice. Always consult the manufacturer if there is any question.

The input capacitor, C_{IN}, should be placed as close as possible to the V_{IN} pins, with a low inductance connection to the PGND (paddle) of the IC. In addition to a larger bulk capacitor, a smaller case-size (0603 or 0805) ceramic decoupling capacitor can be placed closer to the V_{IN} pins to reduce EMI.

Using an LC Input Filter

For high voltage applications, it can be costly to use bulk capacitance that is rated to handle the required RMS input current. Moreover, when using a simple capacitor to filter the AC input current, it is difficult to determine exactly where this AC current is flowing when a power supply is placed into a larger system. To avoid these issues, an LC filter can be used on the power supply input as shown in Figure 4. This keeps the higher AC currents contained in a relatively small and inexpensive capacitor (C_F) whose RMS current rating is known to be adequate. Choose an LC filter such that:

$$\frac{1}{2\pi\sqrt{L_F C_F}} < \frac{f}{5}$$

where f is the switching frequency. This will attenuate the RMS input current by a factor of approximately 5×, greatly alleviating the RMS input requirements of the larger bulk capacitor C_{BULK}. The filter inductor LF should have a saturation current of at least:

$$I_{SAT(LF)} \ge 1.3 \bullet \frac{V_{OUT}\, I_{OUT(MAX)}}{V_{IN(MIN)}}$$

In order to keep the ripple voltage at the filter output to a reasonable level, choose a value of L_F and C_F that also satisfies:

$$\sqrt{\frac{L_F}{C_F}} < 2.9 \bullet \left(\frac{V_{RIPPLE}}{I_{OUT(MAX)}} + \frac{R_{ESR}}{2} \right)$$

where V_{RIPPLE} is the desired ripple voltage at the output of the input filter and R_{ESR} is the ESR of capacitor C_F. A reasonable target for V_{RIPPLE} is 3% of nominal V_{IN}.

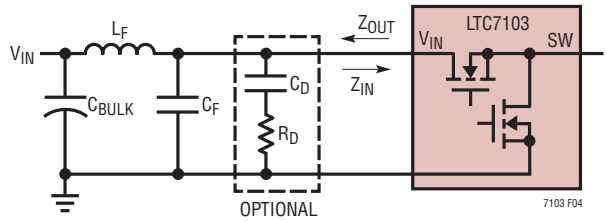

Figure 4. Input Filter with Optional Damping Network

When using an LC input filter, the output impedance of the LC filter (Z_{OUT}) must never be greater in magnitude than the input impedance looking into the power stage of the DC/DC converter (Z_{IN}). This is necessary to avoid ringing

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and possible voltage loop instability. In many applications, this condition is naturally satisfied because the ESR of the bulk input capacitance C_{BULK} is high enough to lower the Q of the LC input filter. In some situations, a series damping network must be added as shown in Figure 4. In order to provide critical damping, choose C_D and R_D according to:

$$C_D \approx 4 \bullet C_F$$

$$R_D = \sqrt{\frac{L_F}{C_F}}$$

C_{OUT} Selection

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

If internal voltage loop compensation is selected, than a minimum amount of bulk output capacitance is required to ensure stability. Loop stability can be checked by viewing the load transient response. See Internal/External Loop Compensation in the Applications Information section.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now available in small case sizes. Their high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors select the X5R or X7R dielectric formulations. These dielectrics provide the best temperature and voltage characteristics for a given value and size. In addition, be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

$INTV_{CC}$ Regulators

The LTC7103 features two separate internal low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the V_{IN} pin or the $EXTV_{CC}$ pin depending on the $EXTV_{CC}$ pin voltage available. $INTV_{CC}$ powers the internal MOSFET gates and most of the internal circuitry. The V_{IN} LDO and the $EXTV_{CC}$ LDO each regulate $INTV_{CC}$ to 3.5V.

The $INTV_{CC}$ pin must be bypassed to ground with a minimum of 1µF ceramic capacitor, placed as close as possible to the $INTV_{CC}$ pin. In order to minimize noise and ripple on the $INTV_{CC}$ supply, always use a capacitor C_{VCC} on $INTV_{CC}$ that is at least 10x greater than the capacitor C_{BST} from BOOST to SW:

$$C_{VCC} > 10 \bullet C_{BST}$$

Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

For high V_{IN} applications it is advantageous to tie $EXTV_{CC}$ to V_{OUT} (bootstrapping), as this will improve efficiency and reduce power dissipation in the V_{IN} LDO. This can be done with any V_{OUT} voltage between 3.3V and 40V. Alternatively, the $EXTV_{CC}$ pin can be tied to any DC voltage between 3.3V and 40V that is capable of delivering the required $INTV_{CC}$ bias current, which varies with switching frequency and operating mode. At full-load operation, which is the worst case, the $INTV_{CC}$ bias current is given approximately by:

$$I_{INTVCC} = 4mA + 1nC\left(8 + \frac{V_{IN}}{20}\right) \bullet f$$

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When $EXTV_{CC}$ is not present, the LDO timeout feature limits the junction temperature rise due to the V_{IN} LDO power dissipation. See Soft-Start and LDO Regulator Timeout section for more information.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the V_{IN} LDO resulting in an efficiency penalty at high input voltages.
2. $EXTV_{CC}$ connected directly to the output voltage V_{OUT}. This is the normal connection for a 3.3V to 40V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 3.3V to 40V range, it may be used to power $EXTV_{CC}$ providing it can supply the required $INTV_{CC}$ current. Operating with $EXTV_{CC} > V_{IN}$ is allowed.
4. $EXTV_{CC}$ connected to an output-derived boost or charge-pump network. For 2.5V and other low voltage buck regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 3.05V.

Most applications will simply tie $EXTV_{CC}$ to V_{OUT} for high efficiency bootstrapping. In this configuration, with Burst Mode operation selected, the no-load V_{IN} current in regulation can be calculated using:

$$I_{VIN} = 1\mu A + \frac{V_{OUT}}{0.8 \bullet V_{IN}} \bullet \left(\frac{V_{OUT}}{R_D} + \frac{V_{OUT}}{6M\Omega} + 8\mu A \right)$$

where R_D is the total resistance of the feedback resistive divider from V_{OUT} to GND. In fixed output voltage mode, where V_{OUT} is programmed using V_{PRG1} and V_{PRG2}, use $R_D = V_{OUT}/1.25\mu A$. For adjustable V_{OUT} mode (Figure 5), use R_D = R1 +R2.

Topside MOSFET Driver Supply (C_{BST})

The boost capacitor, C_{BST}, on the Functional Diagram is used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the boost capacitor is charged through an internal MOSFET switch to a voltage equal to approximately $INTV_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately V_{IN} + 3.5V. For most applications a 0.1µF, X7R ceramic capacitor will provide adequate performance.

The LTC7103 also contains an internal charge pump that supplies a small amount of current to the BOOST pin to allow for continuous operation at 100% duty cycle. This charge pump is adequate to support internal biasing needs and to keep the top MOSFET fully enhanced. Note that the total external leakage on the BOOST pin (including the C_{BST} capacitor leakage) must be less than 4µA to ensure continuous operation at 100% duty cycle.

Output Voltage Programming

The V_{PRG1} and V_{PRG2} pins provide a great deal of flexibility in programming the output voltage of the power supply. Floating both pins selects adjustable V_{OUT} mode. In this mode, the output is programmed using external resistors on the V_{FB} pin as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT} = 1V\left(1 + \frac{R1}{R2}\right)$$

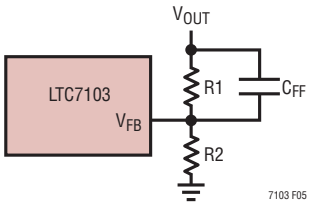

Figure 5. Setting the Output Voltage

Place resistors R1 and R2 very close to the V_{FB} pin to minimize PCB trace length and noise. Great care should be taken to route the V_{FB} trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) may be used.

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If either V_{PRG1} or V_{PRG2} is tied to SGND or $INTV_{CC}$, then fixed output voltage mode is selected. In this mode, precision internal resistor dividers are used to program the output voltage to one of eight fixed voltage levels as shown in Table 4.

Table 4. Output Voltage Programming

V_{PRG1}	V_{PRG2}	V_{OUT}
$INTV_{CC}$	$INTV_{CC}$	1.2V
OPEN	$INTV_{CC}$	1.8V
SGND	SGND	2.5V
SGND	OPEN	3.3V
SGND	$INTV_{CC}$	3.6V
OPEN	SGND	5V
$INTV_{CC}$	OPEN	12V
$INTV_{CC}$	SGND	15V
OPEN	OPEN	Adjustable 1V to V_{IN}

To avoid excessively large values of R1 in high output voltage applications ($V_{OUT} \geq 15V$), a combination of external and internal resistors can be used to set the output voltage. Figure 6 shows the LTC7103 with the V_{FB} pin configured for a 15V fixed output with an external divider to generate a higher output voltage. The internal 12M resistance appears in parallel with R2, and the value of R2 must be adjusted accordingly. R2 should be chosen to be less than 400k to keep the output voltage variation less than 1% due to the tolerance of the LTC7103's internal resistor.

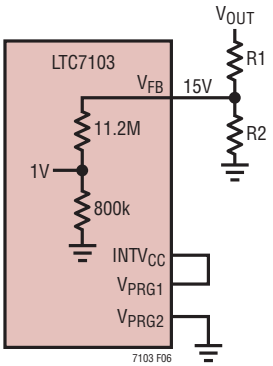

Figure 6. Setting the Output Voltage with External and Internal Resistors

RUN Pin and Overvoltage/Undervoltage Lockout

The LTC7103 has a low power shutdown mode controlled by the RUN pin. Pulling the RUN pin below 0.7V puts the LTC7103 into a low quiescent current shutdown mode (I_Q = 0.7µA). When the RUN pin is greater than $V_{RUN(ON)}$ = 1.21V, switching is enabled. Figure 7 shows examples of configurations for driving the RUN pin from logic. Note that the RUN pin can only be directly controlled as shown in Figure 7 for applications with $V_{OUT} \leq 6V$. See Operating at $V_{OUT} > 6V$ section for more information.

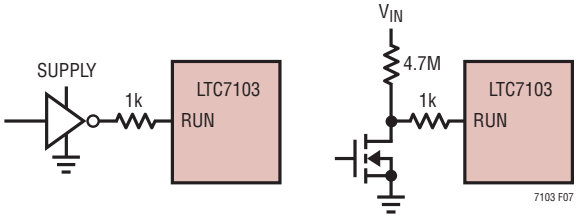

Figure 7. RUN Pin Interface to Logic

The RUN and OVLO pins can alternatively be configured as precise undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistor divider from V_{IN} to ground. A simple resistor divider can be used as shown in Figure 8 to meet specific V_{IN} voltage requirements. For applications with $V_{OUT} > 6V$ that require direct RUN pin control, an open-drain pull-down must be used as shown in Figure 8. See Operating at $V_{OUT} > 6V$ section for more information.

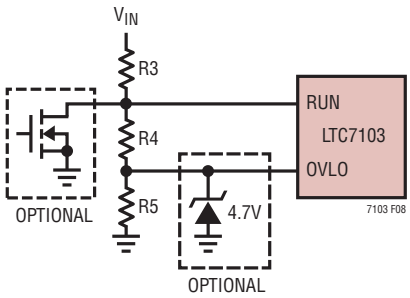

Figure 8. Adjustable UV and OV Lockout

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The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC7103, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R4 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}. The individual values of R3, R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.21V}{\text{RISING } V_{IN} \text{ OVLO THRESHOLD}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.21V}{\text{RISING } V_{IN} \text{ UVLO THRESHOLD}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not need a precise external OVLO, the OVLO pin should be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with R5 = 0Ω.

Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal V_{IN} UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω. Be aware that the OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relation should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R3+R4+R5} \right) < 6V$$

If this equation cannot be satisfied in the application, connect a 4.7V Zener diode between the OVLO pin and ground to clamp the OVLO pin voltage as shown in Figure 8.

Note that in applications with V_{OUT} > 6V, additional constraints on the use of the RUN pin also apply. See Operating at V_{OUT} > 6V section for more information.

Soft-Start and LDO Regulator Timeout

An internal soft-start ramp of 1.2ms will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, a capacitor can be placed from the SS pin to ground. The value of the soft-start capacitor needed to provide a desired soft-start time (t_{SS}) can be calculated by:

$$C_{SS} = t_{SS} \bullet 11\mu A$$

Note that the value of C_{SS} must be greater than 12nF to provide a soft-start time that is greater than the internal default of $t_{SS(INT)}$ = 1.2ms.

The LTC7103 also includes an LDO regulator timeout feature that is essential for limiting die temperature rise due to power dissipation in the V_{IN} LDO. This is useful in high V_{IN} applications, where $EXTV_{CC}$ is tied to V_{OUT}, and V_{OUT} gets shorted to ground. When this occurs, the V_{IN} LDO will take over the $INTV_{CC}$ current, resulting in potentially high power dissipation (>1W) in the V_{IN} LDO pass device. If this condition persists, an LDO timeout occurs, disabling the switching of the top and bottom MOSFETs. Once switching is disabled, the $INTV_{CC}$ bias current is reduced to approximately 4mA, thereby lowering the power dissipation in the LDO. After a long restart delay, a soft-start is again initiated.

The LDO regulator timeout and restart time are dependent on the length of the soft-start time selected, t_{SS}, which is either the default of 1.2ms or set externally. After the soft-start is complete, a timeout will occur if $EXTV_{CC}$ < 3V for a time given by:

$$t_{TIMEOUT} = 1.4 \bullet t_{SS}$$

At this point, switching will stop, and a restart delay timer will be activated. A restart will occur after a delay given by:

$$t_{RESTART} = 46 \bullet t_{SS}$$

As long as this condition persists ($EXTV_{CC}$ < 3V), the LTC7103 will continue operating in a hiccup restart mode. This yields an effective duty cycle of power dissipation in the V_{IN} LDO of approximately 2%, which prevents any significant rise in die temperature. Note, however, that the LDO regulator timeout feature precludes operation

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in constant output current mode in applications where $EXTV_{CC}$ is tied to V_{OUT}, and $V_{OUT} < 3V$.

If the LDO regulator timeout feature is not needed, the SS pin can be tied to $INTV_{CC}$ through a 75k resistor. This will prevent the LDO timeout from occurring, allowing continuous operation even with $EXTV_{CC} = 0V$. The addition of this resistor also affects the soft-start time when an external capacitor is used (the internal 1.2ms soft-start is not affected). With SS tied to $INTV_{CC}$ through 75k, the value of the soft-start capacitor needed to provide a desired soft-start time (t_{SS}) can be calculated by:

$$C_{SS(75k)} = t_{SS} \bullet 51\mu A$$

If the LDO regulator timeout feature is defeated, care must be taken to avoid exceeding the maximum junction temperature. See Thermal Considerations for more information.

Phase-Locked Loop and Frequency Synchronization

The LTC7103 contains a phase-locked loop (PLL) to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. Once synchronized, the turn-on of the top MOSFET is aligned to the rising edge of the synchronizing signal.

The typical capture range of the PLL is from 160kHz to 2.3MHz, with a guarantee over all manufacturing variations to be between 200kHz and 2MHz. The typical input clock thresholds on the PLLIN/MODE pin are 1.5V rising and 1.1V falling, and this input is TTL compatible.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the VCO's filter voltage is prebiased to a level that corresponds to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase-lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

After the PLL has locked to an external clock, if the external clock is stopped, the LTC7103 will immediately detect this condition and momentarily prevent the PLL from adjusting the loop, so that the internal oscillator continues operating at the external clock frequency. After approximately 9µs, the LTC7103 will detect a loss of SYNC, and the oscillator frequency will return to the level set by the FREQ pin. This feature enables smooth transitions into and out of synchronization.

The CLKOUT pin supplies a reference clock that is helpful for synchronizing other switching circuits to the LTC7103 switching frequency. The output high level of this signal is equal to $INTV_{CC}$ (3.5V typical), and the rising edge of the CLKOUT signal is 180° out of phase with respect to the top MOSFET turn-on. This makes it easy to synchronize two LTC7103 converters and operate them out of phase to minimize input current, or to use two LTC7103's together for a higher current, 2-Phase converter. See 2-Phase Operation Section.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC7103 is capable of turning on the top MOSFET. It is determined by internal timing delays. Low duty cycle applications may approach this minimum on-time limit and care should be taken to avoid this by operating at a sufficiency low switching frequency. See Setting the Operating Frequency section.

If the duty cycle does fall below what can be accommodated by the minimum on-time, the LTC7103 will begin to skip cycles, regardless of the mode of operation (burst pulse-skipping modes). The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC7103 is approximately 40ns. If the duty cycle drops below the minimum on-time limit in this situation, cycle skipping can occur with correspondingly larger current and voltage ripple.

Operating at $V_{OUT} > 6V$

The LTC7103 contains circuitry to automatically charge the boost supply for the topside MOSFET driver by activating the bottom MOSFET for short periods of time when necessary. This feature ensures the boost supply is always charged and ready under all operating conditions. When starting up or operating near dropout ($V_{IN} \approx V_{OUT}$) and with $V_{OUT} > 6V$, however, care must be taken to avoid the accumulation of negative inductor current that can arise from the automatic boost charging circuitry.

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There are two optional configurations allowable for applications with V_{OUT} > 6V.

Option 1: 100% Duty Cycle Allowed ($V_{OUT} \leq 43V$). Use this option when operation at or near 100% duty cycle is required or if RUN pin control is not needed. The maximum allowed output voltage for this configuration is 43V. For this option, the RUN pin must be tied to the V_{IN} pin directly, and operation at higher switching frequencies is prohibited. The switching frequency set point must be limited to a maximum value of:

$$f \leq 400kHz$$

and the induction value must be a minimum of:

$$L \geq 4\mu H \bullet (V_{OUT} - 3) - 10\mu H$$

Option 2: High Switching Frequency Allowed. Use this option when either high switching frequency or RUN pin control is needed. In this case, operation near drop-out is prohibited, and a RUN pin divider is required to set the minimum operating input voltage to a value of:

$$V_{IN,MIN} \geq \frac{V_{OUT}}{1 - f \bullet 260ns}$$

As shown in Figure 9, this constraint on minimum operating input voltage establishes a maximum allowable duty cycle that varies with switching frequency. Note that the minimum operating input voltage can be set to any voltage higher than the value for $V_{IN,MIN}$ given above.

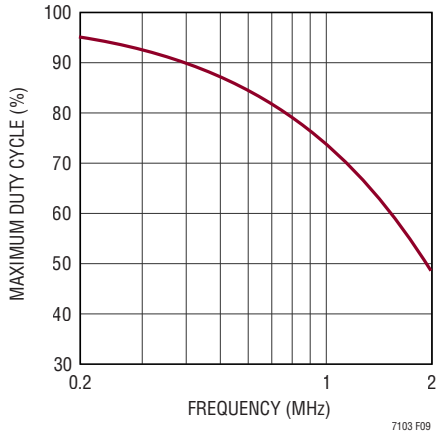

Figure 9. Maximum Allowable Duty Cycle vs Frequency for V_{OUT} > 6V and Option 2 Configuration

When selecting the resistors for the RUN pin divider to limit the minimum operating V_{IN} voltage, use the RUN pin falling threshold minimum value of 1.06V. This ensures that the LTC7103 will not operate below the minimum operating input voltage requirement given in Option 2 above. Referring to Figure 8, calculate the RUN pin divider resistors as:

$$R4 = R_{TOTAL} \bullet \frac{1.06V}{V_{IN,MIN}} - R5$$

$$R3 = R_{TOTAL} - R4 - R5$$

The rising V_{IN} voltage at which the LTC7103 will begin switching is determined by the rising RUN pin threshold of 1.21V (1.26V maximum). The typical rising V_{IN} turn-on voltage is therefore:

$$V_{IN(ON,TYP)} = 1.14 \bullet V_{IN,MIN}$$

Note that for direct RUN pin control in all applications with V_{OUT} > 6V, an open-drain pull-down must be used in conjunction with a RUN pin divider as shown in Figure 8.

Since Option 2 allows for higher switching frequency and smaller size inductors, this option is generally preferred for applications with $V_{OUT} \geq 16V$ or where space is limited, provided that high duty cycle operation is not required. Option 1 is generally a better choice for applications with 6V < V_{OUT} < 16V or whenever high duty cycle operation is required, provided that RUN pin control is not needed.

Internal/External Loop Compensation

The LTC7103 provides the option to use a fixed internal loop compensation network to reduce both the required external component count and design time. The internal loop compensation network can be selected by connecting the I_{TH} pin to the $INTV_{CC}$ pin. Internal compensation can be used at any switching frequency from 200kHz to 2MHz. The LTC7103 automatically adjusts the internal compensation based on switching frequency to maintain an optimum transient response. When using internal compensation, a reasonable starting point for the minimum amount of output capacitance necessary for stability

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can be found as the greater of either 4.7µF or C_{OUT} defined by the equation:

$$C_{OUT} \approx \frac{80}{f \bullet V_{OUT}}$$

where C_{OUT} is the capacitance value at voltage V_{OUT}, noting that most ceramic capacitors lose 50% or more of their rated value when used at their rated voltage.

Alternatively, the user may choose specific external loop compensation components to optimize the main control loop transient response as desired. External loop compensation is chosen by simply connecting the desired network to the I_{TH} pin.

Typical compensation component values are shown in Figure 10. For a 500kHz application, for example, an R-C (R_{COMP} and C_{COMP} in Figure 10) network of 2.2nF and 10kΩ provides a good starting point. The bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. A 10pF bypass capacitor (C_{BYP} in Figure 10) on the I_{TH} pin can be used to filter out high frequency coupling from stray board capacitance. In addition, a feedforward capacitor, C_{FF}, can be added to improve the high frequency response, as previously shown in Figure 5. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R1 which improves the phase margin.

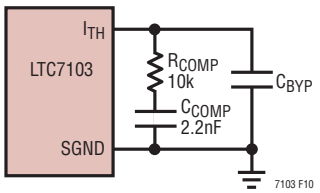

Figure 10. Compensation Components

Checking the Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the I_{TH} pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling behavior at this test point reflect the system's closed loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated by observing the percentage of overshoot seen at this pin with a high impedance, low capacitance probe.

The I_{TH} external components shown in Figure 10 will provide an adequate starting point for most applications. The series R-C filter sets the pole-zero loop compensation. The values can be modified to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The specific output capacitors must be selected because their various types and values determine the loop feedback factor, gain, and phase. An output current pulse of 20% to 100% of full load current, with a rise time of 1µs to 10µs, will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop. As a result, the standard second order overshoot/DC ratio cannot be used to estimate phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Analog Devices Application Note 76.

In some applications, severe transients can be caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this output droop if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limit, short-circuit protection and soft-start functions.

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Average Output Current Limit and Monitor

The LTC7103 contains a fast and accurate average current limit that can be externally controlled and monitored. This fast current loop is useful in applications such as the charging of batteries and capacitors or current programming in LEDs and laser diodes. The average output current limit is set using the I_{CTRL} pin. The voltage on the I_{CTRL} pin sets the average output current limit according to:

$$I_{LIM(AVG)} = \frac{V_{ICTRL} - 0.4}{0.36}$$

This allows for the average current limit to be set anywhere between 0A and 2.5A by adjusting the I_{CTRL} voltage from 0.4V to 1.3V. If the I_{CTRL} voltage is less than 0.4V, it will be internally limited to 0.4V, so that the average output current cannot be set to a negative value. Likewise, the I_{CTRL} voltage is internally limited to 1.3V if the I_{CTRL} pin is floated or tied to a voltage greater than 1.3V.

An internal 20µA pull-up on this pin allows a single resistor to SGND to be used to set the voltage. To program a particular fixed average output current limit $I_{LIM(AVG)}$, chose a resistor according to:

$$R_{ICTRL} = \frac{0.36 \bullet I_{LIM(AVG)} + 0.4}{20\mu A}$$

Since the LTC7103 uses average current mode control with a high speed inner current loop, there are no stability concerns when operating in constant current mode. In addition, the LTC7103 automatically optimizes the current loop based on switching frequency and operating condition. The unity-gain bandwidth of the average current loop is maintained at approximately 1/3 of the switching frequency. This enables the LTC7103 to respond to changes in the I_{TH} pin voltage on a nearly cycle-by-cycle basis. This is orders of magnitude faster than competing solutions, where a slow, average current loop is placed outside of the voltage regulation loop.

When operating in constant current mode with a low voltage on I_{CTRL}, the inductor current will become discontinuous. In this situation, the LTC7103 average current loop maintains good output current programming accuracy down to no load.

The average output current can be monitored at the I_{MON} pin. This pin generates a voltage that represents a filtered version (f_C = 10kHz) of the internally sensed inductor current. The DC voltage on I_{MON} normally varies between 0.4V and 1.3V, corresponding to an average output current between 0A and 2.5A according to:

$$V_{IMON} = 0.36 \bullet I_{OUT(AVG)} + 0.4$$

The I_{MON} voltage may momentarily be less than 0.4V or greater than 1.3V, but eventually is limited to these levels by the average current loop. During SLEEP, this pin is held at 0.4V. Consequently, the IMON voltage will not accurately reflect the average output current at light load in Burst Mode operation. To ensure stability of the internal I_{MON} buffer, place a 2k or higher resistor in series with any capacitive load that is greater than 100pF.

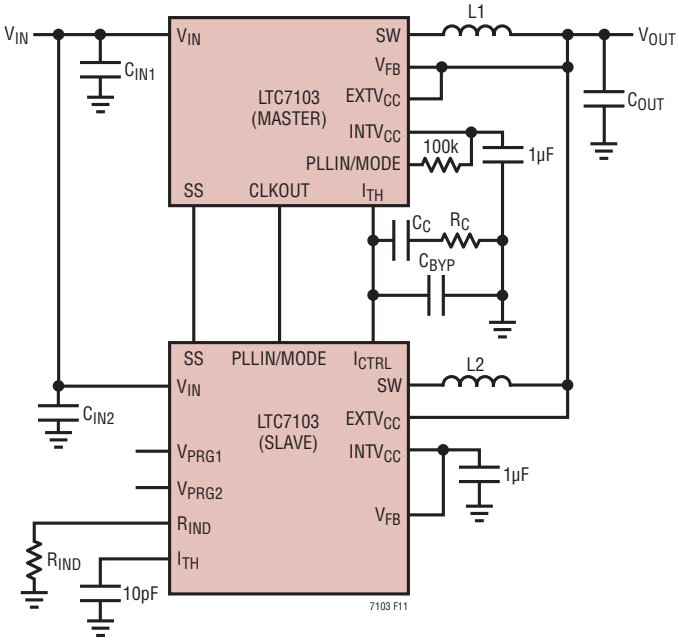

Figure 11. Connections for 2-Phase Operation

2-Phase Operation

The LTC7103 supports parallel operation in order to produce a higher output current. 2-Phase operation is easily implemented as shown in Figure 11. In this figure, the upper LTC7103 operates as the master, and handles voltage regulation. The lower (slave) LTC7103 operates as a current source, the value of which is determined by the demand of the average current loop of the master. The slave is synchronized 180°

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out of phase with respect to the master, dramatically reducing input current ripple. Tying the SS pins together insures that the both parts start up and shut down together. Tying the V_{FB} pin of the slave to $INTV_{CC}$ while floating V_{PRG1} and V_{PRG2} activates slave mode. This disables the 20µA pull-up current on the I_{CTRL} pin and causes the I_{TH} voltage of the slave to track with the I_{CTRL} pin voltage. When operating in slave mode, a resistor on the R_{IND} pin is always required to indicate the inductor value being used. Place a 10pF cap from I_{TH} to GND on the slave to eliminate any high frequency noise.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 +…)

where L1, L2, etc. are the individual loss terms as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources account for the majority of the losses in the LTC7103: 1) I^2R loss, 2) $INTV_{CC}$ regulator current, 3) transition losses and other system losses.

1. I^2R loss is calculated from the DC resistance of the internal switches, R_{SW}, and external inductor, R_L. In continuous current mode, the average output current will flow through inductor L but is chopped between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both the top and bottom MOSFET's $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $R_{SW} = (R_{DS(ON)TOP}) \bullet (DC) + (R_{DS(ON)BOT}) \bullet (1 - DC)$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R loss:

   $I^2R\ Loss = I_{OUT}^2 \bullet (R_{SW} + R_L)$

2. The internal LDO supplies the power to the $INTV_{CC}$ rail. The total power loss here is the sum of the gate drive losses and quiescent current losses from the control circuitry. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous current mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, $(Q_T + Q_B)$ on the LTC7103 is approximately 8nC, although it varies with V_{IN} voltage. To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by voltage:

   $$P_{LDO} = \left[4mA + 1nC\left(8 + \frac{V_{IN}}{20}\right) \bullet f\right] \bullet V_X$$

   where $V_X = V_{IN}$ if the V_{IN} LDO is active or $V_X = EXTV_{CC}$ if the $EXTV_{CC}$ LDO is active. Supplying $INTV_{CC}$ from an output-derived power source through $EXTV_{CC}$ will scale the V_{IN} current required for the gate drive and control circuits by a factor of (duty cycle)/(efficiency). For example, in a 48V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 1.2mA of V_{IN} current. This reduces the mid-current loss from 10% or more to less than 2%.

3. Transition losses apply only to the top MOSFET, and can become significant when operating at high input voltages (typically 40V or greater) and high frequency. Transition losses can be estimated from:

   $Transition\ Loss = (72pF) \bullet V_{IN}^2 \bullet (I_{OUT} + 2.5) \bullet f$

Other hidden losses such as copper trace resistances, and internal battery resistances can account for additional efficiency degradations in the overall power system. Other losses, including diode conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss.

Fault Conditions: Short-Circuit Protection

The architecture of the LTC7103 provides inherent protection against short-circuit conditions, without the need for folding back either the output current or the oscillator frequency. A given switching cycle is skipped only as

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needed to satisfy the high-speed average current loop, resulting in a brick-wall style current limit without any foldback or hiccups in the operation down to V_{OUT} = 0V. Note, however, that hiccup restart will occur due to the LDO timeout feature unless $EXTV_{CC}$ > 3V, or this feature is disabled by tying the SS pin to $INTV_{CC}$ through a 75k resistor.

While the average current loop is extremely fast, a failsafe peak current limit (I_{PK}) comparator has also been incorporated to ensure that the inductor cannot exceed a safe level, even momentarily. In practice, the peak current limit comparator is only needed when there is an abnormal voltage on the average current amplifier output filter and a short-circuit is applied. In this case, the peak current limit comparator may be needed for a few cycles while the average current amplifier filter settles.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating on chip, the overtemperature shutdown circuitry will shut down the LTC7103. When the junction temperature exceeds approximately 171°C, the overtemperature circuitry disables the $INTV_{CC}$ LDO regulator as well as all switching to eliminate internal power dissipation. Once the junction temperature drops back to approximately 155°C, the LTC7103 turns back on and re-initiates a start-up. Long term overstress (T_J > 150°C) should be avoided as it can degrade the performance or shorten the life of the part.

Thermal Considerations

The LTC7103 requires the exposed package backplane metal (PGND) to be well soldered to the PC board to provide both electrical and thermal contact. This gives the QFN package exceptional thermal properties, compared to other packages of similar size. In many applications, the LTC7103 does not generate much heat due to its high efficiency and low thermal resistance package backplane. However, in applications in which the LTC7103 is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 171°C, both power switches will be turned off until temperature decreases by approximately 16°C.

Thermal analysis should always be performed by the user to ensure the LTC7103 does not exceed the maximum junction temperature.

The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated in the I_C and θ_{JA} is the thermal resistance from the junction of the die to the ambient environment. Consider the example in which an LTC7103 is operating with I_{OUT} = 2A, V_{IN} = 50V, f = 500kHz, $V_{OUT} = EXTV_{CC}$ = 5V, and an ambient temperature of 70°C. From the Typical Performance Characteristics section the $R_{DS(ON)}$ of the top switch at this temperature is found to be nominally 335mΩ while that of the bottom switch is nominally 180mΩ yielding an equivalent power MOSFET resistance R_{SW} of:

$$R_{SW} = (335m\Omega)(0.1) + (180m\Omega)(0.9) = 196m\Omega$$

From the previous section, the I^2R losses are $(2^2)(0.196)$ = 780mW. $INTV_{CC}$ power dissipation is:

$$P_{LDO} = \left[4mA + 1nC\left(8 + \frac{50}{20}\right) \bullet 500k\right] \bullet 5 = 46mW$$

The transition losses are approximately:

$$(72pF) \bullet 50^2 \bullet (2 + 2) \bullet 500kHz = 360mW$$

so the total power dissipation is approximately 1.2W. The QFN 5mm × 6mm package junction-to-ambient thermal resistance, θ_{JA}, is approximately 38°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 1.2W \bullet 38°C/W + 70°C = 116°C$$

which is below the maximum junction temperature of 150°C.

Design Example

As a design example, consider the LTC7103 in an application with the following specifications: V_{IN} = 36V to 72V, V_{OUT} = 12V, $I_{OUT(MAX)}$ = 2A, $I_{OUT(MIN)}$ = 20mA, and switching is enabled between 30V and 90V on V_{IN}.

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First, because efficiency is important at both high and low load currents, Burst Mode operation at 500kHz is chosen. The R_{FREQ} resistor for 500kHz switching frequency is calculated using R_{FREQ} = f/40 + 7.5k = 20k. In addition, the PLLIN/MODE pin is tied to ground to select Burst Mode operation.

Next, since the output voltage is available as a preprogrammed value (V_{PRG1} = $INTV_{CC}$ and V_{PRG2} = OPEN), the R_{IND} pin is left floating, and the inductor value chosen according to Table 3 as 28µH. Suitable inductors with a nominal value of 27µH and $I_{SAT} \geq$ 4A are available from multiple manufacturers, so a value of L = 27µH is chosen.

Next, C_{OUT} = 22µF is selected based on the minimum needed for internal voltage loop compensation and output ripple. C_{IN} is sized to handle a ripple current I_{RMS} = $I_{OUT/2}$ = 1A. A low ESR, 100V, 4.7µF ceramic capacitor is chosen. The $INTV_{CC}$ decoupling capacitor is chosen as 1µF and the BOOST capacitor is chosen as 0.1µF. $EXTV_{CC}$ is tied to V_{OUT} to minimize loss in the $INTV_{CC}$ LDO.

The undervoltage and overvoltage lockout requirements on V_{IN} can be satisfied with a resistor divider from V_{IN} to the RUN and OVLO pins (refer to Figure 8). Choose R3+R4+R5 = 2.5MΩ to minimize the loading on V_{IN}. Calculate R3, R4 and R5 as follows:

$$R5 = \frac{1.21V \bullet 2.5M\Omega}{90V} = 33.6k$$

$$R4 = \frac{1.21V \bullet 2.5M\Omega}{30V} - R5 = 67.2k$$

$$R3 = 2.5M\Omega - R5 - R4 = 2.4M\Omega$$

Since specific resistor values in the MΩ range are generally less available, it may be necessary to scale R3, R4, and R5 to a standard value of R3. For this example, choose R3 = 2.2M and scale R4 and R5 by 2.2M/2.4M. Then, R4 = 61.6k and R5 = 30.8k. Choose standard values of R3 = 2.2M, R4 = 62k, and R5 = 30.9k. Note that the falling thresholds for the UVLO and OVLO will be 8% and 5% lower than the rising thresholds, or 27.6V and 85.5V respectively.

Since this application has V_{OUT} > 6V and RUN pin control is desired, Option 2 configuration is selected. The minimum allowed operating input voltage is given by:

$$V_{IN,MIN} \geq 12/(1 - 0.13) = 13.8V$$

This requirement is easily satisfied by the RUN pin divider, which limits operation to input voltages greater than 27.6V.

Internal compensation is selected by tying the I_{TH} pin to $INTV_{CC}$. The I_{CTRL} pin is left floating to select a current limit of 2.5A, and the SS pin is left floating to select the internal soft-start ramp of 1.2ms. Figure 12 shows a complete schematic for this design example.

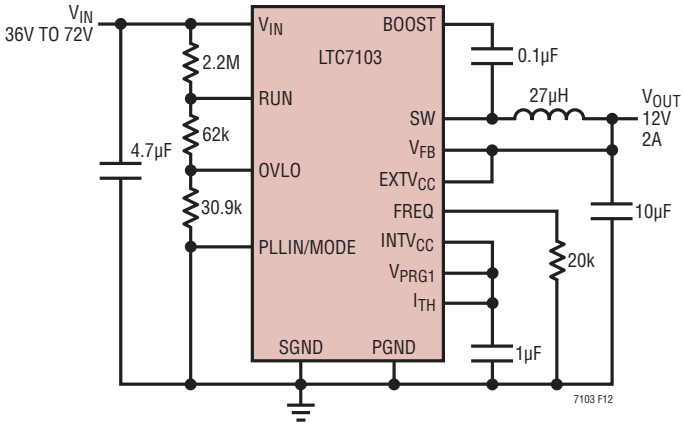


Figure 12. 36V to 72V Input to 12V Output, 2A Regulator

Low EMI PCB Layout

The LTC7103 is designed specifically to minimize EMI/EMC emissions by reducing the parasitic inductance associated with the internal power switches. For optimal performance, the LTC7103 requires two V_{IN} bypass capacitors. As shown in Figure 13, place a smaller 0.1µF capacitor (C_{IN1}, 0805 case) as close as possible to the LTC7103, and a 4.7µF or larger capacitor (C_{IN2}, 1210 case) just beyond C_{IN1}.

For the lowest possible EMI/EMC emissions, an input filter is required. See Figure 17 for an example and the LTC7103 demo board guide for additional details as well as PCB design files.

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC7103 (Refer to Figure 13):

1. Place the input capacitors, inductor and output capacitors on the same side of the circuit board, and make their connections on that layer where possible. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.

APPLICATIONS INFORMATION

2. Connect capacitor C_{IN1} to V_{IN} and PGND as close to the pins as possible. These capacitors provide the AC current to the internal power MOSFETs. The (–) plate of C_{IN1} should be closely connected to PGND and the (–) plate of C_{OUT}.
3. When using adjustable V_{OUT} mode, the resistor divider (R1 and R2) must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. Place these resistors near the IC, keeping the V_{FB} trace short and away from either SW or BOOST.
4. Keep sensitive components (attached to RUN, OVLO, R_{IND}, I_{TH}, V_{FB}, FREQ, I_{MON} and I_{CTRL}) away from the SW and BOOST pins. Make the SW and BOOST nodes as small as possible.
5. Use either one ground plane or segregate the signal and power grounds into two planes connected through a single, low resistance trace to a common reference point, typically at the exposed pad.
6. Flood all unused areas on all layers with copper tied to the exposed pad in order to reduce the temperature rise of the LTC7103.

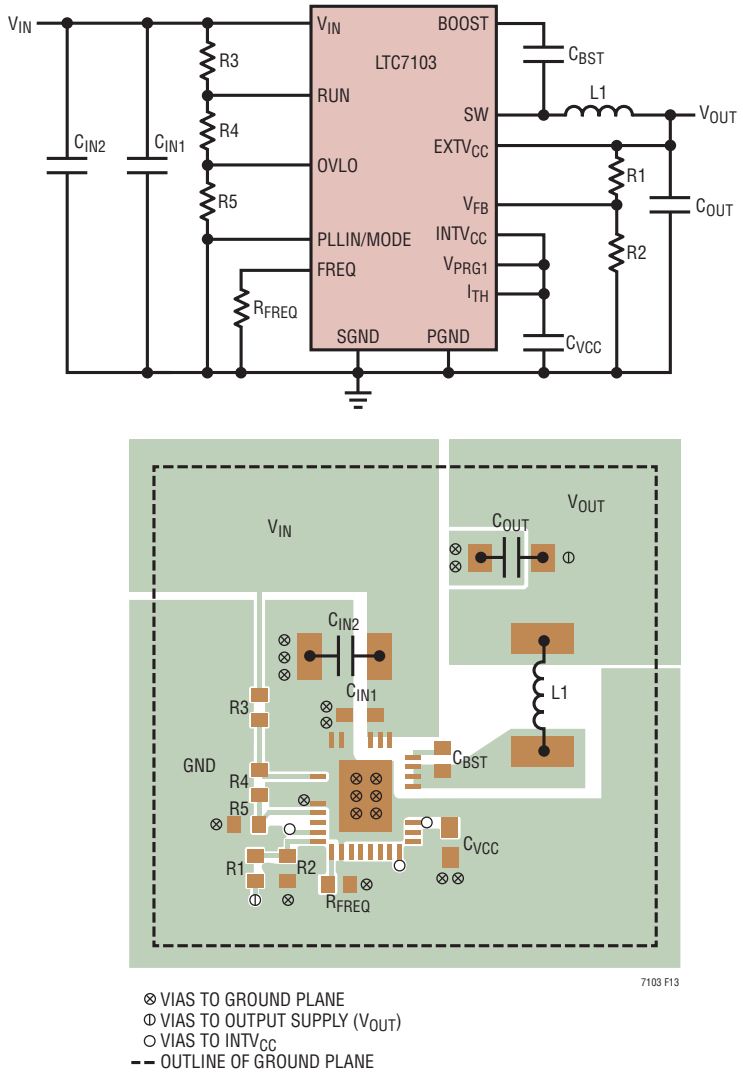


Figure 13. Example PCB Layout

TYPICAL APPLICATIONS

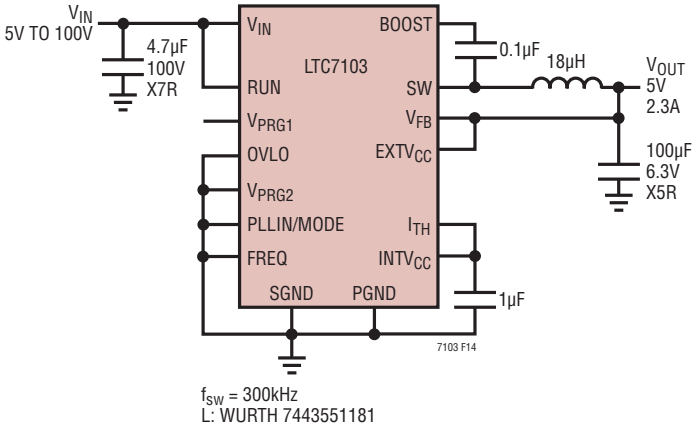


Figure 14. High Efficiency 5V to 100V Input to 5V/2.3A Output Step-Down Regulator

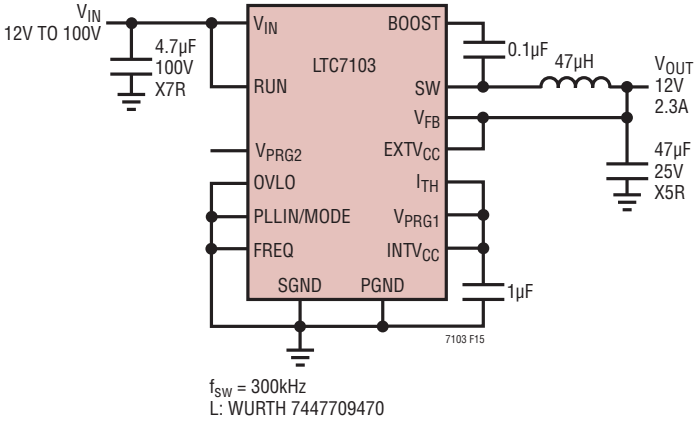


Figure 15. High Efficiency 12V to 100V Input to 12V/2.3A Output Step-Down Regulator

TYPICAL APPLICATIONS

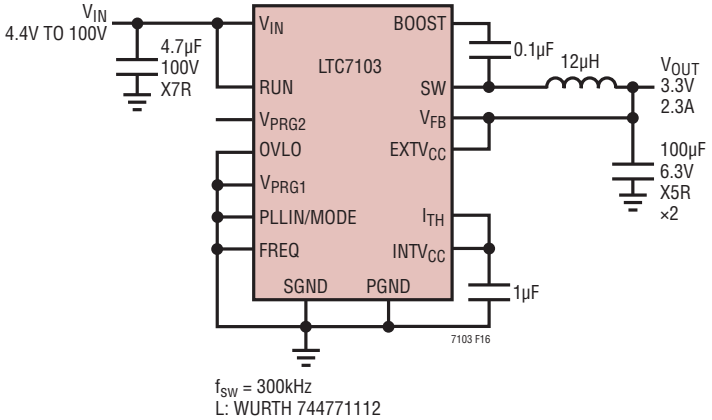


Figure 16. High Efficiency 4.4V to 100V Input to 3.3V/2.3A Output Step-Down Regulator

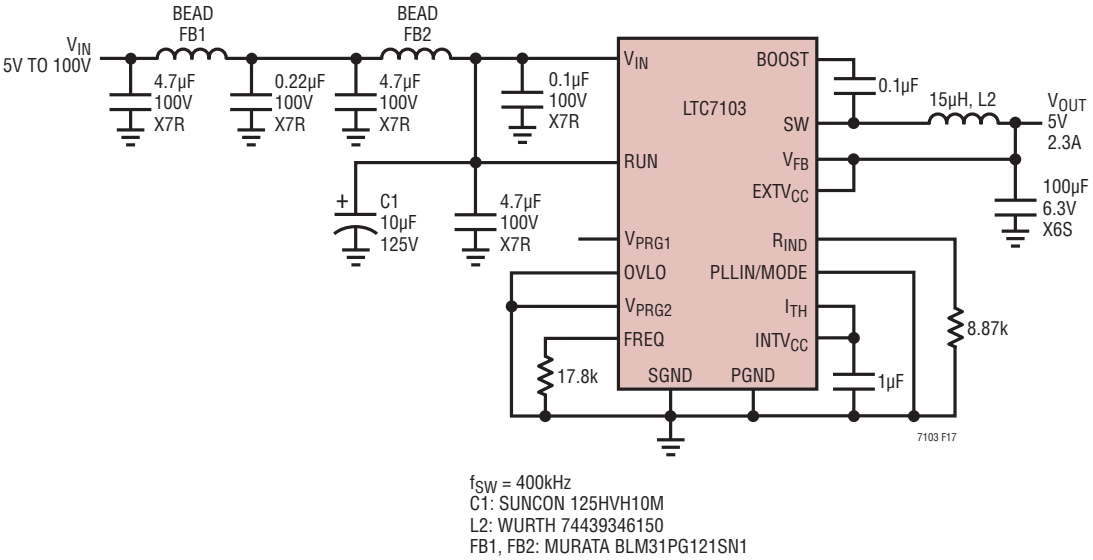
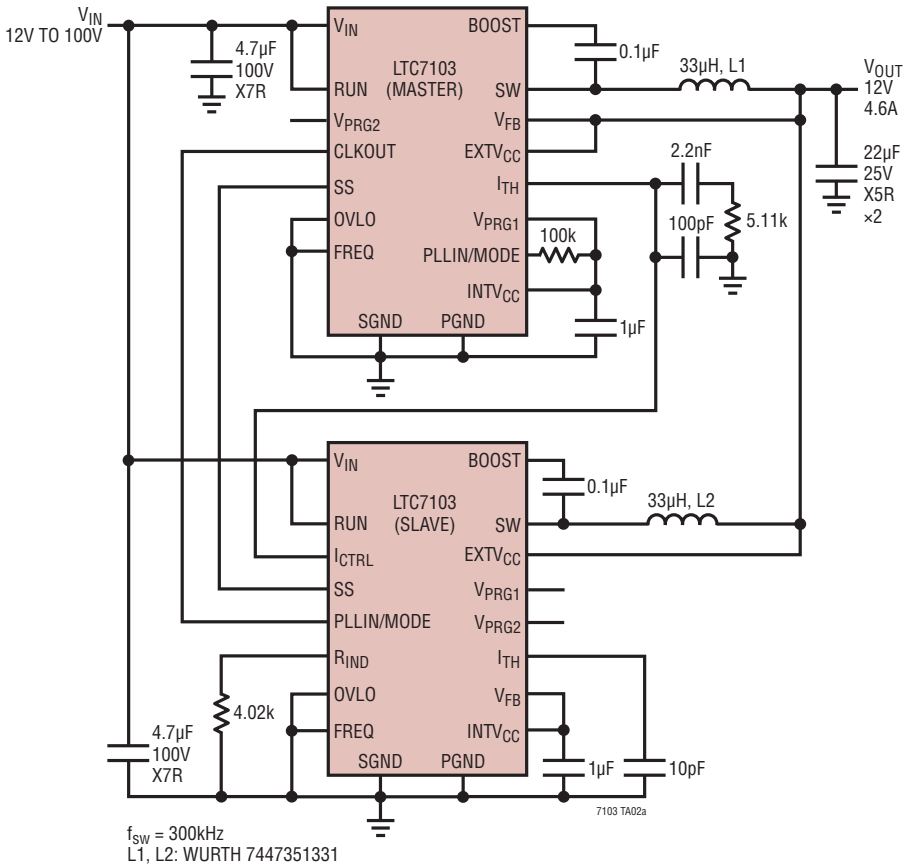


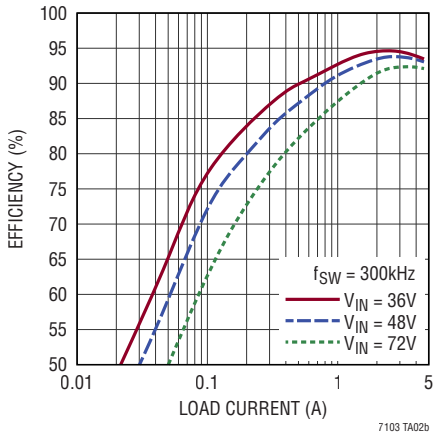
Figure 17. Low EMI 5V to 100V Input to 5V/2.3A Output Step-Down Regulator

TYPICAL APPLICATIONS

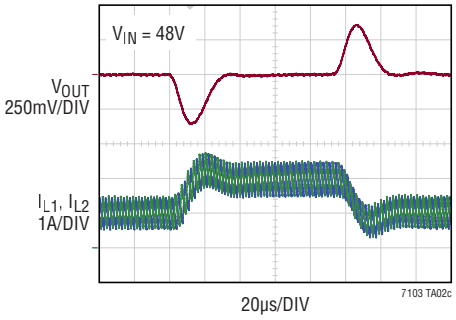
2-Phase, 12V to 100V Input to 12V/4.6A Output Regulator



Efficiency vs Load Current

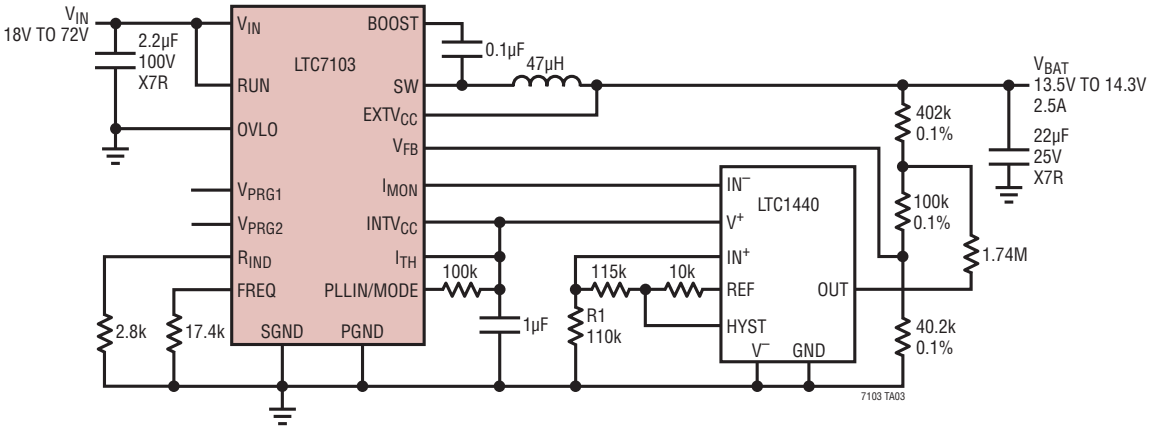


Load Transient



TYPICAL APPLICATIONS

2.5A, 6-Cell SLA Battery Charger with Charge Termination



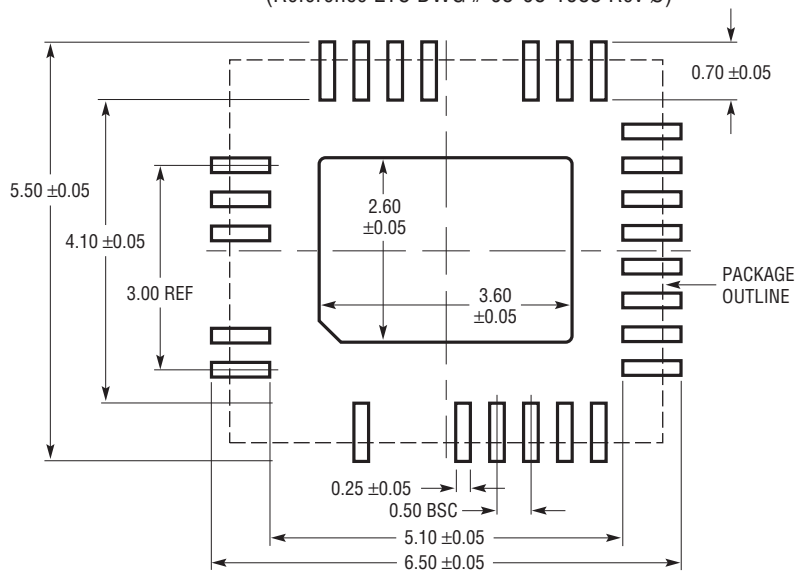
f_{SW} = 400kHz
L: WURTH 7447709470

$$R1 = \frac{125k\,(I_{TERM} + 1.38)}{2.17 - I_{TERM}}$$

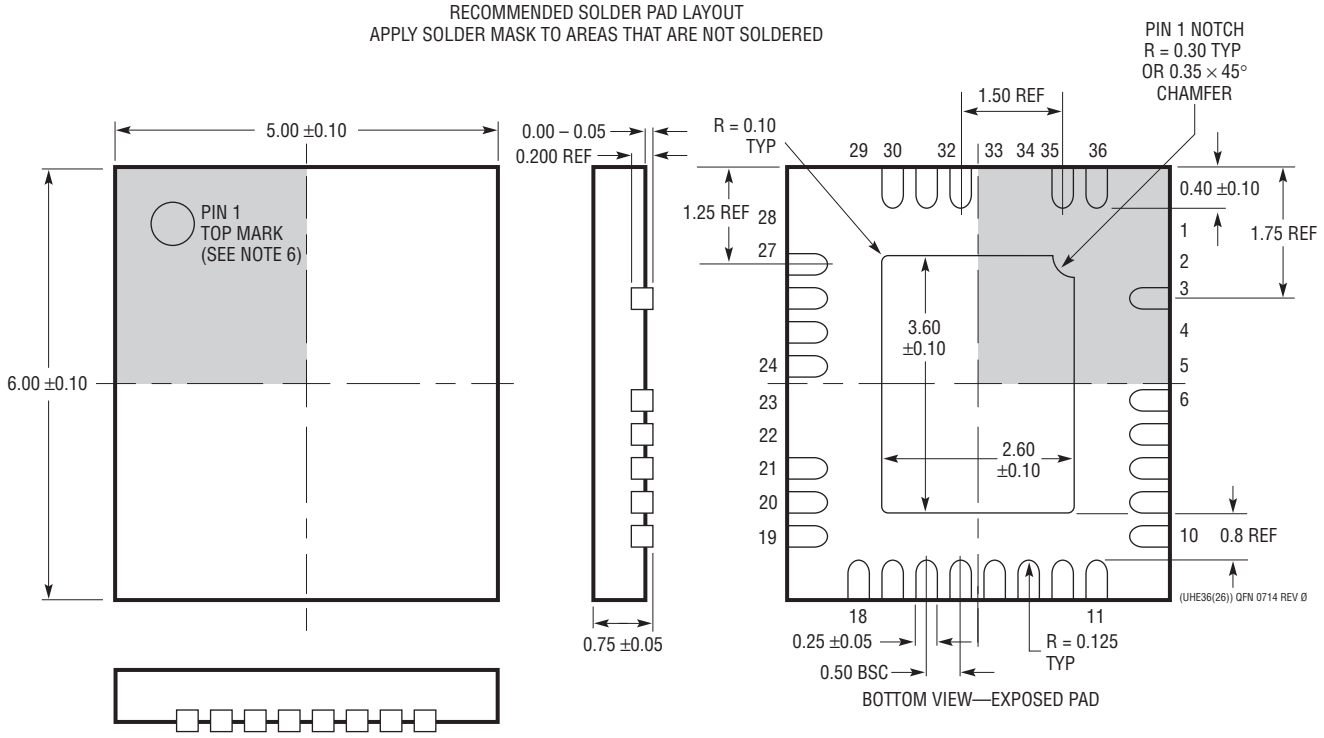
2.5A CHARGING CURRENT
14.3V TOPPING CHARGE VOLTAGE WITH 0.3A TERMINATION
13.4V FLOAT VOLTAGE

PACKAGE DESCRIPTION

UHE Package
Variation: UHE36(26)
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1983 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/18	Added V_{RUN} Falling condition to $V_{RUN(ON)}$	3
		Added Note 9 plus a Note 9 reference to V_{OUT}	3, 4
		Added Operating at V_{OUT} > 6V section	27
B	11/20	Minor changes to the conditions in the Electrical Characteristics table	3
		Corrected R4 Equation	27
		Corrected V_{PRG1} and V_{PRG2} pins on the schematic (Figure 17).	35
C	09/24	Updated Figures 10, 17	28, 35

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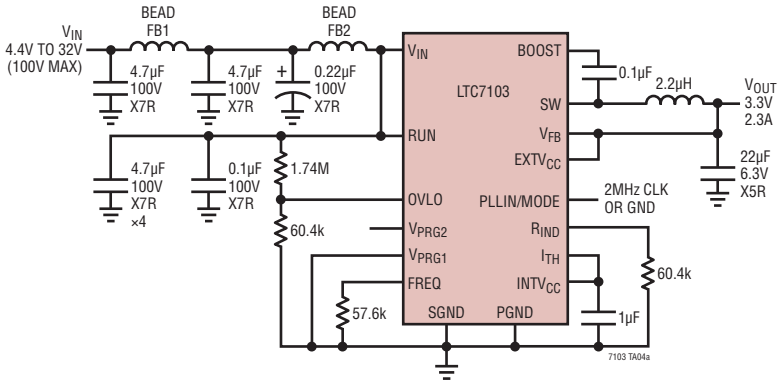
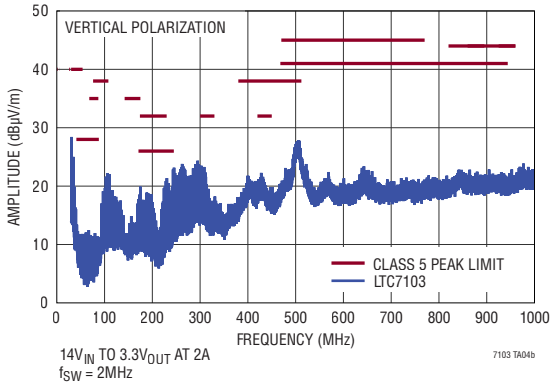
TYPICAL APPLICATION

4.4V to 32V Input to 3.3V/2.3A Output, 2MHz Automotive Supply with Overvoltage Lockout and 100V Input Tolerance



f_{SW} = 2MHz
OVERVOLTAGE LOCKOUT AT 36V
L: COILCRAFT XFL4020-222ME
FB1, FB2: MURATA BLM31PG601SN1
C1: SUNCON 125HVH10M

Radiated EMI Performance (CISPR25) Radiated Emission Test with Class 5 Peak Limits



$14V_{IN}$ TO $3.3V_{OUT}$ AT 2A
f_{SW} = 2MHz

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7801	150V, Low I_Q, Synchronous Step-Down DC/DC Controller	$4V \le V_{IN} \le 140V$, 150V ABS Max, $0.8V \le V_{OUT} \le 60V$, I_Q = 40µA, PLL Fixed Frequency 320kHz to 2.25MHz
LTC7138	High Efficiency, 140V, 400mA Step-Down Regulator	V_{IN}: 4V to 140V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 1.4µA, MSE Package
LTC3637	76V, 1A High Efficiency Step-Down DC/DC Regulator	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 3µA, 3mm × 5mm DFN-16, MSOP-16E Packages
LTC3630A	76V, 500mA Synchronous Step-Down DC/DC Regulator	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 5µA, 3mm × 5mm DFN16, MSOP-16E Packages
LT8631	100V, 1A Synchronous Micropower Step-Down Regulator	V_{IN}: 3V to 100V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7µA, I_{SD} = 5µA, HV TSSOP-20E Package
LT8630	100V, 0.6A Synchronous Micropower Step-Down Regulator	V_{IN}: 3V to 100V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7µA, I_{SD} = 5µA, HV TSSOP-20E Package
LTC7800	60V, Low I_Q, High Frequency Synchronous Step-Down DC/DC Controller	$4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, I_Q = 50µA, PLL Fixed Frequency 320kHz to 2.25MHz
LTC3891	60V Synchronous Step-Down DC/DC Controller with Burst Mode Operation	V_{IN}: 4V to 60V, $V_{OUT(MIN}$ = 0.8V, I_Q = 50µA, I_{SD} < 14µA, 3mm × 4mm QFN-20, TSSOP-20E Packages
LTC3892/ LTC3892-1	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	V_{IN}: 4V to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 29µA, I_{SD} < 14µA, 5mm × 5mm QFN-32, TSSOP-28E Packages
LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz, $4V \le V_{IN} \le 140V$, $0.8V \le V_{OUT} \le 60V$, I_Q = 40µA
LTC4366-1/ LTC4366-2	High Voltage Surge Stopper	V_{IN}: 9V to > 500V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 50µA, I_{SD} < 14µA, 2mm × 3mm DFN-8, TSOT-8 Packages
LTC3649	60V, 4A Synchronous Step-Down Regulator with Rail-to-Rail Programmable Output	V_{IN}: 3.1V to 60V, $V_{OUT(MIN)}$ = 0V, Programmable Output Current with Current Monitor, 4mm × 5mm QFN and TSSOP Packages

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