100MHz Isolated ADC Serial Interface

FEATURES

- **Isolated Interface: 6000V_{RMS} for 1 Minute**
- **CSA (IEC/UL) Approved, File #255632**
- **100MHz SPI-Compatible I/O**
- **Configurable SPI Word Length 8 to 32 Bits**
- **Low Jitter Conversion Start (30ps$_{RMS}$)**
- Supports Simultaneously Sampled ADCs
- Read Only (LTM2893), Read/Write (LTM2893-1)
- Three Isolated Multiplexer Select Signals
- 1.71V to 5.5V I/O Voltages
- 3V to 5.5V Supply Voltages
- High Common Mode Transient Immunity
- 15mm × 6.25mm BGA Package

APPLICATIONS

- Remote Sensing
- High Speed Data Acquisition
- Industrial Process Control
- Test and Measurement Equipment

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DESCRIPTION

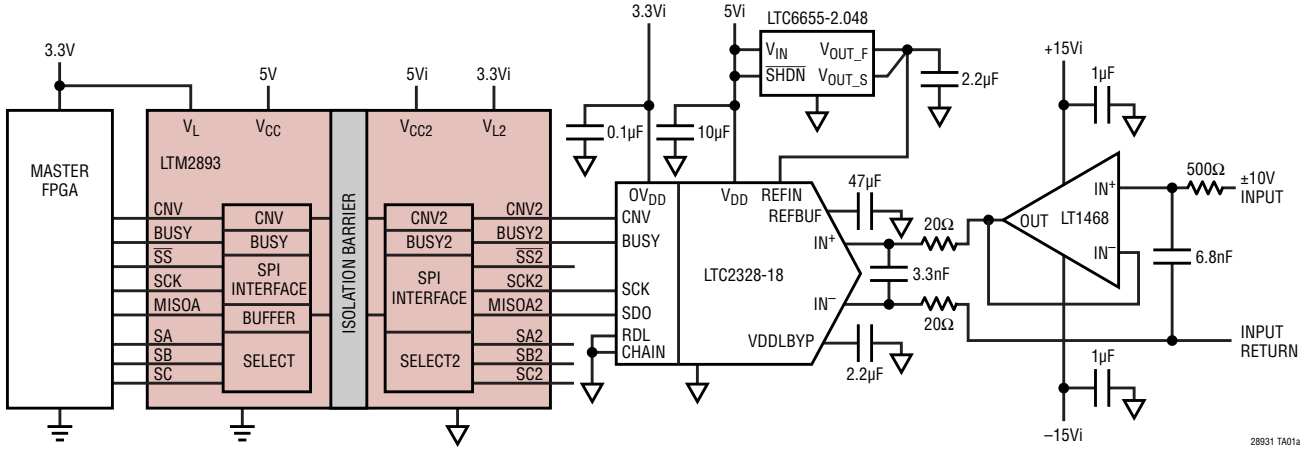
The LTM®2893 is a high speed isolated µModule (micromodule) SPI interface with ADC control signals. The LTM2893 is optimized for isolating 1Msps high resolution 18-bit SAR ADCs, such as the LTC2338 and similar families, and can interface with most general purpose ADCs. The LTM2893-1 is optimized for isolating the LTC2348 and similar families of simultaneous sampling ADCs that require writing configuration settings into the ADC. LTM2893 isolates the conversion start, sampling signal, with very low aperture jitter (30ps) and low latency (20ns).

The interface enables fast throughput with no cycle latency, which makes the LTM2893 ideally suited for a wide variety of applications. The LTM2893 has a high speed SPI-compatible serial port that supports 1.71V to 5.5V logic and is configurable for ADCs with 8 to 32 bit SPI word lengths. It also isolates three select signals (SA, SB, SC) for controlling analog multiplexers or gain settings.

The isolation barrier tolerates large voltage ground variations between the logic interface and the isolated side of the LTM2893. Uninterrupted communication is maintained during voltage transients greater than 50kV/µs.

TYPICAL APPLICATION

LTC2328-18 ADC Isolation A_{IN} = ±10.24V, SNR = 95dB



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

V_L to GND ..... –0.3V to 6V
V_{CC} to GND ..... –0.3V to 6V

Isolated Supply Voltages

V_{L2} to GND2 ..... –0.3V to 6V
V_{CC2} to GND2 ..... –0.3V to 6V

Logic Signals

ON, CNV, BUSY, SA, SB, SC,
$\overline{SS}$, $\overline{CSC}$, MISOA, MISOB,
SCK, MOSI..... GND – 0.3V to V_L + 0.3V
$\overline{FAULT}$..... GND – 0.3V to 6.3V

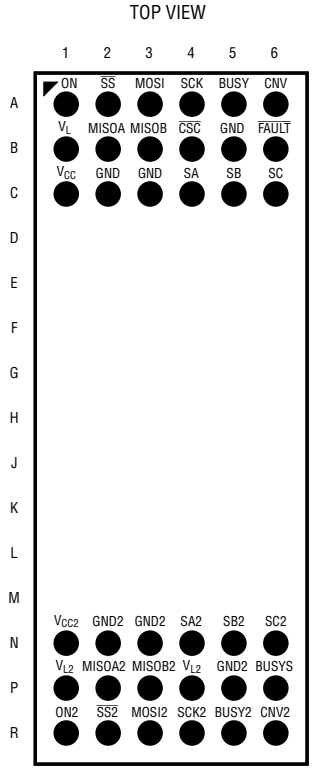
Isolated Signals

MISOA2, MISOB2, ON2, BUSY2,
BUSYS, MOSI2, CNV2, SCK2, $\overline{SS2}$,
SA2, SB2, SC2.....GND2 – 0.3V to V_{L2} + 0.3V

Operating Temperature Range (Note 11)

LTM2893C ..... 0°C to 70°C
LTM2893I ..... –40°C to 85°C
LTM2893H ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Maximum Internal Operating Temperature ..... 125°C
Peak Solder Reflow Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
36-PIN (15mm × 6.25mm × 2.06mm)
T_{JMAX} = 125°C, θ_{JA} = 36°C/W, θ_{JCTOP} = 27.5°C/W, $\theta_{JCBOTTOM}$ = 17.5°C/W
θ_{JB} = 19.1°C/W, WEIGHT = 0.36g

ORDER INFORMATION

PART NUMBER	PACKAGE TYPE	BALL FINISH	PART MARKING		MSL RATING	TEMPERATURE RANGE
			DEVICE	FINISH CODE		
LTM2893CY#PBF	BGA	SAC305 (RoHS)	LTM2893Y	e1	3	0°C to 70°C
LTM2893IY#PBF						–40°C to 85°C
LTM2893HY#PBF						–40°C to 125°C
LTM2893CY-1#PBF	BGA	SAC305 (RoHS)	LTM2893Y-1	e1	3	0°C to 70°C
LTM2893IY-1#PBF						–40°C to 85°C
LTM2893HY-1#PBF						–40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 3.3V, GND2 = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{CC}	Operating Supply Range		●	3.0		5.5	V
I_{CC}	Operating Supply Current	Idle	●		9	12	mA
	Operating Supply Current 1Msps, ADC Conversion Rate	20pF Loads, SCK = 100MHz	●		12	15	mA
V_{CC2}	Isolated Operating Supply Range		●	3.0		5.5	V
I_{CC2}	Isolated Operating Supply Current	Idle	●		9	12	mA
	Isolated Operating Supply Current, 1Msps ADC Conversion Rate	20pF Loads, SCK2 = 100MHz	●		12	15	mA
V_L	Logic Interface Supply Range		●	1.71		5.5	V
I_L	Logic Interface Supply Current	Inputs and Outputs Static at GND or V_L	●			±200	µA
	Logic Interface Supply Current, 1Msps Conversion Rate	SCK = 100MHz, 20pF Load	●		2	5	mA
V_{L2}	Isolated Interface Supply Range		●	1.71		5.5	V
I_{L2}	Isolated Interface Supply Current	Inputs and Outputs Static at GND2 or V_{L2}	●			±200	µA
	Isolated Interface Supply Current, 1Msps ADC Conversion Rate	SCK2 = 100MHz, 20pF Load	●		2.5	5	mA
Digital Inputs and Digital Outputs (Logic Side)							
V_{IH}	High Level Input Voltage	1.71V ≤ V_L ≤ 5.5V	●	0.8 • V_L			V
V_{IL}	Low Level Input Voltage	1.71V ≤ V_L ≤ 5.5V	●			0.2 • V_L	V
	Digital Input Current (MOSI, SCK, CNV)	V_{IN} = 0V to V_L	●			±1	µA
	Digital Input Current ($\overline{SS}$, $\overline{CSC}$, SA, SB, SC, ON)	V_{IN} = 0V to V_L	●			±60	µA
	Digital Input Capacitance	Note 2			5		pF
V_{OH}	High Level Output Voltage	I_{OUT} = –500µA, 1.71V ≤ V_L ≤ 5.5V	●	V_L – 0.2			V
V_{OL}	Low Level Output Voltage	I_{OUT} = 500µA, 1.71V ≤ V_L ≤ 5.5V	●			0.2	V
I_{OZ}	High-Z Output Leakage Current MISOA, MISOB	$\overline{SS}$ = V_L	●			±1	µA
	Output Source Current (Short-Circuit)	V_{OUT} = 0V (Note 2)			–80		mA
	Output Sink Current (Short-Circuit)	V_{OUT} = V_L (Note 2)			80		mA
Digital Inputs and Digital Outputs (Isolated Side)							
V_{IH}	High Level Input Voltage	1.71V ≤ V_{L2} ≤ 5.5V	●	0.8 • V_{L2}			V
V_{IL}	Low Level Input Voltage	1.71V ≤ V_{L2} ≤ 5.5V	●			0.2 • V_{L2}	V
	Digital Input Current (ON2, BUSY2, BUSYS)	V_{IN} = 0V to V_{L2}, ON2 = VL2	●			±60	µA
	Digital Input Current (MISOA2, MISOB2)	V_{IN} = 0V to V_{L2}	●			±10	µA
	Digital Input Capacitance	Note 2			5		pF
V_{OH}	High Level Output Voltage	I_{OUT} = –500µA, 1.71V ≤ V_{L2} ≤ 5.5V	●	V_{L2} – 0.2			V
V_{OL}	Low Level Output Voltage	I_{OUT} = 500µA, 1.71V ≤ V_{L2} ≤ 5.5V	●			0.2	V
	Output Source Current (Short-Circuit)	V_{OUT} = 0V (Note 2)			–80		mA
	Output Sink Current (Short-Circuit)	V_{OUT} = V_{L2} (Note 2)			80		mA
ESD Performance (Note 7)							
	Isolation Barrier Logic Side I/O Pins Isolated Side I/O Pins	From GND, V_L, or V_{CC} to GND2, V_{L2}, or V_{CC2} With Respect to GND, V_L, or V_{CC} With Respect to GND2, V_{L2}, or V_{CC2}			±15 ±4 ±4		kV kV kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 3.3V, GND2 = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Start							
t_{CNVH}	CNV Pulse Width		●	20			ns
t_{BUSYLH}	CNV↑ to BUSY↑ Delay		●			40	ns
t_{DCNV}	CNV↑ to CNV2↑ Delay (Aperture Delay)		●	12	21	33	ns
t_{CNV2H}	CNV2 Pulse Width	(Config. SCK2 Frequency ≥ 40MHz)	●	20		52	ns
		(Config. SCK2 Frequency ≤ 33MHz)	●	35		80	ns
	CNV to CNV2 Rising Edge Jitter RMS	(Note 7)			30		ps
	Minimum Low Time for CNV			100			ns
SPI Timing							
t_{QUIET}	SCK or $\overline{SS}$↑ Space to CNV↑	LTM2893 LTM2893-1, Configuration Register = 0x9F	● 	20 320			ns ns
t_{SCK}	SCK Input Period	SCK2 Frequency 100MHz LTM2893 (Note 3) SCK2 Frequency 100MHz LTM2893-1 (Note 3)	● ●	10 10		 1185	ns ns
t_{SCKH}	SCK Input High Time	(Note 2)	●	4			ns
t_{SCKL}	SCK Input Low Time	(Note 2)	●	4			ns
t_{SCK2}	SCK2 Output Period	SCK2 Frequency 100MHz (Notes 3, 8)	●	9.5	10	10.8	ns
t_{SCK2H}	SCK2 Output High Time	(Note 2)	●	4			ns
t_{SCK2L}	SCK2 Output Low Time	(Note 2)	●	4			ns
$t_{HDMISO2}$	MISOA2, MISOB2 Data Hold Time from SCK2↑	(Note 2)	●	1			ns
t_{DMISO}	MISOA, MISOB Data Valid Delay from SCK↑ SCK2 Frequency = 100MHz or 66MHz or from SCK↓ SCK2 Frequency ≤ 50MHz	C_L = 20pF, V_L = 5.5V (Note 2) C_L = 20pF, V_L = 2.5V (Note 2) C_L = 20pF, V_L = 1.71V (Note 2)	● ● ●		5	7.5 8 9.5	ns ns ns
$t_{SUMISO2}$	MISOA2, MISOB2, Setup Time to SCK2↑	(Note 2)	●	1.8			ns
t_{HMISO}	MISOA, MISOB Data Remains Valid Delay from SCK↑ SCK2 Frequency = 100MHz or 66MHz or from SCK↓ SCK2 Frequency ≤ 50MHz	C_L = 20pF (Note 2)	●	2			ns
$t_{DMISOSSF}$	MISOA, MISOB Data Valid Delay from $\overline{SS}$↓	C_L = 20pF	●			10	ns
	MISOA, MISOB Data Valid Delay from BUSY↓	$\overline{SS}$ = 0V, LTM2893	●			10	ns
t_{SSFSCK}	$\overline{SS}$↓ Delay to SCK↑	SCK2 Frequency 100MHz (Note 8), LTM2893-1	●	20		1185	ns
$t_{BUSYFSCKR}$	BUSY↓ Delay to SCK↑	$\overline{SS}$ = 0V, SCK2 Frequency 100MHz (Notes 9, 10)	●	20			ns
$t_{BUSY2FSS2F}$	BUSY2↓ Delay to $\overline{SS2}$↓		●	15		35	ns
$t_{BUSY2FBUSYF}$	BUSY2↓ to BUSY↓	SCK2 Frequency 100MHz	●			100	ns
$t_{SS2FSCK2}$	$\overline{SS2}$↓ Delay to SCK2↑	SCK2 Frequency 100MHz	●	15		33	ns
t_{DIS}	Bus Relinquish Time After $\overline{SS}$↑		●			35	ns
$t_{SCKSSDIS}$	Last SCK↑ to $\overline{SS}$↑	SCK2 Frequency 100MHz (Note 8) LTM2893-1	●	20		1185	ns
$t_{SCK2SSDIS}$	Last SCK2↑ to $\overline{SS2}$↑	SCK2 Frequency 100MHz	●	8			ns
	$\overline{SS}$↑ to $\overline{SS}$↓ Space	CRCENA Bit = 0		60			ns
		CRCENA Bit = 1		225			ns
t_{SUMOSI}	MOSI Setup to SCK↑	LTM2893-1 or Configuration Port Write (Note 2)	●	1.5			ns
t_{HDMOSI}	MOSI Hold Time to SCK↑	LTM2893-1 or Configuration Port Write (Note 2)	●	1			ns
$t_{SS2FMOSI2}$	$\overline{SS2}$↓ to MOSI2 Valid	LTM2893-1	●			8	ns

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full specified operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 3.3V, GND2 = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{DMOSI2}	MOSI2 Data Valid Delay from SCK2↓	LTM2893-1 C_L = 20pF, V_L = 5.5V (Note 2) C_L = 20pF, V_L = 2.5V (Note 2) C_L = 20pF, V_L = 1.71V (Note 2)	● ● ●		1.5	4.0 4.0 4.5	ns ns ns
t_{HMOSI2}	MOSI2 Data Remains Valid from SCK2↓	LTM2893-1 (Note 2)	●	0.5			ns
	BUSY, MISOA, MISOB Rise/Fall Time	Note 7, C_L = 20pF			500		ps
	CNV2, $\overline{SS2}$, MOSI2, SCK2 Rise/Fall Time	Note 7, C_L = 20pF			500		ps
Configuration Port							
$t_{CSCFSCK}$	$\overline{CSC}$↓ Delay to SCK↑	SCK2 Frequency 100MHz	●	20		1185	ns
$t_{CSCRSCK}$	SCK↑ to $\overline{CSC}$↑	SCK2 Frequency 100MHz	●	20		1185	ns
$t_{CSCSPACE}$	$\overline{CSC}$↑ Delay to $\overline{CSC}$↓	CRCENA = 0 CRCENA = 1		60 320			ns ns
Select Signals (SA, SB, SC, SA2, SB2, and SC2)							
	Propagation Delay	C_L = 20pF, 1.71V ≤ (V_L and V_{L2}) ≤ 5.5V	●	40	80	150	ns
	Rise/Fall Time	C_L = 20pF, 1.71V ≤ (V_L and V_{L2}) ≤ 5.5V	●		10	20	ns

ISOLATION CHARACTERISTICS

T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage (Notes 4, 5, 6)	1 Minute, Derived from 1 Second	6000			V_{RMS}
		1 Second	7200			V_{RMS}
	Common Mode Transient Immunity	(Note 2) V_{CC} = V_L = ON = 5V to GND, V_{CC2} = V_{L2} = ON2 = 5V to GND2, 1000V in 20ns Transient Between GND and GND2	50	100		kV/µs
V_{IORM}	Maximum Working Insulation Voltage	(Note 2)	1000 690			V_{PEAK}, V_{DC} V_{RMS}
	Partial Discharge	V_{PD} = 1830V_{PEAK} (Note 4)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.2		mm
	Input to Output Resistance	(Notes 2, 4)	1	5		TΩ
	Input to Output Capacitance	(Notes 2, 4)		3		pF
	Creepage Distance	(Note 2)		9.2		mm

REGULATORY INFORMATION

CSA (Note 12)

CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1 +A2:
- Basic Insulation at 910V_{RMS}
- Reinforced Insulation at 455V_{RMS}

CSA 62368-1-14 and IEC 62368-1-14:2014, second edition:
- Basic Insulation at 600V_{RMS}
- Reinforced Insulation at 455V_{RMS}

CSA 60601-1:14 and IEC 60601-1, third edition, +A1:
- Two means of patient protection (2 MOPP) at 287.5V_{RMS}

UL 1577-2015:
- Single Protection, 6000V_{RMS} Isolation Voltage

File 255632

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design, not production tested.

Note 3: Guaranteed by other measured parameters and is not directly tested.

Note 4: Device considered a 2-terminal device. Measurement between groups of pins A1 through C6 shorted together and pins N1 through R6 shorted together.

Note 5: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 6: In accordance with UL1577, each device is proof tested for the 6000V_{RMS} rating by applying an RMS voltage multiplied by an acceleration factor of 1.2 for one second.

Note 7: Evaluated by Design, not production tested.

Note 8: See Table 5 for minimum and maximum timing specifications affected by the selection of SCK2 frequencies in the configuration register.

Note 9: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to their corresponding ground unless otherwise specified.

Note 10: See Table 2 for delay requirements between falling edge of BUSY and SCK for large word lengths.

Note 11: Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

Note 12: Ratings are for pollution degree 2, material group 3 and overvoltage category II where applicable. Ratings for other environmental and electrical conditions to be determined from the appropriate safety standard.

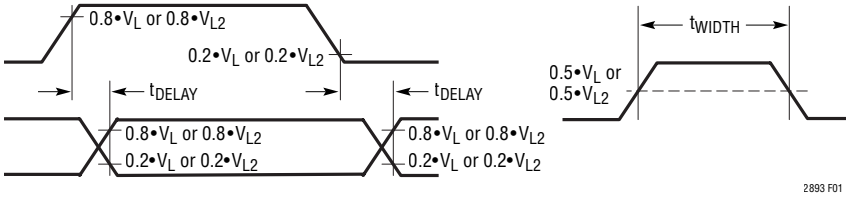
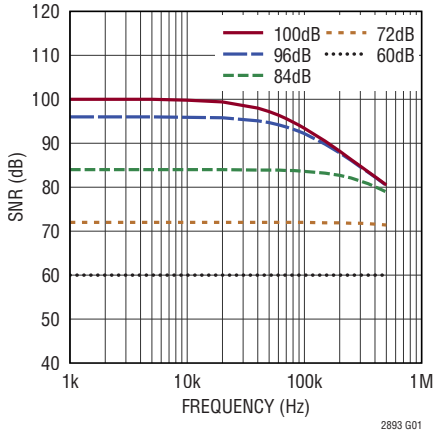


Figure 1. Voltage Levels for Timing Specifications

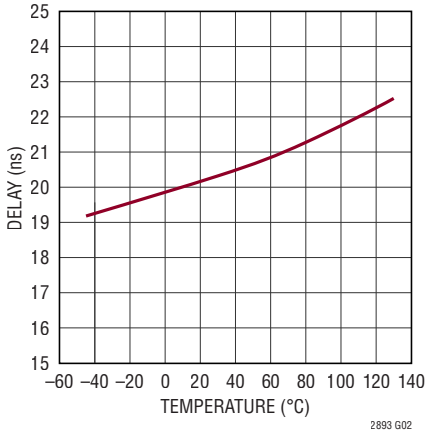
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 5.0V, GND2 = 0V, unless otherwise noted.

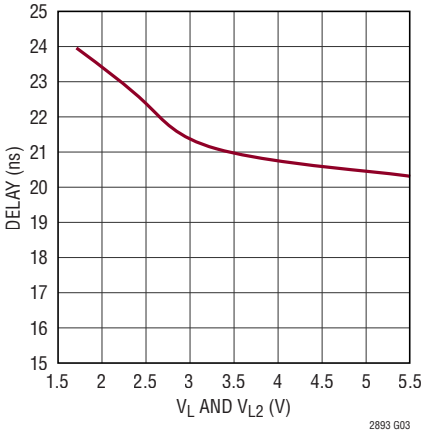
SNR vs f_{IN} for 30ps$_{RMS}$ CNV Jitter



CNV → CNV2 Delay vs Temperature



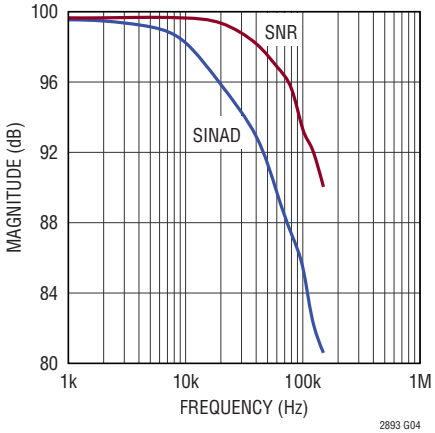
CNV → CNV2 Delay vs V_L and V_{L2}



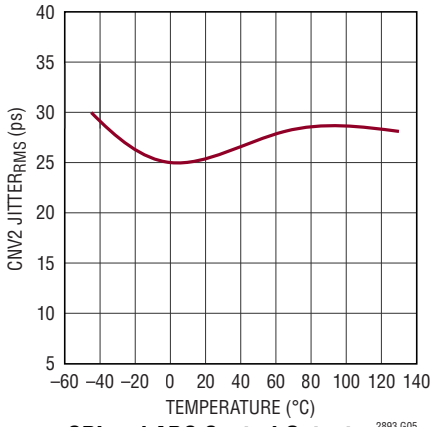
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V, V_{CC2} = 5V, V_{L2} = 5.0V, GND2 = 0V, unless otherwise noted.

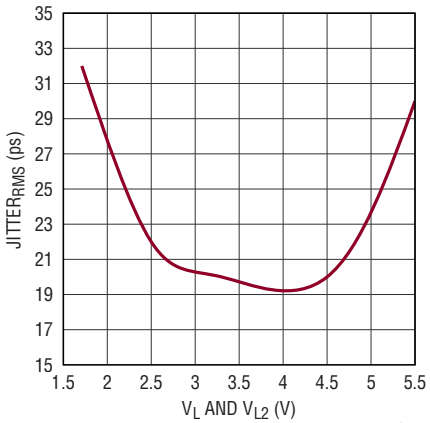
SNR and SINAD Performance with LTC2338-18



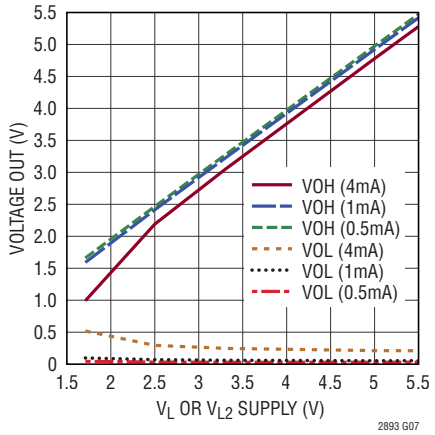
CNV2 Jitter vs Temperature



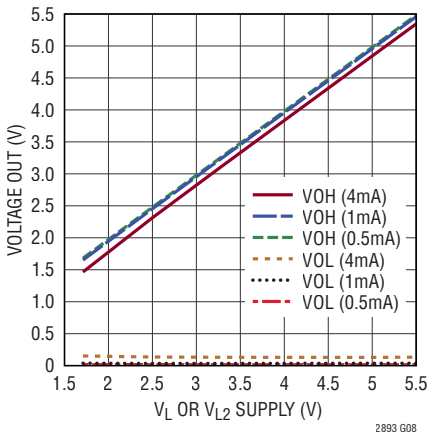
CNV2 Jitter vs V_L and V_{L2}



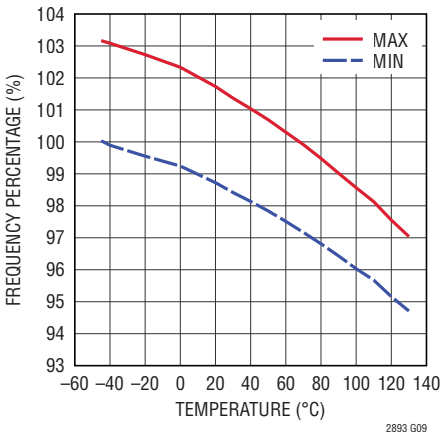
Select Pins (SA, SB, SC, SA2, SB2, SC2) V_{OL} and V_{OH} vs V_L or V_{L2} Voltage



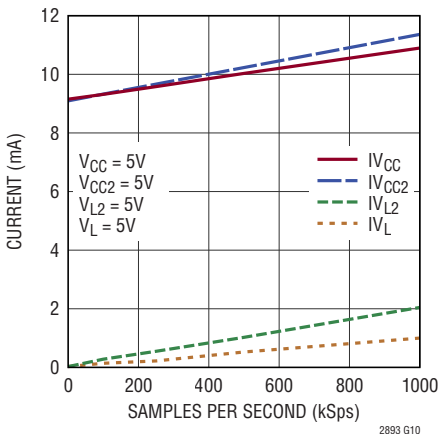
SPI and ADC Control Outputs (MISOA, MISOB, BUSY, CNV2, SCK2, $\overline{SS2}$, MOSI2) V_{OL} and V_{OH} vs V_L or V_{L2} Voltage



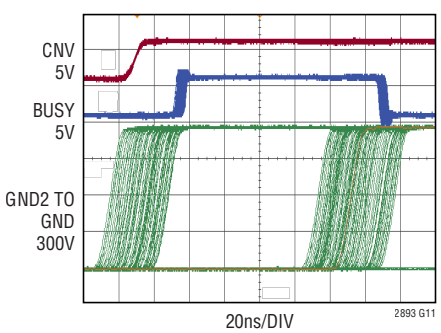
SCK2 Frequency Variation vs Temperature



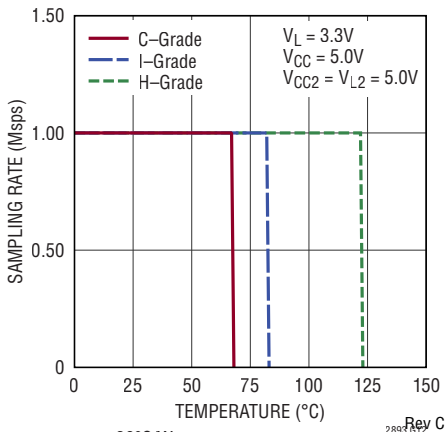
Supply Current vs Sampling Rate 18-Bit, SCK2 Frequency = 100MHz



Communication During 100kV/µs Common Mode Transient Events



Temperature De-Rating for Operating Temperature Range (Communicating with an LTC2378-18)



θ_{JA} = 36°C/W

PIN FUNCTIONS

Logic Side

(All Inputs and Outputs Referenced to V_L and GND)

ON (A1): Enable Input. A high input enables the logic side. When ON is low and V_L is high, MOSI, SCK, CNV, MISOA, and MISOB are high impedance, an external pull-up or pull-down resistor (100k or greater) is required on each pin to minimize possible internal shoot though current if these pins float.

$\overline{SS}$ (A2): Slave Select Input (Low True Slave Chip Select). A low on the $\overline{SS}$ input enables MISOA and MISOB. To clear faults or write the configuration register the $\overline{SS}$ input must be high. With the LTM2893, the $\overline{SS}$ input may remain low between ADC reads. With the LTM2893-1, the $\overline{SS}$ input must frame the SCK transitions and not exceed the defined watchdog timeouts. The $\overline{SS}$ pin contains a weak pull up to the V_L supply. $\overline{CSC}$ must be high for $\overline{SS}$ to be enabled.

MOSI (A3): Master Out Slave In Input. MOSI is the serial data input for the configuration registers or input for serial data to be written to the isolated ADC through MOSI2, (LTM2893-1 option). When MOSI is not used, MOSI should be connected to GND. Connect a weak pull-up to V_L or a weak pull-down to GND to maintain a valid logic input when MOSI is not driven.

SCK (A4): Serial Port Clock Input. MISOA and MISOB data change after a rising edge of the SCK input. MOSI data is read in on the rising edge of the SCK input. Connect a weak pull-up to V_L or a weak pull-down to GND to maintain a valid logic input when SCK is not driven.

BUSY (A5): Busy Output. A high output indicates the ADC is currently converting a result. On the falling edge of the BUSY output the data is ready to be read out of the serial digital interface. At startup, a high on the BUSY output indicates the isolated side is not ready. Once the BUSY output goes low the system is ready.

CNV (A6): Conversion Start Input. The rising edge of CNV is transferred to CNV2 with minimal delay and minimal jitter. Do not change the CNV input during a read of the serial digital interface. The falling edge of CNV is ignored.

V_L (B1): Interface Logic Supply. Recommended operating voltage is 1.71V to 5.5V. Interface supply voltage for pins SA, SB, SC, MISOA, MISOB, MOSI, SCLK, $\overline{SS}$, $\overline{CSC}$, BUSY, and CNV. Internally bypassed to GND with 1µF.

MISOA (B2): Master In Slave Out A Output. Serial data output containing the ADC result from MISOA2. Connect a weak pull-up to V_L or a weak pull-down to GND to maintain a valid logic level when MISOA is high impedance while $\overline{SS}$ is high.

MISOB (B3): Master In Slave Out B Output. Serial data output containing the ADC results from MISOB2. Connect a weak pull-up to V_L or a weak pull-down to GND to maintain a valid logic level when MISOB is high impedance while $\overline{SS}$ is high..

$\overline{CSC}$ (B4): Chip Select Configuration Input ($\overline{CSC}$ Chip Select). A low on the $\overline{CSC}$ input enables access to the configuration register. The Configuration Register section describes configurable options. $\overline{SS}$ must be high for $\overline{CSC}$ to be enabled.

GND (B5): Connect to GND.

$\overline{FAULT}$ (B6): Fault Output Open Drain. A low on the $\overline{FAULT}$ output indicates a communication or command error. Connect to an external 4.7k pull-up to V_L to monitor fault events.

V_{CC} (C1): Supply Voltage. Recommended operating voltage is 3.0V to 5.5V. Internally bypassed to GND with 1µF.

GND (C2-C3): Circuit Ground. Return for V_L logic supply and V_{CC} supply.

SA (C4): Select Enable Input A. Select signal pass through to SA2 to control an external multiplexer or programmable gain amplifier. Transitions must not occur just before the beginning of a CNV or $\overline{SS}$ edge. See the Safe Regions of the Select Enable Signals section for timing constraints. Do not use as a general purpose asynchronous signal. SA contains a weak pull down. Connect to GND when not used.

PIN FUNCTIONS

SB (C5): Select Enable Input B. Select signal pass through to SB2 to control an external multiplexer or programmable gain amplifier. Transitions must not occur just before the beginning of a CNV or $\overline{SS}$ edge. See the Safe Regions of the Select Enable Signals section for timing constraints. Do not use as a general purpose asynchronous signal. SB contains a weak pull down. Connect to GND when not used.

SC (C6): Select Enable Input C. Select signal pass through to SC2 to control an external multiplexer or programmable gain amplifier. Transitions must not occur just before the beginning of a CNV or $\overline{SS}$ edge. See the Safe Regions of the Select Enable Signals section for timing constraints. Do not use as a general purpose asynchronous signal. SC contains a weak pull down. Connect to GND when not used.

Isolated Side

(All Inputs and Outputs Referenced to V_{L2} and GND2)

V_{CC2} (N1): Isolated Voltage Supply. Recommended operating voltage is 3.0V to 5.5V. Internally bypassed to GND2 with 1µF.

GND2 (N2,N3): Isolated Ground Return. Keep separate from GND.

SA2 (N4): Select Output A. Select signal pass through from SA to control an external multiplexer or programmable gain amplifier. See Figure 12 for timing constraints. Do not use as a general purpose asynchronous signal. SA2 contains a weak pull-down. Leave unconnected when not used, or connect to GND2 if unused and configured as an input.

SB2 (N5): Select Output B. Select signal pass through from SB to control an external multiplexer or programmable gain amplifier. See Figure 12 for timing constraints. Do not use as a general purpose asynchronous signal. SB2 contains a weak pull-down. Leave unconnected when not used, or connect to GND2 if unused and configured as an input.

SC2 (N6): Select Output C. Select signal pass through from SC to control an external multiplexer or programmable gain amplifier. See Figure 12 for timing constraints. Do not use as a general purpose asynchronous signal. SC2 contains a weak pull-down. Leave unconnected when not used, or connect to GND2 if unused and configured as an input.

V_{L2} (P1): Interface Supply Voltage. Recommended operating voltage is 1.71V to 5.5V. Interface supply voltage for pins SA2, SB2, SC2, MISOA2, MISOB2, MOSI2, SCLK2, $\overline{SS2}$, BUSYS, BUSY2, and CNV2. Internally bypassed to GND2 with 1µF. Connect to the ADC SPI interface supply.

MISOA2 (P2): Master In Slave Out A Input. Serial data input receiving the results from the ADC. MISOA2 has a weak pull-down when ON2 is high.

MISOB2 (P3): Master In Slave Out B Input. Serial data input receiving the results from the ADC. MISOB2 has a weak pull-down when ON2 is high. Connect to GND2 when not used.

V_{L2} (P4): Connect to V_{L2}.

GND2 (P5): Connect to GND2.

BUSYS (P6): Secondary Busy Input. Connect to secondary ADC BUSY output when two or more ADCs are connected in parallel. Connect to CNV2 to avoid ADC sleep functions. Connect to GND2 when unused.

ON2 (R1): Isolated Enable Input. A high input enables the isolated side communication interface. Do Not Float. When ON2 is low and V_{L2} is high, CNV2, MOSI2, SCK2, MISOA2 and MISOB2 are high impedance, an external pull-up or pull-down resistor (100k or greater) is required on each pin to minimize possible internal shoot though current if these pins float.

$\overline{SS2}$ (R2): Isolated Side Slave Select Output (Slave Chip Select). Output controlled by internal communication functions to fetch data from slave ADC. Connect to external ADC as necessary.

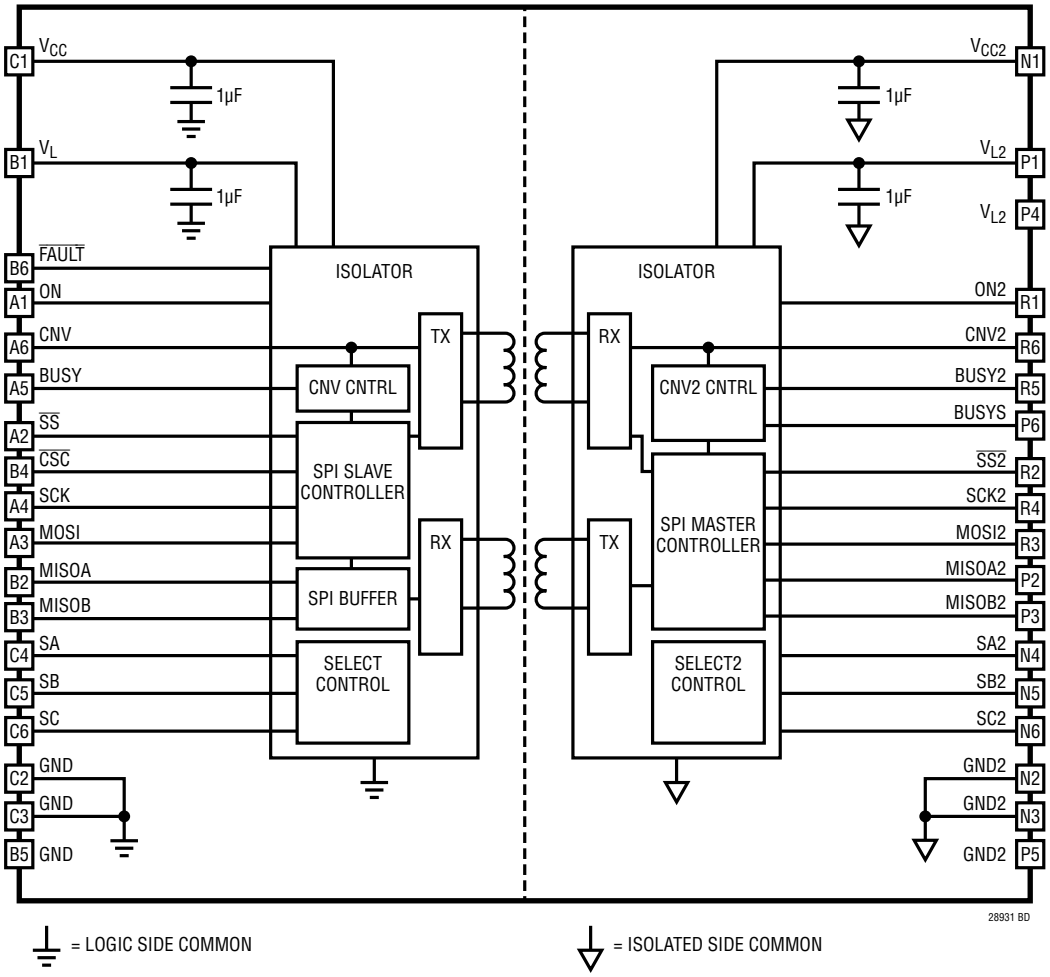
MOSI2 (R3): Isolated Master Out Slave In 2 Output. LTM2893-1 only, serial data output sending command data to the ADC. LTM2893, connect MOSI2 to GND2.

SCK2 (R4): Isolated Serial Clock Output. Serial clock output to the ADC. SCK2 is low when $\overline{SS2}$ is high.

BUSY2 (R5): Isolated Busy Input. Connect to Primary ADC BUSY output. Connect to CNV2 to use fast ADC read mode (ADC sample rate up to 2Msps).

CNV2 (R6): Isolated Conversion Start Output. Connect to ADC conversion start input.

BLOCK DIAGRAM



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OVERVIEW

The LTM2893 contains the functions to communicate with analog to digital converters (ADC) using a fast SPI interface. The LTM2893 utilizes state machines and SPI buffers to manage the ADC-specific operations. An independent configuration chip select ($\overline{CSC}$) allows selection of the SCK frequency, word length, device count, and select signal direction to tailor the operation to a specific ADC. See ADC Requirements for a list of compatibility-tested Analog Devices ADCs.

The LTM2893 follows the signal flow of a standard SAR ADC interface. The process is initiated by the rising edge of the CNV input signal. A high on the BUSY signal follows and the CNV start edge is transferred to the isolated ADC through the CNV2 output. The isolated side waits for the ADC's busy signal, connected to BUSY2, to go high then low. At the falling edge of BUSY2, the isolated side will access the ADC's SPI port and read out the result and transfer it to the logic side, where it is stored in a buffer. When the buffer has data, the logic side BUSY signal will release and the MISOA, MISOB ports are ready to be read. The ADC SPI isolator adds a small delay to the process of an overall ADC cycle. The small delay, approximately 80ns, is observed as a difference in the length of the BUSY and BUSY2 signals.

ISOLATOR µMODULE TECHNOLOGY

The LTM2893 utilizes isolator µModule technology to translate signals across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using differential signaling through coreless transformers formed in the µModule substrate. This system, complete with error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with our SPI transceiver in one small package.

ADC REQUIREMENTS

Ideally Suited ADI ADCs:

LTM2893

- LTC2380/LTC2379/LTC2378/LTC2377/LTC2376
- LTC2338/LTC2337/LTC2336
- LTC2328/LTC2327/LTC2326
- LTC2370/LTC2369/LTC2368/LTC2367/LTC2364
- LTC2383/LTC2382/LTC2381

LTM2893-1

- LTC2348/LTC2345

The following requirements should be met for other ADCs to be compatible with the LTM2893:

- 6.25MHz ≤ SPI shift clock maximum frequency ≤ 100MHz
- Operates in SPI mode (0,0): SCK starts low, data captured on rising edge.
- Meets setup and hold timing requirements ($t_{HDMISO2}$ and $t_{SUMISO2}$) with the SPI shift clock operating between 6.25MHz and 100MHz.
- SPI shift clock (SCK) is static outside of $\overline{CS}$ (the ADC does not require a constant running SCK as a conversion clock)
- If used, the conversion start pulse width minimum is ≤ t_{CNVH}

The following requirements should be met for other ADCs to be compatible with the LTM2893-1 in addition to the LTM2893 requirements:

- The ADC write data is a second transaction. The first transaction reads the ADC result. A second transaction writes the data received into the MOSI pin when the ADC result is read from the LTM2893.

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The SPI bus lacks a formal standard, and therefore, various implementations of protocol, bit lengths, and signal polarities exist. In the universe of analog-to-digital converters (ADCs) with serial peripheral interfaces (SPI), a nominal set of requirements must be met to operate properly with the LTM2893.

First, the LTM2893 operates similar to mode (0, 0). The data is captured and shifted on the rising edge of SCK. All setup and hold timing characteristics are related to the rising edge of the SCK. In a normal mode (0, 0) SPI pattern, the data changes on the falling edge of the SCK. Be aware of the timing delay for the data to be stable before the rising edge SCK capture, if the chosen ADC changes data on the falling edge. At 100MHz and 66MHz, the LTM2893 changes MISOA and MISOB after the rising edge in order to allow for the maximum time for data to change, stabilize, and be ready for the next rising clock edge.

Second, the SCK and $\overline{SS}$ must be dedicated to the operation of reading or writing data. Some ADC interfaces use the SCK as a conversion clock in addition to the shift clock function for the SPI port. Excessive SCK transitions will assert the $\overline{FAULT}$ pin as a SPI buffer under-run. The isolated side will transition SCK2 based on the configured count and will not mimic the extra SCK transitions.

The slave select ($\overline{SS}$) is low true and frames the SPI transaction. With the LTM2893, if a single ADC is implemented, the logic side $\overline{SS}$ can be driven low during normal operation and the isolated side $\overline{SS2}$ can be left open. Otherwise, the $\overline{SS}$ must be returned to a high, and then can be driven low to clear the $\overline{FAULT}$ pin. The LTM2893-1 requires the $\overline{SS}$ to frame the SPI transaction.

The CNV to CNV2 signal is initiated on a rising edge. The falling edge of CNV is ignored. The falling edge of CNV2 is generated internally and has up to 5ns of jitter. The positive pulse width of CNV2 is dependent on the configured SCK2 frequency. SCK2 frequencies of 40MHz or greater have a pulse width of ~40ns, and SCK2 frequencies of 33MHz or below have a pulse width of ~60ns.

ADCs with or without conversion start or busy pins are compatible with the LTM2893.

ADCs that offer conversion start signals and busy signals connect directly to the CNV2 and BUSY2 pins on the LTM2893. The anticipated operation of a conversion start signal is to initiate the conversion operation and for the busy signal to be high during the conversion. The busy signal is anticipated to go low when the conversion is complete.

ADCs that offer conversion start signals without a busy signal are anticipated to allow reading of the prior SPI result while the current conversion is ongoing. Connect the CNV2 signal to the ADC conversion start and the BUSY2 signal. This will force the LTM2893 to read data from the ADC after the CNV2 signal goes low.

ADCs that do not have a conversion start or a busy signal are anticipated to allow reading of the prior SPI result while a conversion is ongoing. Connect the CNV2 signal to the BUSY2 signal. This will force the LTM2893 to read data from the ADC after the CNV2 signal goes low. This may include ADCs that use the $\overline{CS}$ signal to initiate a conversion start. An example of this is shown in Figure 15 with an LTC2314-14.

TIMING AND CONTROL

A conversion is initiated by CNV. A rising edge on CNV will start a conversion and start the process controlling the BUSY output and the collection of ADC results. Once a conversion has been initiated, do not start a new conversion until the current process is completed and the ADC results have been read or else data loss may occur. Once a CNV rising edge is detected, the BUSY output is asserted high and remains high throughout the ADC conversion phase and is de-asserted at the point the most significant bit is ready to be read. Reading data from the serial digital interface before the BUSY output is de-asserted will result in erroneous results and an assertion of the $\overline{FAULT}$ flag. To enable the serial digital interface assert the $\overline{SS}$ input low. The $\overline{SS}$ input allows the serial digital interface to be shared with other devices. When the device count is 1-2, the $\overline{SS}$ input may be held low at all times or asserted low at each read of the ADC results after the BUSY output has gone low. Asserting $\overline{SS}$ low at each ADC result read will allow a $\overline{FAULT}$ report to be cleared. At each SCK rising edge, the MISOA and MISOB data is read by the external master controller and the next data bit is registered to the MISOA and MISOB pin. The external master controller must read the result in one transaction prior to the next CNV rising edge.

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DIGITAL INTERFACE

The LTM2893 has a serial digital interface. The flexible V_L supply allows the LTM2893 to communicate with digital logic operating between 1.71V and 5.5V, including 2.5V and 3.3V systems. The serial digital interface matches the characteristics of a serial peripheral interface bus (SPI) mode (0, 0) with a minor variation that data is captured on the rising edge and changes after the rising edge for SCK2 frequencies of 100MHz and 66MHz, except for MOSI2 on the LTM2893-1, which changes data on the falling edge of SCK2 in all cases. This variation allows for additional propagation and setup time to the next rising clock (SCK) edge, and should be transparent in most applications. For SCK2 frequencies of 50MHz or less, data is captured on the rising edge of SCK and changes on the falling edge of SCK.

The serial output data is clocked out on the MISO pin when $\overline{SS}$ is low and an external clock is applied to the SCK pin. Clocking out the data immediately after the BUSY signal goes low will yield the best performance. When $\overline{SS}$ is high, the MISOA and MISOB pins are high impedance.

The serial digital interface is monitored by the fault detection system watchdog for conditions that are considered a stalled process. Input timing is monitored for delays longer than $t_{WATCHDOG_TIMEOUT}$ between the rising edges of adjacent SCKs. The SCKs are counted and if the expected number is exceeded, the $\overline{FAULT}$ output will go low.

The rise and fall time of the logic signals into and out of the serial digital interface are approximately 1ns or less. Careful routing between the master device and the LTM2893 are necessary to avoid reflections resulting in incorrect data sampling or double clocking. Short direct routing with ground shielding is necessary. Avoid adding stubs to the signal routing as these may cause reflections.

STARTUP

The LTM2893 has an internal startup communication routine to verify both sides of the isolation barrier are ready for communication. The startup routine is initiated when voltage is supplied to V_{CC} and V_{CC2} inputs above 2.75V, V_L and V_{L2} inputs above 1.5V, the logic side ON signal is high, and the Isolated ON2 signal is high. The BUSY signal will go high and then low indicating the two internal isolators have completed the communication startup routine. Once the BUSY output goes low, the system is ready.

The isolated ON2 pin can be controlled by an external voltage supervisor to delay the system ready signal until all isolated supplies and systems are ready. An example of this is demonstrated in Figure 16 with a LTC2917 configurable voltage supervisor. The logic side BUSY signal will stay high until the isolated side supervisor has verified the supplies are above the specified voltage.

BUSY INDICATOR (LOGIC SIDE)

The BUSY output pin goes high under three conditions: at startup, during data conversion, and when a watchdog timeout occurs. During normal operation, after a CNV rising edge, a high on the BUSY output indicates the ADC is currently converting an ADC result and is de-asserted when the data is ready to be read from MISOA and MISOB. Wait for the BUSY output to go low and wait a t_{SSFSCK} delay before initiating the first SCK after $\overline{SS}$ is set low. This delay allows the most significant bit to be setup properly.

During startup the BUSY output is set high to indicate the LTM2893 is powering up and will be de-asserted when isolated communication is verified.

If a watchdog time-out occurs the BUSY signal will go high and the $\overline{FAULT}$ pin will go low.

BUSY2 AND BUSYS INPUTS (ISOLATED SIDE)

The isolated side signals BUSY2 and BUSYS control when the LTM2893 reads data from the ADC(s). Multiple configurations of the two isolated busy signals exist. Internally, the BUSY2 and the BUSYS input are logically OR-ed into a single busy response for which the falling edge is used to trigger the ready to read isolated SPI port function.

If a single ADC is connected to the LTM2893, the ADC BUSY output connects to the BUSY2 signal and BUSYS is connected to GND2, see Figure 14. Once the BUSY2 signal goes high then low, a SPI transaction will begin.

ADCs that contain a sleep function when two conversion start events are triggered without a SPI read must be treated differently. The LTM2893 does not wake up ADCs

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that use this function, such as the LTC2338 and LTC2328. In order to defeat this, connect the BUSYS signal to CNV2, and the ADCs' BUSY signal to BUSY2. This will always keep the ADC awake, see Figure 13.

If the sleep function is needed, a select signal (SA, SB, or SC) can be used with 74VHC02 logic gates to disable this keep-alive function shown in Figure 2.

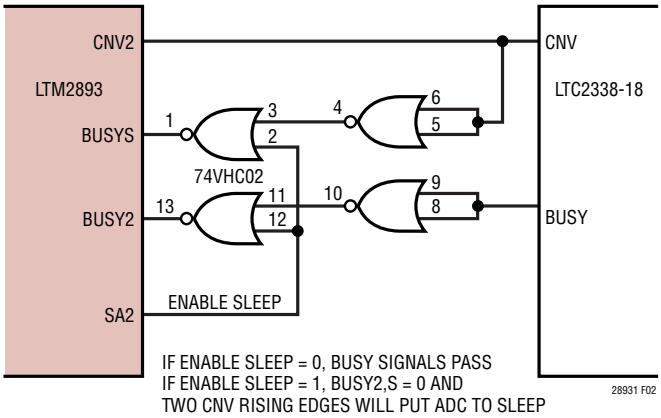


Figure 2. ADC Keep-Alive and Sleep Enable

FAULT REPORTING

The $\overline{\text{FAULT}}$ pin indicates the occurrence of an internal communication error or an erroneous input condition. The $\overline{\text{FAULT}}$ pin is an open drain and requires an external pull up resistance for monitoring. If the $\overline{\text{FAULT}}$ pin is asserted low, data loss may have occurred and the current transaction is suspected to contain an error. To clear the $\overline{\text{FAULT}}$ pin, return CNV low and $\overline{\text{SS}}$ high and initiate a new transaction with CNV or $\overline{\text{SS}}$.

The LTM2893 does not have the provisions to provide the reason for the fault condition. Possible fault conditions are listed in Table 1. If the BUSY signal goes high and the $\overline{\text{FAULT}}$ pin goes low a watchdog time out has occurred. The configuration register is cleared and must be rewritten.

Table 1. Fault Reporting

FAULTS	CAUSE/TROUBLESHOOTING
Idle time during serial digital interface read during configuration write ($\overline{\text{CSC}}$) or LTM2893-1	SCK↑ to SCK↑ > $t_{WATCHDOG_TIMEOUT}$ or $\overline{\text{SS}}$ or $\overline{\text{CSC}}$↓ to SCK↑ > $t_{WATCHDOG_TIMEOUT}$. Minimize delay between this relationship to less than $t_{WATCHDOG_TIMEOUT}$. SCK frequency must be greater than the minimum referenced in Table 5.
Exceeding configured SCKs within a cycle	Exceeding the configured WORDLENGTH number of SCKs during a read is considered a fault.
Data loss in isolation communication	Common mode transients (GND to GND2) greater than 50kV/µs. High transient EM field disturbances greater than specified in EN61000, or an ESD event
Isolated side power loss	ON2, V_{L2}, or V_{CC2} was removed and returned. Indicates unexpected interface loss.
CNV rising edge during serial digital interface read	Avoid transitioning CNV during the read of the serial digital interface. CNV will be ignored during the read of the serial digital interface.

SELECT SIGNALS

The select signal inputs SA, SB, and SC are communicated to the isolated side and output on SA2, SB2, and SC2 respectively. The select signals allow control of an external device related to the acquisition of an analog input signal. Select signals are communicated through the isolator on edge events. A static condition at start up is not communicated to the isolated side. A transition is required to exit the default low output. Examples of device types anticipated for use on these pins are analog multiplexers (Figure 18) or programmable gain amplifiers. The signals can be used as logic controls for resets or power down functions that are not expected to occur during a conversion of an analog signal. The select signals are not designed for use as general purpose logic signals with asynchronous transition times relative to an analog to digital conversion. Use of these signals must be kept synchronous and outside of the operation of the CNV, BUSY, or $\overline{\text{SS}}$ active duration. Data and time sensitive information may be lost if a select signal transitions within 150ns of the CNV or $\overline{\text{SS}}$ signal.

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The direction of the SA, SB, or SC signals may be changed independently with the configuration register. The default condition of '0' for each select bit maintains the signal flow from logic-to-isolated. Loading a '1' into the direction bits will change the direction for that pin(s) to isolated-to-logic.

Warning: Careful planning is required for the use of SA, SB, and SC signals. Figure 12 shows the regions were transitions are safe and not safe for the logic side interface.

The select signals are sampled and transferred as a packet of the current value of the three signals. The select signal sampling will have up to 10ns of sampling jitter. If a signal transitions after another signal was sampled and is in the process of being transferred to the adjacent side, it will be delayed until the next available transmission slot. The delay may cause a perceived jitter or uncertainty of 80ns.

CONFIGURATION REGISTER

The LTM2893 contains a configuration register to adjust parameters of the speed and features of the ADC write and read process. After power up, write the configuration register by setting the $\overline{CSC}$ chip select input low and clocking in a one-byte configuration word with SCK and MOSI. The configuration register contains two bytes where the most significant bit of the SPI word selects which byte is addressed. Complete each configuration word by reasserting $\overline{CSC}$ high. The isolated side will be configured through an internal communication.

Table 3 shows the configuration register bit map for controlling the operation and frequency of the logic and isolated interfaces. The configuration register allows adjustment of the default SCK frequency, direction of the SA, SB, SC to SA2, SB2, SC2 signals, the length of the SPI word and number of SPI words to process per $\overline{SS}$ cycle. Figure 8 demonstrates access to the configuration register.

SCK AND SCK2 FREQUENCY

The SCK2 frequency selection list is shown in Table 4. Select the SCK2 frequency that is equal or less than the specifications of the ADC's SPI port. Example: the LTC2338 has a 100MHz SCK maximum, 10ns minimum SCK period; therefore configure SCK2 for 100MHz.

The isolated SCK2 frequency is an internal trimmed oscillator. Graph SCK2 Frequency Variation versus Temperature shows the minimum and maximum characteristics over temperature and trim variation of the SCK2 frequency.

The logic-side SPI SCK frequency may be selected within a range that is dependent on the isolated-side's SCK2 frequency. The minimum SCK frequency is limited to avoid triggering the watchdog timer and the maximum SCK frequency is limited to prevent a SPI buffer under-run.

To prevent a watchdog time out, the logic-side SPI SCK frequency must be at least 0.00795 times SCK2. If a watchdog timeout occurs, the FAULT flag will assert low.

To prevent a SPI buffer under-run, either the logic-side SPI SCK frequency must be less than the SCK2 frequency or there needs to be a sufficient delay after BUSY falls, $t_{BUSYFSCKR}$, so that the buffer will be full enough to allow its reading at the desired logic-side SPI SCK frequency. If these conditions are not met and a buffer under-run occurs, then the FAULT flag will assert low.

Accounting for temperature and trim variations, the lowest SCK2 frequency will be 0.925 times the nominal SCK2 frequency.

The delay $t_{BUSYFSCKR}$ is calculated using Equation 1 and Table 2 lists values of $t_{BUSYFSCKR}$ for common operating conditions.

Equation 1:

$$t_{BUSYFSCKR} \geq \max \left[\left(\frac{\text{WORD COUNT} \bullet \text{WORDLENGTH} - 2}{\text{SCK2} \bullet 0.925} \right) - \left(\frac{\text{WORD COUNT} \bullet \text{WORDLENGTH} - 1}{\text{SCK}_{MAX}} \right) + 2\text{ns}, t_{SSFSCK,MIN} \right]$$

where $t_{BUSYFSCKR}$ is the time between the falling edge of BUSY and the 1st rising edge of SCK, SCK2 is the nominal configured frequency in Hz and SCK_MAX is the maximum frequency in Hz.

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Note that, provided the timing for SCK_MAX doesn't violate the other SCK timing specifications, SCK_MAX may exceed SCK2 if the corresponding $t_{BUSYFSCKR}$ is observed.

Note that the minimum t_{SSFSCK} of 20ns must also be independently satisfied and so, if the falling edge of SS is delayed sufficiently past the falling edge of BUSY, then the reading may need to be delayed beyond the value of $t_{BUSYFSCKR}$ calculated in Equation 1.

When the number of bits to be transferred (WORDCOUNT • WORDLENGTH) is equal to or less than 32 bits, the delay needed to meet timing at the maximum SCK frequency of 100MHz is equal to the minimum SS to SCK required and therefore no additional delay is required.

Table 2. BUSY Fall to SCK Rising Delay Required for Major Word Boundaries to Operate at Maximum SCK Under Worst Case SCK2 Tolerance

$t_{BUSYFSCKR}$	TOTAL NUMBER OF BITS PER SPI TRANSACTION			
SCKMAX	32	64	96	128
100MHz	20ns	43ns	69ns	95ns
66MHz	24ns	64ns	103ns	142ns
50MHz	31ns	83ns	135ns	187ns
40MHz	38ns	103ns	168ns	233ns
33MHz	46ns	125ns	203ns	282ns
25MHz	60ns	164ns	267ns	371ns
12.5MHz	117ns	325ns	532ns	740ns
6.25MHz	232ns	647ns	1062ns	1477ns

CYCLIC REDUNDANCY CHECK (CRC)

The CRC enable selection bit (Config Register 0, bit 3) enables an internal CRC process to be completed during the communication of SPI data across the internal isolation barrier. The CRC is a 3-bit message added to the end of a SPI data word and is checked on the receiver side. The CRC is an internal function and the values are not readable. If the check fails, the $\overline{FAULT}$ pin is asserted low. When CRC is enabled, an additional wait of 225ns is required for the CRC to complete processing before the reassertion of a new SPI transaction or a new rising edge on CNV.

DEVICECOUNT AND WORDLENGTH

The DEVICECOUNT configuration bits select the number of words the LTM2893 will process. The selection of this value is based on the number of ADCs isolated or the number of words that must be written or read from the ADC. The DEVICECOUNT selection is used in conjunction with the WORDLENGTH selection bits. The WORDLENGTH is set to the number of bits per word. The WORDLENGTH selection allows the SPI access to be tailored to a specific ADC result length to maximize throughput. When a controller that requires byte wide increments is used, set the word length to the number of bits on a byte size boundary (8, 16, 24, or 32). The total number of bits per SPI transaction is the WORD COUNT • WORDLENGTH as referenced in Table 6 and Table 7.

For example, a single 16-bit ADC is selected as DEVICECOUNT of 1-2 with a WORDLENGTH of 16. Two 16 bit ADCs in parallel (SDO of ADC1 connected to MISOA2 and SDO of ADC2 connected to MISOB2) are also selected as a DEVICECOUNT of 1-2 with a word length of 16. Chaining a device increases the DEVICECOUNT. Chaining two additional ADCs through the first pair of ADCs would change the DEVICECOUNT to 3-4 with a word-length of 16.

The DEVICECOUNT is interchangeable with the number of words, WORD COUNT, a device requires for communication. An example ADC may need 4 words of 32 bits. In this case, selecting the maximum DEVICECOUNT of 7-8 will write or read 4 words and setting the WORDLENGTH to 32 will set the length of each word. The LTM2893 writes or reads ½ the number of words as the DEVICECOUNT value. WORD COUNT is equal to ½ of DEVICECOUNT, see Table 7. A DEVICECOUNT of 1-2 will read 1 word, a DEVICECOUNT of 3-4 will read 2 words, a DEVICECOUNT of 5-6 will read 3 words, and a DEVICECOUNT of 7-8 will read 4 words.

LTM2893-1 ADC READ/WRITE

The LTM2893-1 writes a SPI word to the isolated ADC after the read operation. On the logic side, a SPI transaction will output data from MISOA, MISOB and read in a

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command for the ADC in the MOSI pin. At start-up, prior to a CNV rising edge, an ADC command may be written to the LTM2893 and it is transferred to the ADC. On all future transactions, the isolated side will communicate to the ADC through a two-step process. The ADC is read, in the first cycle, when data is ready, indicated by the ADC's BUSY signal into BUSY2. Then the ADC is written on a second cycle after write data is received from the logic side. See Figure 11 for a timing representation of the transactions.

The writing of data to the ADC will begin after a full word is received from the master and at the next available isolated side word boundary. Due to a built-in delay across the isolation barrier, the writing of a word is forced to the next available time slot. Examples of the overall delay that can occur are shown in Figure 3, Figure 4, and Figure 5. Delay between conversion starts must be added to account for the write delays. Not all ADCs will accept the second SPI transaction and may not operate as expected.

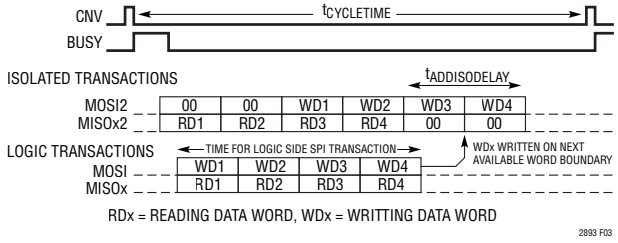


Figure 3. LTM2893-1 Example Word Delay on Isolated Transactions When Logic Side Reads and Writes After BUSY Falls

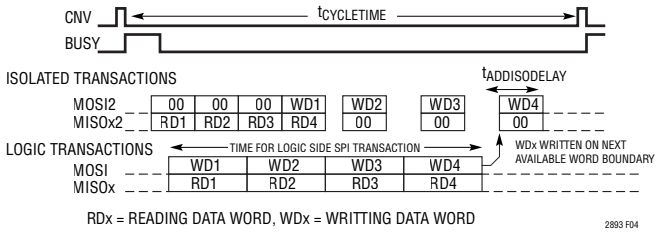


Figure 4. LTM2893-1 Example Word Delay on Isolated Transactions When Logic Side Reads and Writes After a Delay and with a Slower SCK

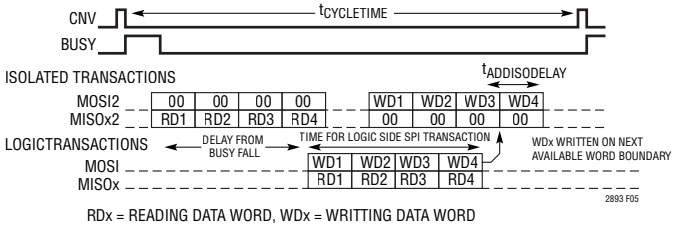


Figure 5. LTM2893-1 Worst Case Example Word Delay on Isolated Transactions When Logic Side Reads and Writes After a Long Delay

ADDITIONAL ADC CONFIGURATIONS

To interface ADCs without a BUSY signal and to allow immediate reading, including the LTC2314-14, connect CNV2 to BUSY2 and connect BUSYS to GND2. This configuration will read the ADC SPI port shortly after the CNV2 signal goes low, maximizing data rate. In this configuration, a sampling rate of 2Msps can be achieved with the LTC2314-14, see Figure 15. The sampling rate is constrained by the data changing on the falling edge of SCK and the delay for the data to be valid is as much as 9.1ns (per the LTC2314-14 data sheet). To guarantee setup time SCK2 frequency is set to 50MHz.

PARALLEL CONNECTING ADCs

MISOA and MISOB pins allow two data words to be read simultaneously. Connect pairs of ADC SDO outputs to the isolated side MISOA2 and MISOB2 inputs. The pairs of ADCs are read simultaneously with the SCK2 signal. OR the BUSY outputs of the ADCs so the last ADC ready initiates the reading of the results. If one pair of ADCs is connected, the BUSY2 and BUSYS inputs accomplish the OR function. If additional ADCs are connected, an external OR is necessary.

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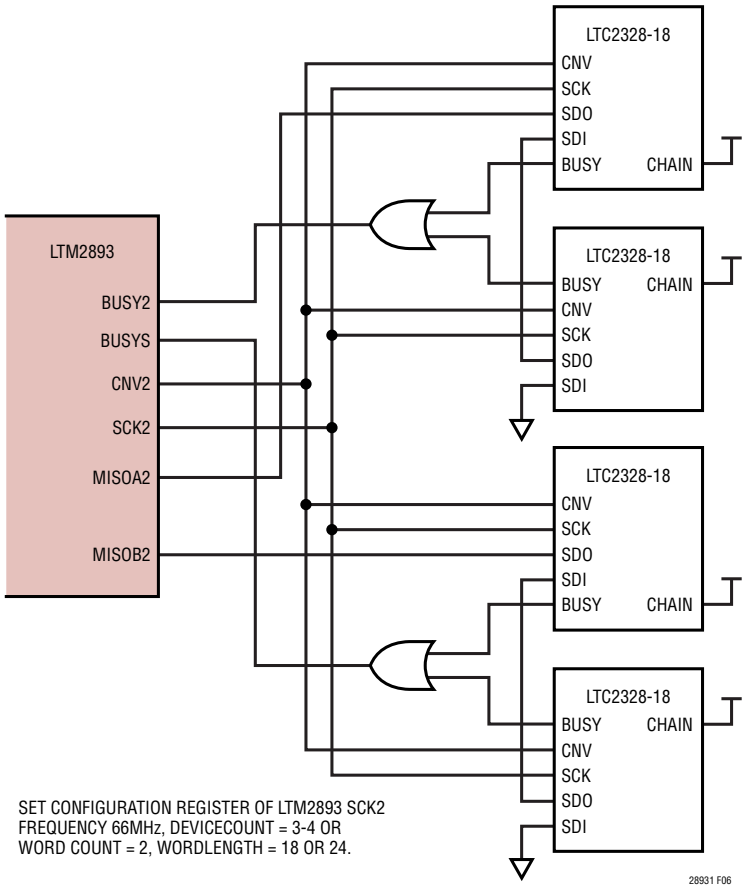
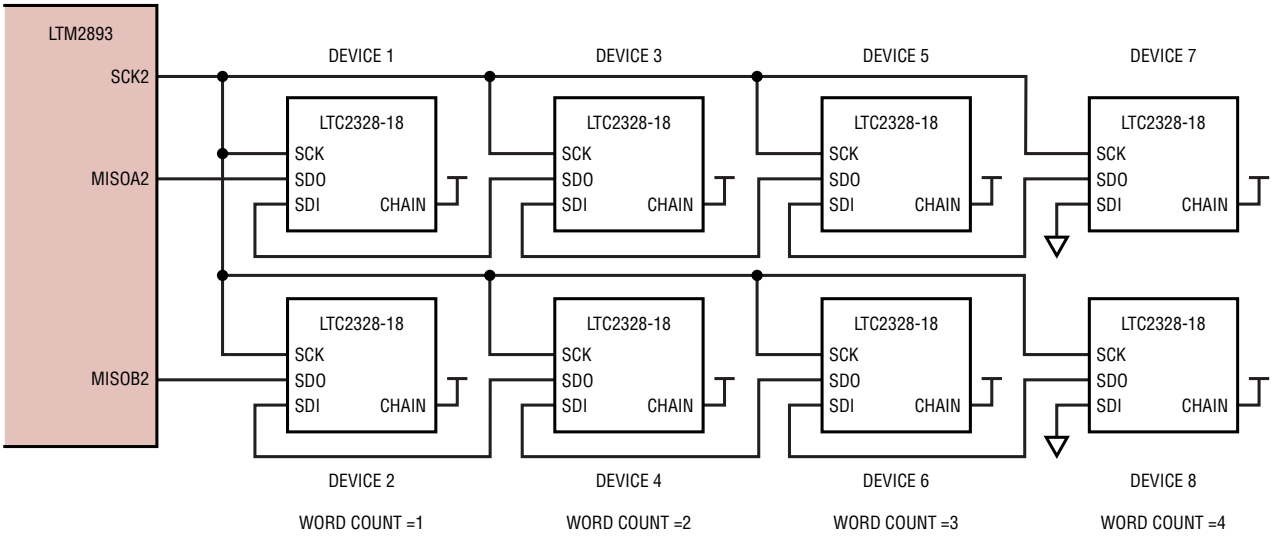


Figure 6. Connecting Four ADCs, One Chain Into MISOA2 and One Chain Into MISOB2



SET CONFIGURATION REGISTER OF LTM2893 SCK2
DEVICECOUNT = 7-8 OR WORD COUNT = 4
CONFIGURATION REGISTER COMMANDS
0x10h, 0x9Eh (66MHz, 24-BITS) or 0x10h, 0x94h (66MHz, 18-BITS)

Figure 7. DEVICECOUNT, WORDCOUNT in Parallel and Chain Configuration

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Table 3. Configuration Registers

	BIT 7 ADDRESS (AD7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
Configuration address 0	0	OSCDIV2	OSCDIV1	OSCDIV0	CRC enable 0 = disabled 1 = enabled	SC direction 0 = logic-to-iso 1 = Iso-to-logic	SB direction 0 = logic-to-iso 1 = Iso-to-logic	SA direction 0 = logic-to-iso 1 = Iso-to-logic
Configuration address 1	1	Reserved 0	Reserved 0	DEVICECOUNT1	DEVICECOUNT0	WORDLENGTH2	WORDLENGTH1	WORDLENGTH0

Table 4. SCK2 Frequency Selection Table (Configuration Register 0 Bit 6, 5, 4)

OSCDIV2 (BIT 6)	OSCDIV1 (BIT 5)	OSCDIV0 (BIT 4)	NOMINAL SCK2 FREQUENCY	MINIMUM SCK2 FREQUENCY	LTM2893-1 MINIMUM SCK FREQUENCY	LTM2893-1 $t_{WATCHDOG_TIMEOUT}$ MAXIMUM t_{SCK} PERIOD OR IDLE TIME WITH $\overline{SS}$ LOW (t_{SSFSCK}, $t_{SCKSSDIS}$)
0	**0**	**0**	**100MHz**	**92.5MHz**	**824kHz**	**1.185µs**
0	0	1	66MHz	61.5MHz	550kHz	1.84µs
0	1	0	50MHz	46.25MHz	412kHz	2.45µs
0	1	1	40MHz	36.5MHz	330kHz	3.08µs
1	0	0	33MHz	30.5MHz	274kHz	3.7µs
1	0	1	25MHz	23.1MHz	206kHz	4.9µs
1	1	0	12.5MHz	11.6MHz	103kHz	9.9µs
1	1	1	6.25MHz	5.8MHz	26kHz	39.0µs

Note: Factory Default Settings are in bold. The LTM2893 may exceed the Minimum SCK Frequency when reading ADC results when $\overline{SS}$ is low. The $\overline{CSC}$ configuration register write requires adherence to the minimum SCK frequency specification.

Table 5. SCK Frequency Selection Timing Specifications

SCK2 FREQUENCY, MAXIMUM SCK FREQUENCY	t_{SCK} PERIOD (ns)		t_{SCK2} PERIOD (ns)		t_{SSFSCK} / $t_{CSCFSCK}$ (ns)		LTM2893-1 $t_{SCKSSDIS}$ (ns)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
100MHz	**10**	**1185**	**9.5**	**10.8**	**20**	**1185**	**20**	**1185**
66MHz	15	1840	14.25	16.2	20	1840	20	1840
50MHz	20	2450	19.0	21.6	20	2450	20	2450
40MHz	25	3080	23.75	27	20	3080	20	3080
33MHz	30	3700	28.0	32.4	20	3700	20	3700
25MHz	40	4900	38.0	43.2	20	4900	20	4900
12.5MHz	80	9900	76.0	86.4	20	9900	20	9900
6.25MHz	160	39000	152.0	172.8	20	39000	20	39000

Note: Exceeding Max of t_{CSFSCK} on the LTM2893, or t_{SCK}, t_{SSFSCK}, or $t_{SCKSSDIS}$ on the LTM2893-1 will result in a watchdog timeout setting $\overline{FAULT}$ low.

Table 6. SPI Word Length Selection Table (Configuration Register 1 Bits 2, 1, 0)

BITS PER WORD (WORDLENGTH)	WORDLENGTH2 (BIT 2)	WORDLENGTH1 (BIT 1)	WORDLENGTH0 (BIT 0)
8	0	0	0
12	0	0	1
14	0	1	0
16	0	1	1
18	1	0	0
20	1	0	1
24	**1**	**1**	**0**
32	1	1	1

APPLICATIONS INFORMATION

Table 7. SPI Device Count or Word Count Selection Table (Configuration Register 1 Bits 4, 3)

NUMBER OF DEVICES	WORD COUNT	DEVICECOUNT1 (BIT 4)	DEVICECOUNT0 (BIT 3)
1-2	**1**	**0**	**0**
3-4	2	0	1
5-6	3	1	0
7-8	4	1	1

CHAIN CONNECTING ADCs

Connecting multiple chain-capable ADCs is done with the following guidelines. The ADC must have a chain-capable SDI input. Set the ADC into a chain mode if necessary to enable the passing of data through the SDI input to the SDO output. Connect all the SCK clock signals in parallel with a star configuration from SCK2 to minimize reflections and path delays. Connect the CNV inputs from CNV2 in a similar parallel star configuration. OR all BUSY signals into the BUSY2 and BUSYS inputs. Pair the SDO outputs to take advantage of the MISOA2 and MISOB2 data paths, see Figure 6.

In the Configuration Registers, select the appropriate word length and device count. Select the appropriate SCK2 frequency for the chain mode. Some ADCs may require a reduced SCK frequency in chain mode to account for processing the serial data through their ports. Set the device count based on the word count; two chained devices will require the word count to be two.

RF, Magnetic Field Immunity

The isolator µModule technology used within the LTM2893 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulsed Magnetic Field Immunity

Tests were performed using an un-shielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 8.

Table 8. Immunity Testing

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60 Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

*Non IEC method

PCB Layout

The high integration of the LTM2393 makes PCB layout very simple. However, to maintain its electrical isolation characteristics and signal integrity, some layout considerations are necessary.

- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The edge rates of the ADC interface signals are between 300ps and 1ns. At these edge rates the routing must be treated as a distributed transmission line for lengths greater than 2cm, (length > $t_{RISEFALL}/(2 \bullet 33.3\sqrt{\varepsilon_r})$. Length is in units of cm and $t_{RISEFALL}$ is in units of ps. ε_r is the relative dielectric constant of the circuit board material, typically ~4.8. The isolated side pin-out is organized for direct short connection to LTC2328, LTC2338, and LTC2378 ADCs referenced in the Typical Applications section. For longer lengths or branching to multiple devices routing as a transmission line is required.

TIMING DIAGRAMS

SAMPLING RATE

Achieving a specified sampling rate is the typical goal for systems integrating ADCs. The LTM2893 adds a small amount of overhead to the sampling rate or ADC CYCLE TIME. The selection of the SCK2 frequency and the master SCK frequency will impact the overall time in-between CNVs. The following is a description of each timing characteristic to be calculated to achieve a sampling rate.

1. t_{DCNV}: the delay from CNV to CNV2, maximum of 28ns, is the delay before the ADC receives a conversion start signal.
2. $t_{CNV2toADCstart}$: the ADC aperture delay or the CNV to BUSY delay of the ADC.
3. t_{CNVADC}: the conversion time of the ADC, duration of the ADC's BUSY signal.
4. $t_{BUSY2FBUSYF}$: LTM2893 delay in buffering the first 2 bits from the ADC. $t_{BUSY2FBUSYF} = t_{BUSY2FSS2F} + t_{SS2FSCK2} + 1 \bullet t_{SCK2}$. $t_{SS2FSCK2}$ is $3 \bullet t_{SCK2}$ when SCK2 frequency = 100MHz or 66MHz, $2 \bullet t_{SCK2}$ when SCK2 frequency = 50MHz to 25MHz, or $1 \bullet t_{SCK2}$ when SCK2 frequency is 12.5MHz or 6.25MHz.
5. $t_{BUSYFSCKR}$: time between the master response to BUSY falling and the first SCK rising edge. If $\overline{SS}$ is always low reference Table 2 or Equation 1. If $\overline{SS}$ is used, reference the timing in Table 2 or Equation 1 for BUSY falling to the SCK rising edge with the additional requirement that a minimum time from $\overline{SS}$ falling to SCK rising, t_{SSFSCK}, is maintained.
6. $t_{DATAREAD}$: ((WORD COUNT • WORDLENGTH)-1)/(SCK frequency) is the time for the master to read the data from the SPI port.
7. $t_{SCKSSDIS}$: delay from last SCK rising edge to the release of SS, minimum of 20ns.
8. t_{CRC}: 0ns if CRCENA = 0, 225ns if CRCENA=1.
9. t_{QUIET}: space between the SS rising edge and the next CNV rising edge, minimum of 20ns.

The minimum sampling time is the sum of these timing characteristics for a selected SCK2 frequency and a master SCK frequency. The following equation defines this minimum sample time (2893ADC CYCLE $TIME_{MIN}$), assuming SCK frequency ≤ SCK2 frequency. Figure 9 shows the relationship of these parameters to a conversion cycle.

2893ADC CYCLE $TIME_{MIN} = t_{DCNV} + t_{CNV2toADCstart} + t_{CNVADC} + t_{BUSY2FBUSYF} + t_{BUSYFSCKR} + t_{DATAREAD} + t_{SCKSSDIS} + t_{CRC} + t_{QUIET}$

LOGIC INTERFACE

The LTM2893 logic side interface is similar to an ADC that has a conversion start and busy control signals. Figure 9 shows the interaction of control signals CNV, BUSY, and the SPI serial interface. The CNV transition starts the process and BUSY responds to indicate the ADC is converting a result and masking the propagation delay of signals processed through the isolation barrier. The BUSY signal is up to 95ns longer than the ADC's BUSY signal (when SCK2

CONFIGURING THE LTM2893 WITH $\overline{CSC}$ CHIP SELECT LOGIC SIDE INTERFACE

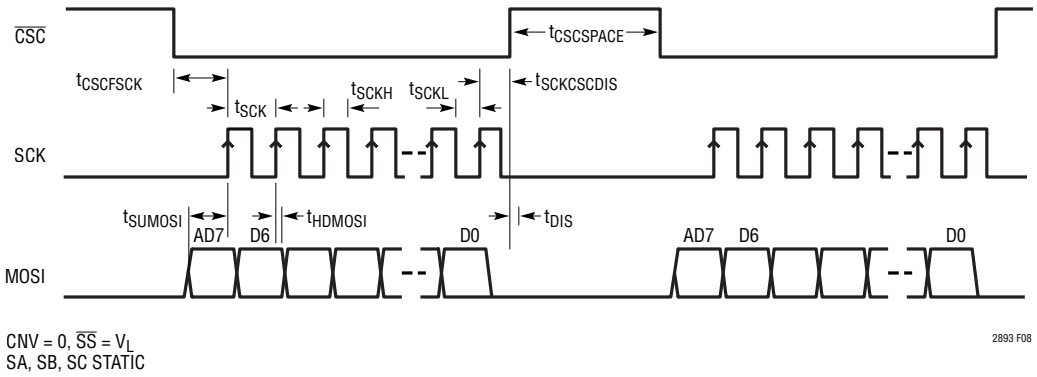


Figure 8. Writing Configuration Registers Timing Diagram

TIMING DIAGRAMS

frequency = 100MHz) to mask the propagation delay of the CNV signal to the isolated ADC and the return of the first two bits in the SPI result. Once the LTM2893 has received the first two bits from the ADC and stored them in the logic side serial buffer, the BUSY signal goes low indicating the data is ready for reading. The $\overline{SS}$ input is driven low by the host controller to enable the SPI serial interface. The MSB of the ADC result is set on the MISOA and MISOB pins. MISOA output results correspond to the data read into the MISOA2 isolated input, MISOB output result corresponds to the data read into the MISOB2 isolated input. MISOA and MISOB will contain two independent serial output streams of the specified WORDLENGTH. After the MSB of the MISOA and MISOB data is available the host controller can clock the SCK signal the specified number of times to read in the full ADC result or pair of results. The host must release the $\overline{SS}$ signal shortly after the final SCK. The fault monitor counts the time between $\overline{SS}$ transitions and SCK rising edges for stall conditions. Connect a resistor from MISOB to GND and connect MISOB2 to GND2 if the second SPI data path is not used.

The LTM2893 uses the $\overline{SS}$ signal as a framing signal around the data transfer of the SPI data. However, the $\overline{SS}$ signal can be held low continuously if only one or one pair of simultaneously sampled ADCs exists on the isolated side and the logic side SPI bus is not shared by other peripherals. In the event that a fault occurs the $\overline{SS}$ signal must be driven high to allow the $\overline{FAULT}$ flag to be cleared on the next transaction.

ISOLATED INTERFACE LTM2893

The LTM2893 autonomously interacts with the isolated ADC when a CNV is initiated. The isolated side CNV2 is asserted to the ADC and the LTM2893 watches for a rising edge on BUSY2 and BUSYS. After the BUSY2 or BUSYS goes high and then low, the isolated side of the LTM2893 will begin reading the ADC. During the SPI read, both MISOA2 and MISOB2 are captured in parallel using the same SCK and $\overline{SS}$ signal. If a single ADC is used with one MISOA2 connection, connect MISOB2 to GND2. Once the SPI transaction is complete the LTM2893 is ready for an additional conversion request on CNV.

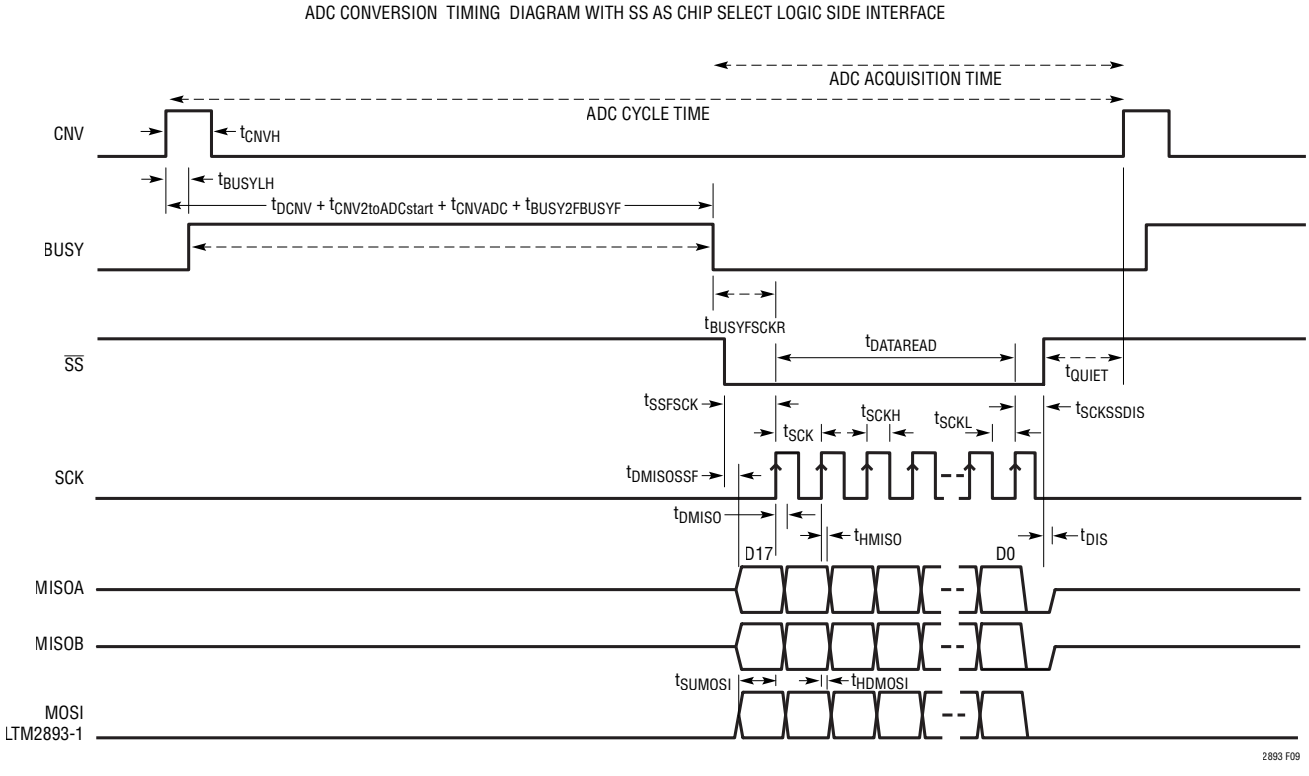


Figure 9. Logic Side Interface of ADC

TIMING DIAGRAMS

The $\overline{SS2}$ signal is not necessary on all ADC parts. The $\overline{SS2}$ signal can be left unconnected if the interfaced ADC does not require a chip select.

The period of time referenced as t_{QUIET2} is the acquisition quiet time allocated to the connected ADC. t_{QUIET2} is a minimum of $t_{BUSY2FBUSYF}$ + t_{QUIET}, the additional delay is added by delaying the next CNV rising edge from the last rising edge of $\overline{SS}$ or SCK. $t_{SCK2SSDIS}$ is approximately 1.5/SCK2.

The default SCK2 frequency is 100MHz; configure the SCK2 frequency to match the requirements of the ADC. The range of variations in the SCK2 period are detailed in Table 5. The temperature dependence of the SCK2 Frequency is shown in the Typical Performance Characteristics section's SCK2 Frequency Variation vs Temperature plot. For example, using the limits from Table 5, an H-grade part configured for SCK2 = 50MHz may operate from 46.25 to 52.65MHz over the entire temperature range

ISOLATED INTERFACE WITH READ AND WRITE USING THE LTM2893-1

The LTM2893-1 isolated side operates ahead of the logic side when reading data from the ADC. In order to write data to the ADC a second SPI transaction is initiated after the full logic side SPI word has been received from MOSI. The logic side sees one write/read SPI transaction and the isolated side sees two transactions, a read and then a write. The second SPI transaction on the isolated side incurs a time penalty and requires flexibility on the part of the ADC. Figure 11 demonstrates the signal patterns that the ADC will see when written. The first SPI transaction reads the ADC results on MISOA2 and MISOB2 while MOSI2 is '0' and then clears the $\overline{SS2}$ signal. A second SPI transaction occurs, after the write data is received, in which the MOSI2 data is written to the ADC. The ADC cycle time must be extended by the master controlling device to accommodate the additional SPI write.

To calculate the time to the next CNV rising edge for the LTM2893-1:

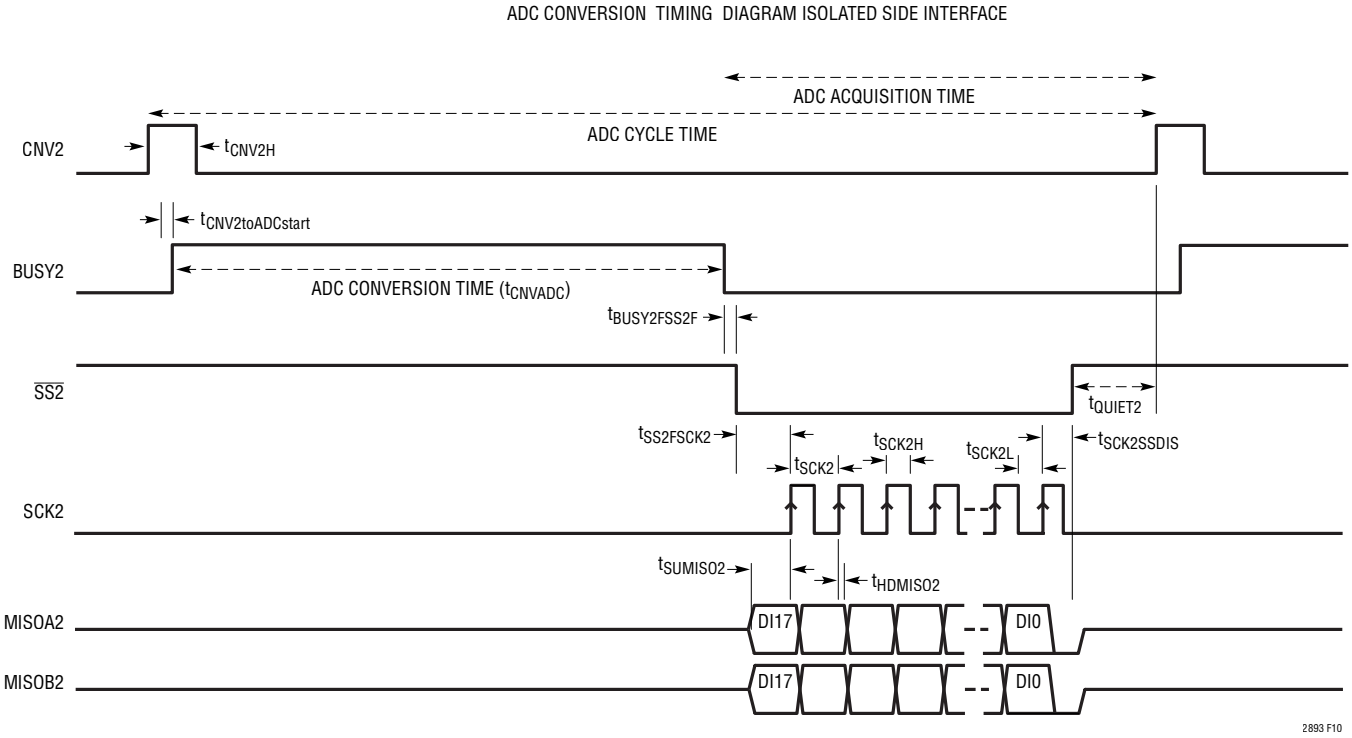


Figure 10. Isolated Side Interface for an ADC Conversion

TIMING DIAGRAMS

28931ADC CYCLE TIME$_{MIN}$ = t_{DCNV} + $t_{CNV2toADCstart}$ + t_{CNVADC} + $t_{BUSY2FBUSYF}$ + $t_{BUSYFSCKR}$ + $t_{DATAREAD}$ + $t_{SCKSSDIS}$ + t_{CRC} + t_{QUIET} + $t_{ADDISODELAY}$.

where:

If wordcount =1:

$t_{ADDISODELAY}$ = (2 + WORDLENGTH) • t_{SCK2}

If wordcount ≥ 2:

$t_{ADDISODELAY}$ = 2 • (2 + WORDLENGTH) • t_{SCK2}

See the Sampling Rate section for the definition of the other timing parameters.

SAFE REGIONS OF THE SELECT ENABLE SIGNALS

The select enable signals SA, SB, and SC must be limited in use to transition in a fixed set of safe regions. Transitions within the collision regions may cause data loss or timing loss to important conversion or result information.

If the SA2, SB2, or SC2 are configured as inputs, do not change 150ns prior to the $\overline{SS2}$ signal falling. The $\overline{SS2}$ signal fall is triggered by BUSY2 or BUSYS falling. If one of these signals changes in this collision region, the SPI process will be corrupted.

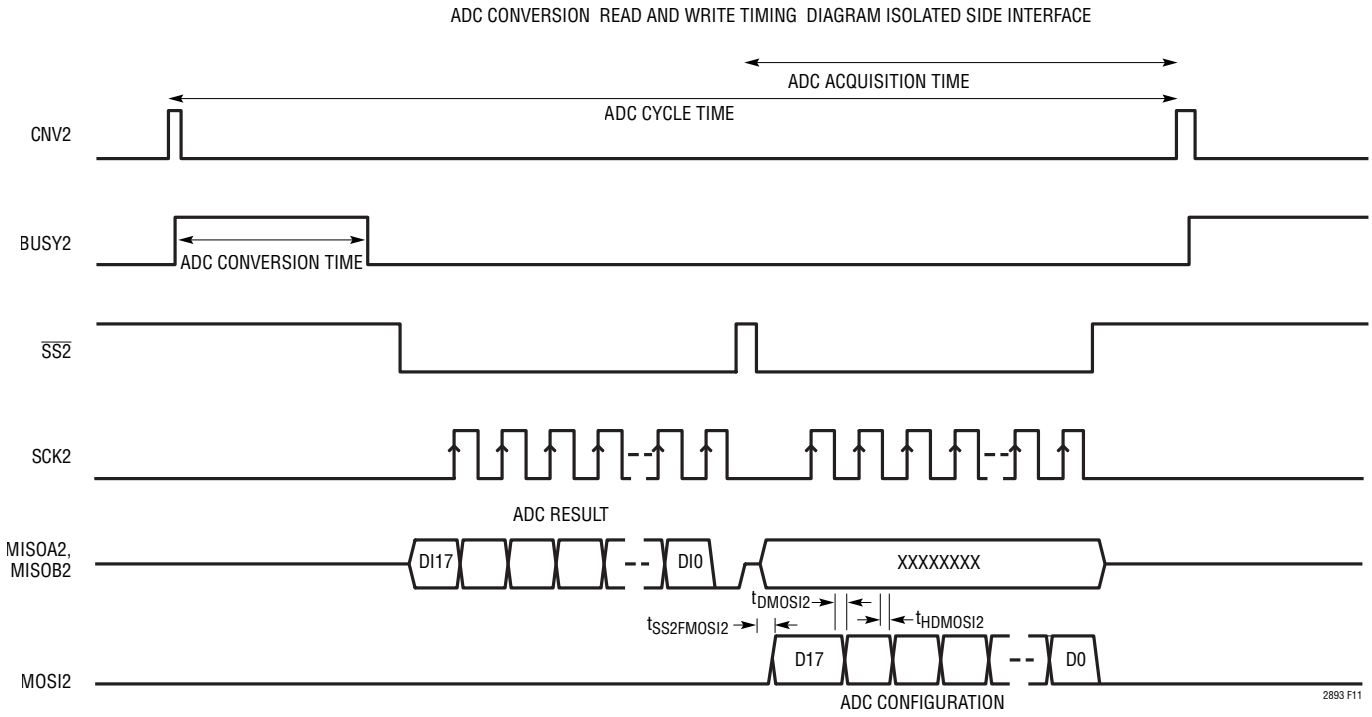


Figure 11. Isolated Side Read and Write to ADC (LTM2893-1)

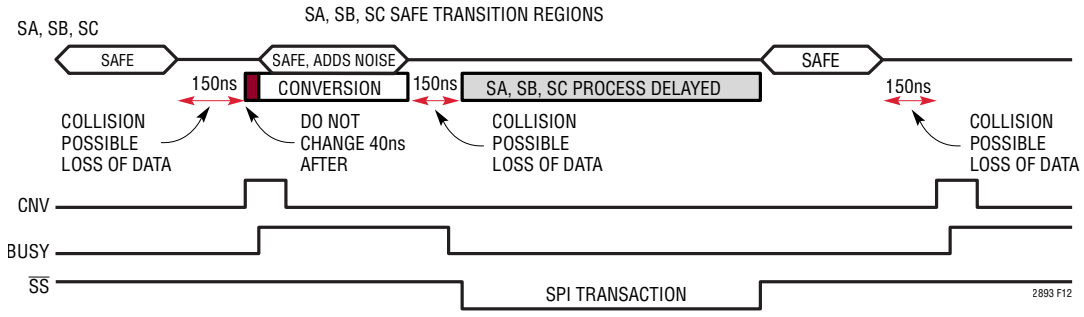


Figure 12. Select Signals Safe Transition Regions

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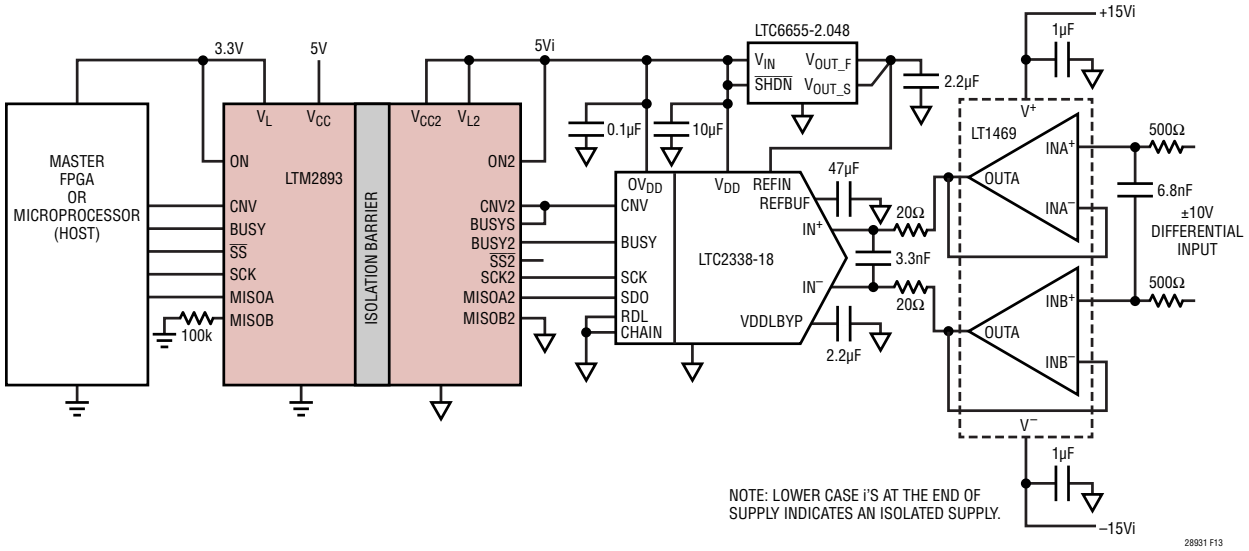


Figure 13. Isolated 1Msps LTC2338-18 Fully Differential ±10V Input Range, with ADC Sleep Disabled (CNV2 = BUSYS)

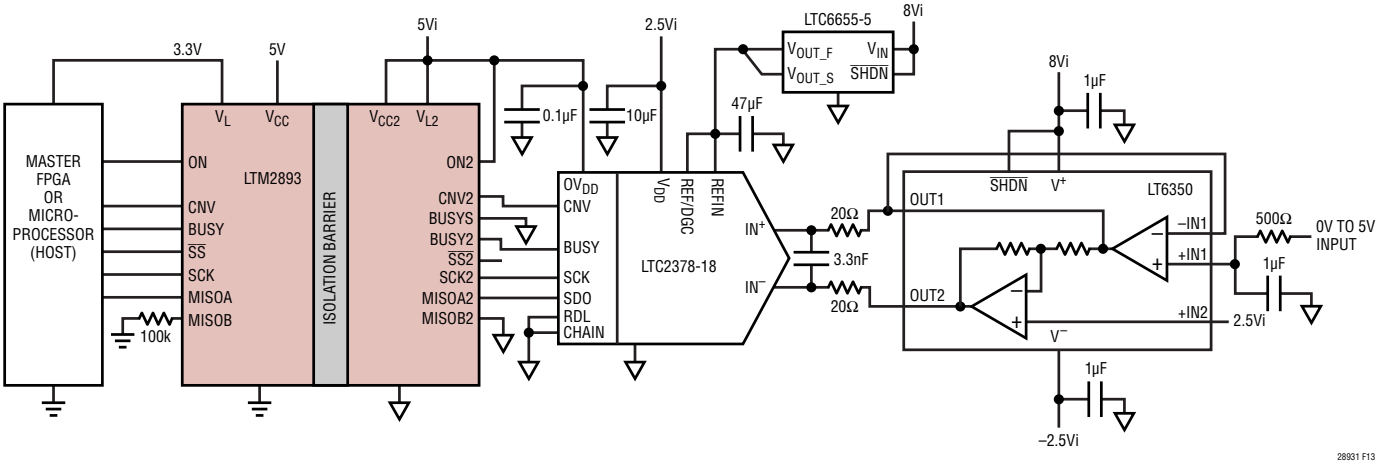


Figure 14. Isolated 1Msps LTC2378-18 Single-Ended 0V to 5V Input (BUSYS = GND2)

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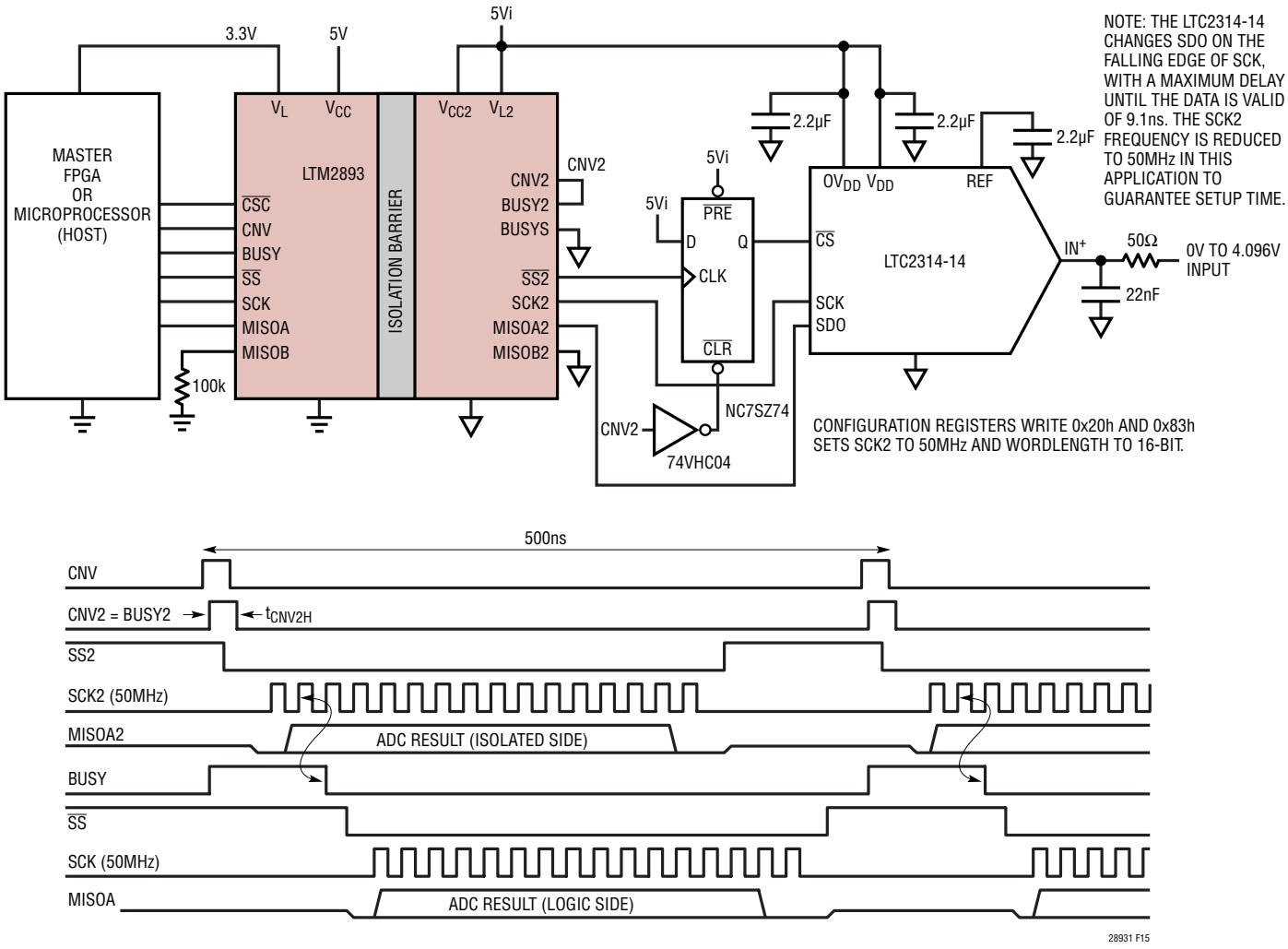


Figure 15. Isolated 2Msps LTC2314-14 0V to 4.096V Input Range, ADC Without a CNV or BUSY, LTC2314 $\overline{CS}$ Is Synchronized to Low Jitter CNV2

TYPICAL APPLICATIONS

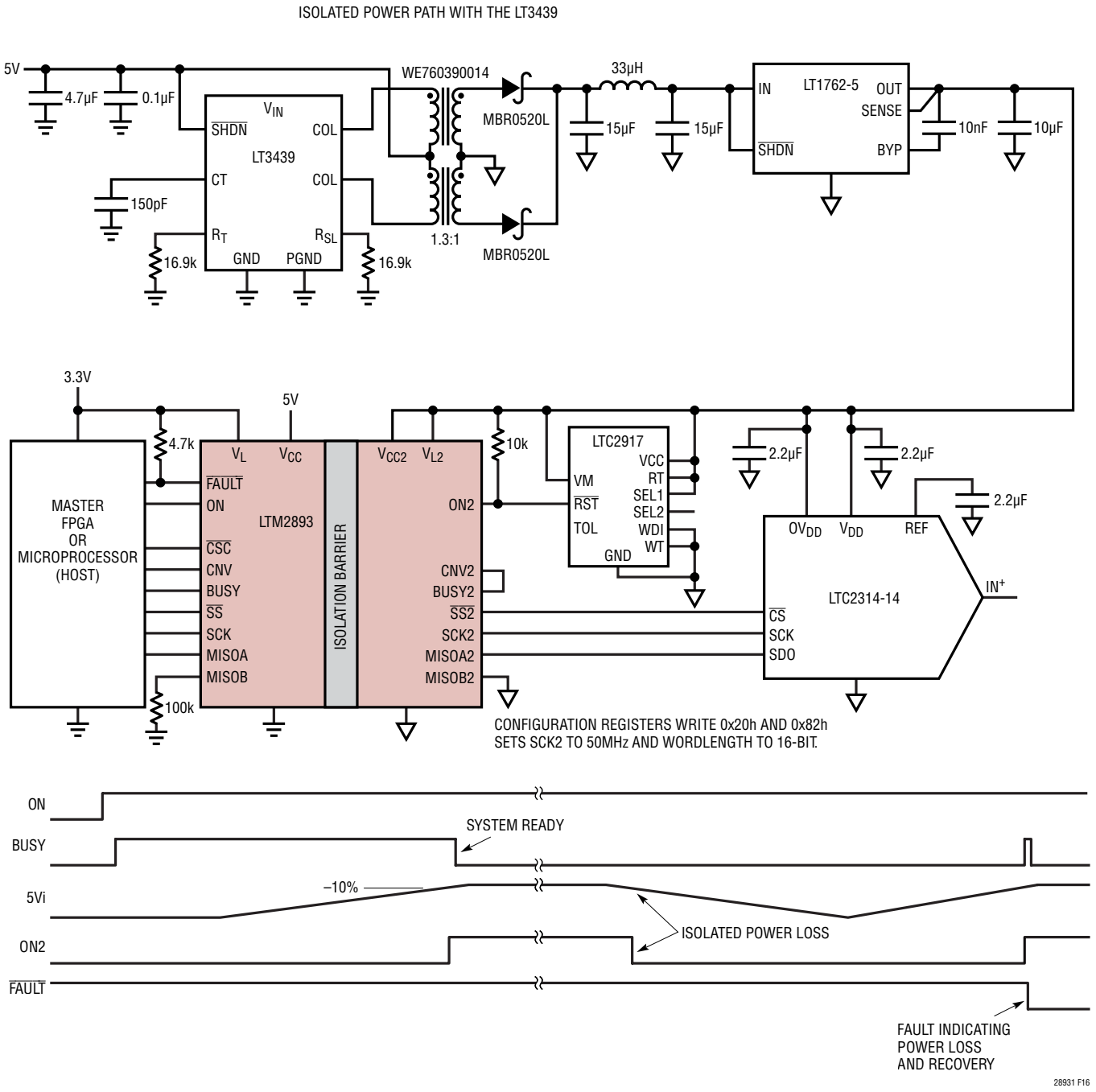


Figure 16. Startup Sequence with a Voltage Supervisor Enabling Isolated Side Including Isolated Power Solution

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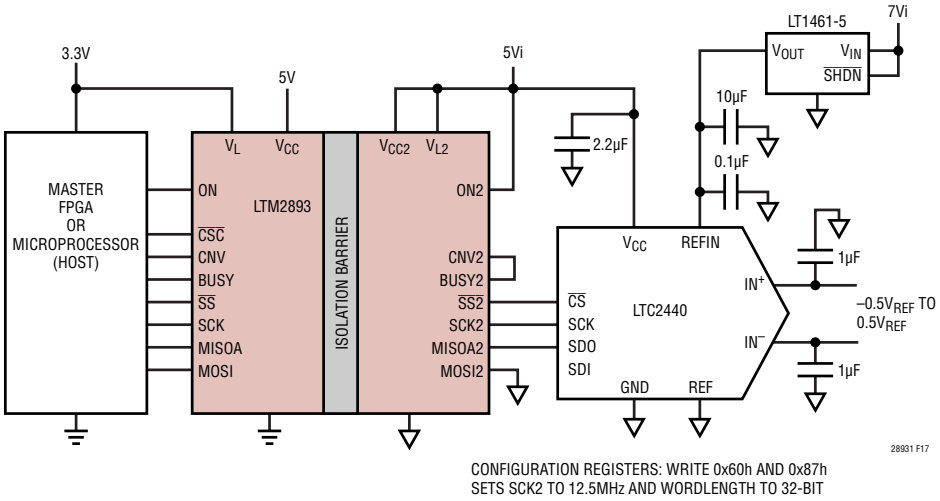


Figure 17. LTM2893 with LTC2440 Delta Sigma ADC

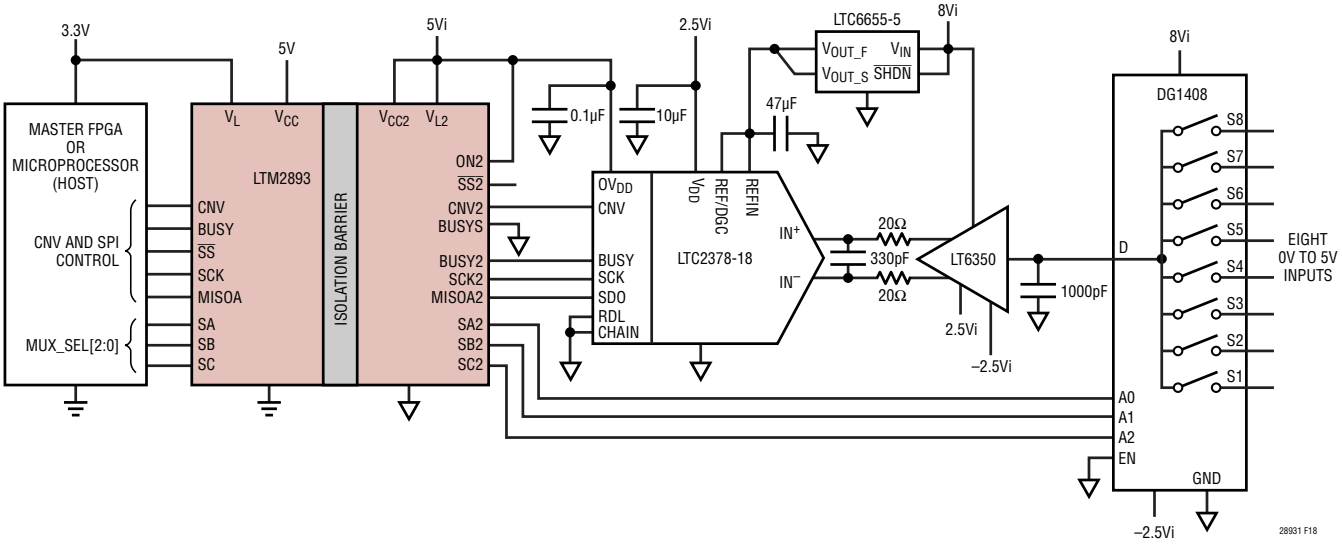


Figure 18. Use of SA, SB, SC Pins for Multiplexing Analog Inputs to ADC

TYPICAL APPLICATIONS

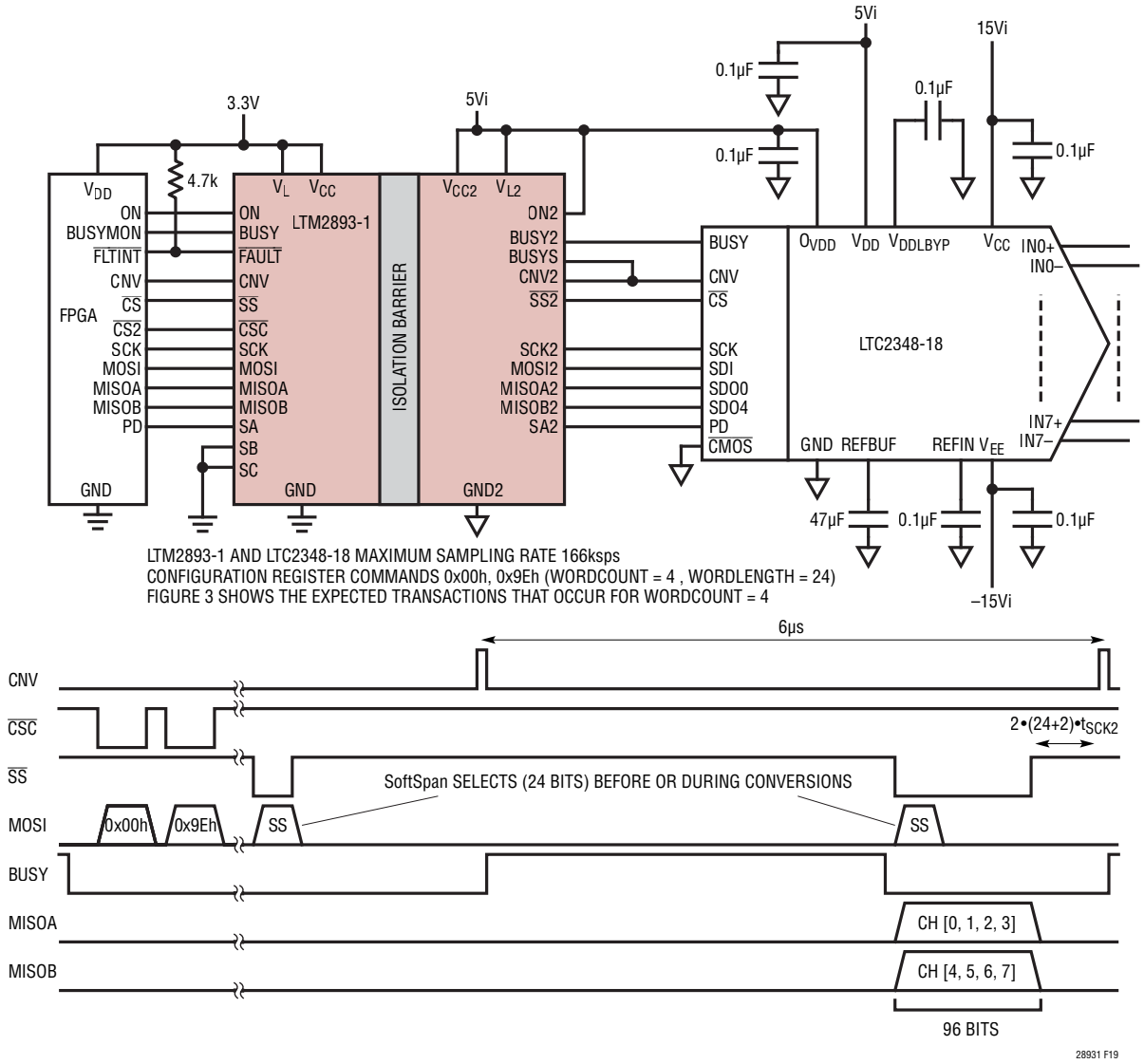
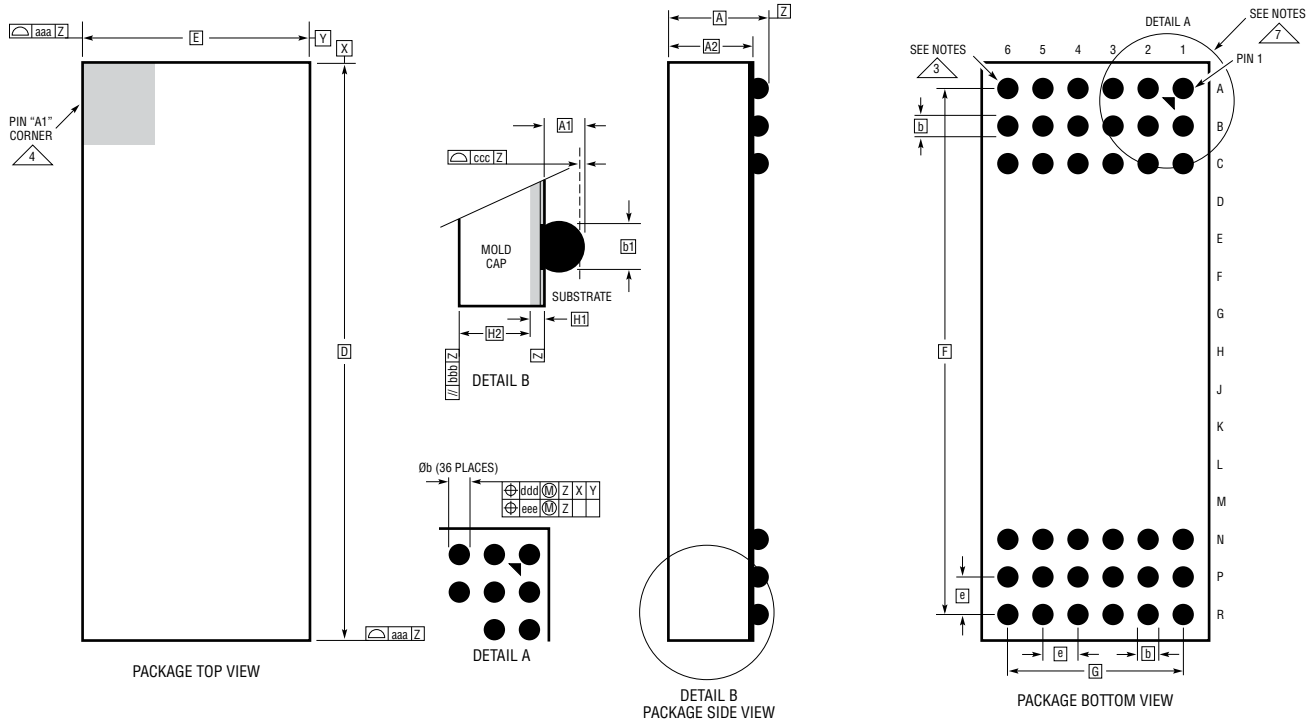
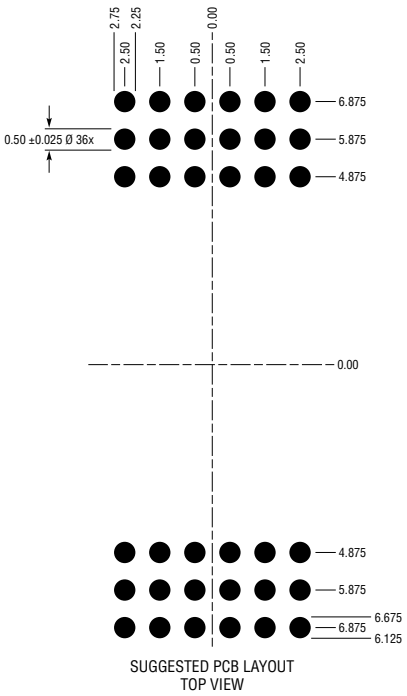


Figure 19. LTM2893-1 with SoftSpan™ Configurable LTC2348-18 8-Channel Simultaneous Sampling ADC

PACKAGE DESCRIPTION

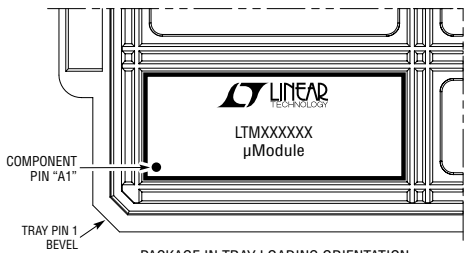
BGA Package
36-Lead (15mm × 6.25mm × 2.06mm)
(Reference LTC DWG # 05-08-1987 Rev Ø)





DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	1.86	2.06	2.26	
A1	0.40	0.50	0.60	
A2	1.46	1.56	1.66	
b	0.45	0.60	0.75	
b1	0.47	0.50	0.53	
D		15.00		
E		6.25		
e		1.00		
F		13.75		
G		5.00		
H1	0.51	0.56	0.61	
H2	0.95	1.00	1.05	
aaa			0.15	
bbb			0.10	
ccc			0.15	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 36				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



PACKAGE IN TRAY LOADING ORIENTATION

BGA 36 0914 REV Ø

Rev C

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/17	Corrected V_{CC2} pin number on Block Diagram	10
		Corrected SCK and $t_{BUSYFSCKR}$ formulas	15
		Correction to Table 2. BUSY Fall to SCK Rising Delay Required for Major Word Boundaries to Operate at Maximum SCK Under Worst Case SCK2 Tolerance	16
		Correction to Table 4. SCK2 Frequency Selection	19
		Multiple corrections to Table 5. SCK Frequency Selection Timing Specifications	19
		Corrections to multiple sampling rate parameters ($t_{BUSY2FBUSYF}$, $t_{BUSYFSCKR}$, $t_{DATAREAD}$)	21
B	05/17	Revised $\overline{SS}$ pin description	8
		Revised SCK2 frequency range calculation for H-grade	23
		Revised tADC_CYCLE_TIME_MIN equation	24
C	02/18	Added UL/CSA Certifications	1, 5

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TYPICAL APPLICATION

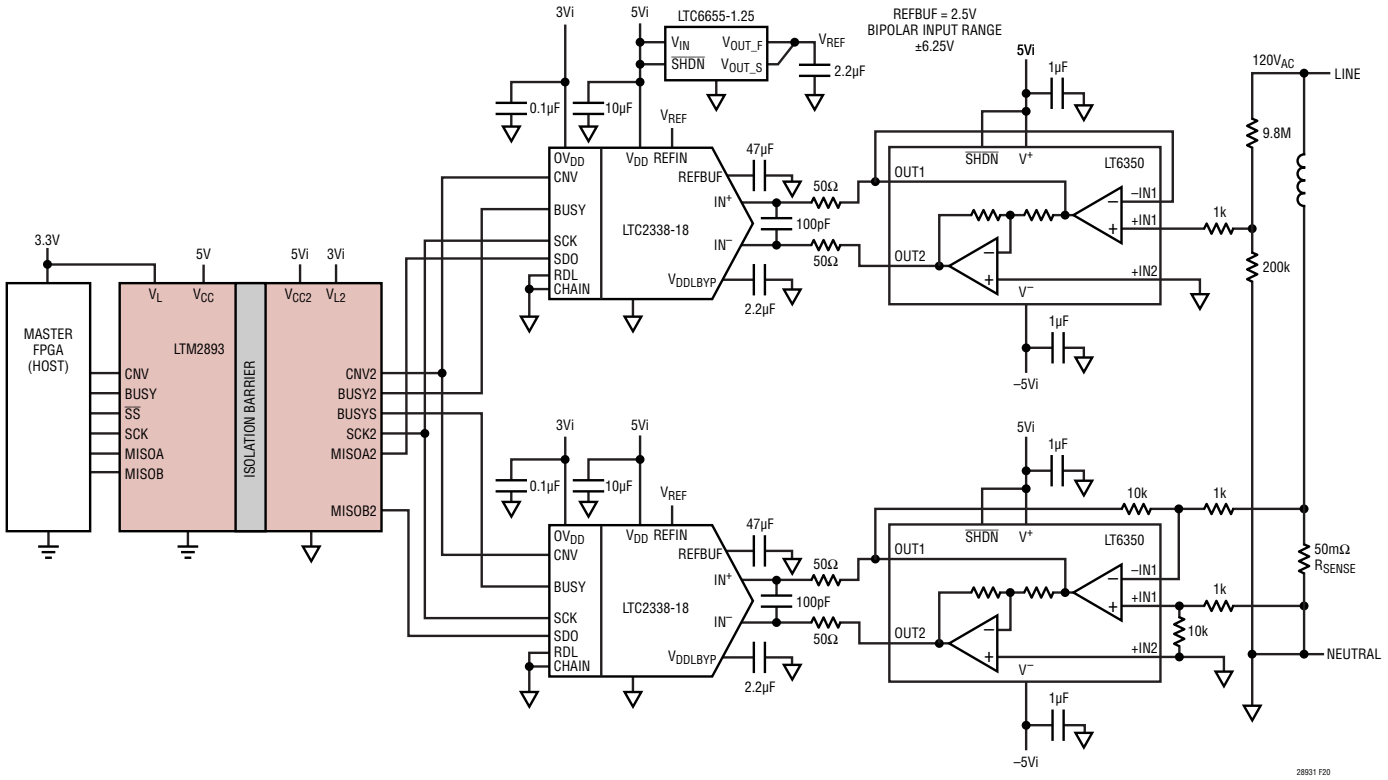


Figure 20. Simultaneous Sampled Line Current and Voltage Measurements with Two LTC2338-18 ADCs

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2892	3500V_{RMS} SPI or I^2C Isolator	Up to 8Mbps SPI Transactions
LTM2883	2500V_{RMS} SPI or I^2C Isolator with Power	Up to 8Mbps SPI Transactions
LTM2881	Complete Isolated RS485/RS422 µModule Transceiver + Power	2500V_{RMS} Isolation in Surface Mount BGA or LGA
LTM2882	Dual Isolated RS232 µModule Transceiver with Integrated DC/DC Converter	2500V_{RMS} Isolation in Surface Mount BGA or LGA
LTC2884	Isolated USB Transceiver with Isolated Power	2500V_{RMS} Isolation in Surface Mount BGA
LTC2348	18-Bit/16-Bit Octal 200ksps Serial ADC	Differential ±10.24V Input SoftSpan ADC with Wide Input Common Mode Range in a 48-Lead Plastic LQFP
LTC2328/LTC2327/ LTC2326	18-Bit/16-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	5V Supply, ±10.24V True Bipolar, Pseudo Differential Input, 95dB SNR, Pin-Compatible Family in MSOP-16 Packages
LTC2338/LTC2337/ LTC2336	18-Bit/16-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	5V Supply, ±10.24V True Bipolar, Pseudo Differential Input, 100dB SNR, Pin-Compatible Family in MSOP-16 Packages
LTC2379/LTC2378/ LTC2377/LTC2376	18-Bit/16-Bit, 1Msps/500ksps, 250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages

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