Ordering number : EN6982B

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV8018W — For Portable MD 4ch PWM H-bridge Driver

Overview

The LV8018W is 4-chnnel PWM-drive H-bridge driver for portable MD.

Functions

- 4-chnnel PWM-drive H-bridge driver.
- Built-in charge pump circuit.
- Built-in thermal shutdown circuit.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage (Output block)	VBAT max		7	V
Supply voltage (Control block)	V_{CC} max		7	V
Predrive voltage (gate voltage)	VG max		9.5	V
Maximum output current (ch1-ch4)	I_O max		500	mA
Allowable power dissipation	Pd max	Independent IC	0.5	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage (Output block)	VBAT max		7	V
Recommended supply voltage (Control block)	V_{CC} max		7	V
Predrive voltage (gate voltage)	VG max		9.5	V

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Electrical Characteristics at Ta = 25°C, $V_{CC}1, 2$ = 3.0V, VBAT = 3.0V

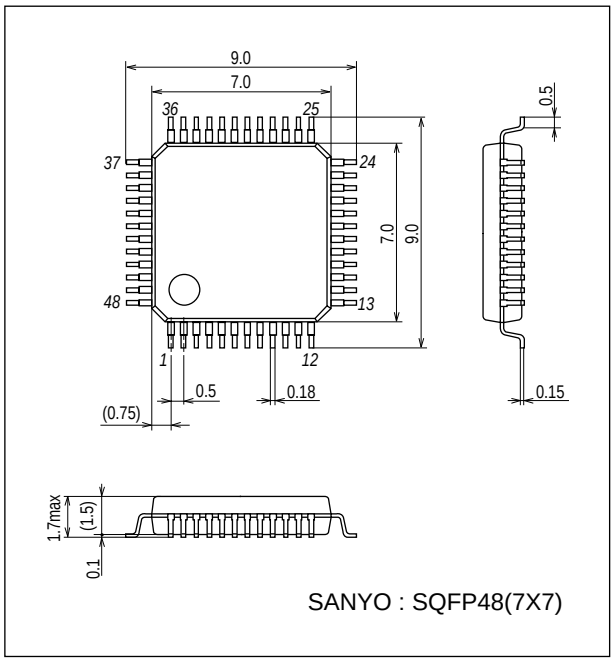
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby current dissipation	I_{CCO}				10	μA
Current dissipation	I_{CC} (A)	V_{GOFF} = "L"		1.4	1.9	mA
	I_{CC} (B)	V_{GOFF} = "H"		1.0	1.5	mA
Predrive block current dissipation	I_{GO}	VG = 7V, each logic input = "L"		70	105	μA
	I_G	VG = 7, input frequency 88kHz		1.0	1.5	mA
S/S bias current	I_{SS}	S/S = 3.0V		80	120	μA
S/S input "High" voltage	V_{SSH}		$V_{CC}2$-0.6		$V_{CC}1$	V
S/S input "Low" voltage	V_{SSL}		0		0.6	V
VBATT/2 set voltage accuracy	ΔV_{MON}				±10	%
VBATT/2 limit voltage	V_{MONLIM}		$V_{CC}1$-0.2	$V_{CC}1$		V
VBATT monitor input resistance	R_{MON}		35	50	75	kΩ
Logic input bias current	I_{LG}				±1	μA
Logic input "High" voltage	V_{LGH}		$V_{CC}2$-0.6		$V_{CC}2$	V
Logic input "Low" voltage	V_{LGL}		0		0.6	V
Booster circuit						
Output voltage	V_{GO}	No load	8.5	8.8		V
	V_G	I_{GOUT} = -1mA	6.7	7.2		V
Output oscillation-frequency	F_{OSC}		100	115	130	kHz
Clamp voltage	V_{GLIM}	V_{GOFF} = "L", $V_{CC}1, 2$ = 3.6V	9.2	9.5	9.8	V
MOS driver output stage (VG = 7V)						
Output ON resistance	Ron1, 2, 3, 4	I_O = 100mA, sum of upper and lower outputs		1.3	2.0	Ω
Output propagation delay time	TRISE	*		0.2	1.0	μs
	YFALL	*		0.1	0.7	μs
Minimum pulse width	Tmin	Output pulse width ≥ (2/3) Tmin *	200			ns
TSD circuit						
Operating temperature	TSD	*	150	180		°C
Hysteresis width	ΔTSD	*		30		°C

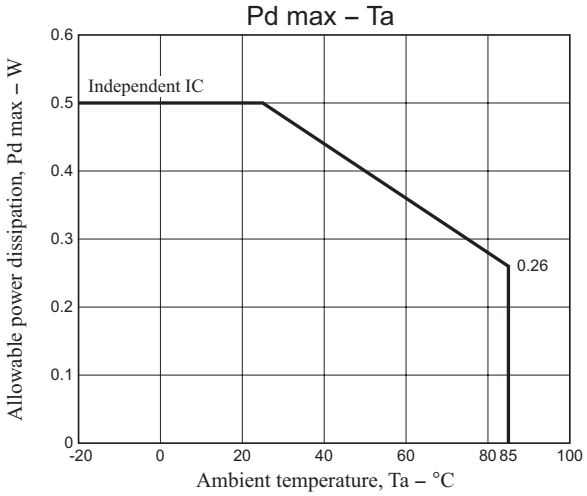
* : "Design" indicates the design target, not the measured value.

Package Dimensions

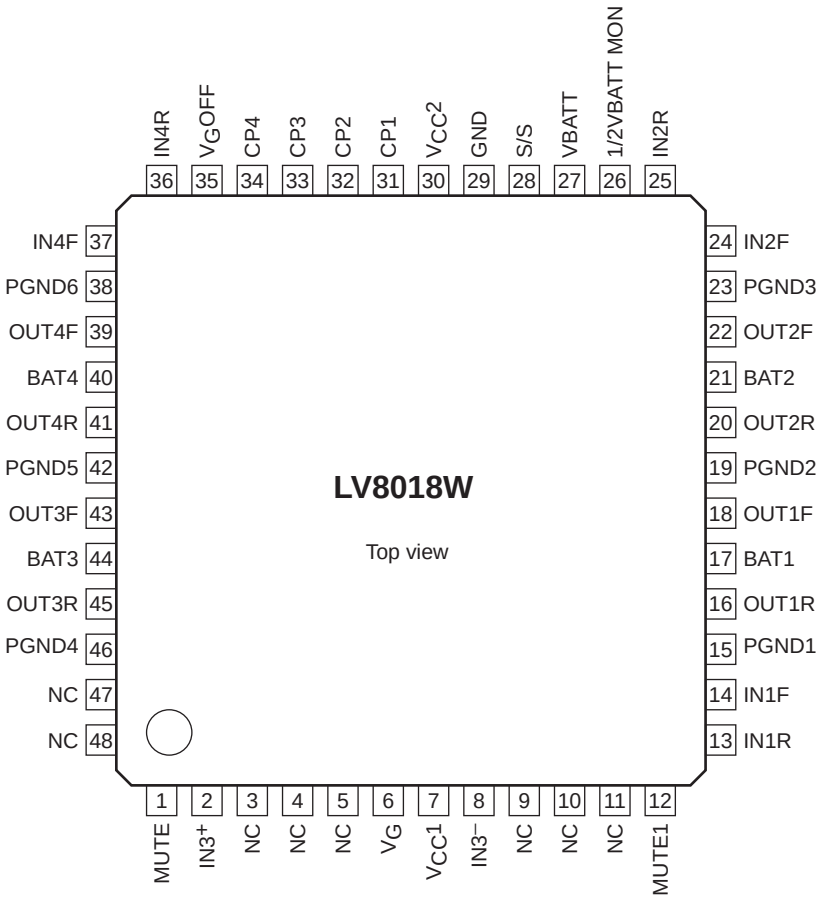
unit : mm (typ)

3163B





Pin Assignment



Truth table

Ch1, 2, 4 (for focus, tracking, and traverse)

S/S	MUTE1	IN1, 2, 4F	IN1, 2, 4R	OUT1, 2, 4F	OUT1, 2, 4R
H	H	L	L	L	L
H	H	H	L	H	L
H	H	L	H	L	H
H	H	H	H	L	L
H	L	×	×	Z	Z
L	×	×	×	Z	Z

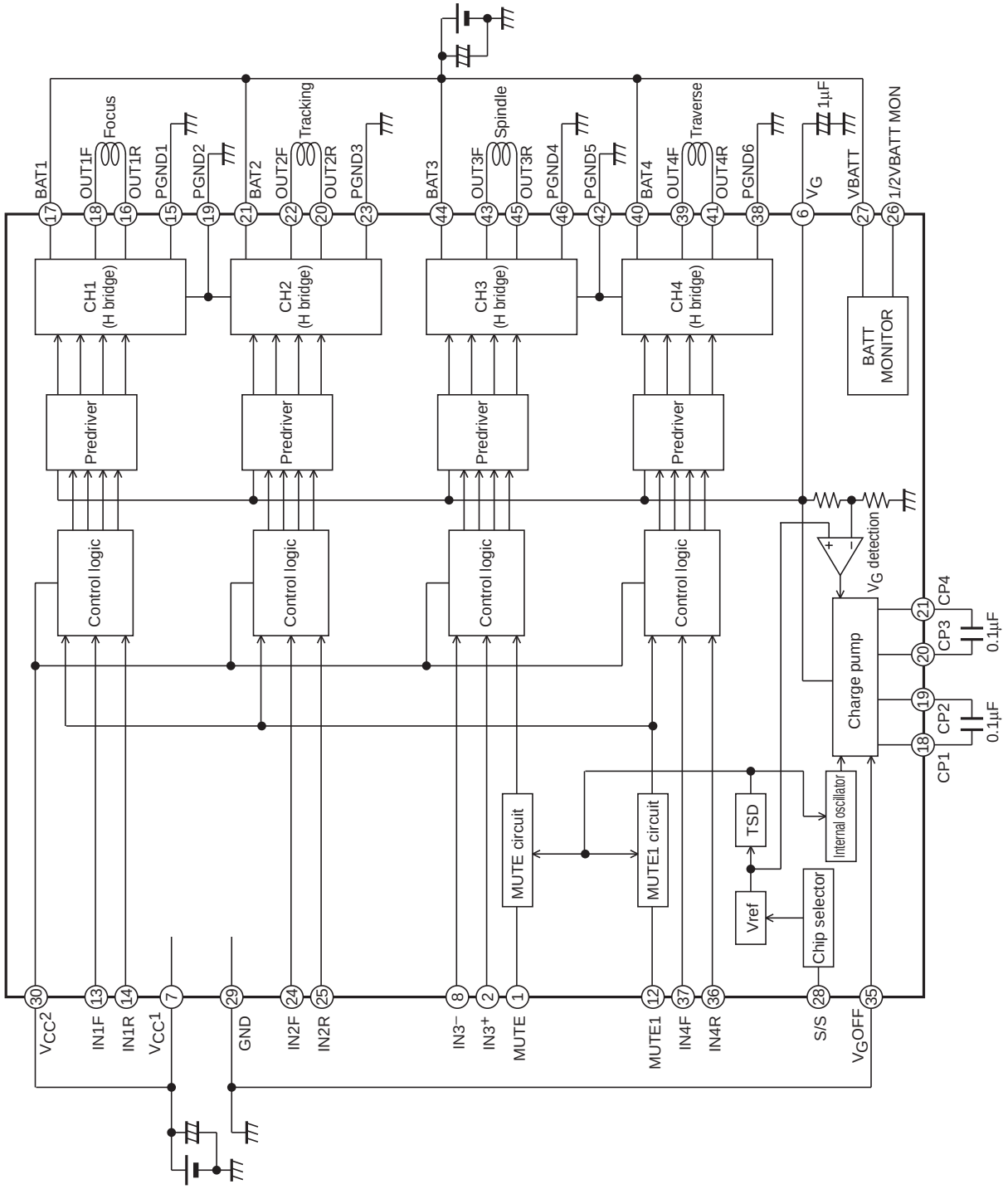
× : Don't Care, Z : Open

Ch3 (for spindle)

S/S	MUTE	IN3+	IN3-	OUT3F	OUT3R
H	H	L	L	L	L
H	H	H	L	H	L
H	H	L	H	L	L
H	H	H	H	L	H
H	L	×	×	Z	Z
L	×	×	×	Z	Z

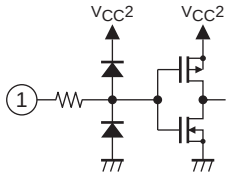
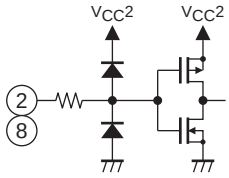
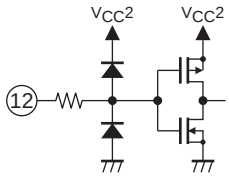
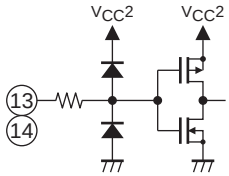
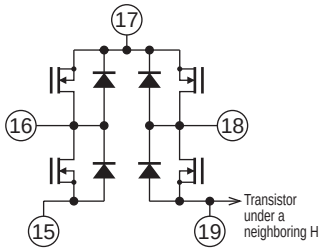
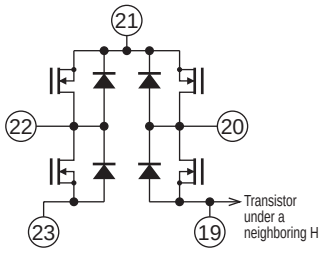
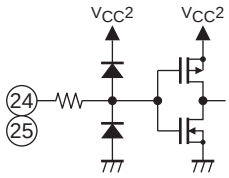
× : Don't Care, Z : Open

Block Diagram



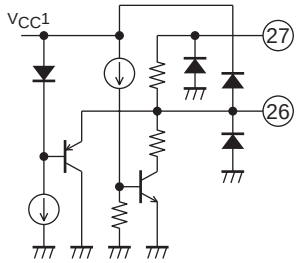
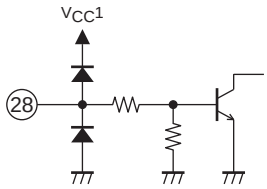
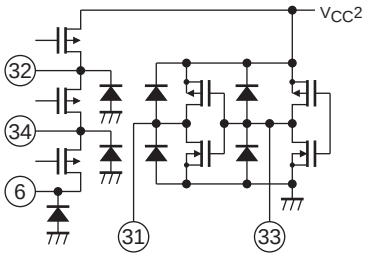
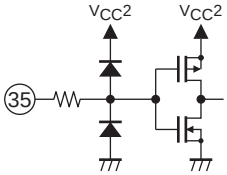
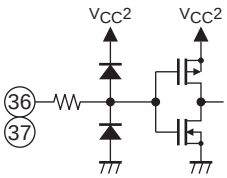
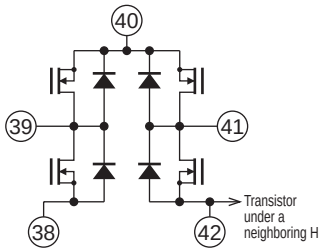
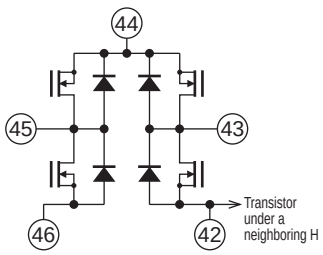
* Constants of external parts are for reference and not guaranteed

Pin Functions

Pin No.	Pin neme	Function	Equivalent Circuit
1	MUTE	Channel 3 MUTE pin. L for MUTE ON.	
2 8	$IN3^+$ $IN3^-$	Input pins, each on the forward side and reverse side of Channel 3. (Digital input)	
6	V_G	Pin to provide the supply voltage to the predrive. With V_GOFF = “L”, the output voltage of booster circuit is output to this pin. This voltage acts directly as the supply voltage of predrive.	
7	$V_{CC}1$	Pin to provide the supply voltage of analog signal system.	
12	MUTE1	MUTE pin common to Channel 1, 2, and 4. L for MUTE ON.	
14 13	IN1F IN1R	Input pins, each on the forward side and reverse sides of Channel 1. (Digital input)	
18 16 17 15 19	OUT1F OUT1R BAT1 PGND1 PGND2	OUT1F : Channel 1 forward side output pin. OUT1R : Channel 1 reverse side output pin. BAT1 : Channel 1 output power pin. PGND1, 2 : Power GND pin.	
22 20 21 23	OUT2F OUT2R BAT2 PGND3	OUT2F : Channel 2 forward side output pin. OUT2R : Channel 2 reverse side output pin. BAT2 : Channel 2 output power pin. PGND3 : Power GND pin.	
24 25	IN2F IN2R	Input pins, each on the forward side and reverse side of Channel 2. (Digital input)	

Continued on next page.

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Pin No.	Pin neme	Function	Equivalent Circuit
27 26	VBATT 1/2VBATT MON	Output power connection pin Pin to monitor 1/2 of output power supply. Used to monitor the output power supply at the digital servo and to correct the voltage dependence of servo.	
28	S/S	Start/stop pin. H for start and L for stop.	
29	GND	Signal GND pin.	
30	$V_{CC}2$	Pin to provide supply voltage of the logic signal system.	
31 32 33 34	CP1 CP2 CP3 CP4	CP1, 3 : Switching pins of booster circuit CP2, 4 : Pins to which the rectifier transistor of booster circuit is connected	
35	V_GOFF	Booster circuit ON/OFF selector pin. L for booster circuit ON H for booster circuit OFF	
37 36	IN4F IN4R	Input pins, each on the forward side and reverse side of Channel 4.	
39 41 40 42 38	OUT4F OUT4R BAT4 PGND5 PGND6	OUT4F : Channel 4 forward side output pin. OUT4R : Channel 4 reverse side output pin. BAT4 : Channel 4 output power pin. PGND5, 6 : Power GND pin.	
43 45 44 46	OUT3F OUT3R BAT3 PGND4	OUT3F : Channel 3 forward side output pin. OUT3R : Channel 3 reverse side output pin. BAT3 : Channel 3 output power pin. PGND4 : Power GND pin.	

Cautions for use

1. Apply power in the order from V_{CC} to each BAT. When the external power supply is used for V_G, apply power in the order from V_{CC}, through V_G, to each BAT. For each BAT, turn ON power supply after complete rising of V_{CC} and VG voltages.

2. Each power supply must be stabilized by inserting a capacitor to GND to prevent entry of ripple and noise.
   In particular, the capacitor of sufficient capacitance must be used for the output because the large current flows here.
   The capacitor to be inserted in each power supply should be installed as near as possible to the IC pin.

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