To :

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SPECIFICATIONS

Product Type LZ9F Series 7000 Gates Gate Array

LZ9FC23

Model No.

※This specifications contains 23 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

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- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4)Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. Introduction

This data sheet is to introduce the specification of LZ9FC23, which is designed by Mobile Liquid Crystal Display Group Sharp Corporation, Timing Control IC for TFT-LCD module.

Applicable TFT-LCD module : QVGA(Portrait/Landscape)pixel type module

Functions: Timing Control IC for TFT-LCD module

(1) By inputting Clock signal, Horizontal sync. signal, Vertical sync. signal, the following signals synchronized with above signal are generated.

(A) The signal for driving a source driver :CLK, SPL, SPR, LP, PS
(B) The signal for driving a gate driver :CLS, SPS
(C) The signal for creating the voltage which applies to common electrode. :REV
(D) The signal for creating standard voltage :REVV0

(2) Horizontal and Vertical reverse scanning function

Input/Output signal timing chart for above cases
: See Fig. 1. Fig. 2. Fig. 3. Fig. 4. Fig. 5.

2. Feature

Process	:	CMOS
Wafer substrate	:	P-type silicon substrate
Package	:	72QFP (0.5mm pin pitch)
Materials	:	Plastics
Operating Temperature	:	-30℃ ～ +85℃
Propagation delay time	:	1.0ns/gate

(Condition : 2-input NAND, Fanout=2, wire length=2mm, supply voltage=3.3V, Operating temperature Topr=25℃)

＊REMARK
Not designed or rated as radiation hardened.
You cannot rewrite the program.

3. Pin Assignments

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	IC	DCLK	37	O3M	CLK
2	ICU	SETR	38	-	GND
3	IC	R0	39	O2M	OB5
4	IC	R1	40	O2M	OB4
5	IC	R2	41	O2M	OB3
6	IC	R3	42	O2M	OB2
7	IC	R4	43	O2M	OB1
8	IC	R5	44	O2M	OB0
9	-	GND	45	-	V_{DD}
10	ICU	SDRSEL	46	-	GND
11	IC	G0	47	O2M	OG5
12	IC	G1	48	O2M	OG4
13	IC	G2	49	O2M	OG3
14	IC	G3	50	O2M	OG2
15	IC	G4	51	O2M	OG1
16	IC	G5	52	O2M	OG0
17	ICU	TEST	53	-	GND
18	IC	B0	54	O2M	OR5
19	IC	B1	55	O2M	OR4
20	IC	B2	56	O2M	OR3
21	IC	B3	57	O2M	OR2
22	IC	B4	58	O2M	OR1
23	IC	B5	59	O2M	OR0
24	ICU	TEST	60	-	GND
25	ICU	HREV	61	TO2M	CLS
26	ICD	ENAB	62	TO2M	SPS
27	-	V_{DD}	63	-	V_{DD}
28	-	GND	64	-	GND
29	ICU	TEST	65	TO2M	UBL
30	O2M	REV	66	ICU	VREV
31	O2M	REVV0	67	IC	TEST
32	O2M	PS	68	IC	SIZEC0
33	TO2M	SPR	69	O2M	MOD
34	O2M	LBR	70	ICU	REM
35	TO2M	SPL	71	IC	HS
36	O2M	LP	72	IC	VS

IC :Input buffer CMOS level

ICU :Input buffer CMOS level with PULL UP resistance (R=300kΩ)

ICD :Input buffer CMOS level with PULL DOWN resistance (R=300kΩ)

O2M :Output buffer (I_{OL}=0.8mA)

O3M :Output buffer (I_{OL}=1.2mA)

TO2M :Tri-state Output buffer (I_{OL}=0.8mA)

V_{DD} :Power supply pin

GND :Earth pin

4. Function of Input/Output signal

Pin No.	Signal Name	Explanation	I/O
1	DCLK	Input terminal for data clock signal	I
2	SETR	Input terminal for control signal for PS(Effective only in SIZECO="L") SETR="H" :PS signal serves as operation for specific models. SETR="L" :PS signal is normal operation.	I
3	R0	Input terminal for red data signal (LSB)	I
4	R1	Input terminal for red data signal	I
5	R2	Input terminal for red data signal	I
6	R3	Input terminal for red data signal	I
7	R4	Input terminal for red data signal	I
8	R5	Input terminal for red data signal (MSB)	I
9	GND	Ground	-
10	SDRSEL	Input terminal for control signal for CLK and DATA output timing SDRSEL="H" :Normal (Effective only in SIZECO="L") SDRSEL="L" :4clk delay mode	I
11	G0	Input terminal for green data signal (LSB)	I
12	G1	Input terminal for green data signal	I
13	G2	Input terminal for green data signal	I
14	G3	Input terminal for green data signal	I
15	G4	Input terminal for green data signal	I
16	G5	Input terminal for green data signal (MSB)	I
17	TEST	Input terminal for test mode (Connect this terminal to "H")	I
18	B0	Input terminal for blue data signal (LSB)	I
19	B1	Input terminal for blue data signal	I
20	B2	Input terminal for blue data signal	I
21	B3	Input terminal for blue data signal	I
22	B4	Input terminal for blue data signal	I
23	B5	Input terminal for blue data signal (MSB)	I
24	TEST	Input terminal for test mode (Connect this terminal to "H")	I
25	HREV	Input terminal for setting up horizontal scan direction HREV="H" :Normal scan HREV="L" :Horizontal reversal scan	I
26	ENAB	Input terminal for signal to settle the Horizontal display position	I
27	V_{DD}	Input terminal for Power Supply voltage	-
28	GND	Ground	-
29	TEST	Input terminal for test mode (Connect this terminal to "H")	I
30	REV	Signal output for common electrode preparation	O
31	REVV0	Signal output for standard voltage preparation	O
32	PS	Control signal output for source driver	O
33	SPR	Start signal output for source driver When HREV="H" :SPR output is High impedance. When HREV="L" :SPR output is valid.	O
34	LBR	Output signal for source driver for setting up Horizontal scan direction When HREV="H",LBR="H"output. When HREV="L",LBR="L"output.	O
35	SPL	Start signal output for source driver When HREV="H" :SPL outout is valid. When HREV="L" :SPL outout is High impedance.	O
36	LP	Data transferring signal output for source driver	O

Pin No.	Signal Name	Explanation	I/O
37	CLK	Clock signal output for source driver	O
38	GND	Ground	–
39	OB5	Blue data signal output for source driver (MSB)	O
40	OB4	Blue data signal output for source driver	O
41	OB3	Blue data signal output for source driver	O
42	OB2	Blue data signal output for source driver	O
43	OB1	Blue data signal output for source driver	O
44	OB0	Blue data signal output for source driver (LSB)	O
45	V_{DD}	Power Supply voltage	–
46	GND	Ground	–
47	OG5	Green data signal output for source driver (MSB)	O
48	OG4	Green data signal output for source driver	O
49	OG3	Green data signal output for source driver	O
50	OG2	Green data signal output for source driver	O
51	OG1	Green data signal output for source driver	O
52	OG0	Green data signal output for source driver (LSB)	O
53	GND	Ground	–
54	OR5	Red data signal output for source driver (MSB)	O
55	OR4	Red data signal output for source driver	O
56	OR3	Red data signal output for source driver	O
57	OR2	Red data signal output for source driver	O
58	OR1	Red data signal output for source driver	O
59	OR0	Red data signal output for source driver (LSB)	O
60	GND	Ground	–
61	CLS	Clock signal output for source driver	O
62	SPS	Start signal output for gate driver	O
63	V_{DD}	Power Supply voltage	–
64	GND	Ground	–
65	UBL	Output signal for gate driver for setting up Vertical scan direction When VREV="H", UBL="H"output When VREV="L", UBL="L"output	O
66	VREV	Input terminal for setting up vertical scan direction VREV="H" :Normal scan VREV="L" :Vertical reversal scan	I
67	TEST	Input terminal for test mode (Connect this terminal to "L")	I
68	SIZEC0	Input terminal for setting up display resolution SIZEC0="H" :Portrait QVGA(240RGB×320) SIZEC0="L" :Landscape QVGA(320RGB×240)	I
69	MOD	Output signal for gate driver	O
70	REM	Input terminal for reset signal (Give the signal that becomes H level fixation from the L level at the time of the power supply input.)	I
71	HS	Input terminal for Horizontal sync. signal	I
72	VS	Input terminal for Vertical sync. signal	I

5. Absolute Maximum Ratings

Parameter	Symbol	Rating			Unit
Supply voltage	V_{DD}	−0.3	～	+6.0	V
Input voltage	V_I	−0.3	～	V_{DD}+0.3	V
Output voltage	V_O	−0.3	～	V_{DD}+0.3	V
Operating temperature	Topr	−30	～	+85	℃
Storage temperature	Tstg	−55	～	+150	℃

6. Electrical Specifications

6-1. Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	+2.7	+3.3	+3.6	V
Operating temperature	Topr	-30		+85	℃

6-2. Electrical Characteristics

(V_{DD}=+2.7～+3.6V, Topr=-30～+85℃)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit	#
Input"Low" voltage	V_{IL}				0.3×V_{DD}	V	
Input"High"voltage	V_{IH}		0.7×V_{DD}			V	1
Input"High"current	$\lvert I_{IH1} \rvert$	$V_I = V_{DD}$			1.0	μA	
Input"Low" current	$\lvert I_{IL1} \rvert$	V_I= 0 V			1.0	μA	2
Input"High"current	$\lvert I_{IH2} \rvert$	$V_I = V_{DD}$			1.0	μA	
Input"Low" current	$\lvert I_{IL2} \rvert$	V_I= 0 V	2.0		36.0	μA	3
Input"High"current	$\lvert I_{IH3} \rvert$	$V_I = V_{DD}$	2.0		36.0	μA	
Input"Low" current	$\lvert I_{IL3} \rvert$	V_I= 0 V			1.0	μA	4
Output"Low" voltage	V_{OL1}	I_{OL}= 0.8mA			0.4	V	
Output"High"voltage	V_{OH1}	I_{OH}=−0.4mA	V_{DD}-0.5			V	5
Output"Low" voltage	V_{OL2}	I_{OL}= 1.2mA			0.4	V	
Output"High"voltage	V_{OH2}	I_{OH}=−0.6mA	V_{DD}-0.5			V	6
Output Leakage Current	$\lvert I_{OZ} \rvert$	High-impedance state			1.0	μA	7

#1: Applied to Input pins (IC, ICU, ICD).
#2: Applied to Input pins (IC).
#3: Applied to Input pins (ICU).
#4: Applied to Input pin (ICD).
#5: Applied to Output pins (O2M, TO2M).
#6: Applied to Output pin (O3M).
#7: Applied to Output pins (TO2M).

7. Timing Characteristics of Input/Output Signals

Input Timing Characteristics

(1) Portrait QVGA (240RGBx320):SIZECO="H"

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	f_{DCLK}	4.5		6.8	MHz
HS frequency	f_{HS}	$f_{DCLK}/330$		$f_{DCLK}/254$	kHz
		15		26	kHz
VS frequency	f_{VS}	$f_{HS}/440$		$f_{HS}/332$	Hz
		50		80	Hz

(2) Landscape QVGA (320RGBx240):SIZECO="L"

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	f_{DCLK}	4.5		6.8	MHz
HS frequency	f_{HS}	$f_{DCLK}/440$		$f_{DCLK}/334$	kHz
		12.5		20	kHz
VS frequency	f_{VS}	$f_{HS}/330$		$f_{HS}/248$	Hz
		50		82	Hz

8. Input/Output signal timing chart for above cases

Horizontal Timing Portrait Type QVGA (240RGB × 320) (SIZEC0 = "H", ENAB : Valid)

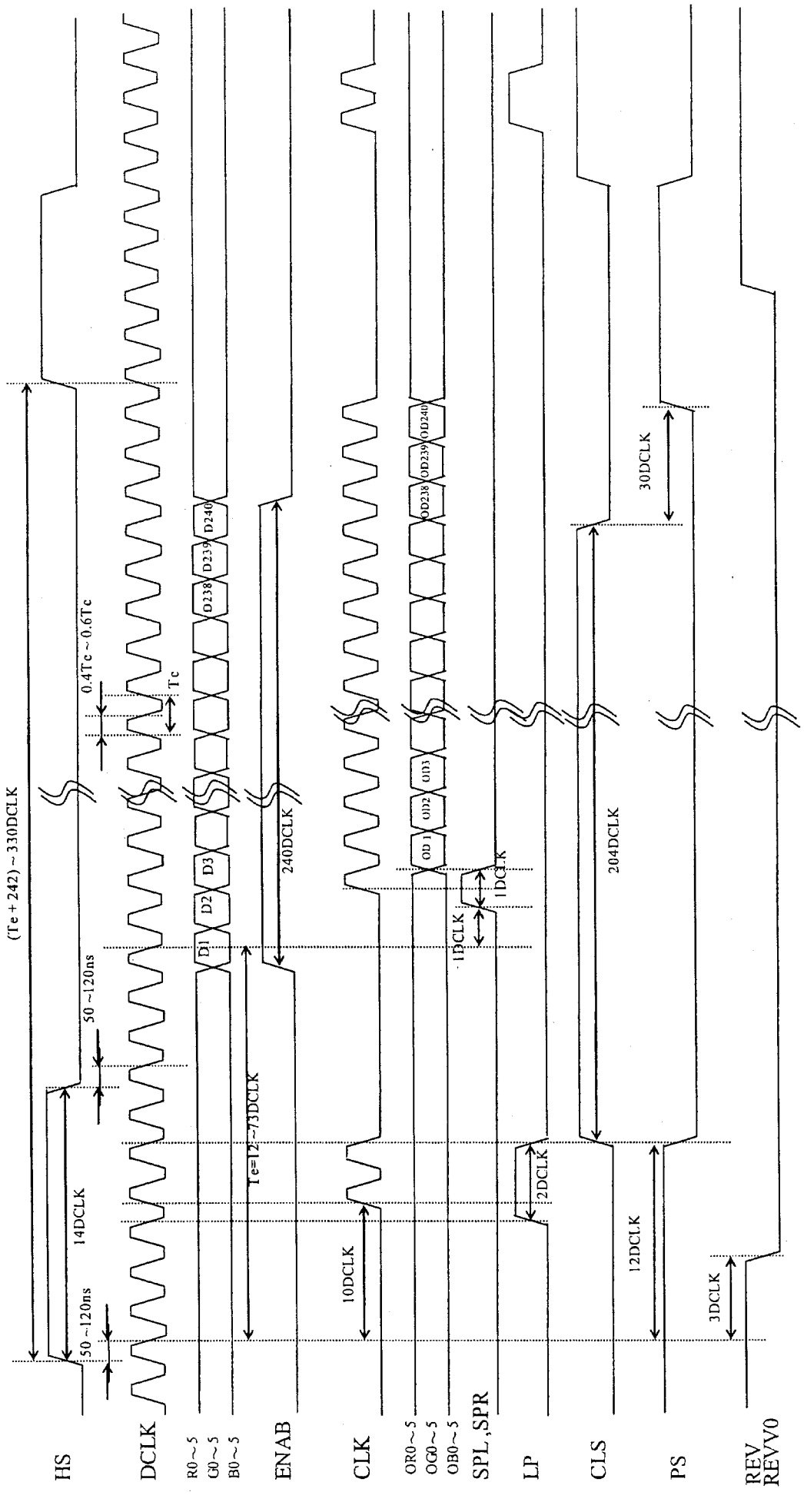


Fig. 1

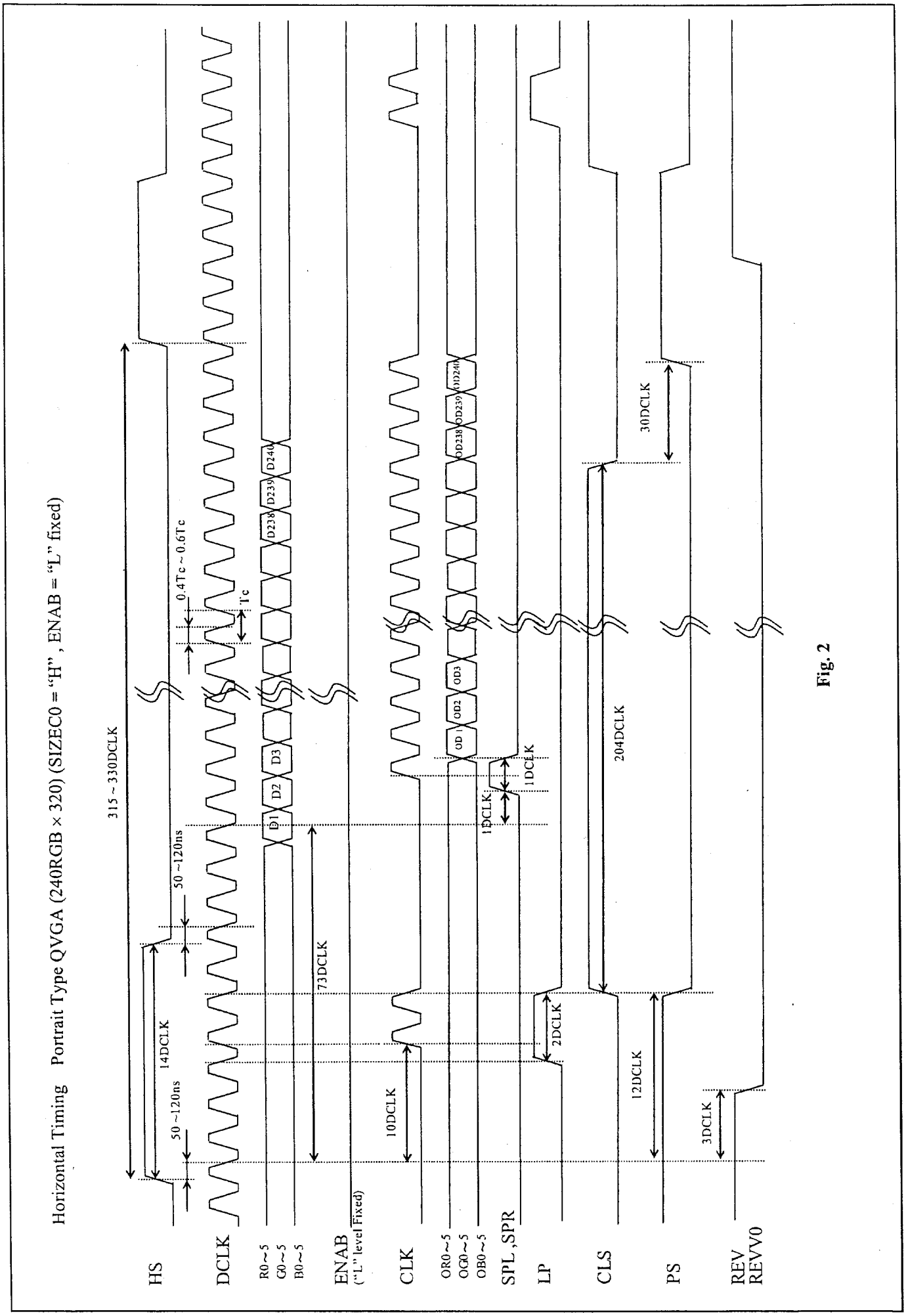

Horizontal Timing Portrait Type QVGA (240RGB × 320) (SIZEC0 = "H" , ENAB = "L" fixed)
315 ~ 330DCLK
14DCLK
50 ~120ns
50 ~120ns
0.4Tc ~ 0.6Tc
Tc
73DCLK
HS
DCLK
R0~5
G0~5
B0~5
D1
D2
D3
D238
D239
D240
ENAB
("L" level Fixed)
10DCLK
CLK
OR0~5
OG0~5
OB0~5
OD 1
OD2
OD3
OD238
OD239
OD240
1DCLK
1DCLK
SPL ,SPR
2DCLK
LP
204DCLK
CLS
30DCLK
12DCLK
PS
3DCLK
REV
REVV0

Fig. 2

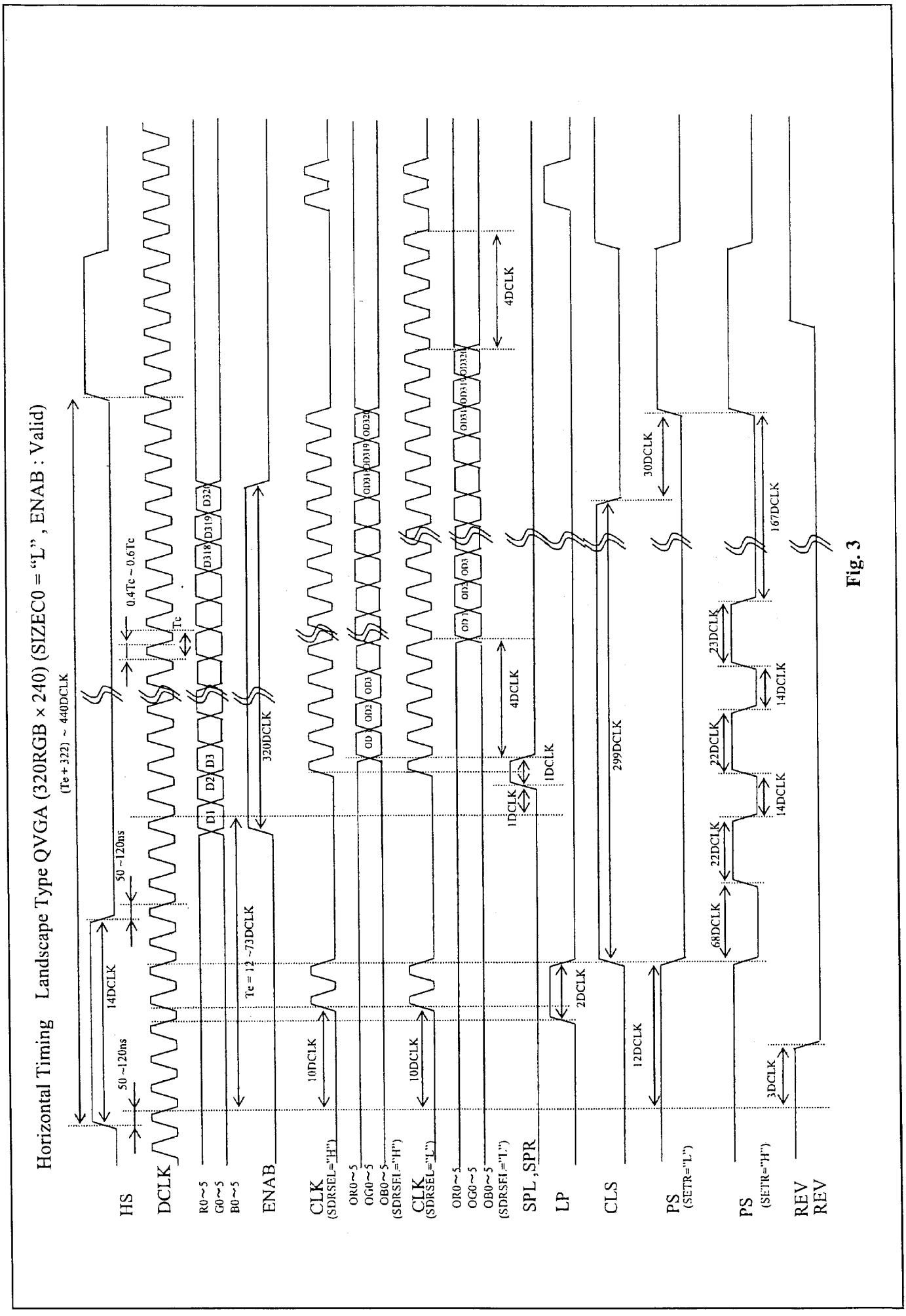

Horizontal Timing Landscape Type QVGA (320RGB × 240) (SIZEC0 = "L", ENAB : Valid)
(Te + 322) ~ 440DCLK
HS
DCLK
R0~5
G0~5
B0~5
ENAB
CLK
(SDRSEL="H")
OR0~5
OG0~5
OB0~5
(SDRSFI="H")
CLK
(SDRSEL="L")
OR0~5
OG0~5
OB0~5
(SDRSFI="L")
SPL, SPR
LP
CLS
PS
(SETR="L")
PS
(SETR="H")
REV
REV
14DCLK
50~120ns
50~120ns
0.4Tc~0.6Tc
Tc
Te = 12~73DCLK
320DCLK
10DCLK
10DCLK
1DCLK
1DCLK
4DCLK
4DCLK
2DCLK
299DCLK
12DCLK
30DCLK
68DCLK
22DCLK
22DCLK
14DCLK
14DCLK
23DCLK
167DCLK
3DCLK
D1
D2
D3
D318
D319
D320
OD1
OD2
OD3
OD318
OD319
OD320
OD321

Fig. 3

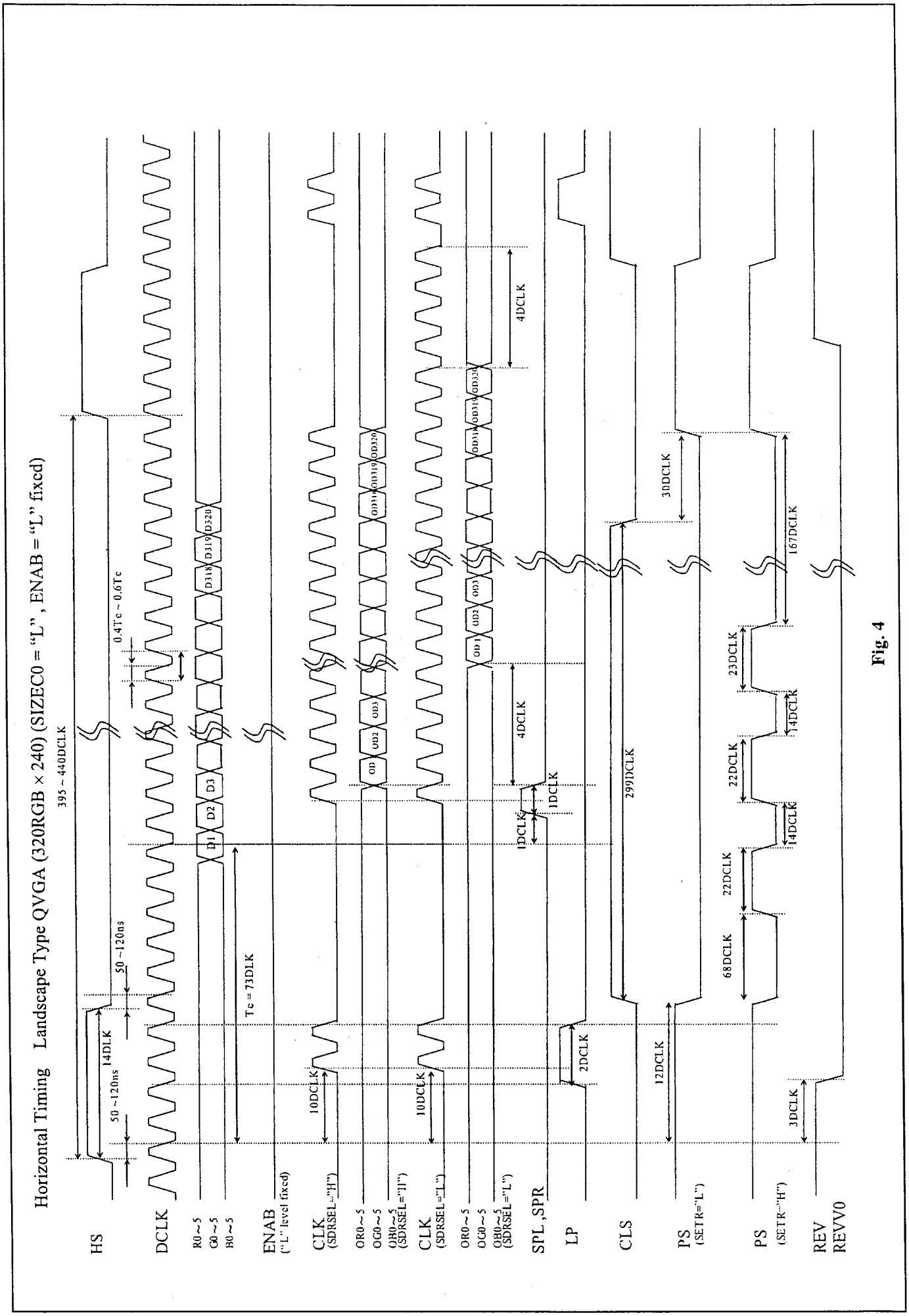

Horizontal Timing Landscape Type QVGA (320RGB × 240) (SIZEC0 = "L" , ENAB = "L" fixed)
395 ~ 440DCLK
HS
14DLK
50 ~ 120ns
50 ~ 120ns
0.47Tc ~ 0.6Tc
DCLK
R0~5
G0~5
B0~5
D1
D2
D3
D318
D319
D320
Tc = 73DLK
ENAB
("L" level fixed)
CLK
(SDRSEL="H")
10DCLK
OR0~5
OG0~5
OB0~5
(SDRSEL="H")
OD
OD1
OD2
OD3
OD318
OD319
OD320
CLK
(SDRSEL="L")
10DCLK
OR0~5
OG0~5
OB0~5
(SDRSEL="L")
OD1
OD2
OD3
OD318
OD319
OD320
4DCLK
SPL, SPR
1DCLK
1DCLK
4DCLK
LP
2DCLK
CLS
299IDCLK
12DCLK
30DCLK
PS
(SETR="L")
68DCLK
22DCLK
22DCLK
23DCLK
PS
(SETR="H")
14DCLK
14DCLK
167DCLK
REV
REVV0
3DCLK

Fig. 4

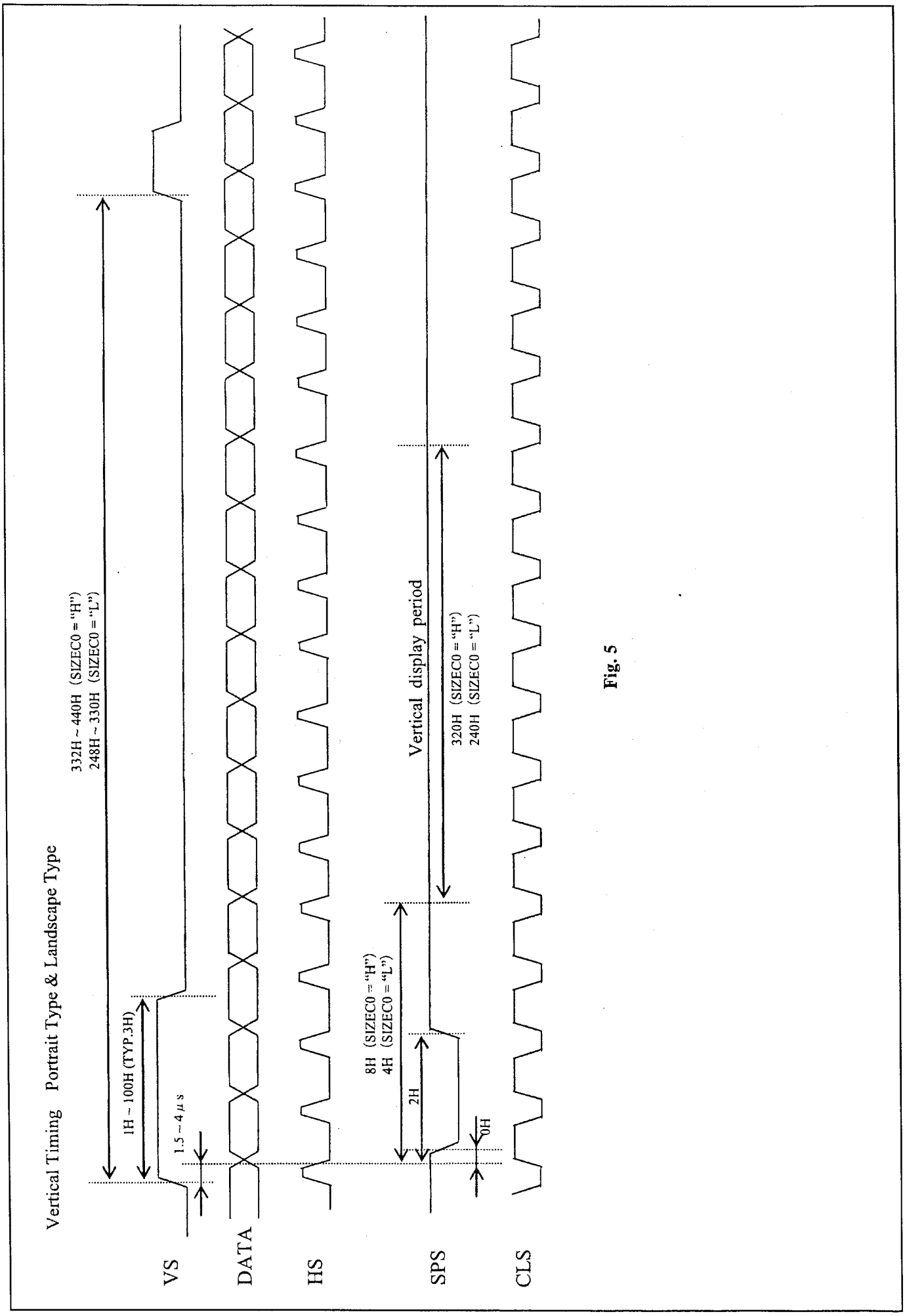

Vertical Timing Portrait Type & Landscape Type
332H ~ 440H (SIZEC0 = "H")
248H ~ 330H (SIZEC0 = "L")
1H ~ 100H (TYP.3H)
1.5 ~ 4 μ s
VS
DATA
HS
8H (SIZEC0 = "H")
4H (SIZEC0 = "L")
2H
0H
Vertical display period
320H (SIZEC0 = "H")
240H (SIZEC0 = "L")
SPS
CLS

Fig. 5

9 Package and packing specification

[Applicability]

This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80%(Relative humidity) max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1, or Manual soldering.)

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 168 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

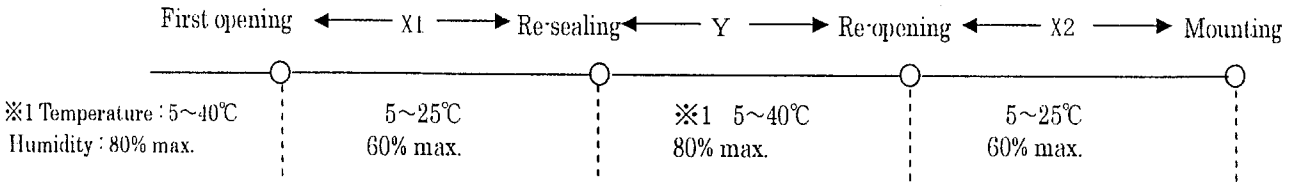
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1＋X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
  (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period :
  120℃ for 16～24 hours.
- The above baking conditions apply since the trays are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

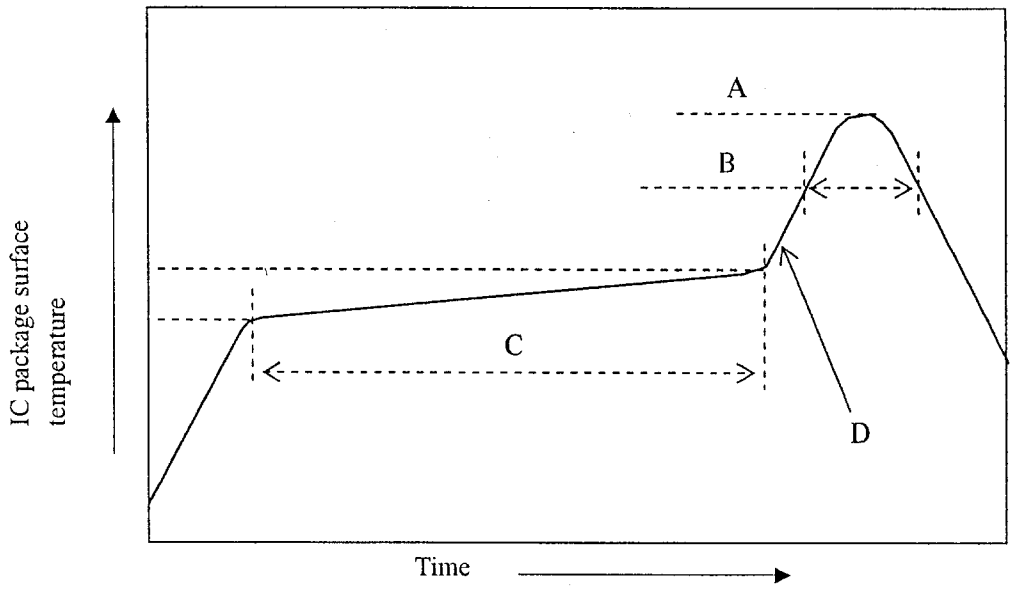
3. Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1.Soldering.

(1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  - A) Peak temperature. 250℃ max.
  - B) Heating temperature. 40 to 60 seconds as 220℃
  - C) Preheat temperature. It is 150 to 200℃, and is 120±30 seconds
  - D) Temperature increase rate. It is 1 to 3℃/seconds
- Measuring point : IC package surface.
- Temperature profile:



(2) Manual soldering (soldering iron) (one-time soldering only)
Soldering iron should only touch the IC's outer leads.
- Temperature and period :
  350℃ max. for 3 seconds / pin max.
  (Soldering iron should only touch the IC's outer leads.)
- Measuring point : Soldering iron tip.

4. Condition for removal of residual flux.
(1) Ultrasonic washing power : 25 watts / liter max.
(2) Washing time : Total 1 minute max.
(3) Solvent temperature : 15～40℃

5. Package outline specification.
Refer to the attached drawing.
(Plastic body dimensions do not include burr of resin.)
The contents of LEAD-FREE TYPE application of the specifications. (*2)

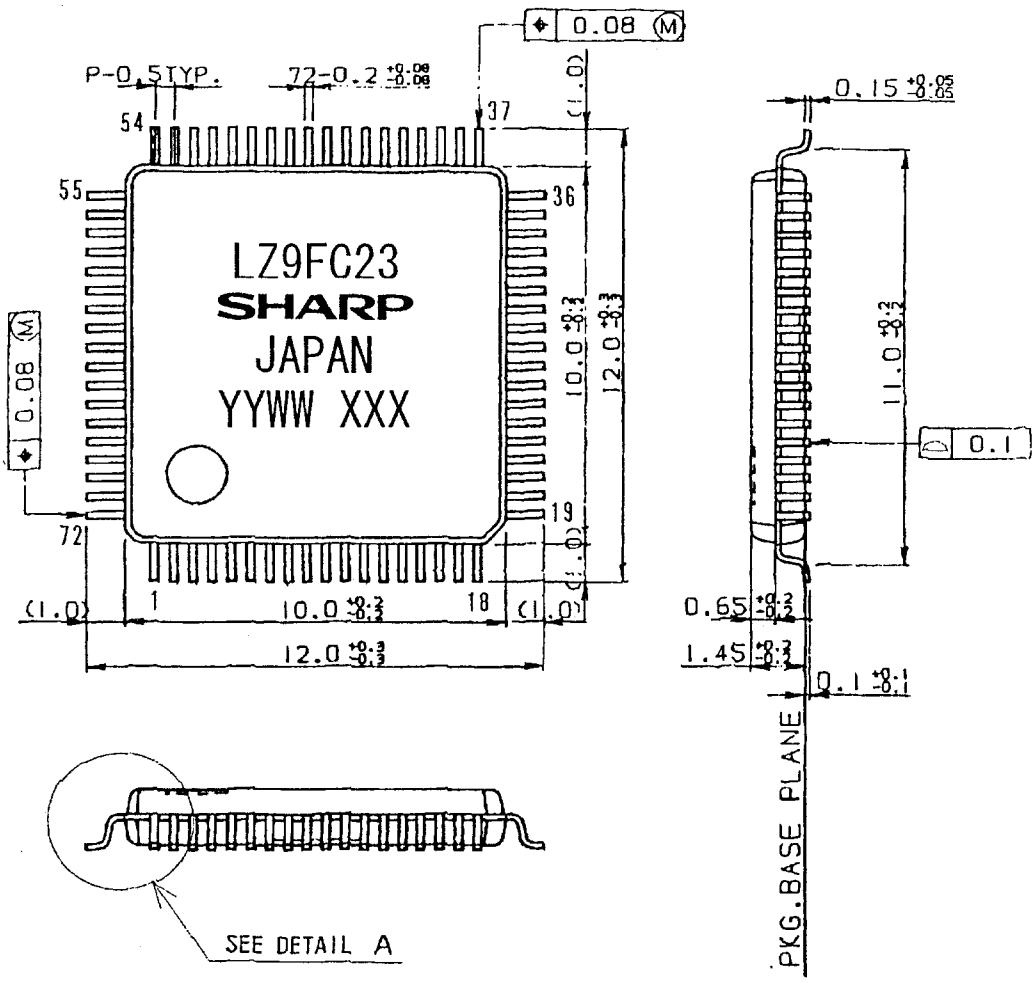
6. Markings.
6-1.Marking details. (The information on the package should be given as follows.)
(1) Product name : LZ9FC23
(2) Company name : SHARP
(3) Date code : (Example) YYWW XXX
YY → Denotes the production year. (Last two digits of the year.)
WW → Denotes the production week. (01・02・～・52・53)
XXX → Denotes the production ref. code (1～3 digits).
(4) "JAPAN" indicates the country of origin.

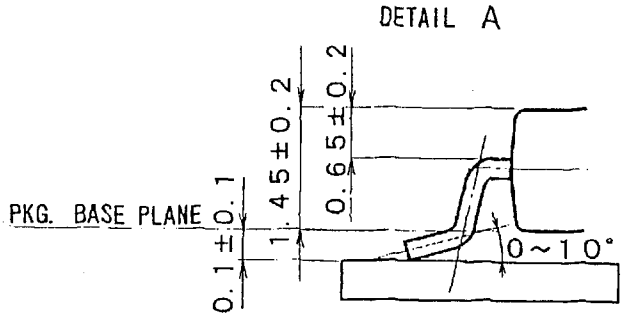
6-2.Marking layout.
The layout is shown in the attached drawing.
(However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Bi)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note)It is those with an underline printing in a date code because of a LEAD-FREE type.





QFP072-P-1010-AA1034

LEAD TYPE	LEAD FINISH	LEAD MATERIAL
	Sn-Bi PLATING	42Alloy

NAME	QFP072-P-1010			NOTE : Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1034	UNIT	mm	

7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (800 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (80 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (3200 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

Refer to the attached drawing.

7-3.Outline dimension of carton.

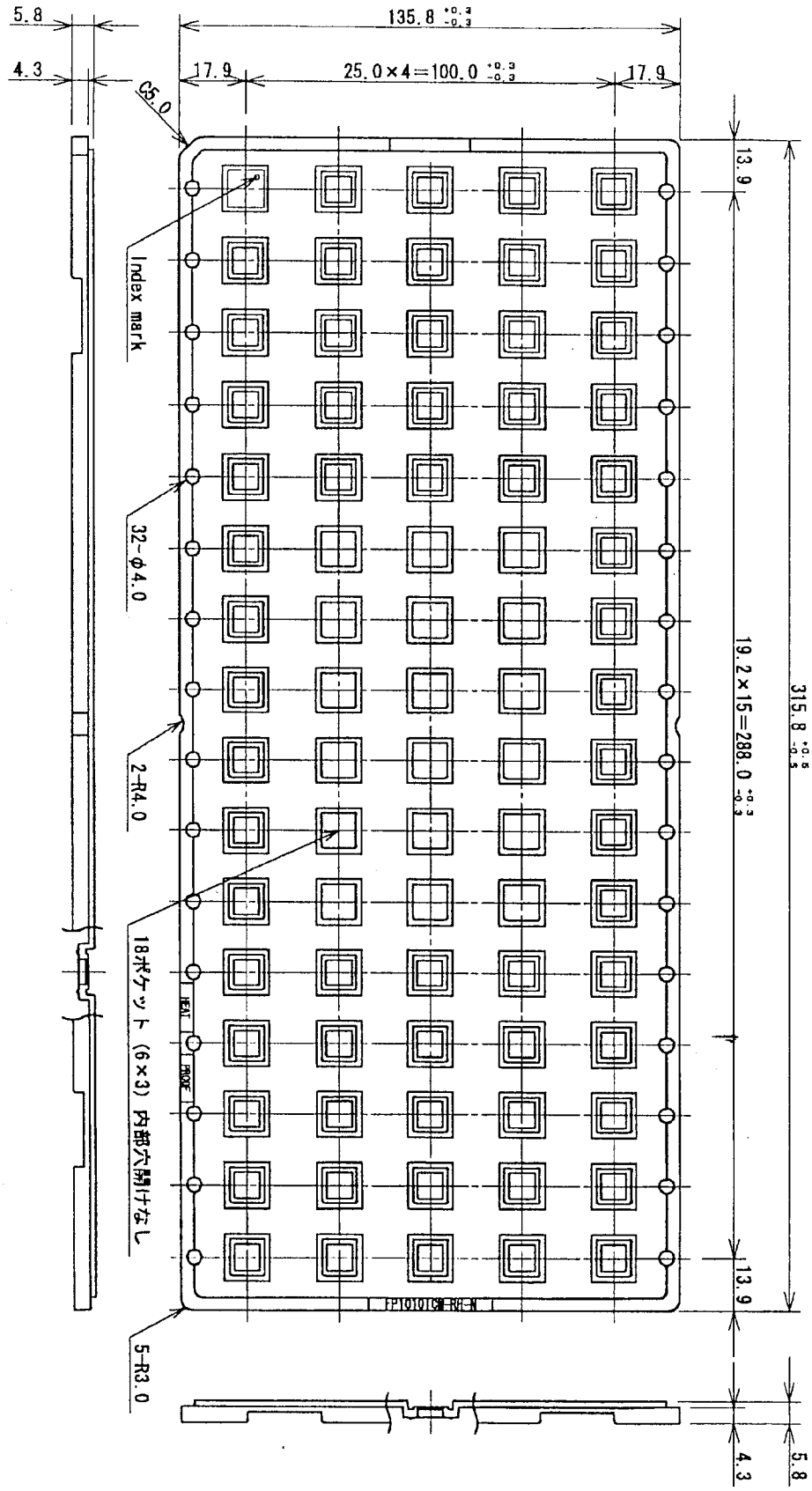
Refer to the attached drawing.

8. Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.

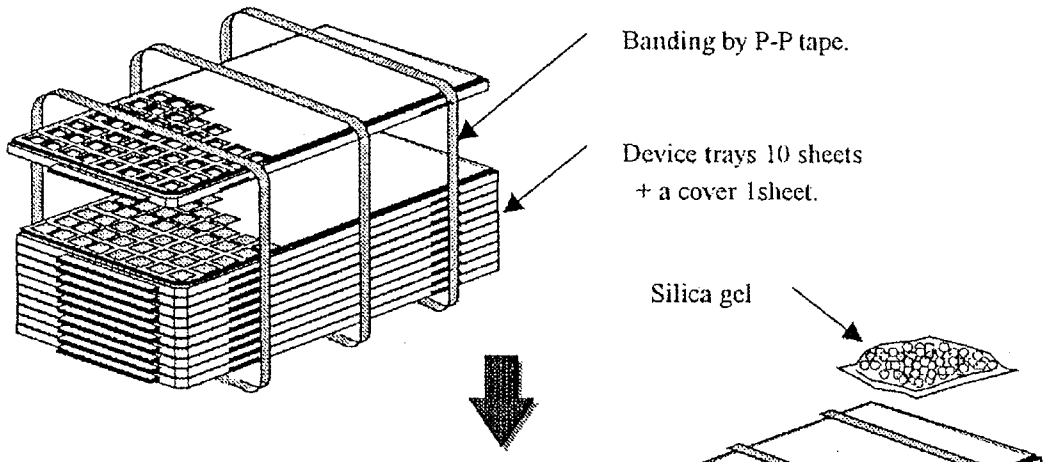
(3) The devices should be mounted within one year of the date of delivery.



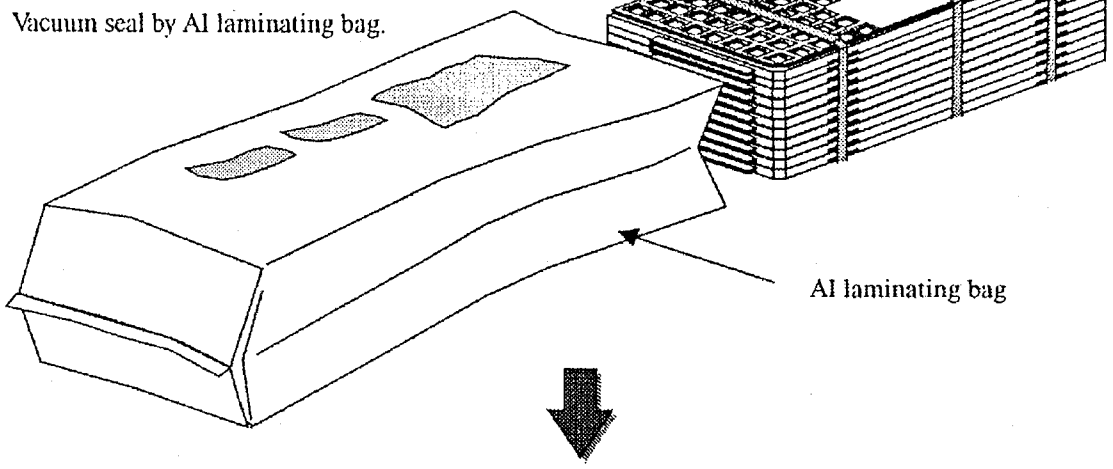
名称 NAME	FP1010TCM-RH-N	備考 NOTE
DRAWING NO. CV830	単位 UNIT mm	

20040930

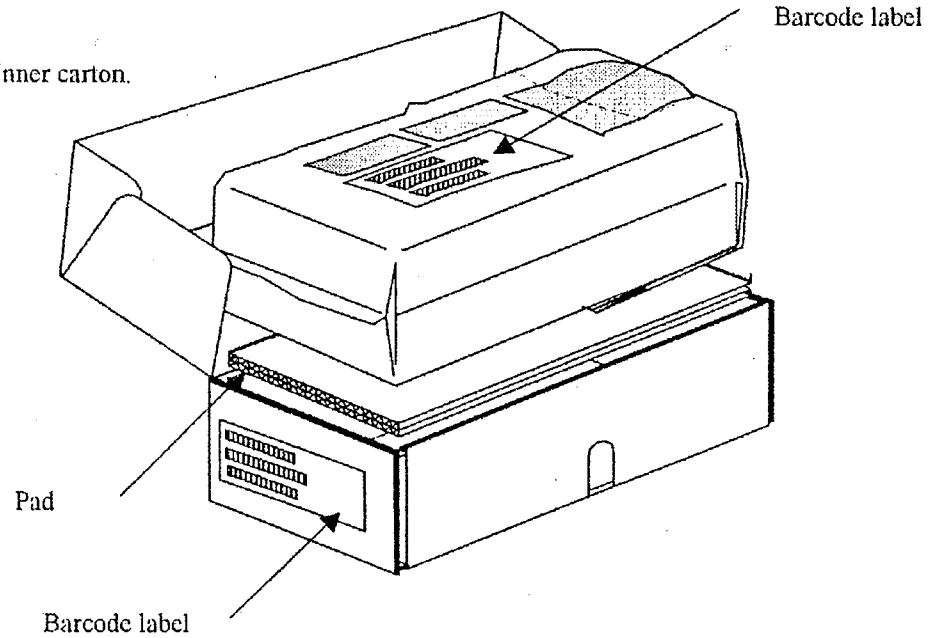
(1) Banding device tray together.



(2) Vacuum seal by Al laminating bag.



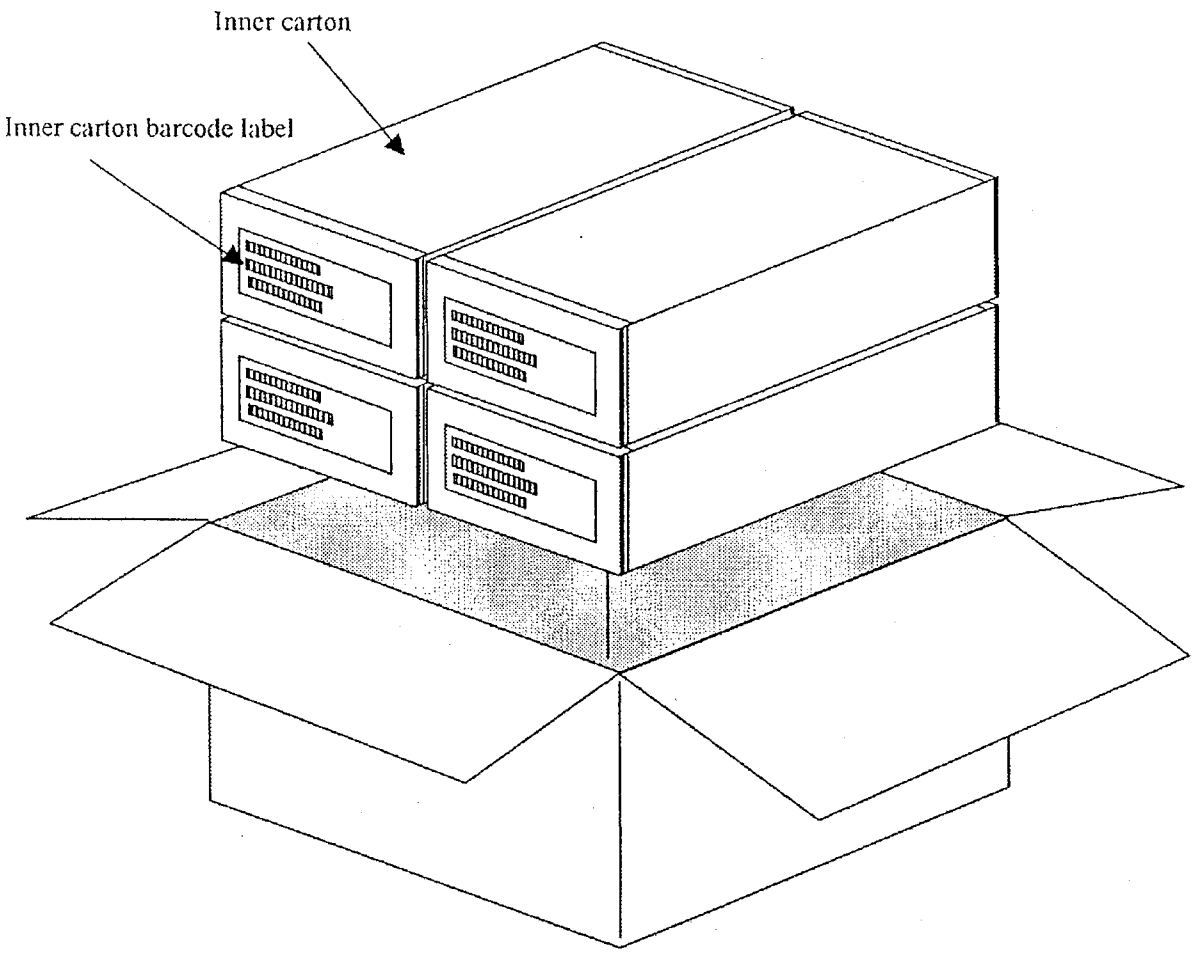
(3) Packing by Inner carton.

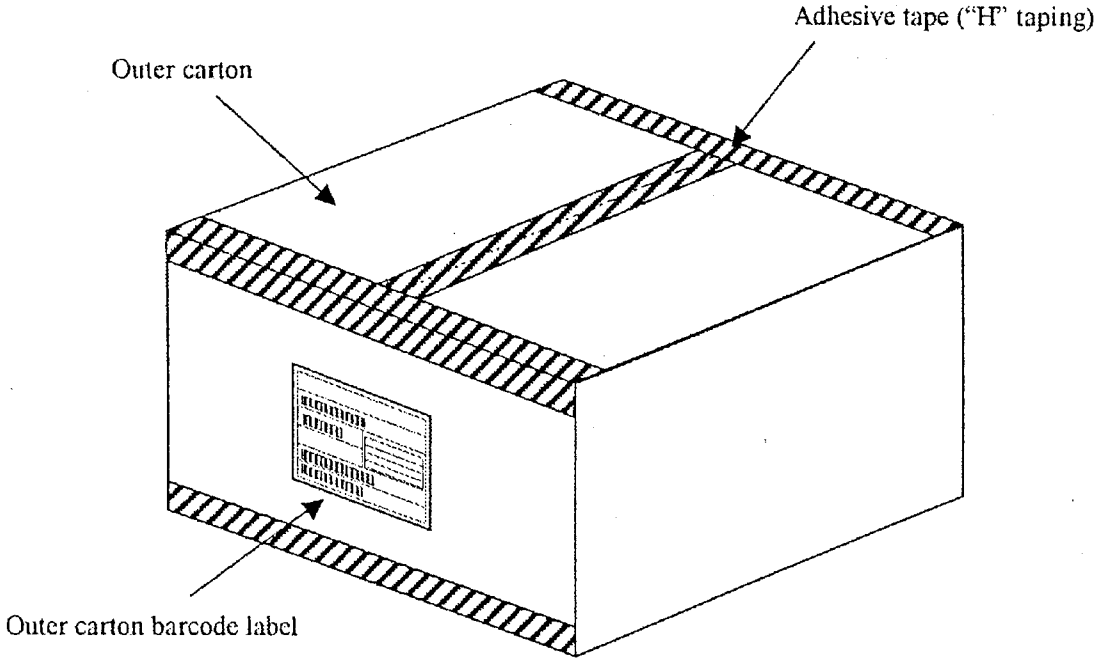


NAME	Packing specifications		
DRAWING NO.	BJ433c	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.

20040930





L × W× H

Inner carton - Outer dimensions : 360×150×95

Outer carton - Outer dimensions : 390×335×230

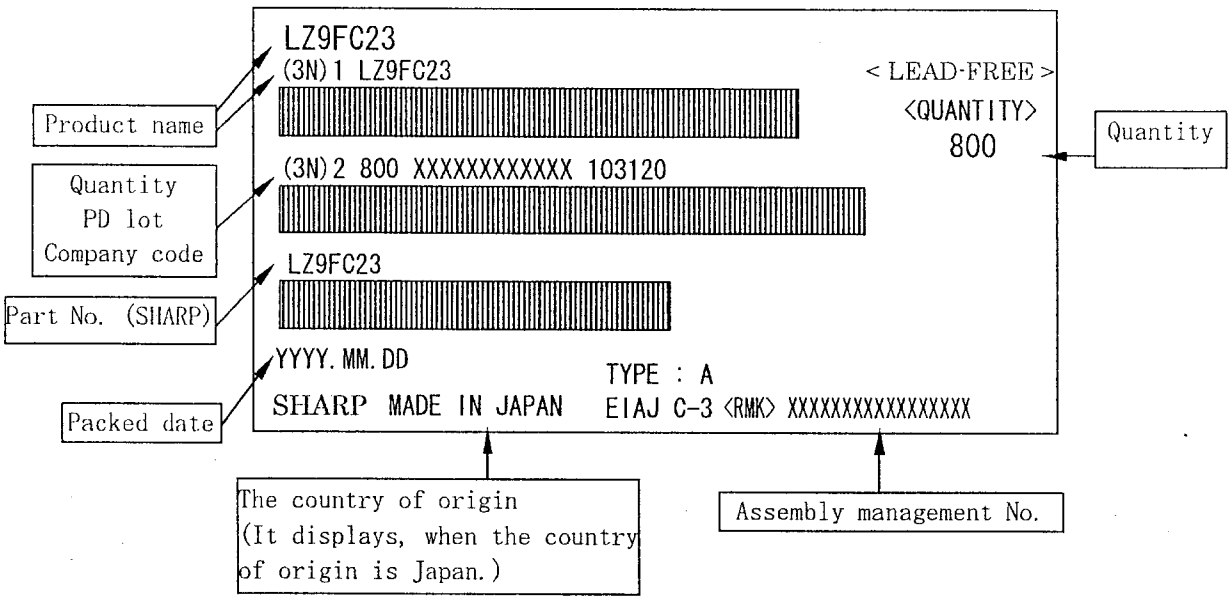
NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.

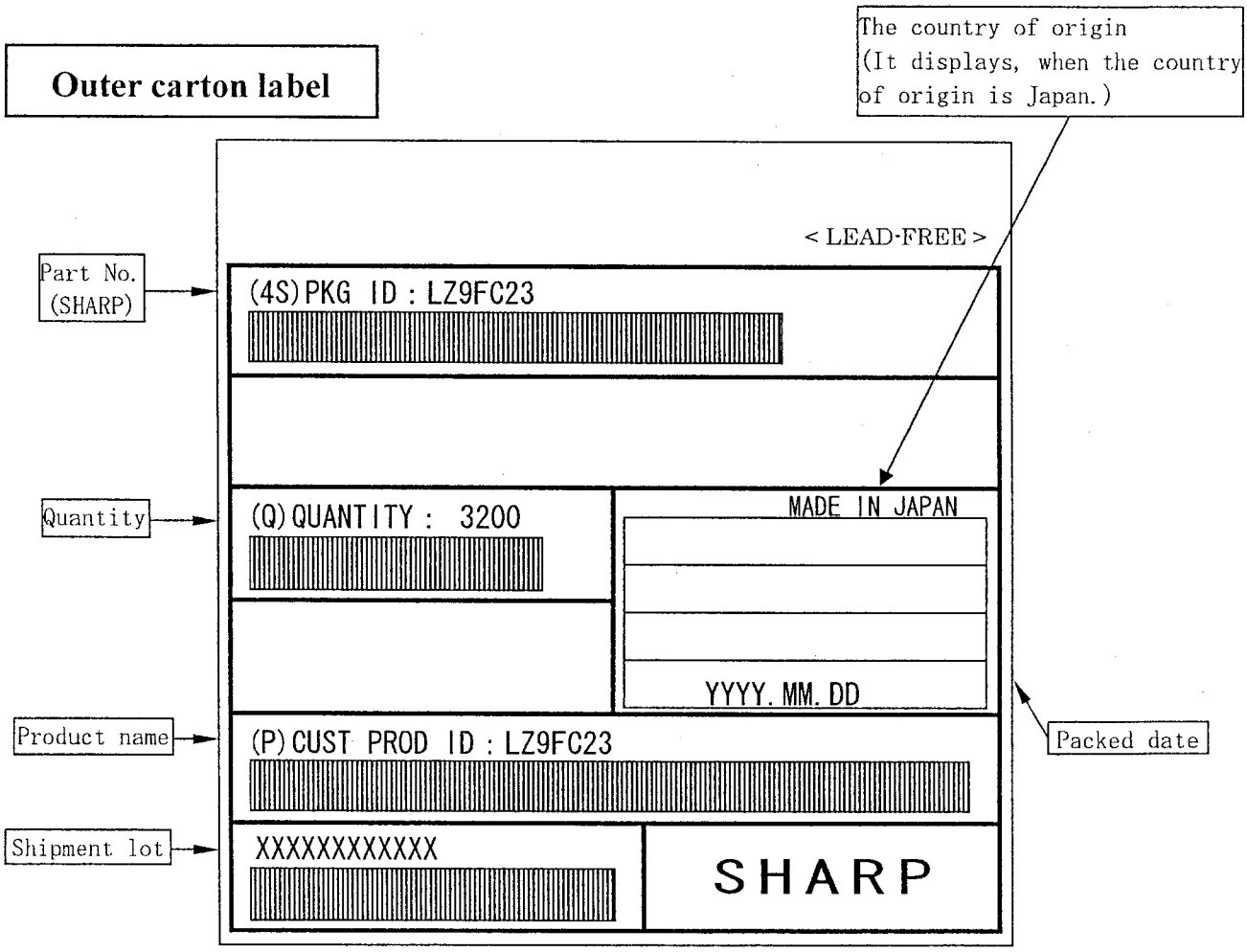
20040930

(Note) The <LEAD-FREE> display shows a lead-free article.

Inner carton label



Outer carton label



(Former) EIAJ B Standard conforming