

Silicon Motion, Inc.

Mobile Computer Display Controller

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LynxEM+ DataBook

Silicon Motion®, Inc.

LynxEM+ DataBook

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Version Number	Date	Note
0.1	9/30/99	• All registers are the same as the LynxEM with the exception of the following: CCR62 bit 7:6, and MCR62 bit 7, bit 6, bit 2
0.2	11/12/99	• Figure 2 Pin Diagram updated • Table 1: Pin Description - Updated • Table 2: SM712 Pin Diagram for 256 BGA Package - Updated
0.3	12/20/99	• Add VCLK table to register CCR6D
0.4	02/16/99	• Updates to Pin Description table and Power-on configuration table
0.5	05/23/00	• Change to Pin Description Table (VCC & Ground Pins) delete 5V reference from FPVDD • Delete 5V reference to I2C Bus or VESA DDC2B Interface
0.6	12/07/00	• Added 4Mbyte internal memory configuration • Minor corrections based on field input. • Change M4 in pin diagram to VCC.
0.7	3/31/01	• Changed M4 and K1 in Pin List • Added ordering information table
0.8	6/27/01	• Changed ICC Digital DC Specification and operating power dissipation • Revised block diagram
0.9	10/18/01	• Changed DC Specification MCLK in Electrical Specifications • Added ICC Sleep Mode to Digital DC Specification table in Electrical Specifications

Version Number	Date	Note
1.0	3/28/02	• Change pin M17 to N/C • Removed panel support for 1280x1024 • Changed VCCA and VCC to VDD • Delete External 2MG SGRAM Configuration figure • Minor corrections based on field input • Changed Digital DC Specificaitons for V_{IH} and I_{CC}
1.1	7/16/02	• Changed pin K3 from MEMINT to DSF • Clarified definition of PCI Bus Interface page 4-1
1.2	1/14/03	• Removed AGP references • Removed Bus Master Mode with DMA - LynxEM+ does not support this feature
1.3	4/23/03	• Added clarifcation to PCI Interface burst read and burst write. The LynxEM+ supports burst read and burst write for master mode and burst write for slave mode. • Added clarification to the Drawing Engine Control Registers. The LynxEM+ supports Bresenham line draw (8 and 16-bit only) and rectangle fill (8 and 16-bit only). • Changed SCR18 [0] enable definition.

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Chapter 1: Overview

The LynxEM+ combines Silicon Motion's unique multimedia features into a MCB solution. The LynxEM+ includes 2MB and 4MB of video memory within a single footprint. This powerful single footprint solution, when combined with SMI's Virtual Refresh™ architecture provides a complete video subsystem which consumes very little power.

LynxEM+ offers enhanced capabilities for dual view and for handling dual applications. Through its Virtual Refresh architecture, LynxEM+ can simultaneously drive LCD/CRT and LCD/TV display combinations. Each display can support independent full screen full motion video, as well as independent graphics refresh rates, resolutions, and color depths. LynxEM+ can display slides on TV/CRT while the attached speaker notes are available on the LCD display, invisible to the audience. For a dual application experience, a spreadsheet can be displayed on the LCD, while a word processing application or web browser can be displayed on the CRT. Dual view and dual application support is provided under Windows 95, Windows 98, Windows NT, and Windows 2000.

The LynxEM+ incorporates three separate PLLs to allow flexible control of functional blocks within the device. A robust 2D Drawing Engine supports 3 ROPs, BitBLT, transparent BLT, pattern BLT, color expansion, and line draw. The Host Interface Unit is PCI 2.1 compliant and supports bus mastering. The Power Down Control Unit with Dynamic Power Management provides individual block shutdown capability and complete Standby and Suspend support. A VGA Core, LCD Backend Controller and 135 MHz RAMDAC are incorporated as well.

The LynxEM+'s Concurrent Video Processor and Video Capture Unit provide superior video quality for real-time video capture and playback. LynxEM+'s Video Processor supports multiple independent full screen, full motion video windows with overlay. Each motion video window uses hardware YUV-to-RGB conversion, scaling, and color interpolation. When combined with the dual view capabilities of the chip, these independent video streams can be output to separate display devices and bilinear scaled to support applications such as full screen display of local and remote images for video conferencing.

LynxEM+ is designed with 0.35m, TLM, 3.3V CMOS process technology. A hierarchical layout approach provides enhanced internal timing control. In addition to built-in test modes and a signature analyzer, the LynxEM+ incorporates a 20-bit test bus designated the TD Bus. The TD bus can be used to simultaneously monitor 20 internal signals from 8 functional blocks through Zoom Video (ZV) Port Interface. The capability can be used to increase fault coverage, and reduce silicon validation and debugging time. The LynxEM+ is available in a 256 BGA package.

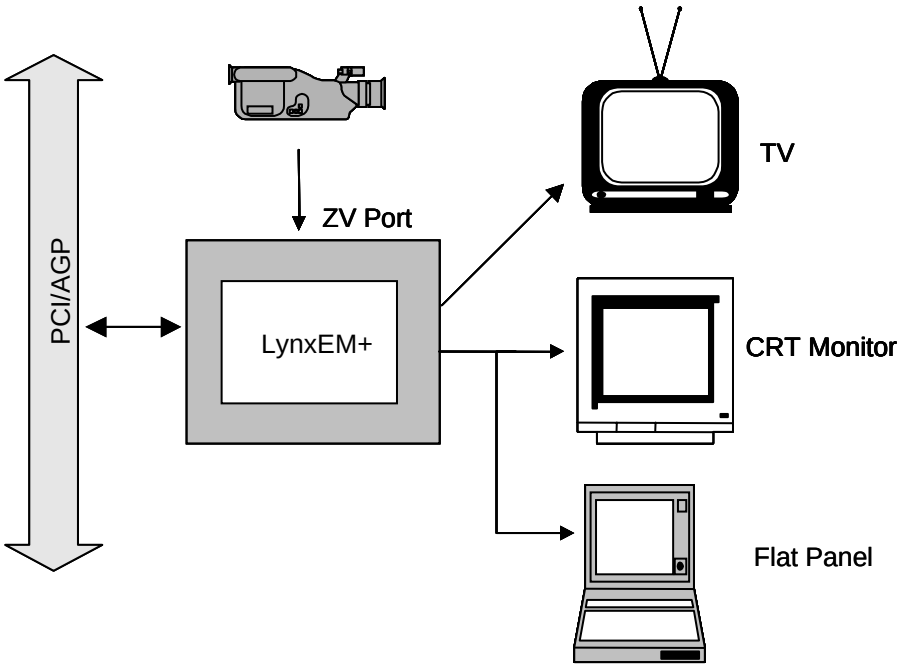


Figure 1: System Block Diagram for the LynxEM+

Features	Benefits
Dual Application support under Microsoft Windows 95, Windows 98, and Windows NT with one LynxEM+ device	• Two applications available at the same time across two display devices. Example: Word on LCD, Excel on CRT • Single chip implementation ideal for mobile systems
Dual Display support under Microsoft Windows 95, Windows 98, and Windows NT	Portion of primary display can be zoomed up for display on secondary display. Example: Zoom up power point slide to CRT, slide and accompanying speaker notes visible on LCD
Virtual Refresh Architecture	• Low operational power consumption • Simultaneous display of CRT and LCD at different resolutions and refresh rates • Simultaneous display of interlaced TV and non-interlaced LCD display
Dynamic power management • Individual functional block shut-down • Standby, Suspend support	Minimize power dissipation to extend battery life
Multiple independent hardware video windows • YUV-RGB color space conversion • Bilinear XY interpolation	• Independent full screen, full motion video for separate displays. • Complete dual view support for video under Windows98 • Example: For video conferencing - Full screen local view on LCD, full screen remote view on CRT/TV.
Robust, single clock cycle Drawing Engine • BitBLT, Transparent BLT, Pattern BLT • 3 ROPs • Color Expansion • Line Draw	Top notch graphics performance for mobile systems
High performance memory interface • 2MB or 4 MB internal memory • 64-bit memory bus	LynxEM+ provides up to 400MB/s bandwidth to support graphics and video. LynxEM4+ provides up to 688MB/s bandwidth to support graphics and video.
PCI Bus Mastering	Move graphics data and video to/from system memory to local graphics memory without impacting CPU performance. Example: Bus Master local videoconferencing image to system memory.
DSTN and TFT panel support up to 1024x768	Supports all panel requirements for mobile systems
TVout support • Flicker filter • Overscan/Underscan support	Graphics and/or video display on TV
135MHz 24-bit RAMDAC	Provides for PC99 compliant refresh rates
Zoom Video Port	Provides support for camera or TV tuner input, or input to VCR
Hardware support for LCD landscape/portrait rotation	Portrait view for desktop publishing, word processing applications
PC99 Compliant, ACPI Compliant	Meets WHQL certification requirements
SW support for Microsoft Windows 95, Microsoft Windows NT, and Microsoft Windows 98	Complete OS support
Hardware Video “Bob” Support	Improves DVD playback quality

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Functional Block Summary

The LynxEM+ consists of a logic block which interfaces to a 2MB or 4MB block of internal memory. The internal memory configuration consists of one 512Kx32 SGRAM, and supports single clock cycle transfers up to 100MHz. Peak memory bandwidth for the internal memory bus is over 500MB/s.

The logic within the LynxEM+ consists of 11 functional blocks: PCI Interface, Host Interface (HIF), Memory Controller, Drawing Engine, Power Down Control Unit, Video Processor, Video Capture Module, LCD Backend Controller, VGA Core, PLL Module, and RAMDAC. A summary of each of the functional blocks, along with important features follows:

PCI Interface and HIF

LynxEM+'s PCI Host Interface Unit supports burst read and burst write for master mode, and burst write for slave mode. The Host Interface Unit decodes I/O read, I/O write, memory read, memory write, memory mapped access, 2D Drawing Engine access, VGA access, and others. The unit also supports Little-Endian and Big-Endian format, and 8-bit ROM decode for on board video BIOS ROM. A dual aperture feature is designed to support VGA modes and non-VGA modes. In addition, a special VGA aperture function is added to allow 64-bit memory access in VGA modes.

LynxEM+ has an internal HIF (Host Interface) bus which is designed to transfer data between PCI Host Interface Unit and other functional blocks. The PCI Host Interface Unit controls the HIF bus protocol to effectively deliver PCI I/O and memory cycles to each functional block.

Key Feature Summary:
- 33 MHz & 66 MHz PCI Master/Slave interface
- PCI 2.1 compliant
- Dual aperture feature for concurrent VGA and video/drawing engine access

Memory Controller

Memory control is provided for the 2MB and 4MB internal memory. Page Break Look Ahead support assures a memory cycle is not broken if there is a change of memory bus agent within the same memory page. Programmable memory arbitration allows memory interface usage to be fully optimized - priority and round robin arbitration is supported.

Key Feature Summary:
- 500MB/s memory bandwidth

Drawing Engine

The LynxEM+'s Drawing Engine is designed to accelerate 2D through APIs such as Direct Draw. The engine pipeline runs at a single clock per cycle at speeds up to 62.5MHz. The engine supports key GUI functions such as 3 operand ALU with 256 raster operations, pattern BLT, color expansion, trapezoid fill, and line draw.

Key Feature Summary:
- 62.5MHz single clock/cycle engine (EM+)
- 86MHz single clock/cycle engine (EM4+)
- Designed to accelerate DirectDraw

Power Down Control Unit

The Power Down Control unit provides Dynamic Power Management for all functional blocks within the LynxEM+. Dynamic Power Management is made possible by individual clocking control to each of the functional blocks within LynxEM+. Each clock to a given functional block is skew matched to maintain synchronization between blocks. The functional blocks can then be turned on/off "on the fly" as needed. Power savings under fully operational conditions is maximized, yet the process completely transparent to the user.

Control for Virtual Refresh is provided through the Power Down Control unit as well. Through Virtual Refresh, LCD panel timing may be driven from a fully independent PLL. VLCK can be significantly reduced, while retaining full graphics performance. The result is significant power savings for LCD only configurations.

Finally, the Power Down Control unit generates power down sequencing for Standby and Suspend modes. Internal auto-standby and system standby implementations are supported.

Under sleep mode, options for memory refresh type and use of internal PLL/external clock for memory refresh clock are provided. Activity detection is supported for resuming from Standby or Suspend modes.

Key Feature Summary:
- Dynamic Power Management
- Virtual Refresh
- Standby and Suspend model support
- ACPI, DPMS, APM compliant

Video Processor

The Video Processor module manages video playback to an LCD, CRT, or TV display. Independent video sources can be scaled up and displayed full screen different display devices - ideal for videoconferencing applications. The Video Processor module supports, bi-linear scaling, YUV to RGB color space conversion, color key, and overlay of graphics over video. The Video Processor module also supports flicker reduction and adjustable overscan/underscan for TV display.

Key Feature Summary:
- Multiple video windows in HW
- Independent video sources on different displays
- Bi-linear scaling
- Flicker filter and underscan for TV display

Video Capture

The Video Capture module processes incoming video data from the Zoom Video Port and sends the data to the local video frame buffer. From there, the data may be displayed, as well as bus mastered out for storage on a hard drive. Incoming data from the Zoom Video port can be interlaced or non-interlace and in YUV or RGB format. The data can be cropped, horizontally filtered (2,3,or 4-tap), and shrunk to ¼ size. Single buffer as well as double buffer capture is supported.

Key Feature Summary:
- Support for Zoom Video Port interface
- Crop, filter, shrink support
- Support BOB implementation when interlaced data is captured

LCD Backend Controller

The LCD Backend Controller module manages data flow and generates timing to the selected LCD display. The module provides support for 3, 9, 12, 18, 24, 36-bit TFT and 16 or 24-bit DSTN panels up to 1024x768 resolution. The backend controller contains a color encoder, dithering engines for TFT and DSTN panels, frame accelerator, and a Virtual Refresh timing generation block. Each of the blocks within the LCD Backend controller module can be powered down if not in use. In addition LynxEM+ integrates innovative circuitry for reducing EMI.

Key Feature Summary:
- TFT and DSTN support up to 1024x768
- Timing generation for Virtual Refresh
- EMI reduction circuit

Popup Icon

The LynxEM+ support 64x64 popup icon which can be zoomed up by 2 to become 128x128 popup icon. The popup icon can be programmed to anywhere on the screen display. In addition, the popup icon has transparency support.

Key Feature Summary:
- Popup icon location flexible
- Transparency color support

VGA Core

The LynxEM+ has a high performance 32-bit VGA core which is 100% IBM VGA compatible. In addition to standard VGA functions, the LynxEM+'s VGA core module generates LCD timing, performs LCD screen autocentering and expansion, generates TV timing, and provides Hardware Cursor control.

Key Feature Summary:
- 100% IBM VGA compatible

PLL Module

The PLL module provides three separate PLLs for MCLK, VCLK, and Virtual Refresh clock to drive LCD panel timing. A 14.318MHz base clock is used to drive TV timing. This allows for completely independent timing for LCD/CRT or LCD/TV under dual application or dual view. For instance, the LCD panel can be driven at 60Hz while CRT refresh is 85Hz.

Key Feature Summary:
- Separate PLL for LCD panel timing

RAMDAC

The integrated RAMDAC supports pixel clock frequencies up to 135MHz at 3.3V. Anti-sparkle logic is provided for read/ writes to the palette. An internal band gap voltage reference saves need for external RC components.

Key Feature Summary:
- 135MHz at 3.3V

Table 1: LynxEM+: Display Support Modes

CRT Only				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
	75	x	x	x
	85	x	x	x
800x600	60	x	x	x
	75	x	x	x
	85	x	x	x
1024x768	60	x	x	x
	75	x	x	x
	85	x	x	x

Simultaneous Mode				
Display Resolution	**Refresh (Hz)**	**Color Depth**		
		8 bpp	**16 bpp**	**24 bpp**
640x480	60	x	x	x
800x600	60	x	x	x
1024x768	60	x	x	x

Dual Display Mode				
Display 1 (D1)	**Display 2 (D2)**	**Color Depth (Max Color Depth Display 2 bpp)**		
		when D1 is 8 bpp	**when D1 is 16 bpp**	**when D1[1] is 24 bpp**
640x480	640x480	24 (D2)	24 (D2)	-
	800x600	24	24	-
	1024x768	24	24	-
800x600	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	24	-
1024x768	640x480	24	24	-
	800x600	24	24	-
	1024x768	24	8	-

[1]Max color depth for display 1, 16bpp under dual display

Chapter 2: Pins

The SM712 is in a 256 BGA package.

Figure 2 illustrates the pinout diagram for SM712 256 BGA package. Figure 34 illustrates the mechanical dimensions of the BGA package.

LynxEM+ Pin Descriptions

The following table, Table 2 provides brief description of each BGA ball of the LynxEM+. Signal names with ~ preceding are active "LOW" signals, whereas signal names without ~ preceding are active "HIGH" signals. Also, the following abbreviations are used for Pin Type.

Table 3 outlines the numerical SM712 BGA pins.

I	-	INPUT SIGNAL
O	-	Output Signal
I/O	-	Input or Output Signal

Note: All Outputs and I/O signals are tri-stated. Internal pull-up for I/O pad are all 100KΩ resistor, with the exception for CPUCLK, which is 200KΩ resistor. Internal pull-down for I/O pad are all 100KΩ resistor.

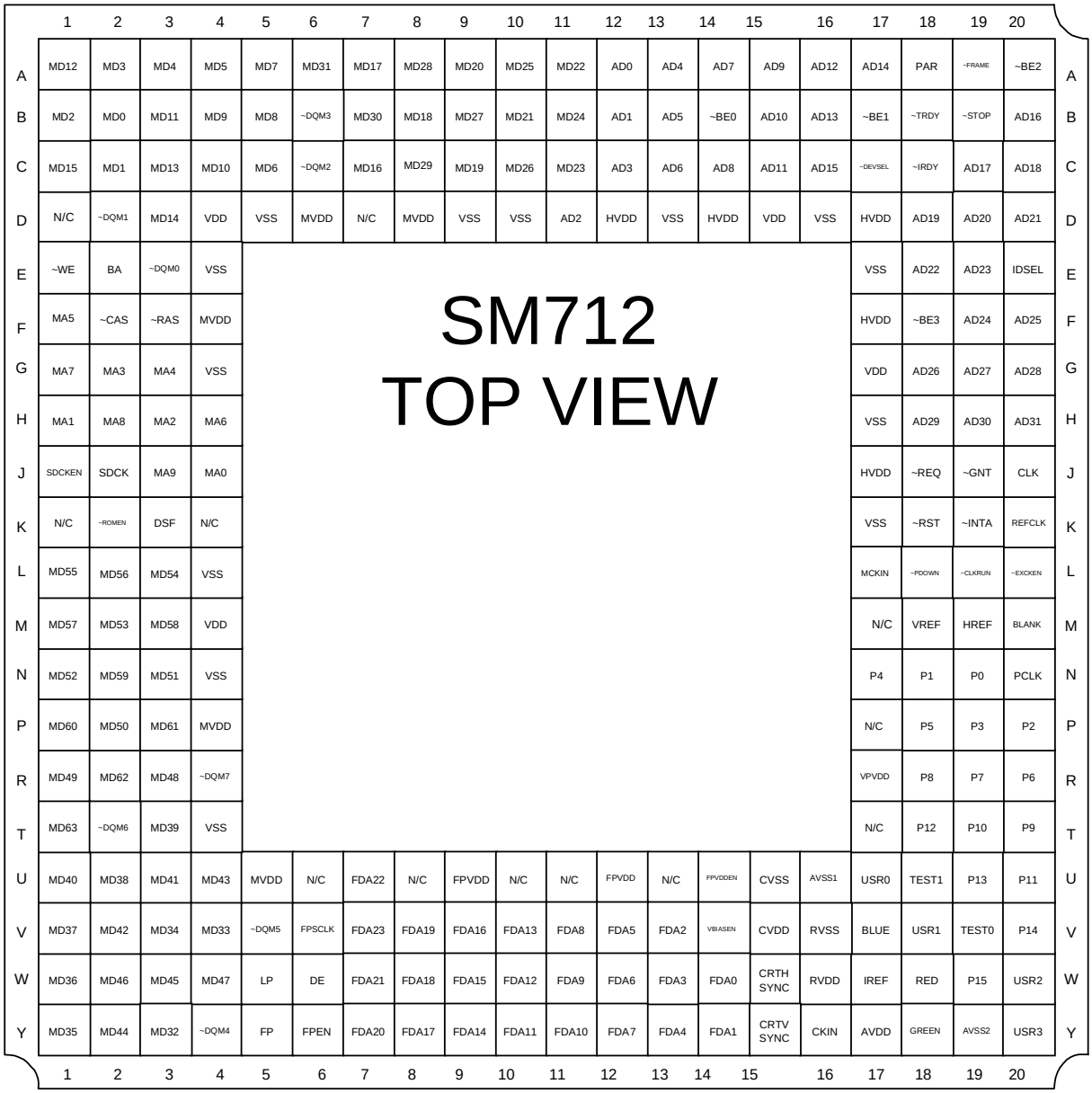
Table 2: Pin Description

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
Host Interface					
AD [31:0]	I/O		16	120	PCI multiplexed Address and Data Bus. A bus transaction consists of an address cycle followed by one or more data cycles.
C/ ~BE [3:0]	I/O		16	120	PCI Bus Command and Byte Enables. These signals carry the bus command during the address cycle and byte enable during data cycles.
PAR	I/O		16	120	Parity. LynxEM+ asserts this signal to verify even parity across AD [31:0] and C/~BE [3:0].
~FRAME	I/O		16	120	Cycle Frame. LynxEM+ asserts this signal to indicate the beginning and duration of a bus transaction. It is de-asserted during the final data cycle of a bus transaction.
~TRDY	I/O		16	120	Target Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~IRDY	I/O		16	120	Initiator Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~STOP	I/O		16	120	Stop. LynxEM+ asserts this signal to indicate that the current target is requesting the master to stop current transaction.
~DEVSEL	I/O		16	120	Device Select. LynxEM+ asserts this signal when it decodes its addresses as the target of the current transaction.
IDSEL	I				ID Select. This input is used during PCI configuration read/write cycles.
CLK	I				PCI System Clock, 33 MHz.
~RST	I				PCI System Reset. LynxEM+ asserts this signal to force registers and state machines to initial default values
~REQ	O		8	120	PCI Bus Request (bus master mode)
~GNT	I				PCI Bus Grant (bus master mode)
~INTA	O		8	120	PCI Interrupt
Power Down Interface					
~PDOWN	I	pull-up			Power down mode enable
~CLKRUN/ ACTIVITY	O	pull-up	4	60	~CLKRUN or LynxEM+ Memory and I/O activity detection depending on SCR18 [7] 0 = select ~CLKRUN 1 = select ACTIVITY
Clock Interface					
REFCLK	I	pull-up			32 KHz refresh clock source for power down or PALCLK for PALTV
CKIN	I	pull-up			14.318 MHz clock (~EXCKEN = 1) or Video Clock (~EXCKEN = 0)
MCKIN/ LVDSCLK	I/O	pull-up	4	60	Memory Clock In (~EXCKEN = 0) or LVDSCLK Out (~ESCKEN = 1), LVDSCLK is a free running clock which can be used to drive LVDS transmitter for DSTN panels.
~EXCKEN	I	pull-up		60	External Clock Enable. Select external VCLK form CKIN and MCLK from MCKIN.

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
External Display Memory Interface					
MA [9:0]	O		8	50	External Memory Address Bus. The video memory row and column addresses are multiplexed on these lines.
MD [63:0]	I/O	pull-up	4	20	External Memory Data Bus
~WE	O	pull-up	8	50	External Memory Write Strobe
~RAS	O	pull-up	8	50	External Memory SDRAM Row Address Select
~CAS	O	pull-up	8	50	External SGRAM Column Address Select
~CS0	O	pull-up	8	50	External SGRAM Chip Select 0, select 1st 1MB within the 2MB memory, or select 1st 2MB within the 4MB memory
~DQM [7:0]	O	pull-up	8	50	External SGRAM I/O mask [7:0]. DQM [7:0] are byte specific. DQM0 masks MD [7:0], DQM1 masks MD [15:8],Ö,and DQM7 masks MD [63:58].
DSF	O	pull-up	8	50	External SGRAM Block write
BA	O		8	50	External SGRAM Bank Select. SDRAM has dual internal banks. Bank address defines to which bank the current command is being applied.
SDCK	I/O	pull-up	16	50	External SGRAM clock. SDCK is driven by the memory clock. All SDRAM input signals are sampled on the positive edge of SDCK.
SDCKEN	I/O	pull-up	8	50	External SGRAM clock enable. SDCKEN activates (HIGH) and deactivates (LOW) the SDCLK signal. Deactivating the SDCK provides POWER-DOWN and SELF-REFRESH mode.
~ROMEN	O	pull-up	4	20	ROM Enable
Flat Panel Interface					
FDATA [23:0]	O	pull-down	6	50	Flat Panel Data bit 23 to bit 0. Note: For SM712, the upper 12 bits [25:24] are multiplexed with ZV port, and the upper 12 bits [23:11] are dedicated for flat panel data
LP/FHSYNC	O	pull-down	6	50	DSTN LCD: Line Pulse TFT LCD: LCD Horizontal Sync
FP/FVSYNC	O	pull-down	6	50	DSTN LCD: Frame Pulse TFT LCD: LCD vertical sync
M/ DE	O	pull-down	6	50	M-signal or Display Enable. This signal is used to indicate the active horizontal display time. FPR3E [7] is used to select 1 = M-signal 0 = Display Enable
FPSCLK	O	pull-down	6	50	Flat Panel Shift Clock. This is the pixel clock for Flat Panel Data.
FPEN	O	pull-down	4	20	Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are supplied. This signal also needs to become inactive before any panel voltages or control signals are removed. FPEN is part of the VESA FPDI-1B specification.
FPVDDEN	O	pull-down	4	20	Flat Panel VDD Enable. This signal is used to control LCD logic power.
VBIASEN	O	pull-down	4	20	Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power.

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
CRT Interface					
RED	O				Analog Red Current Output
GREEN	O				Analog Green Current Output
BLUE	O				Analog Blue Current Output
IREF	I				Current Reference Input
CRTVSYNCC	O	pull-up	6	50	CRT Vertical Sync
CRTHSYNC/ CSYNC	O	pull-up	6	50	CRT Horizontal Sync or Composite Sync depending on CCR65 [0] 0 = CRT Horizontal Sync 1 = Composite Sync
Video Port Interface					
P [15:0]	I/O		4	20	RGB or YUV input/ RGB digital output
PCLK	I/O	pull-up	4	20	Pixel Clock
VREF	I/O	pull-up	4	20	VSYNC input from PC Card or video decoder
HREF	I/O	pull-up	4	20	HSYNC input from PC Card or video decoder
BLANK/ TVCLK	I/O	pull-up	4	20	Blank output or TVCLK output depending on CCR69 bit 7. 0 = BLANK output 1 = TVCLK output TVCLK output is used to drive external NTSC/PAL TV encoder. To select NTSC or PAL TV, please refer to CCR65 register
General Purpose Registers / I2C					
USR3	I/O	pull-up	4	20	General Purpose register. It is recommended to use USR3 to control TV On/Off. 0 = TV display is OFF 1 = TV display is ON
USR2	I/O	pull-up	4	20	General Purpose register. It is recommended to use USR2 to select NTSC/PAL TV settings. 0 = PALTVCLK 1 = NTSCTVCLK or REFCLK
USR1 / SDA	I/O	pull-up	4	20	General Purpose register. USR1/ DDC2/ I2C Data. Can be used to select different test modes.
USR0 / SCL	I/O	pull-up	4	20	General Purpose register. USR0/ DDC2/ I2C Clock. Can be used to select different test modes.
Test Mode Pins					
TEST [1:0]	I	pull-down			Test mode selects
VCC and GROUND Pins					
HVDD					Host Interface VDD on I/O Ring, 3.3V
MVDD					Display Memory Interface VDD on I/O Ring, 3.3V
FPVDD					Flat Panel Interface VDD on I/O Ring, 3.3V
VPVDD					VPort Interface VDD on I/O Ring 3.3V
CVDD					Clock (PLL) Analog Power, 3.3V
AVDD					DAC Analog Power, 3.3V

Signal Name	Type	Pull-up/ Pull-Down	IOL (mA)	Max. Load (pF)	Description
RVDD					RAM Filtered Palette Power, 3.3V
CVSS					PLL Analog Ground
AVSS1					DAC Analog Ground
AVSS2					DAC Analog Ground
RVSS					RAM Filtered Palette Ground
VDD					Digital 3.3V Core Power Supply Digital 3.3V Internal Memory Power Supply
VSS					Digital Ground



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	MD12	MD3	MD4	MD5	MD7	MD31	MD17	MD28	MD20	MD25	MD22	AD0	AD4	AD7	AD9	AD12	AD14	PAR	~FRAME	~BE2	A
B	MD2	MD0	MD11	MD9	MD8	~DQM3	MD30	MD18	MD27	MD21	MD24	AD1	AD5	~BE0	AD10	AD13	~BE1	~TRDY	~STOP	AD16	B
C	MD15	MD1	MD13	MD10	MD6	~DQM2	MD16	MD29	MD19	MD26	MD23	AD3	AD6	AD8	AD11	AD15	~DEVSEL	~IRDY	AD17	AD18	C
D	N/C	~DQM1	MD14	VDD	VSS	MVDD	N/C	MVDD	VSS	VSS	AD2	HVDD	VSS	HVDD	VDD	VSS	HVDD	AD19	AD20	AD21	D
E	~WE	BA	~DQM0	VSS													VSS	AD22	AD23	IDSEL	E
F	MA5	~CAS	~RAS	MVDD													HVDD	~BE3	AD24	AD25	F
G	MA7	MA3	MA4	VSS													VDD	AD26	AD27	AD28	G
H	MA1	MA8	MA2	MA6													VSS	AD29	AD30	AD31	H
J	SDCKEN	SDCK	MA9	MA0													HVDD	~REQ	~GNT	CLK	J
K	N/C	~ROMEN	DSF	N/C													VSS	~RST	~INTA	REFCLK	K
L	MD55	MD56	MD54	VSS													MCKIN	~PDOWN	~CLKRUN	~EXCKEN	L
M	MD57	MD53	MD58	VDD													N/C	VREF	HREF	BLANK	M
N	MD52	MD59	MD51	VSS													P4	P1	P0	PCLK	N
P	MD60	MD50	MD61	MVDD													N/C	P5	P3	P2	P
R	MD49	MD62	MD48	~DQM7													VPVDD	P8	P7	P6	R
T	MD63	~DQM6	MD39	VSS													N/C	P12	P10	P9	T
U	MD40	MD38	MD41	MD43	MVDD	N/C	FDA22	N/C	FPVDD	N/C	N/C	FPVDD	N/C	FPVDDEN	CVSS	AVSS1	USR0	TEST1	P13	P11	U
V	MD37	MD42	MD34	MD33	~DQM5	FPSCLK	FDA23	FDA19	FDA16	FDA13	FDA8	FDA5	FDA2	VBIASEN	CVDD	RVSS	BLUE	USR1	TEST0	P14	V
W	MD36	MD46	MD45	MD47	LP	DE	FDA21	FDA18	FDA15	FDA12	FDA9	FDA6	FDA3	FDA0	CRTH SYNC	RVDD	IREF	RED	P15	USR2	W
Y	MD35	MD44	MD32	~DQM4	FP	FPEN	FDA20	FDA17	FDA14	FDA11	FDA10	FDA7	FDA4	FDA1	CRTV SYNC	CKIN	AVDD	GREEN	AVSS2	USR3	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 2: SM712 Pin Diagram for 256 BGA Package

N/C = Not Connected but compatible with SM810.

Table 3: SM712 Pin Diagram for 256 BGA Package

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
A1	MD12					MVDD
A2	MD3	***{ROM}***				MVDD
A3	MD4	ROMD4				MVDD
A4	MD5	ROMD5				MVDD
A5	MD7	ROMD7				MVDD
A6	MD31					MVDD
A7	MD17					MVDD
A8	MD28					MVDD
A9	MD20					MVDD
A10	MD25					MVDD
A11	MD22					MVDD
A12	AD0					HVDD
A13	AD4					HVDD
A14	AD7					HVDD
A15	AD9					HVDD
A16	AD12					HVDD
A17	AD14					HVDD
A18	PAR					HVDD
A19	~FRAME					HVDD
A20	C/~BE2					HVDD
B1	MD2	ROMD2				MVDD
B2	MD0	ROMD0				MVDD
B3	MD11					MVDD
B4	MD9					MVDD
B5	MD8					MVDD
B6	~DQM3					MVDD
B7	MD30					MVDD
B8	MD18					MVDD
B9	MD27					MVDD
B10	MD21					MVDD
B11	MD24					MVDD
B12	AD1					HVDD
B13	AD5					HVDD
B14	C/~BE0					HVDD
B15	AD10					HVDD
B16	AD13					HVDD
B17	C/~BE1					HVDD
B18	~TDRY					HVDD
B19	~STOP					HVDD
B20	AD16					HVDD
C1	MD15					MVDD

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
C2	MD1	ROMD1				MVDD
C3	MD13					MVDD
C4	MD10					MVDD
C5	MD6	ROMD6				MVDD
C6	~DQM2					MVDD
C7	MD16					MVDD
C8	MD29					MVDD
C9	MD19					MVDD
C10	MD26					MVDD
C11	MD23					MVDD
C12	AD3					HVDD
C13	AD6					HVDD
C14	AD8					HVDD
C15	AD11					HVDD
C16	AD15					HVDD
C17	~DEVSEL					HVDD
C18	~IDRY					HVDD
C19	AD17					HVDD
C20	AD18					HVDD
D1	N/C					MVDD
D2	~DQM1					MVDD
D3	MD14					MVDD
D4	**VDD**					
D5	VSS					
D6	**MVDD**					
D7	**N/C**					
D8	**MVDD**					
D9	**VSS**					
D10	**VSS**					
D11	AD2					HVDD
D12	**HVDD**					
D13	**VSS**					
D14	**HVDD**					
D15	**VDD**					
D16	**VSS**					
D17	**HVDD**					
D18	AD19					HVDD
D19	AD20					HVDD
D20	AD21					HVDD
E1	~WE					MVDD
E2	BA					MVDD
E3	~DQM0					MVDD

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
E4	**VSS**					
E17	**VSS**					
E18	AD22					HVDD
E19	AD23					HVDD
E20	IDSEL					HVDD
F1	MA5					MVDD
F2	~CAS					MVDD
F3	~RAS					MVDD
F4	**MVDD**					
F17	**HVDD**					
F18	C/~BE3					HVDD
F19	AD24					HVDD
F20	AD25					HVDD
G1	MA7					MVDD
G2	MA3					MVDD
G3	MA4					MVDD
G4	VSS					
G17	VDD					
G18	AD26					HVDD
G19	AD27					HVDD
G20	AD28					HVDD
H1	MA1					MVDD
H2	MA8					MVDD
H3	MA2					MVDD
H4	MA6					MVDD
H17	**VSS**					
H18	AD29					HVDD
H19	AD30					HVDD
H20	AD31					HVDD
J1	SDCKEN					MVDD
J2	SDCK					MVDD
J3	MA9					MVDD
J4	MA0					MVDD
J17	HVDD					
J18	~REQ					HVDD
J19	~GNT					HVDD
J20	CLK					HVDD
K1	**NC**					
K2	~ROMEN					MVDD
K3	DSF					MVDD
K4	**N/C**					
K17	**VSS**					

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
K18	~RST					HVDD
K19	~INTA					HVDD
K20	REFCLK					HDD
L1	MD55					MVDD
L2	MD56					MVDD
L3	MD54					MVDD
L4	VSS					
L17	MCKIN/LVDSCK	MCKIN		LVDSCK		HVDD
L18	~PDOWN					HVDD
L19	~CLKRUN / ACTIVITY					HVDD
L20	~EXCKEN					HVDD
M1	MD57					MVDD
M2	MD53					MVDD
M3	MD58					MVDD
M4	VDD					
M17	N/C					
		{ZV IN}		**{TESTMODE1}**	**{VP OUT}**	
M18	VREF	VS		TD19	R2	VPVDD
M19	HREF	HREF	**{External TV encoder}**	TD18	R3	VPVDD
M20	BLANK/TVCLK		TVCLK	TD17	BLANK	VPVDD
N1	MD52					MVDD
N2	MD59					MVDD
N3	MD51					MVDD
N4	VSS		**{TFT 18x2}**			
N17	P4	UV4	Ge4	TD4	B3	VPVDD
N18	P1	UV1	Be5	TD1	B6	VPVDD
N19	P0	UV0	Be4	TD0	B7	VPVDD
N20	PCLK	PCLK		TD16	PCLK	VPVDD
P1	MD60					MVDD
P2	MD50					MVDD
P3	MD61					MVDD
P4	**MVDD**					
P17	N/C					
		{ZV IN}				
P18	P5	UV5	Ge5	TD5	B2	VPVDD
P19	P3	UV3	Bo5	TD3	B4	VPVDD
P20	P2	UV2	Bo4	TD2	B5	VPVDD
R1	MD49					MVDD
R2	MD62					MVDD
R3	MD48					MVDD

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
R4	~DQM7					MVDD
R17	**VPVDD**					
R18	P8	Y0	Re4	TD8	G5	VPVDD
R19	P7	UV7	Go5	TD7	G6	VPVDD
R20	P6	UV6	Go4	TD6	G7	VPVDD
T1	MD63					MVDD
T2	~DQM6	***{ROM}***				MVDD
T3	MD39	ROMA7				MVDD
T4	VSS					
T17	N/C	***{ZV IN}***				
T18	P12	Y4		TD12	R7	VPVDD
T19	P10	Y2	Ro4	TD10	G3	VPVDD
T20	P9	Y1	Re5	TD9	G4	VPVDD
		{ROM}				
U1	MD40	ROMA8				MVDD
U2	MD38	ROMA6				MVDD
U3	MD41	ROMA9				MVDD
U4	MD43	ROMA11				MVDD
U5	**MVDD**					
U6	N/C	***{DSTN}***			RB5	
U7	FDATA22	UD10	Ro2		R6	FPVDD
U8	N/C				RB4	
U9	**FPVDD**					
U10	N/C				GB4	
U11	N/C				BB5	
U12	**FPVDD**					
U13	N/C				BA4	
U14	FPVDDEN					
U15	**CVSS**					
U16	**AVSS1**	***{I^{2}C/DDC}***	***{USR CFG}***			
U17	USR0/SCL	SCL (Prim)	USR0			VPVDD
U18	TEST1	{ZV IN}		TEST1		VPVDD
U19	P13	Y5	***{TFT18x2}***	TD13	R6	VPVDD
U20	P11	Y3	Ro5	TD11	G2	VPVDD
		{ROM}				
V1	MD37	ROMA5				MVDD
V2	MD42	ROMA10				MVDD
V3	MD34	ROMA2				MVDD
V4	MD33	ROMA1				MVDD
V5	~DQM5	***{DSTN}***				MVDD
V6	FPSCLK	XCK			CK	FPVDD
V7	FDATA23	UD11	Ro3		R7	FPVDD

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
V8	FDATA19	UD7	Re3		R3	FPVDD
V9	FDATA16	UD4	Re0		R0	FPVDD
V10	FDATA13	UD1	Go1		G5	FPVDD
V11	FDATA8	LD8	Ge0		G0	FPVDD
V12	FDATA5	LD5	Bo1		B5	FPVDD
V13	FDATA2	LD2	Be2		B2	FPVDD
V14	VBIASEN					FPVDD
V15	**CVDD**					
V16	**RVSS**					
V17	BLUE	***{I²C/DDC}***	***{USR CFG}***			
V18	USR1/SDA	SDA (Prim)	USR1			VPVDD
V19	TEST0	***{ZV IN}***		TEST0		VPVDD
V20	P14	Y6		TD14	R5	VPVDD
		{ROM}				
W1	MD36	ROMA4				MVDD
W2	MD46	ROMA14				MVDD
W3	MD45	ROMA13				MVDD
W4	MD47	ROMA15				MVDD
		{DSTN}				
W5	LP/ FHSYNC	LP			FHSYNC	FPVDD
W6	M/ DE	M/DE			DE	FPVDD
W7	FDATA21	UD9	Ro1		R5	FPVDD
W8	FDATA18	UD6	Re2		R2	FPVDD
W9	FDATA15	UD3	Go3		G7	FPVDD
W10	FDATA12	UD0	Go0		G4	FPVDD
W11	FDATA9	LD9	Ge1		G1	FPVDD
W12	FDATA6	LD6	Bo2		B6	FPVDD
W13	FDATA3	LD3	Be3		B3	FPVDD
W14	FDATA0	LD0	Be0		B0	FPVDD
			{External TV encoder}			
W15						
CSYNC		CSYNC			VPVDD	
W16	RVDD					
W17	IREF					
W18	RED	***{ZV IN}***				
W19	P15	Y7		TD15	R4	VPVDD
		{I²C/DDC}	***{USR CFG}***			
W20	USR2	SCL	USR2/NTSCPAL			VPVDD
		{ROM}				
Y1	MD35	ROMA3				MVDD
Y2	MD44	ROMA12				MVDD

#	SM712 Name	{Function1}	{Function2}	{Function3}	{Function4}	VDD
Y3	MD32	ROMA0				MVDD
Y4	~DQM4	***{DSTN}***			***{TFT}***	MVDD
Y5	FP/ FVSYNC	FP			FVSYNC	FPVDD
Y6	FPEN	FPEN	***{TFT 18x2}***		FPEN	FPVDD
Y7	FDATD20	UD8	Ro0		R4	FPVDD
Y8	FDATA17	UD5	Re1		R1	FPVDD
Y9	FDATA14	UD2	Go2		G6	FPVDD
Y10	FDATA11	LD11	Ge3		G3	FPVDD
Y11	FDATA10	LD10	Ge2		G2	FPVDD
Y12	FDATA7	LD7	Bo3		B7	FPVDD
Y13	FDATA4	LD4	Bo0		B4	FPVDD
Y14	FDATA1	LD1	Be1		B1	FPVDD
Y15	CRTVSYNC					FPVDD
Y16	CKIN					
Y17	AVDD					
Y18	GREEN					
Y19	AVSS2	***{I2C/DDC2}***	***{USR CFG}***			
Y20	USR3	SDA	USR3/ TVONOFF			VPVDD

LynxEM+ NAND Tree Scan Testing

The LynxEM+ NAND Tree scan test circuit is designed for verifying the device being properly soldered to the board. It detects opened/shorted traces of a signal pin with a simple test pattern which, for this particular case, only ~200 vectors in length. The NAND Tree scan test circuit uses Combinational logic; therefore, no clock pulses are required during the testing.

General Information

The LynxEM+ NAND Tree scan test circuit is a long chain of 2-input NAND gates. The first pin of the NAND chain is an input (signal pin "MCKIN"), the last pin of the chain is an output (signal pin "BLANK"). In order to setup LynxEM+ for NAND Tree scan testing, program USR[3:0] pins to 0011h and Test[1:0] pins to 10h. ALL VDD's, VSS's, and Analog pins RED, GREEN, BLUE, IREF, and Control pins USR[3:0], Test[1:0] are not included in the scan chain.

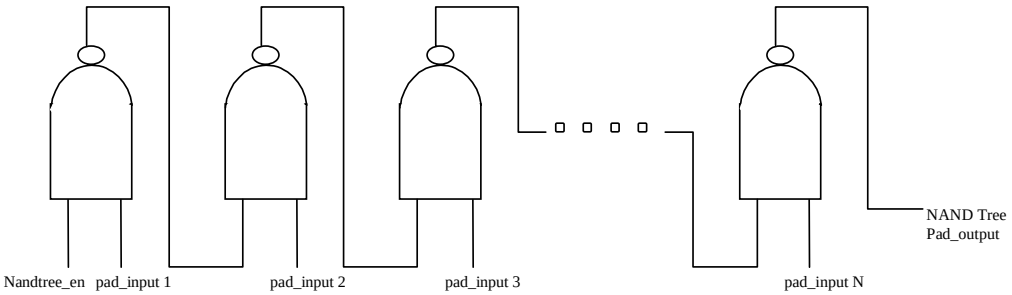


Figure 3: NAND Tree Connection

Table 4: NAND Tree Scan Test Order

Nand Tree Scan Pin Order #	Pin Name	In/Out
1	MCKIN	In
2	~PDOWN	In
3	ACTIVITY	In
4	EXCKEN	In
5	REFCLK	In
6	~INTA	In
7	~RST	In
8	CLK	In
9	~GNT	In
10	~REQ	In
11	AD31	In
12	AD30	In
13	AD29	In
14	AD28	In
15	AD27	In
16	AD26	In
17	AD25	In
18	AD24	In

Nand Tree Scan Pin Order #	Pin Name	In/Out
19	~CBE3	In
20	IDSEL	In
21	AD23	In
22	AD22	In
23	AD21	In
24	AD20	In
25	AD19	In
26	AD18	In
27	AD17	In
28	AD16	In
29	CBE2	In
30	~FRAME	In
31	~IRDY	In
32	~TRDY	In
33	~DEVSEL	In
34	~STOP	In
35	PAR	In
36	~CBE1	In
37	AD15	In
38	AD14	In
39	AD13	In
40	AD12	In
41	AD11	In
42	AD10	In
43	AD9	In
44	AD8	In
45	~CBE0	In
46	AD7	In
47	AD6	In
48	AD5	In
49	AD4	In
50	AD3	In
51	AD2	In
52	AD1	In
53	AD0	In
54	MD23	In
55	MD24	In
56	MD22	In
57	MD25	In
58	MD21	In
59	MD26	In

Nand Tree Scan Pin Order #	Pin Name	In/Out
60	MD20	In
61	MD27	In
62	MD19	In
63	MD28	In
64	MD18	In
65	MD29	In
66	MD17	In
67	MD30	In
68	MD16	In
69	MD31	In
70	DQM3	In
71	DQM2	In
72	MD7	In
73	MD8	In
74	MD6	In
75	MD9	In
76	MD5	In
77	MD10	In
78	MD4	In
79	MD11	In
80	MD3	In
81	MD12	In
82	MD2	In
83	MD13	In
84	MD1	In
85	MD14	In
86	MD0	In
87	MD15	In
88	DQM1	In
89	DQM0	In
90	BA	In
91	~WE	In
92	~RAS	In
93	~CAS	In
94	MA5	In
95	MA4	In
96	MA6	In
97	MA3	In
98	MA7	In
99	MA2	In
100	MA8	In

Nand Tree Scan Pin Order #	Pin Name	In/Out
101	MA1	In
102	MA9	In
103	MA0	In
104	SDCK	In
105	SDCKEN	In
106	DSF	In
107	~ROMEN	In
108	~CS0	In
109	MD55	In
110	MD56	In
111	MD54	In
112	MD57	In
113	MD53	In
114	MD58	In
115	MD52	In
116	MD59	In
117	MD51	In
118	MD60	In
119	MD50	In
120	MD61	In
121	MD49	In
122	MD62	In
123	MD48	In
124	MD63	In
125	DQM7	In
126	DQM6	In
127	MD39	In
128	MD40	In
129	MD38	In
130	MD41	In
131	MD37	In
132	MD42	In
133	MD36	In
134	MD43	In
135	MD35	In
136	MD44	In
137	MD34	In
138	MD45	In
139	MD33	In
140	MD46	In
141	MD32	In

Nand Tree Scan Pin Order #	Pin Name	In/Out
142	MD47	In
143	DQM5	In
144	DQM4	In
145	FHSYNC	In
146	FVSYNC	In
147	FPSCLK	In
148	DE	In
149	FPEN	In
150	FDATA23	In
151	FDATA22	In
152	FDATA21	In
153	FDATA20	In
154	FDATA19	In
155	FDATA18	In
156	FDATA17	In
157	FDATA16	In
158	FDATA15	In
159	FDATA14	In
160	FDATA13	In
161	FDATA12	In
162	FDATA11	In
163	FDATA10	In
164	FDATA9	In
165	FDATA8	In
166	FDATA7	In
167	FDATA6	In
168	FDATA5	In
169	FDATA4	In
170	FDATA3	In
171	FDATA2	In
172	FDATA1	In
173	FDATA0	In
174	FPVDDEN	In
175	VBIASEN	In
176	CRTVSYNC	In
177	CRTHSYNC	In
178	P15	In
179	P14	In
180	P13	In
181	P12	In
182	P11	In

Nand Tree Scan Pin Order #	Pin Name	In/Out
183	P10	In
184	P9	In
185	P8	In
186	P7	In
187	P6	In
188	P5	In
189	P4	In
190	P3	In
191	P2	In
192	P1	In
193	P0	In
194	PCLK	In
195	VREF	In
196	HREF	In
197	BLANK	Out

Chapter 3: Initialization

LynxEM+ generates an internal power-on reset during system power-on. After receiving the system ~RESET signal, LynxEM+ will release its internal power-on reset circuit and enter the RESET period until the host de-asserts the ~RESET signal. During the RESET period, LynxEM+ resets its internal state machines and registers to the power-on default states. During power-on, LynxEM+ is configured based on configuration lines MD [22:0].

Table 5 (see end of this section) provides a detailed description of each configuration line. All MD (memory data) lines have internal pull-up resistors on I/O pads which are latched into the corresponding register as logic "1" on the rising edge (trailing edge) of the ~RESET. To set a specific bit as logic "0" during power-on reset, an external pull-down resistor must be added on the corresponding MD line.

In addition to power-on configuration, LynxEM+ performs an initialization sequence for the 2MB or 4MB of internal memory.

Figure 4 illustrates the power-up sequence.

- DQM and SDCKEN signals go HIGH, initially tracking VCC.
- 200ms delay
- PRECHARGE command for all banks
- LOAD MODE REGISTER command
- 8 AUTO REFRESH cycles

After memory initialization has been completed, LynxEM+'s video BIOS is ready to service system BIOS requests. System BIOS passes a pointer to the LynxEM+ video BIOS to start the video BIOS initialization sequence.

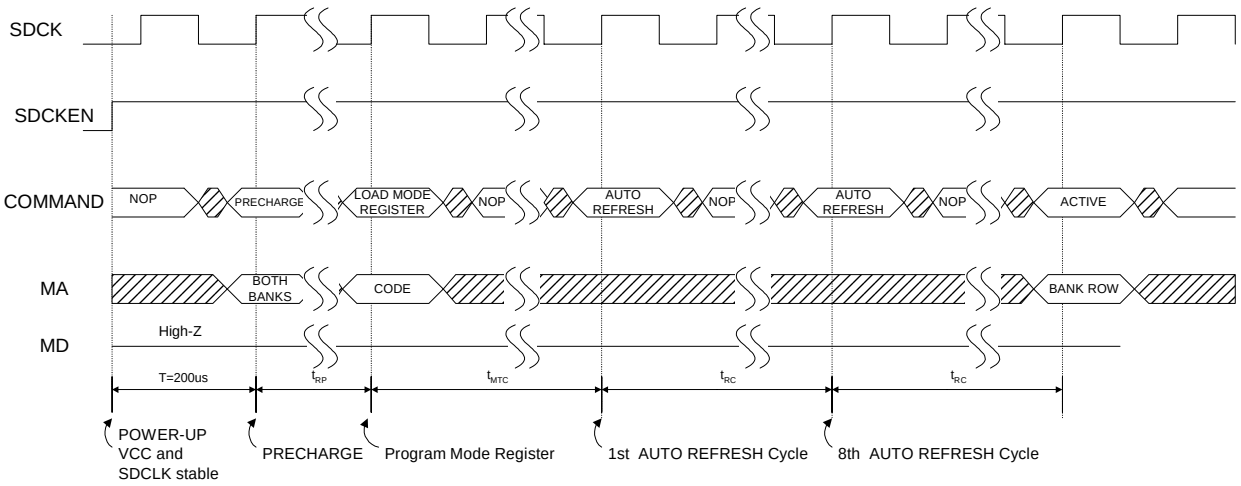


Figure 4: External SGRAM Power-Up and Initialization Sequence

Figure 5 illustrates the LynxEM+ Video BIOS initialization flow. The initialization sequence consists of the following stages:

- Determine memory size
- Check for display type. (FPR31 [2:0]) LCD only, CRT only, LCD and CRT or LCD and TV, etc.
- Program the appropriate timing registers based on the display type
- Set to mode 3h to display characters on the display for users to read
- Pass the pointer back to system BIOS

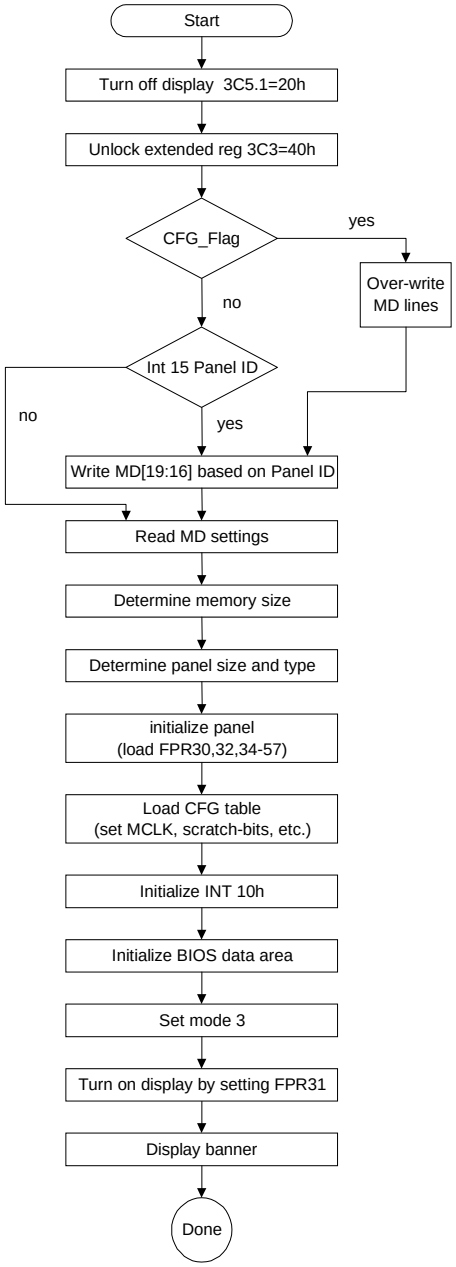


Figure 5: LynxEM+ BIOS Initialization Flowchart

LynxEM+ Power-On Configurations

- All MD (memory data) lines have internal pull-up resistors on I/O pads.
- 0 = external pull-down resistor (recommended value is 1K ohm)
- 1 = no external pull-down resistor

Table 5: Power-On Configurations

Signal Name	Read/Write	Register Bits	Address	LynxEM+ Description
MD [23]	R	CPR00 [25]		0 = External memory access only 1 = Allows both internal and external memory access (default)
MD [22]	CONFIG ONLY			0 = 32K 1 = 64K BIOS size default
MD [21] 1	CONFIG ONLY			**EBROM Generate** 0 = EBROM 1 = no EBROM (default)
MD [20] 1	CONFIG ONLY			**Expansion ROM** 0 = Expansion ROM 1 = no Expansion ROM (default)
MD [19:16]	R/W	GPR70 [3:0]	3C5h.70	**User configuration Bits**
MD15	R/W	FPR30 [7]	3C5h.30	**DSTN Interface Type** 0 = 16-bit interface 1 = 24-bit interface
MD [14:12]	R/W	FPR30 [6:4]	3C5h.30	**Color TFT Interface Type** 000 = 9-bit, 3-bit per R, G, B 001 = 12-bit, 4-bit per R, G, B 010 = 18-bit, 6-bit per R, G, B 011 = 24-bit, 8-bit per R, G, B 100 = 24-bit, (12+12-bit, 2 pixels/clock) 101 = Analog TFT w/ analog R, G, B interface 110 = 36-bit, (18+18-bit, 2 pixels/clock)
MD [11:10]	R/W	FPR30 [3:2]	3C5h.30	**LCD Display Size** 00 = 640 x 480 01 = 800 x 600 10 = 1024 x 768
MD9	R/W	FPR30 [1]	3C5h.30	**TFT FPCLK Select** 0 = Normal 1 = Inverted
MD8	R/W	FPR30 [0]	3C5h.30	**Color LCD Type** 0 = color TFT 1 = color STN
MD7	R/W	MCR62 [7]	3C5h.62	**Internal Logic** 0 = Internal logic will be running 1/2X MCLK 1 = Internal logic will be running 1X MCLK
MD6	R/W	MCR62 [6]	3C5h.62	**Enable Memory Data Bus** 0 = Enable 32-bit memory data bus 1 = Enable 64-bit memory data bus
MD [5:4]	R/W	MCR62 [5:4]	3C5h.62	**External SGRAM Memory Column Address Select** 11 = 8-bit column address 10 = 9-bit column address 0x = 10-bit column address
				Memory Pre-charge Timing Select Reserved

Signal Name	Read/Write	Register Bits	Address	LynxEM+ Description
MD2	R/W	MCR62 [2]	3C5h.62	**External Memory Enable** 0 = Enable external 32-bit memory 1 = Disable external 32-bit memory
MD1	R/W	MCR62 [1]	3C5h.62	**External SGRAM Memory Active-to-Precharge Delay Select** 0 = 7 MCLK 1 = 6 MCLK
MD0	R/W	MCR62 [0]	3C5h.62	**External SGRAM Memory Refresh to Command Delay** 0 = 10 MCLK 1 = 9 MCLK

Chapter 4: PCI Bus Interface

LynxEM+ provides a glue-less interface to the PCI system bus, and the PCI Host Interface Unit supports burst read and burst write for master mode and burst write for slave mode. To maximize performance, the Host Interface unit also supports burst write and burst read with Read Look Ahead. The LynxEM+ is fully compliant with PCI Verison 2.1, but does not have 5V tolerant I/O cell. If the LynxEM+ is used with 5V PCI then it will need an external glue-logic.

The LynxEM+'s PCI Host Interface Unit manages data transfer between the external PCI bus and internal Host Interface (HIF) bus. All functional blocks, with the exception of the Drawing Engine, are tied to the HIF bus through a proprietary protocol. Separate decode logic and a dedicated FIFO are used for the Drawing Engine.

In addition to PCI Configuration Space Registers, the PCI Host Interface Unit contains Power Down Control Registers (PDR20-PDR23) and System Control Registers (SCR10-SCR1A). These Registers may accessed by the CPU even while internal PLLs are turned off.

PCI Configuration Registers

The PCI configuration registers are designated CSR00 - CSR3D. A brief description of key elements of the register set follows:

- Vendor ID register (CSR00) - hardwired to 126Fh to identify Silicon Motion, Inc. as the chip vendor.
- Device ID register (CSR02) - hardwired to 0810h to identify the LynxEM+ device. The ~DEVSEL timing in the
- Status register (CSR06) - hardwired to 01b, which indicates medium speed for ~DEVSEL.
- Class Code register (CSR08) - hardwired to 030000h to specify LynxEM+ as a VGA compatible device. Bit [7:0] used to identify the revision of the LynxEM+.
- Memory Base Address register (CSR10) - specifies the PCI configuration space for address relocation. After power-on, the register defaults to 00h, which indicates the base register can be located anywhere in a 32-bit address space and that the base register is located in memory space.
- Subsystem Vendor ID and Subsystem ID (addressable at CSR2C and CSR2E respectively) - 32-bit read only registers. These registers are used to differentiate between multiple graphics adapters within the same system.

Chapter 5: Display Memory Interface

Memory Configuration

The LynxEM+ supports a 2 or 4 Mbytes of memory. There are three memory configurations:

1. 2 Mbytes internal memory only
2. 4 Mbytes of internal memory (there is no option for external memory with this configuration)

The internal memory is 2 or 4 Mbytes of 512Kx32 SGRAM. The LynxEM+ single cycle interface may be clocked up to 129 MHz, which provides over 516 MB/s. The LynxEM4+ single cycle interface may be clocked up to 86 MHz, which provides over 688 MB/s.

The LynxEM+ supports a total 2 Mbytes external memory composed of 256Kx32 SGRAM.

Page Break Look Ahead

For standard architectures, the memory controller will break cycle when the bus agent changes. LynxEM+ can allow a "No Wait Cycle" during agent changes if the preceding and current agents are in the same page. Both the internal memory bus and external memory bus support this capability.

Memory Timing Control

Memory timing control is configurable via MD[7:0] during power-on reset. See Table 5 in the Initialization section for a complete description of these memory configuration bits.

Note: All MD lines have internal pull-up resistors on I/O pads. The default configuration is therefore a logical "1" during power-on reset. To set an MD line to 0, an external pull-down resistor needs to be added. After power-on initialization, software can be used to overwrite the initial setting by writing to MCR62 -- bits 7-0 correspond to MD[7:0].

Chapter 7: Video Processor

LynxEM+'s Video Processor manages video data streams, as well as graphics data streams in non-VGA modes. The Video Processor can process two independent video data streams. The two video windows (primary and secondary) can be displayed at any screen location with any size, and can be overlaid with graphics data.

Within the Video Processor, the Graphics Source Control block, Video Window I Control block, Video Window II Control block, and HW Pop-up Icon Control block all have independent Starting Address and Offset Address registers. This means that each control block can fetch data from any display memory location. Video Window I source control block supports double-buffered video capture. Internal logic automatically detects the control/status bits of the two capture buffers and fetches the captured video data from the buffer which is not used.

The Video Processor supports TV flicker reduction for direct color modes (64K colors or 16M colors), as well as index color modes (256 colors and 16 colors). A special data path is designed to feed the outputs of the color palette RAM back to the TV Flicker Reduction block. The TV Overscan & Underscan Control block is used to convert 480 lines into 400 visible lines on NTSC TV display. The same function can also be used on PAL TV display. When the TV display is enabled, the Shadow registers need to be locked as 640 x 480 mode (or 720 x 525 for PAL).

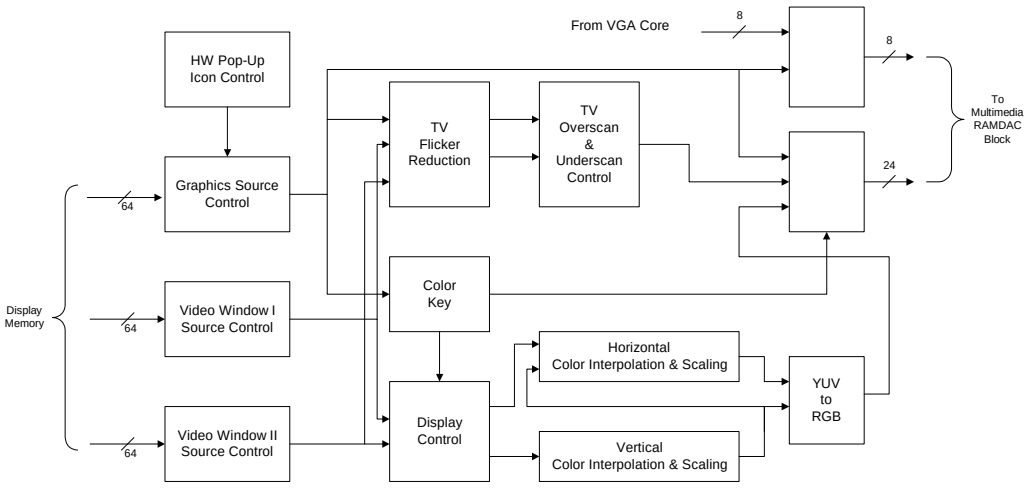


Figure 6: Video Processor Block Diagram

Chapter 6: Drawing Engine

LynxEM+'s Drawing Engine is designed to accelerate Microsoft's DirectDraw applications. The engine contains a 3-operand ALU with 256 raster operations, source and destination FIFOs, as well as a host data FIFO. The drawing engine pipeline allows single cycle operations and runs at the memory clock speed.

LynxEM+'s Drawing Engine includes several key functions to achieve the high GUI performance. The device supports color expansion with packed mono font, color pattern fill, host BLT, stretch BLT, short stroke, line draw, and others. Dedicated pathways are designed to transfer data between host interface (HIF) bus and Drawing Engine, and memory interface (MIF) bus and Drawing Engine. In addition, the drawing engine supports rotation BIBLT for any block size, and automatic self activate rotation BLIT. This feature allows conversion between landscape and portrait display without the need for special software drivers.

LynxEM+ also supports fast DMA BLT, source clear during BLT, transparent BLT, programmable blter stride, page flip, and current scan line refresh.

LynxEM+'s Drawing Engine is also used to bus master captured data to the hard disk drive or to system memory during video capture. To accomplish this, the video capture driver turns on the Drawing Engine Capture Enable bit (DPR0E bit4), selects HOST BLT Read command function (DPR0E [3:0]), and enables PCI bus master mode (SCR17 bit 6). The Video Capture Unit loads the incoming video stream into Capture Buffer 1 or 2, depending on which is idle (VPR3C bit 1 or bit 2 = 0 indicates idle status). The Drawing Engine resets Capture Buffer I or Capture Buffer II control/Status bit to 0 (VPR3C bit 1 or bit 2) after a transfer has completed.

Chapter 8: Zoom Video Port and Video Capture Unit

Zoom Video Port

LynxEM+'s Zoom Video Port (ZV Port) is designed to interface with video solutions implemented as PCMCIA (or PC CardBus) cards: examples are NTSC/PAL decoders, MPEG-2 decoders, and JPEG Codecs. The ZV Port can also directly interface with an NTSC/PAL decoder, such as Phillips 7111 or BT819. Figure 7 illustrates an example of the Phillips video encoder interface via the ZV Port.

Incoming video data from the ZV Port interface can be YUV or RGB format. The data can be interlaced or non-interlaced. The ZV Port can be configured for output if the video capture function is disabled. 18-bit graphics and video data in RGB format can be sent out when the ZV Port is configured for output mode.

The ZV Port may also be configured as a test port. Up to 20 signals from each of the logic blocks within the LynxEM+ can be brought out to an internal test bus (TD Bus) connected to the ZV Port. System designers or silicon validation engineers can access these signals by setting the TEST0, TEST1, USR0, USR1, and USR2 pins. This approach can bring out a total of 180 internal signals to the primary I/O pins. The test port capability can be used to enhance fault coverage, as well as reduce silicon validation or debugging time.

Table 6 lists signal definitions for the following ZV Port interface configurations: YUV input mode, RGB input mode, and graphics/video (output mode).

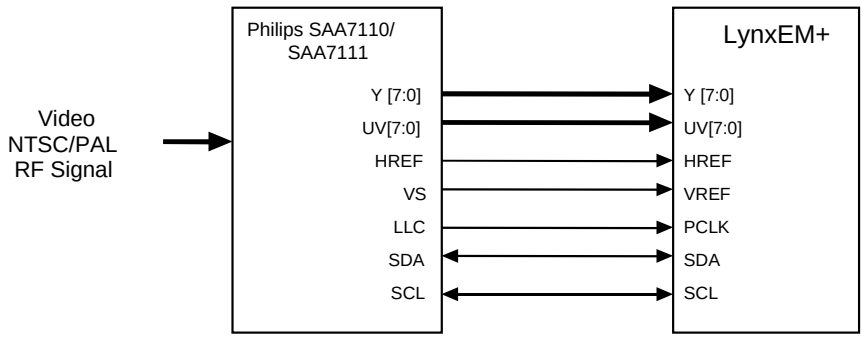


Figure 7: Video Encoder Interface via Video Port

Table 6: LynxEM+ Video Port Interface I/O Configurations

Video Port Interface	ZV Port (Input mode)	I/O	NTSC/PAL Decoder (Input mode)	I/O	Graphics/Video (Output mode)	I/O
VREF	VS	I	VS	I	R2	O
HREF	HREF	I	HREF	I	R3	O
BLANK	(note1)		(note1)		BLANK	O
PCLK	PCLK	I	PCLK	I	PCLK	O
P15	UV7	I	R7	I	R4	O
P14	UV6	I	R6	I	R5	O
P13	UV5	I	R5	I	R6	O
P12	UV4	I	R4	I	R7	O
P11	UV3	I	R3	I	G2	O
P10	UV2	I	G7	I	G3	O
P9	UV1	I	G6	I	G4	O
P8	UV0	I	G5	I	G5	O
P7	Y7	I	G4	I	G6	O
P6	Y6	I	G3	I	G7	O
P5	Y5	I	G2	I	B2	O
P4	Y4	I	B7	I	B3	O
P3	Y3	I	B6	I	B4	O
P2	Y2	I	B5	I	B5	O
P1	Y1	I	B4	I	B6	O
P0	Y0	I	B3	I	B7	O

Note 1: BLANK pin can used as TVCLK output, which is independent of ZV port.

Video Capture Unit

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer. The Video Capture Unit support several features to maintain display quality, and balance the capture rate:

- 2-tap, 3-tap, and 4-tap horizontal filtering
- 2 to 1 and 4 to 1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swap, RGB 5:5:5, and RGB 5:6:5
- Multiple frame skipping methods
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

LynxEM+ uses the Video Processor block to display the captured data on the LCD, TV, or CRT display. The captured data can be displayed through Video Window I or Video Window II. The stretching, color interpolation, YUV-to-RGB conversion, and color key functions are performed in the Video Processor. LynxEM+'s Video Processor can simultaneously process captured video data and perform CD-ROM playback on two independent video windows.

LynxEM+ also supports real-time video capture to the hard drive or system memory through PCI master mode or slave mode. In PCI bus master mode, LynxEM+ uses the Drawing Engine's Host BLT and Host DMA functions to maximize performance.

Functional Description

LynxEM+'s Video Capture Unit supports the Video Port Extension (VPE) specification for video stream processing. This capture unit includes CLIP block, FILTER block, SHRINK block, and FIFO control block. Figure 8 and Figure 9 illustrate the LynxEM+ Video Capture Block Diagram and Data Flow. The CLIP functional block is used to select the desired rectangles from the video stream to be captured. VPR40 register (Video Source Clipping Control) is used to define the upper left corner of the rectangle from the video source. VPR44 register (Video Source Capture Size Control) is used to define the height and width of the rectangle from the video source.

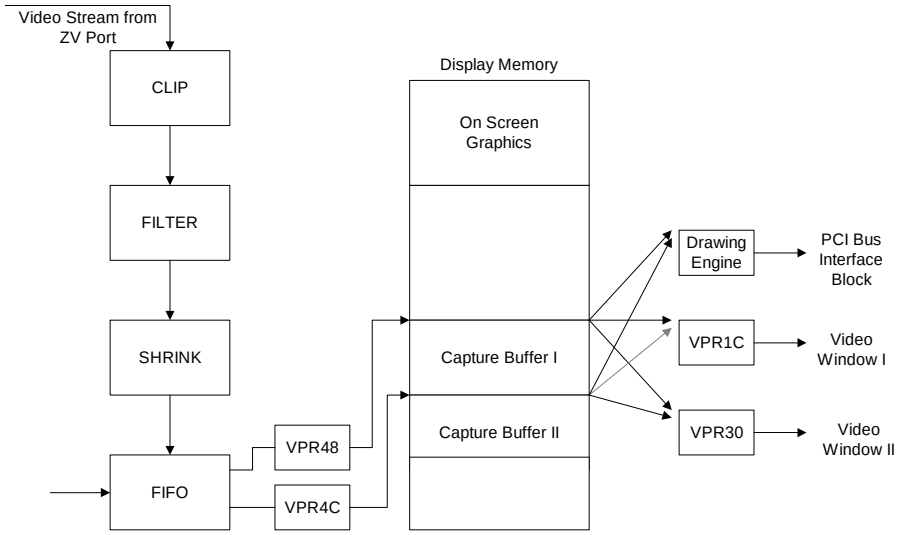


Figure 8: Video Capture Block Diagram

The FILTER functional block controls horizontal filtering logic. VPR3C (Capture Port Control) bit 21 and bit 20 are used to select 2 tap, 3 tap, and 4 tap filtering. The SHRINK functional block is used to not only reduce the storage area for both display memory and hard drive, but also increase performance of video capture and video playback. VPR3C bit 19 and 18 are used to enable vertical reduction, and bit 17 and bit 16 are used to enable horizontal reduction. With filter and shrink functions, LynxEM+ is able to achieve high video capture performance and maintain optimal video playback quality.

VPR3C bit 13 to bit 11 are use to select 8 different frame skipping options in the event the capture rate is less than the incoming video stream. CPR00 bit 10 and bit 9 are used to support interlaced capture and double buffer capture. CPR00 bit 1 and bit 2 are used as control/status bits for Buffer I and Buffer II.

The captured data can be displayed on either Video Window I or Video Window II. The video capture driver needs to program VPR1C (or VPR30), Video Window I (or II) Source Start Address, with the same address value from Capture Port Buffer I or II Start Address register. VPR00 (Miscellaneous Graphics and Video Control) bit 24 may be used to automatically display the capture data on Video Window I without programming VPR1C register. This feature is independent of single buffer or double buffer mode. If double buffer mode is at Video Window I, it will display the buffer which is not currently used to capture data. This feature allows the user to capture interlaced data and together with programming VPR24 bit [23:16] and VPR24 bit [31:24] it will display BOB implementations on Video Window I.

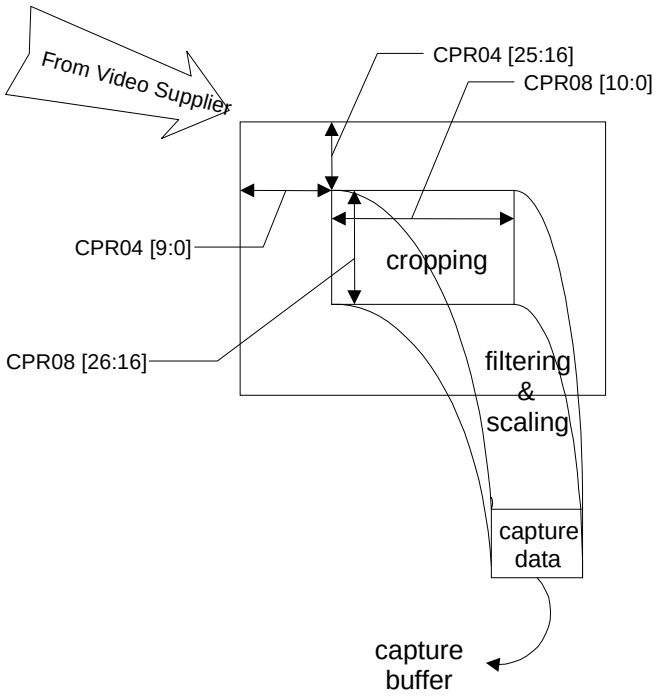


Figure 9: Video Capture Data Flow

Theory of Operation

Initialization

- Enable Video Capture (CPR00 bit 0 = 1)
- Preset Buffer I and Buffer II Status/Control bits (CPR00 [2:1] = 11b)
- Enable Drawing Engine (DPR0E bit 4 = 1)
- Select Host BLT Read Command function (DPR0E [3:0] =9h)
- Enable PCI bus master mode (SCR17 bit 6 = 1)
- Select Field Detection, VREF/HREF polarity, Vertical/Horizontal Reduction, Horizontal Filtering, Video Capture Input Data Format, Frame Skip, Interlaced/non-interlaced and other miscellaneous settings (CPR00, Capture Port Control Register)

Table 7: Bit Setting Summary for Video Capture

B1S	Buffer 1 Status/Control (CPR00 bit 1)
B2S	Buffer 2 Status/Control (CPR00 bit 2)
Continuous Capture	CPR00bit 8 = 0
Conditional Capture	CPR00 bit 8 = 1
Single Buffer	CPR00 bit 9 = 0
Double Buffer	CPR00 bit 9 = 1
Non-interlaced Mode	CPR00 bit 10 = 0
Interlaced Mode	CPR00 bit 10 = 1

The Video Capture Unit supports the following types of capture modes:

- Single Buffer Mode with Continuous Capture
- Single Buffer Mode with Conditional Capture
- Double Buffer Mode with Continuous Capture
- Double Buffer Mode with Conditional Capture
- Interlace and Non-Interlaced Mode

A Summary of each of the video capture modes follows:

- Single Buffer Mode with Continuous Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
3. Continuously capture incoming video data to capture buffer 1 4. Independent of B1S and B2S bits	It is not recommended to use the Drawing Engine to transfer captured data from display memory to hard drive or system memory in this mode. This mode is used to view the captured data only.	1. VPR00 bit 24 = 0 2. Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. 3. VPR00 bit 24 = 1 4. Captured data is automatically displayed on Video Window I.

- Single Buffer Mode with Conditional Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
1. VCU monitors B1S bit 2. If B1S = 1, start capture 3. VCU will reset B1S to 0 after it completes a frame 4. Go to step “a”	1. Test 2. If B1S = 0, SW will activate the DE to transfer captured data from capture buffer 1 to hard drive or system memory 3. DE will set B1S bit to 1 after it completes a frame 4. Go to step "a”	1. VPR00 bit 24 = 0 2. Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. 3. VPR00 bit 24 = 1 4. Captured data is automatically displayed on Video Window I

- Double Buffer Mode with Continuous Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
1. Continuously capture the incoming video data into capture buffer 1 or buffer 2 2. Automatically switch from one buffer to the other when VCU completes a frame 3. Independent of B1S and B2S bits	It is not recommended to use DE to transfer captured data from display memory to hard drive or system memory in this mode. This mode is used to view the captured data only.	1. VPR00 bit 24 = 0 2. Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. 3. 4. VPR00 bit 24 = 1 5. Captured data is automatically displayed on Video Window I. If capture buffer 1 is used by VCU, Video Window I will display captured data from capture buffer 2

- Double Buffer Mode with Conditional Capture

Video Capture Unit (VCU)	Drawing Engine (DE)	Video Processor (VP)
1 VCU monitors B1S and B2S bits 2. If B1S (or B2S) = 1, start video capture and store into capture buffer 1 (or buffer 2). 3. VCU will reset B1S (or B2S) to 0 after it completes a frame 4. VCU will continue video capture if B1S or B2S = 1 5. Go to step "a" if both bits = 0	1. SW monitors B1S or B2S bit 2. If B1S (or B2S) = 0, SW will activate the DE to transfer captured data from capture buffer 1(or buffer 2) to hard drive or system memory 3. DE will set B1S (or B2S) bit to 1 after it completes a frame 4. DE will continuously transfer 5. Data from capture buffer 1 or 2 if B1S or B2S = 0 6. Go to step "a " if both bits = 1	1. VPR00 bit 24 = 0 2. Captured data can be displayed on either Video Window I or Video Window II by setting video window start address register. 3. 4. VPR00 bit 24 = 1 5. Captured data is automatically displayed on Video Window I. If capture buffer 2 is used by VCU, Video Window I will display captured data from capture buffer 1.

- Interlaced Capture

CPR00 bits 10 are used to select the interlaced capture mode. In most of video capture applications, an interlaced video stream will be treated as non-interlaced video stream by dropping all even frames (CPR00[13:11] = 010b), or dropping all odd frames (CPR00[13:11] = 011). This approach will reduce artifacts when playing back the captured data. However, in some video capture applications, de-interlacing is needed to handle the incoming interlaced video stream.

For the de-interlacing case, CPR00 bit 10 needs to be set to 1 to enable interlaced capture for incoming interlaced video stream. The double buffer mode (CPR00 bit 9 = 1) needs to be turned on at the same time. Capture Buffer 1 and Capture Buffer 2 are combined together as a single buffer with one line offset. Figure 9 illustrates the capture buffer structure. The video capture driver will preset B1S and B2S bits to 1 to initialize the buffer 1 and 2 status/control bits. The Video Capture Unit will start video capture if any one of B1S and B2S = 1. After VCU fills capture buffer 1 and 2, both B1S and B2S bits are set to "0" by VCU. The video capture driver will activate Drawing Engine to transfer captured data in capture buffer 1 and 2 to system memory or hard drive when both B1S and B2S are "0". After the completion of the transfer, the Drawing Engine will set both B1S and B2S to "1". The Video Capture Unit then continues video capture and repeats the same protocol.

During video playback, the captured data can be displayed on either Video Window I or Video Window II. It is not recommended to display both even frame and odd frame for video playback. The video captured driver can program Video Window I (or II) Source Start Address Register and Video Window I (or II) Source Width and Offset Register in such a way that odd frame (or even frame) captured data will be dropped during video playback. The scaling, color interpolation, and YUV-to-RGB conversion functions can also be enabled at the same time.

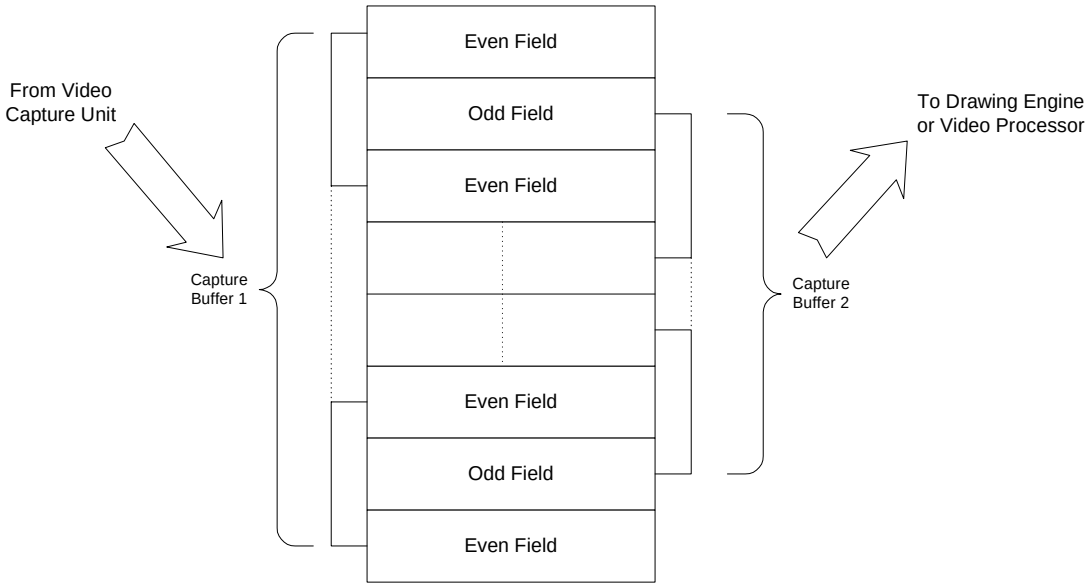


Figure 10: Capture Buffer Structure in Interlaced Mode

Chapter 9: Flat Panel Interface

LynxEM+ supports both color dual scan STN (passive) and color TFT (active) panel interface for notebook computers. It can also support color TFT panel with RGB analog interface. For color TFT panel, LynxEM+ can support single pixel per clock of 9-bit, 12-bit, 18-bit, 24-bit, or double-pixel per clock of 24-bit, 36-bit interfaces up to 1024x768 resolution. Table 8 lists the complete set of LynxEM+ panel interface pins for both color DSTN and TFT LCD. Figure 12 shows the single-pixel per clock TFT interface, Figure 13 shows the double-pixel per clock TFT interface, Figure 14 shows the 16-bit DSTN interface, and Figure 15 shows the 24-bit DSTN interface.

EMI Reduction Circuit

The LynxEM+ provides an EMI reduction circuit for the flat panel interface. The EMI circuit is controlled by the EMI Control Register (Address: 3C5h Index: 58h). EMI reduction control is enabled by setting bit 3 to a logical 1. When the circuit is turned on, the flat panel interface signals are driven in independent groups (e.g. for a 24-bit interface, 4 groups of 6 signals each) which are delayed by small time delta relative to one another. This approach eliminates noise peaks which occur when significant numbers of flat panel interface signals transition at the same time. The EMI spectrum is therefore flattened out and EMI is reduced.

LynxEM+ Flat Panel Enhancements

LynxEM+ integrates various flat panel enhancement features such as: LCD screen auto-centering, LCD screen expansion (including XY interpolated screen expansion), Virtual Refresh, and special dithering engines for TFT and DSTN flat panels.

LynxEM+ Graphics/Text Expansion Information

Introduction

LynxEM+ provides full expansion capability for text and graphics modes. Text as well as graphics expansion is supported up to XGA resolution. Expansion is supported on TFT and DSTN panels. A detailed description of the expansion algorithms of these devices follows:

Horizontal Expansion for Text and Graphics

Horizontal expansion is handled in 8 pixel pieces whether the mode is text or graphics. There are two expansion mechanisms: 10-dot expansion and 12-dot expansion. 10-dot expansion is used to expand to 800 pixels, 12-dot is used to expand to 960 pixels for XGA panel sizes.

For 10-dot expansion, every 4th pixel is duplicated. For example, for mode3h (80x25 text) or mode 12h(640x480 graphics), where p0 is pixel one and p7 is pixel 8 - p0p1p2**p3p3**p4p5p6**p7p7** - the 4th pixel (p3) is duplicated, as well as the 8th pixel (p7). The pattern repeats for each 8 pixel piece.

For 12-dot expansion, every other pixel, beginning with p1 is duplicated. For example, for mode 3h or mode 12h - p0**p1p1**p2**p3p3**p4**p5p5**p6**p7p7**. Again, the pattern repeats for each pixel piece.

So far, all examples assume 8x16 font size. There is also 9x16 font size to consider (in this case the actual font is still 8x16, but an additional 9th dot - either the background color or a repeat of the 8th pixel - is inserted). For 9x16 case, pixel p3 is duplicated just like 8x16 case. Pixel p7 is handled somewhat differently depending on whether the character is a text character or graphics character - for text character case, the second p7 value becomes the background color. For graphics case, p7 is repeated.

Vertical Expansion for Text and Graphics

Vertical expansion for text or graphics uses a Dynamic Duplication Algorithm (DDA) method to achieve expansion. The same basic methodology is used independent of resolution. First, an initial DDA constant value (for LynxEM+ this is a 10-bit value) is loaded into the Vertical Screen Expansion DDA Constant Registers. This value is used as part of a logical algorithm to determine which lines on the display to duplicate. Figure 11 is a diagram of the algorithm.

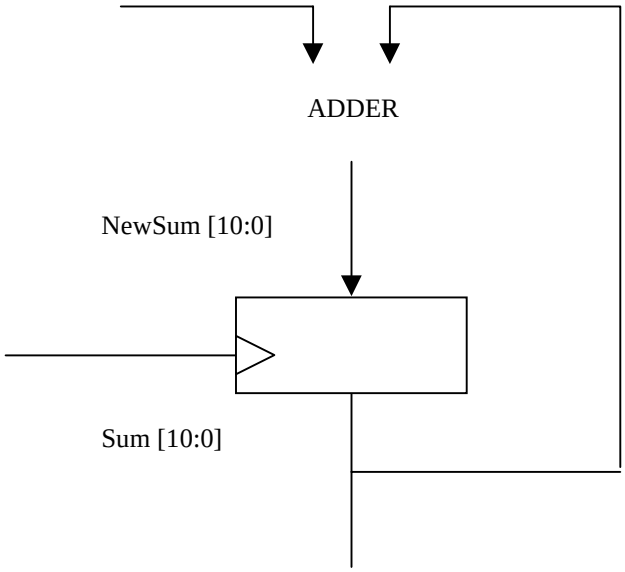


Figure 11: DDA Expansion Algorithm

For each line of the display, the following equation is calculated via the illustrated algorithm:

NewSum [10:0] = Sum[10:0] + DDA

If Sum [10:0] = NewSum [10:0], the given line is duplicated.

For text case, the DDA logic algorithm will reset each character block, so expansion is handled in terms of character rows (e.g. 25 character rows of 16 lines each). For the graphics case, the DDA logic algorithm will reset when the bottom of the display is reached.
The DDA constant may be calculated by the following equation:

$$\frac{1024}{DDA} = \frac{\text{Expanded Resolution}}{\text{Existing Resolution}}$$

For example, to expand a 480 line mode to 768, the equation would be:

$$\frac{1024}{DDA} = \frac{768\ \text{Lines}}{480\ \text{Lines}}$$

DDA constant may then be calculated and entered into the expansion algorithm.

DDA[9:0]

LCD Dithering Engine

LynxEM+ has separate dithering engines for color DSTN LCD and color TFT LCD. The DSTN dithering engine includes a set of 32 different dithering patterns which are developed with LCD's response time and contrast ratio in mind. FPR32 bit 5 is used to select 16 gray levels or 32 gray levels for each Red, Green, and Blue color. The TFT dithering engine includes a set of 8 different dithering patterns which combine frame rate modulation and space dithering algorithm. FPR32 bit 7 and 6 are used to select 4-gray level dithering, 8-gray level dithering, and no dithering.

Flat Panel Power ON/OFF Sequencing

LynxEM+ integrates logic for panel power ON/OFF sequencing during power down modes and display switching.

There are two ways to power ON/OFF the flat panel: hardware panel power sequencing and software panel power sequencing.

Hardware panel power sequencing:

Hardware panel power sequencing is selected when FPR34 bit 7 =1. Whenever FPR31 bit toggles, LynxEM+ automatically controls LCD data, LCD controls, FPEN, FPVDD, and VBIASEN pins. FPR33 [3:2] determines the time period from FPEN to VBIASEN, from VBIASEN to LCD controls/data, and from LCD controls/data to FPVDDEN.

FPR33[3:2]	Power On Sequencing Time Select
00	1 vertical frame
01	2 vertical frames
10	4 vertical frames
11	8 vertical frames

Figure 16 shows the auto panel power on sequencing timing relationship. Figure 17 shows the auto panel power off sequencing timing relationship.

For flat panels which have non-standard requirements for on/off power sequencing, LynxEM+ supports panel power on/off sequencing through software programming.

Below are examples of software programming for panel power on sequencing:

Software panel power sequencing- ON:

- Set FPR34 bit 7 = 0 (software panel power sequencing)
- Setup shadow registers: SVR40 to SVR4B
- Set FPR31 bit 0 = 1 (enable LCD display)
- After X vertical frames, set PDR22 bit 0 = 1 (turn on FPVDDEN)
- After X vertical frames, set PDR22 bit 1 = 1 (enable LCD controls and data)
- After X vertical frame, set PDR22 bit 2 = 1 (turn on VBIASEN)
- After X vertical frames, set PDR22 bit 3 = 1 (turn on FPEN)

Note: LCD backlight control is independent of power sequencing. The VBKLGT can be turned on at the same time as FPEN.

Software panel power sequencing - OFF:

- Set FPR34 bit 7 = 0 (software panel power sequencing)
- Select FPR33 [3:2] for panel power on/off timing:
- Set PDR22 bit 3 = 1 (turn on FPEN)
- After X vertical frames, set PDR22 bit 2 = 1 (turn on VBIASEN)
- After X vertical frames, set PDR22 bit 1 = 1 (enable LCD controls and data)
- After X vertical frames, set PDR22 bit 0 = 1 (turn on FPVDDEN)
- Set FPR31 bit 0 = 0 (disable LCD display)

Table 8: Flat Panel Interface Pins listing for color DSTN and color TFT LCD

LynxEM+	**Color DSTN**			**Color TFT**				
Pin Name	***16-bit***	***24-bit***	***9-bit***	***12-bit***	***18-bit***	***24-bit***	***12-bit x2***	***18-bit x2***
LP/FHSYNC	LP	LP	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
FP/FVSYNC	FP	FP	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
FPSCLK	XCK	XCK	CK	CK	CK	CK	CK	CK
DE			ENAB	ENAB	ENAB	ENAB	ENAB	ENAB
FPEN	FPEN	FPEN	FPEN	FPEN	FPEN	FPEN	FPEN	FPEN
FDA23		UD11				R7	RB3	RB3
FDA22		UD10				R6	RB2	RB2
FDA21		UD9			R5	R5	RB1	RB1
FDA20		UD8			R4	R4	RB0	RB0
FDA19	UD7	UD7		R3	R3	R3	RA3	RA3
FDA18	UD6	UD6	R2	R2	R2	R2	RA2	RA2
FDA17	UD5	UD5	R1	R1	R1	R1	RA1	RA1
FDA16	UD4	UD4	R0	R0	R0	R0	RA0[1]	RA0
FDA15	UD3	UD3				G7	GB3	GB3
FDA14	UD2	UD2				G6	GB2	GB2
FDA13	UD1	UD1			G5	G5	GB1	GB1
FDA12	UD0	UD0			G4	G4	GB0[1]	GB0
FDA11		LD11		G3	G3	G3	GA3	GA3
Pin Name	***16-bit***	***24-bit***	***9-bit***	***12-bit***	***18-bit***	***24-bit***	***12-bit x2***	***18-bit x2***
FDA10		LD10	G2	G2	G2	G2	GA2	GA2
FDA9		LD9	G1	G1	G1	G1	GA1	GA1
FDA8		LD8	G0	G0	G0	G0	GA0	GA0
FDA7	LD7	LD7				B7	BB3	BB3
FDA6	LD6	LD6				B6	BB2	BB2
FDA5	LD5	LD5			B5	B5	BB1	BB1
FDA4	LD4	LD4			B4	B4	BB0	BB0
FDA3	LD3	LD3		B3	B3	B3	BA3	BA3
FDA2	LD2	LD2	B2	B2	B2	B2	BA2	BA2

LynxEM+	Color DSTN			Color TFT				
FDA1	LD1	LD1	B1	B1	B1	B1	BA1	BA1
FDA0	LD0	LD0	B0	B0	B0	B0	BA0	BA0
FPVDDEN	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
VBIASEN	VEE	VEE	VEE	VEE	VEE	VEE	VEE	VEE
[2]P11 (FDA35)								RB5
P10 (FDA34)								RB4
P9 (FDA33)								RA5
P8 (FDA32)								RA4
P7 (FDA31)								GB5
P6 (FDA30)								GB4
P5 (FDA29)								GA5
P4 (FDA28)								GA4
P3 (FDA27)								BB5
P2 (FDA26)								BB4
P1 (FDA25)								BA5
P0 (FDA24)								BA4

[1] RA0 denotes first pixel of R0 for 2 pixels/clk interface. RB0 denotes second pixel of R0 for 2 pixels/clk interface.
[2] For LynxEM+ SM712 pinout, upper 12 bits of panel data multiplexed with ZV port pins P11-P0.

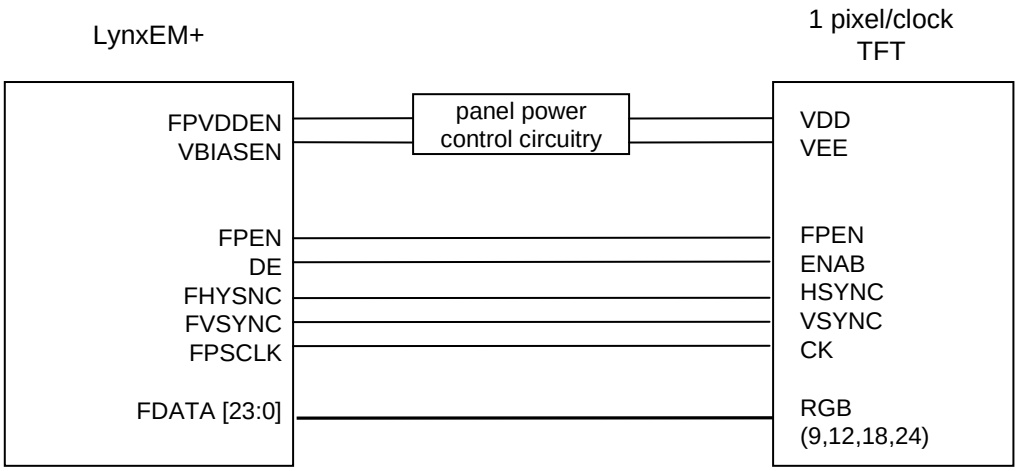


Figure 12: TFT (Single Pixel/Clock) Interface Diagram

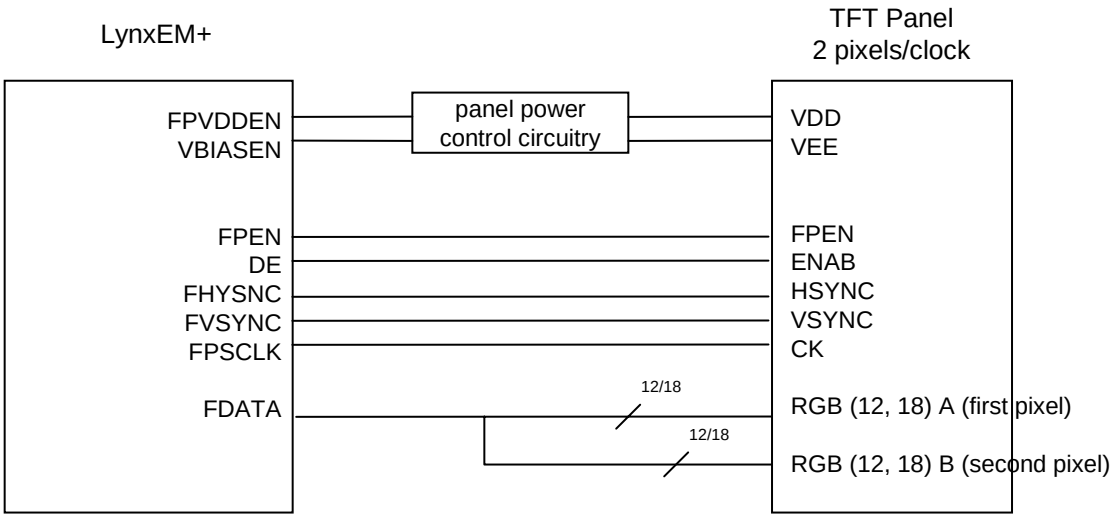


Figure 13: TFT Panel (2 pixels/clock) Interface Diagram

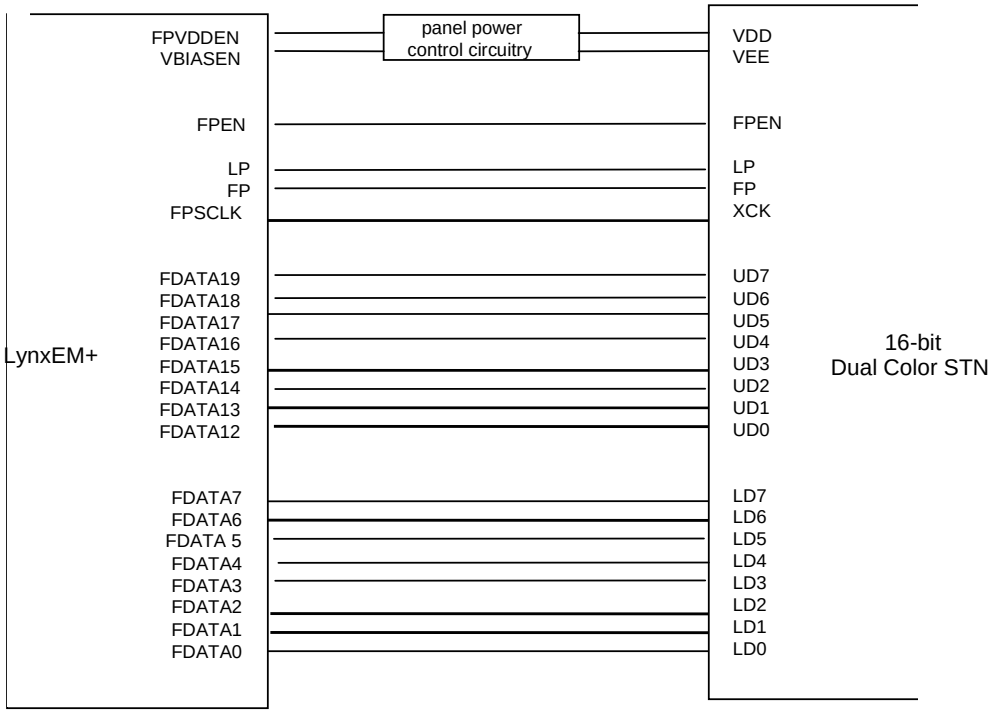


Figure 14: 16-bit DSTN Interface Configuration

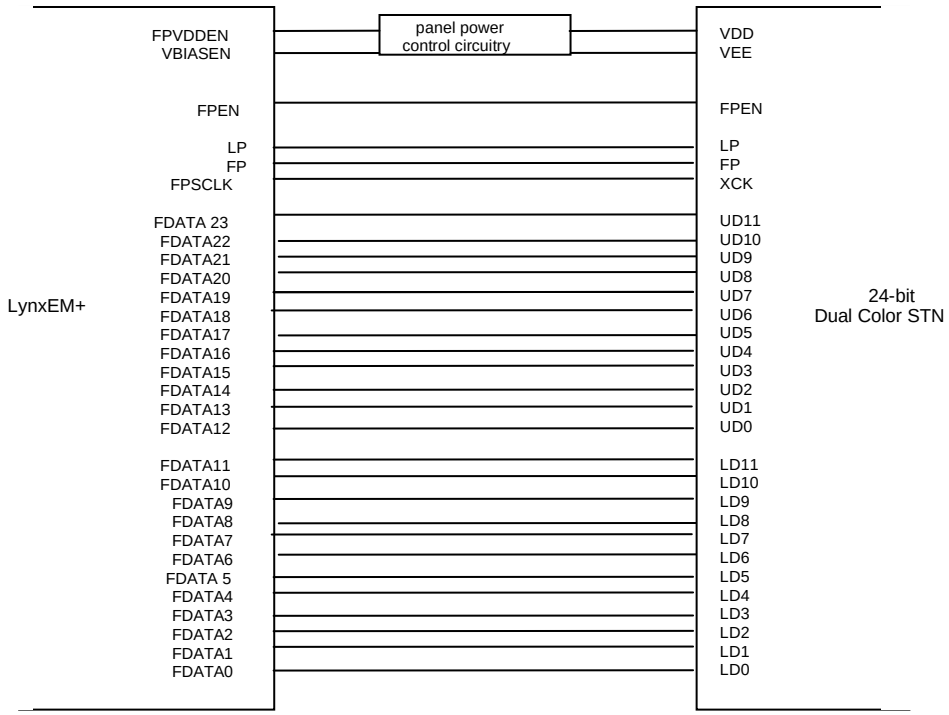
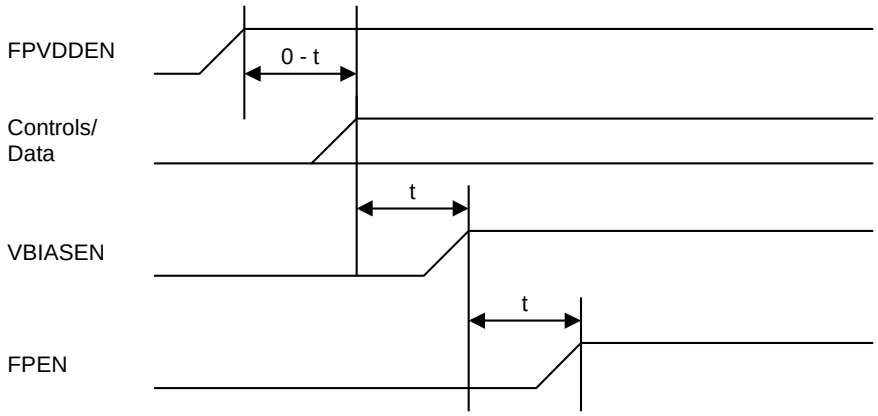


Figure 15: 24-bit Dual Color STN Interface Diagram



t is programmed via FPR33 [3:2]

Figure 16: Panel Power On Sequencing Timing Diagram

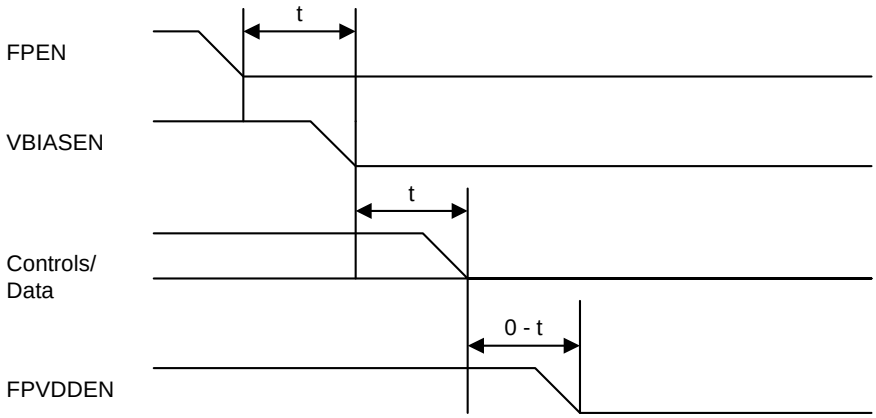


Figure 17: Panel Power Off Sequencing Timing Diagram

FPR33[3:2]	Power On/Off Sequencing Time Select
00	1 vertical frame
01	2 vertical frames
10	4 vertical frames
11	8 vertical frames

LVDS Chipset Interface

In order to address EMI and cable issues associated with a wide, high speed TTL/CMOS panel interface, designers may choose to use an LVDS (Low Voltage Differential Signaling) chipset or a PanelLink chipset (each chipset type includes a transmitter and a receiver). Examples of the LVDS chipset include National Semiconductor DS90C383/4 (3.3V, 65 MHz) or Texas Instruments' SN75LVDS83/2 (3.3V, 65 MHz); the copyists from these vendors are pin-compatible. The PanelLink chipset is available from Silicon Image (SiI100). LynxEM+ supports a direct interface to the transmitter of either LVDS or PanelLink chipset types. Figure 18 and Figure 19 illustrate the 24-bit interfaces for TFT and DSTN LVDS panels. Figure 21 and Figure 22 illustrate the 24-bit interfaces for TFT and DSTN PanelLink panels. For 36-bit LVDS interface (2 channel LVDS), please refer to Figure 20.

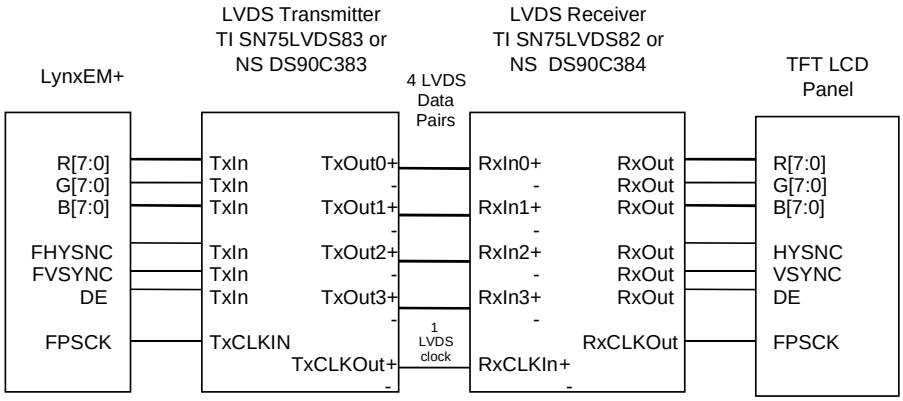


Figure 18: LVDS Interface with TFT LCD Panel

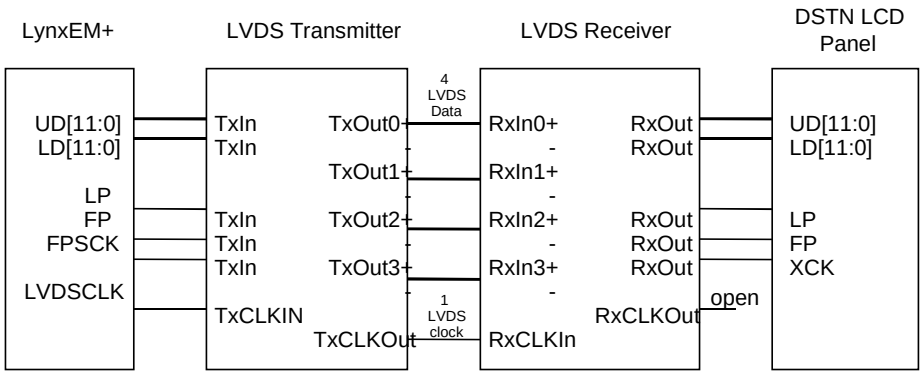


Figure 19: LVDS Interface with DSTN LCD Panel

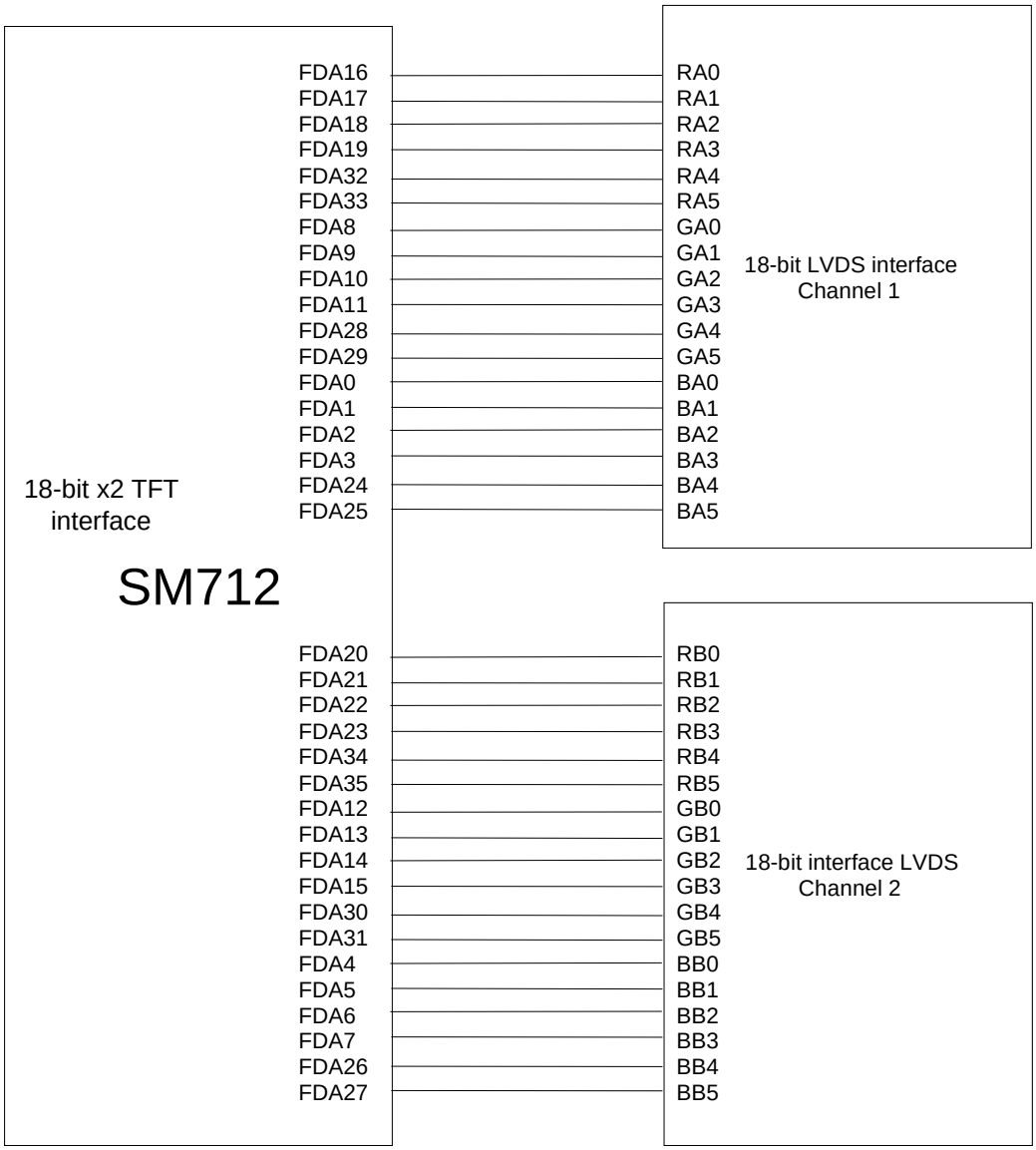


Figure 20: 36-bit (18x2-bit) TFT Interface Diagram

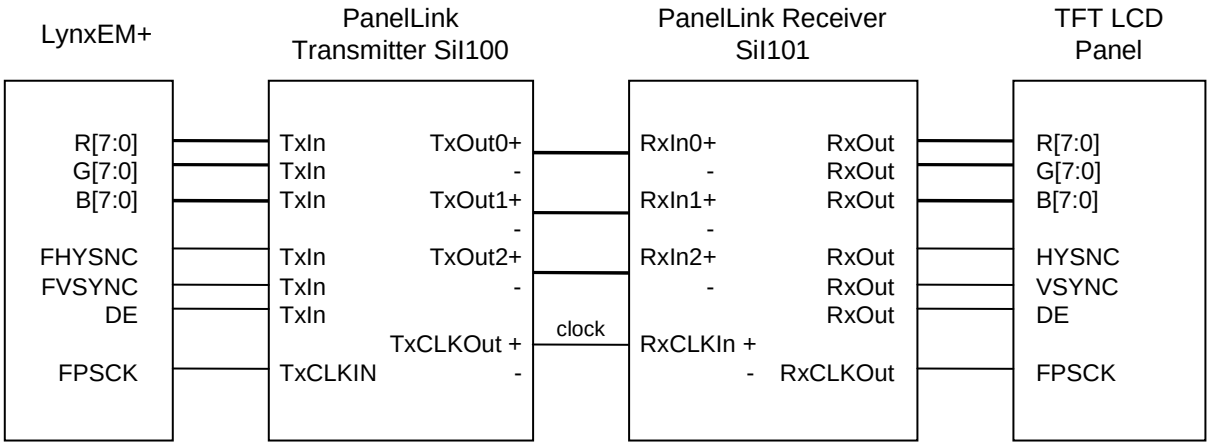


Figure 21: PanelLink Interface with TFT LCD Panel

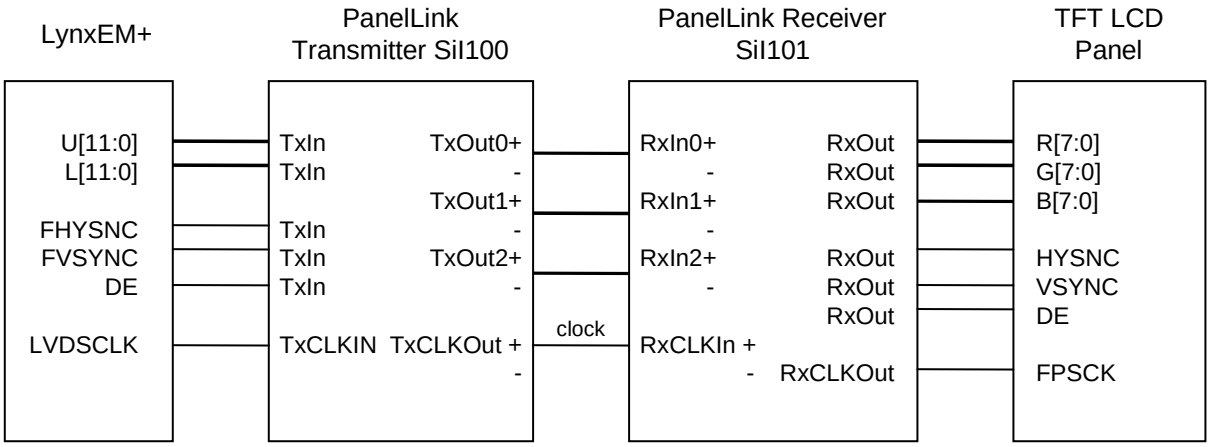


Figure 22: PanelLink Interface with DSTN LCD Panel

Table 9 and Table 10 list the pin mapping for an LVDS transmitter with LynxEM+ for LVDS TFT and DSTN panels. Table 11 and Table 12 list the pin mapping for a PanelLink transmitter with LynxEM+ for PanelLink TFT and DSTN panels.

Please consult your panel manufacturer to verify the pin mapping between the LVDS receiver and the panel. The pin mapping from the transmitter side must correspond with the pin mapping from the receiver side in order to ensure that the panel will function properly.

Table 9: LVDS Transmitter Pin Mapping for TFT Interface

LynxEM+ Pin Name	TFT interface	LVDS Transmitter SN75LVDS83/DS90C383 Pin #	LVDS Transmitter Pin Name
FPDATA16	R0	51	TxIN0
FPDATA17	R1	52	TxIN1
FPDATA18	R2	54	TxIN2
FPDATA19	R3	55	TxIN3
FPDATA20	R4	56	TxIN4
FPDATA21	R5	3	TxIN6
FPDATA22	R6	50	TxIN27
FPDATA23	R7	2	TxIN5
FPDATA8	G0	4	TxIN7
FPDATA9	G1	6	TxIN8
FPDATA10	G2	7	TxIN9
FPDATA11	G3	11	TxIN12
FPDATA12	G4	12	TxIN13
FPDATA13	G5	14	TxIN14
FPDATA14	G6	8	TxIN10
FPDATA15	G7	10	TxIN11
FPDATA0	B0	15	TxIN15
FPDATA1	B1	19	TxIN18
FPDATA2	B2	20	TxIN19
FPDATA3	B3	22	TxIN20
FPDATA4	B4	23	TxIN21
FPDATA5	B5	24	TxIN22
FPDATA6	B6	16	TxIN16
FPDATA7	B7	18	TxIN17
LP/FHSYNC	FHSYNC	27	TxIN24
FP/FVSYNC	FVSYNC	28	TxIN25
DE	DE	30	TxIN26
-	-	25	TxIN23
FPSCLK	FPSCLK	31	TxCLKIN

Table 10: LVDS Transmitter Pin Mapping for DSTN Interface

LynxEM+ Pin Name	STN interface	LVDS Transmitter SN75LVDS83/DS90C383 Pin #	LVDS Transmitter Pin Name
FPDATA12	UD0	12	TxIN13
FPDATA13	UD1	14	TxIN14
FPDATA14	UD2	8	TxIN10
FPDATA15	UD3	10	TxIN11
FPDATA16	UD4	51	TxIN0
FPDATA17	UD5	52	TxIN1
FPDATA18	UD6	54	TxIN2
FPDATA19	UD7	55	TxIN3
FPDATA20	UD8	56	TxIN4
FPDATA21	UD9	3	TxIN6
FPDATA22	UD10	50	TxIN27
FPDATA23	UD11	2	TxIN5
FPDATA0	LD0	15	TxIN15
FPDATA1	LD1	19	TxIN18
FPDATA2	LD2	20	TxIN19
FPDATA3	LD3	22	TxIN20
FPDATA4	LD4	23	TxIN21
FPDATA5	LD5	24	TxIN22
FPDATA6	LD6	16	TxIN16
FPDATA7	LD7	18	TxIN17
FPDATA8	LD8	4	TxIN7
FPDATA9	LD9	6	TxIN8
FPDATA10	LD10	7	TxIN9
FPDATA11	LD11	11	TxIN12
LP/FHSYNC	LP	27	TxIN24
FP/FVSYNC	FP	28	TxIN25
DE	-	30	TxIN26
FPSCLK	FPSCLK	25	TxIN23
LVDSCLK	LVDSCLK	31	TxCLKIN

Table 11: PanelLink Transmitter Pin Mapping for TFT Interface

LynxEM+ Pin Name	TFT interface	PanelLink Transmitter SiI100 Pin #	PanelLink Transmitter Pin Name
FPDATA16	R0	63	D0
FPDATA17	R1	62	D1
FPDATA18	R2	61	D2
FPDATA19	R3	60	D3
FPDATA20	R4	59	D4
FPDATA21	R5	58	D5
FPDATA22	R6	57	D6
FPDATA23	R7	56	D7
FPDATA8	G0	55	D8
FPDATA9	G1	54	D9
FPDATA10	G2	52	D10
FPDATA11	G3	51	D11
FPDATA12	G4	50	D12
FPDATA13	G5	49	D13
FPDATA14	G6	48	D14
FPDATA15	G7	47	D15
FPDATA0	B0	46	D16
FPDATA1	B1	44	D17
FPDATA2	B2	43	D18
FPDATA3	B3	42	D19
FPDATA4	B4	41	D20
FPDATA5	B5	40	D21
FPDATA6	B6	38	D22
FPDATA7	B7	37	D23
LP/FHSYNC	FHSYNC	2	HSYNC
FP/FVSYNC	FVSYNC	3	VSYNC
DE	DE	1	DE
FPSCLK	FPSCLK	12	IDCK

Table 12: PanelLink Transmitter Pin Mapping for DSTN Interface

LynxEM+ Pin Name	STN interface	PanelLink Transmitter SiI100 Pin #	PanelLink Transmitter Pin Name
FPDATA12	UD0	50	D12
FPDATA13	UD1	49	D13
FPDATA14	UD2	48	D14
FPDATA15	UD3	47	D15
FPDATA16	UD4	63	D0
FPDATA17	UD5	62	D1
FPDATA18	UD6	61	D2
FPDATA19	UD7	60	D3
FPDATA20	UD8	59	D4
FPDATA21	UD9	58	D5
FPDATA22	UD10	57	D6
FPDATA23	UD11	56	D7
FPDATA0	LD0	46	D16
FPDATA1	LD1	44	D17
FPDATA2	LD2	43	D18
FPDATA3	LD3	42	D19
FPDATA4	LD4	41	D20
FPDATA5	LD5	40	D21
FPDATA6	LD6	38	D22
FPDATA7	LD7	37	D23
FPDATA8	LD8	55	D8
FPDATA9	LD9	54	D9
FPDATA10	LD10	52	D10
FPDATA11	LD11	51	D11
LP/FHSYNC	LP	2	HSYNC
FP/FVSYNC	FP	3	VSYNC
DE	DE	1	DE
LVDSCLK	LVDSCLK	12	IDCK

Chapter 10: Miscellaneous Functions

This chapter describes functions of LynxEM+ such as the Video ROM BIOS interface, VESA DPMS, and I^2C / VESA DDC2B.

Video BIOS ROM Interface

The Video BIOS contains code for chip power-on initialization, graphics mode setup, and various read/write routines to the frame buffer. The Video BIOS can be burned LynxEM+ into a separate video BIOS EPROM (this is the typical case for add-in cards) or be integrated into the system BIOS ROM (this is the typical case for a motherboard graphics implementation).

To support separate video BIOS ROM access, BIOS address decode must be enabled by setting CSR30 (Expansion ROM Enable Base Address Register) bit 0 = 1. For implementations where video BIOS is integrated into the system BIOS ROM, BIOS address decode access must be disabled by clearing CSR30 bit 0.

Figure 23 shows the external video BIOS ROM configuration interface for LynxEM+. The ~ROMEN (ROM Enable) signal from LynxEM+ connects to the OE and CE signals of the BIOS ROM. Since video BIOS ROM address and data are shared with the video memory data (MD) lines, programmers must ensure that the memory bus is inactive when reading from the Video BIOS ROM. For this case, the Video BIOS ROM must be read out and shadowed (typically in system memory at C0000) immediately after reset. Direct physical access to the Video BIOS must then be disabled to prevent interference with ensuing graphics operations.

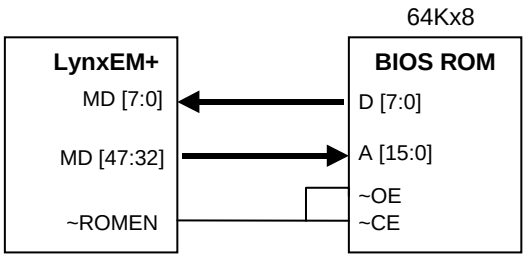


Figure 23: Video BIOS ROM Configuration Interface

VESA DPMS Interface

LynxEM+ supports the VESA Display Power Management Signaling (DPMS) via direct programming PDR22 (LCD Panel Control Select Register) bits 5, 4, or through implementation of the chip's power down states. Table 13 shows the VESA DPMS states and methods for entering each of the DPMS states.

Table 13: DPMS Summary

DPMS State	HSYNC State	VSYNC State	RGB State	Direct Programming Method	Power Down State Method
ON	Pulses	Pulses	Active	PDR22 [5:4] = 00	-
Standby	No pulses	Pulses	Blank	PDR22 [5:4] = 01	Automatic Standby DPMS state when enter Standby mode
Suspend	Pulses	No pulses	Blank	PDR22 [5:4] = 10	CCR69[2]=0 selects Suspend DPMS state when in Sleep mode
OFF	No pulses	No pulses	Blank	PDR22 [5:4] = 11	CCR69[2]=1 selects OFF DPMS state when in Sleep mode

I^2C Bus or VESA DDC2B Interface

LynxEM+ provides dual ports for I^2C-Bus through USR [3:0] I/O pins for various applications such as VESA's DDC2B monitor interface. It is recommended to use USR1 and USR0 as the primary port for SDA and SCL signals on I^2C Bus. USR3 and USR2 are reserved as a secondary port. GPR72 (User Defined Register 1) and GPR73 (User Defined Register 2) are defined to support I^2C/DDC2 bus protocol. LynxEM+, as an I^2C master controller only, is designed to initiate a transfer, generate clock signal, and terminate a transfer to a slave I^2C component.

LynxEM+'s I^2C-Bus interface is designed to interface with NTSC/PAL decoders, Proems, audio decoders, and others. Each of the USR [3:0] I/O pins has an internal pull-up resistor. To enable the data (SDA) and the clock (SCL) from LynxEM+'s primary port, bit 5 and bit 4 of GPR72 (3C5h index 72h) must be set as "11". To drive a logic "0" to SDA line (USR1) and SCL line (USR0), program GPR72 bit 1 and bit 0 to "0". The SDA and SCL can be read back from bit 3 and bit 2 of GPR72.

Figure 24 shows the basic I^2C-Bus protocol of LynxEM+ as a master transmitter.

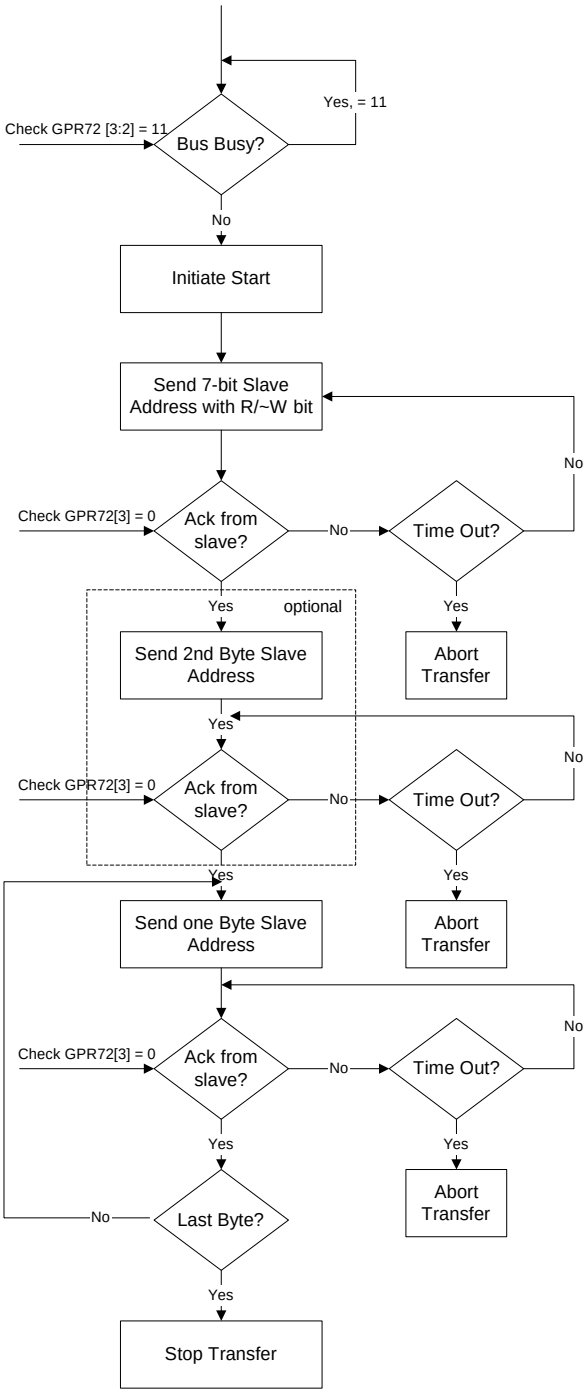


Figure 24: LynxEM+ I^{2}C Bus Protocol Flow Chart

Chapter 11: Clock Synthesizers

LynxEM+ integrates three programmable clock synthesizers for memory clock (MCLK), Video Clock 1 (VCLK), and Video Clock 2(VCLK2). VCLK1 is utilized for standard CRT only, LCD only, or CRT/LCD display modes for which the refresh rate for both devices is the same. VCLK2 may be utilized when Virtual Refresh mode is implemented - for this case, VCLK1 is utilized for panel timing and to clock the panel display block within LynxEM+. VCLK2 may be utilized to clock the CRT interface independently for LCD/CRT display modes or to independently clock various functional blocks within the device to save power under LCD only display mode. Please see the Virtual Refresh discussion under the Power Management section for additional details regarding power saving capabilities under Virtual Refresh architecture.

Figure 25 illustrates the control logic for MCLK, VCLK, VCLK2. The figure also shows the clock generator module for WFIFO (WFIFOCLK), RFIFO (RFIFOCLK), RAM (RAMCLK), Video Capture (VCMCLK), Drawing Engine (DPMCLK), and Video Processor (VPCLK). TVCLK is used for an external analog TV encoder (this clock is either derived from 14.318MHz base clock - NTSC, or from separate 17.734480MHz clock source connected to input signal PALCLK - PAL).

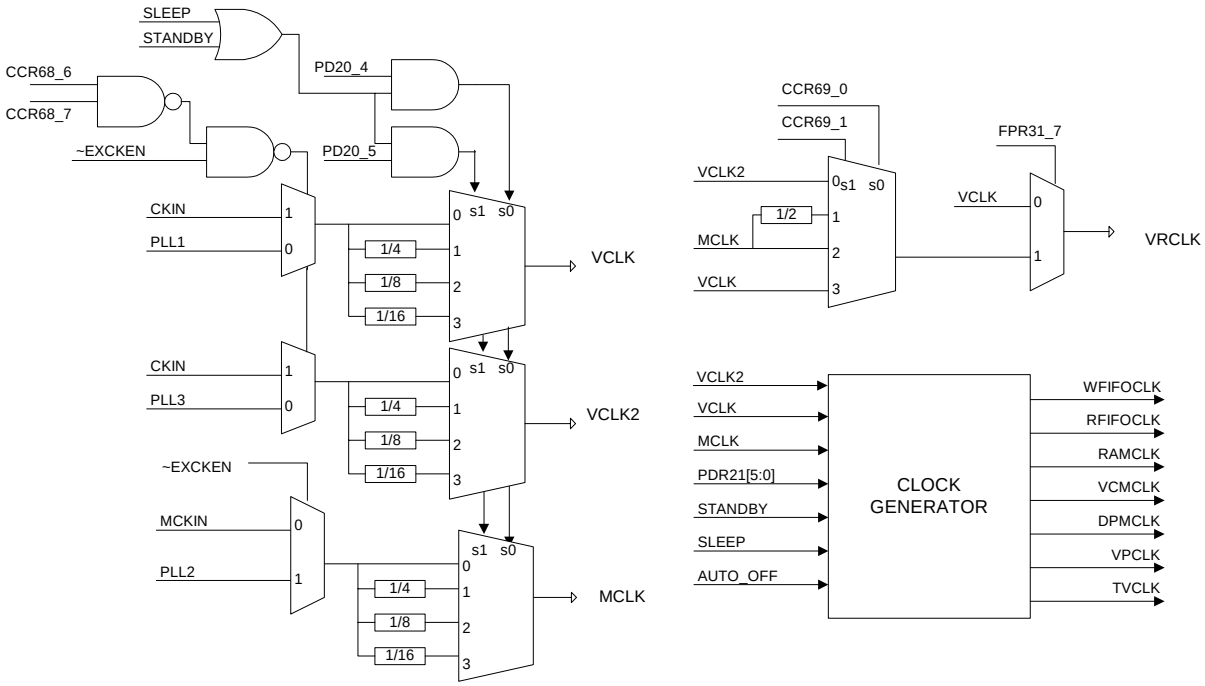


Figure 25: Clocks Generator Block Diagram

The VCLK PLL is programmed using the VCLK Numerator Register (VNR), CCR6C, and VCLK Denominator (VDR) and Post Scalar (PS) register, CCR6D. The VCLK frequency is based on the following equation:

$$VCLK = 14.31818\ MHz \times \frac{VNR}{VDR} \times \frac{1}{1+PS}$$

The post scalar is used to support VCLK frequencies which need a large VDR number. With PS enabled, the VDR number can be set to ½ of the original VDR number. This helps to reduce jitter and maintain accuracy.

The VCLK2 PLL is programmed using the VCLK2 Numerator Register (VCLK2NR), CCR6E, and VCLK Denominator (VCLK2DR) register CCR6F. The VCLK2 frequency is based on the following equation:

$$VCLK2 = 14.31818\ Mhz * \frac{VCLK2NR}{VCLK2DR}$$

Table 14: Recommended VNR and VDR Values for Common VCLK Settings

Mode	Ref. Rate	CCR68 [7]	CCR68 [6]	CCR68 [5]	3C2.3	3C2.2	VCLK (MHZ)	VNR	VDR
640x480	60Hz	0	01	0	0	0	25.180	33h	1Dh
720x400									
(text)	70Hz	0	0	0	0	1	28.325	5Bh	97h2
640x480	85Hz	0	0	1	0	0	31.500	2Ch	14h
800x600	56Hz	0	0	1	0	1	35.484	39h	17h
--	--	1	1	x	x	x	14.318	x	x
800x600	72Hz	0	1	x	x	x	49.517	53h	18h
1024x768	75Hz	0	1	x	x	x	78.750	6Eh	14h

Notes:
1. VNR and VDR numbers are hard coded in VGA modes.
2. Post scalar enabled.

The MCLK PLL is programmed using the MCLK Numerator Register (MNR), CCR6A, and MCLK Denominator Register (MDR), CCR6B. MCLK frequency is based on the following equation:

$$MCLK = 14.31818\ MHz \times \frac{MNR}{MDR}$$

Chapter 12: Multimedia RAMDAC

LynxEM+ contains a multimedia RAMDAC, which supports gamma correction with a maximum frequency of 135 MHz (3.3V power supply). The multimedia RAMDAC includes two 256 x 18 color palette RAMs (RAM0 for CRT display, RAM1 for LCD display), RAM Sequencer, Hardware Cursor Registers (foreground and background), Hardware Pop-up Icon Registers (foreground and background), Data Mixer, Power-On Reset, Bias circuit, Monitor Detect circuit, and three 8-bit DACs (R, G and B). Anti-flicker logic for I/O read/writes is also built in the color palette RAM blocks. Figure 26 shows a block diagram of LynxEM+ Multimedia RAMDAC.

LynxEM+ uses an internal band gap voltage reference circuit to supply the reference voltage. This circuit automatically compensates for temperature and power supply variation. The external portion of the circuit consists of a single RSET resistor used to set the full scale voltage of RGB output from DAC.

The RAMDAC supports two types of modes, color palette index mode and direct color mode. In color palette index mode, the 8-bit input data of a given pixel goes to the color palette RAM block through VGA mask register. In direct color mode, if gamma correction is off pixel data will bypass the color palette RAM. If gamma correction is on, the pixel data will go through the color palette RAM which is being used as a gamma correction look up. To activate gamma correction refer to CCR65: TV Encoder Control Registers.

LCD Backend RAM (RAM1)

LynxEM+ includes a separate 18-bit RAM (6 bits each RGB) module for the LCD backend. The RAM allows support for color palette index modes for the LCD display. This RAM module is written concurrently with RAM0.

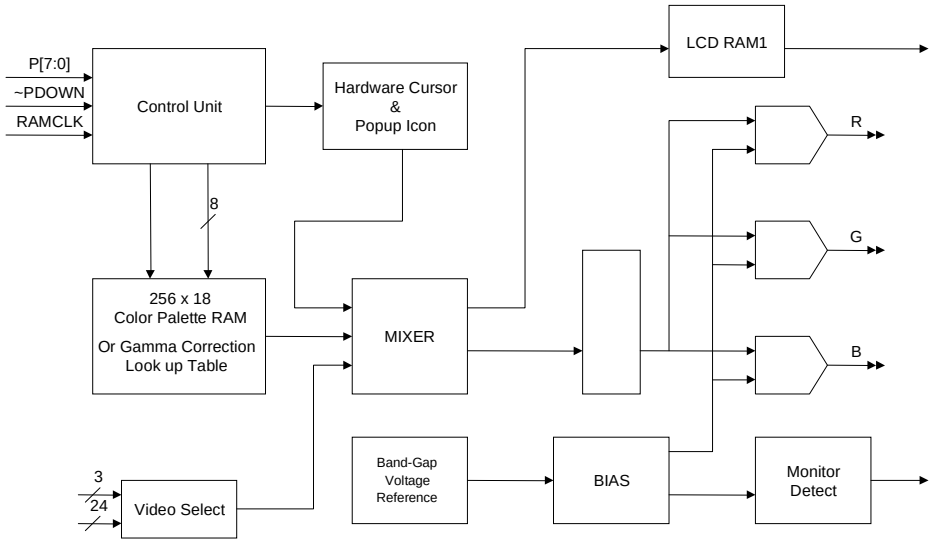


Figure 26: LynxEM+ RAMDAC Block Diagram

Chapter 13: Signature Analyzer

LynxEM+ includes several built-in test features to enhance testability and fault coverage. LynxEM+'s signature analyzer is designed to reduce LSI tester time and manufacturing test time. This signature analyzer resides within the Video Processor block and receives 24-bit RGB data from Multimedia RAMDAC block. It can be used to test CRT graphics modes, TV display modes, and motion video with single frame data. It can also be used to test data combinations such as: graphics, video 1, video 2, HW cursor, and HW pop-up icon at the same time.

The primary variables for a the signature analyzer are the length of the internal shift registers and the number of feedback terms. LynxEM+ implements the CRC-CCITT polynomial (X16 + X12 + X5 + 1) on a 16-bit signature shift register. VPR64 (Signature Analyzer Control and Status) register is used to define and control the operation of LynxEM+'s signature analyzer. Bit 3 is used as a Enable/Stop bit. Bit 2 is used as a Reset/Normal bit. Bit 1 and 0 are used to select 8-bit Red, Green, or Blue data from the 24-bit outputs of Multimedia RAMDAC. Bit 31 to bit 16 are used to read back the signature from the signature analyzer.

To turn on the signature analyzer, both bit 3 and bit 2 must be set as "11". The signature shift register will be reset to "0" as its initial value. On the rising edge of the 1st vertical sync pulse after VPR64 bit [3:2]=11, the state machine will start collecting signature data. Bit 2 is automatically reset to "0" at the same time. On the rising edge of the next vertical sync pulse, the signature analyzer stops and Bit 3 is automatically reset to "0". The test software can read back the 16-bit signature from Bit [31:16] to compare the golden signature for the test patterns. Figure 27 is a block diagram of the signature analyzer.

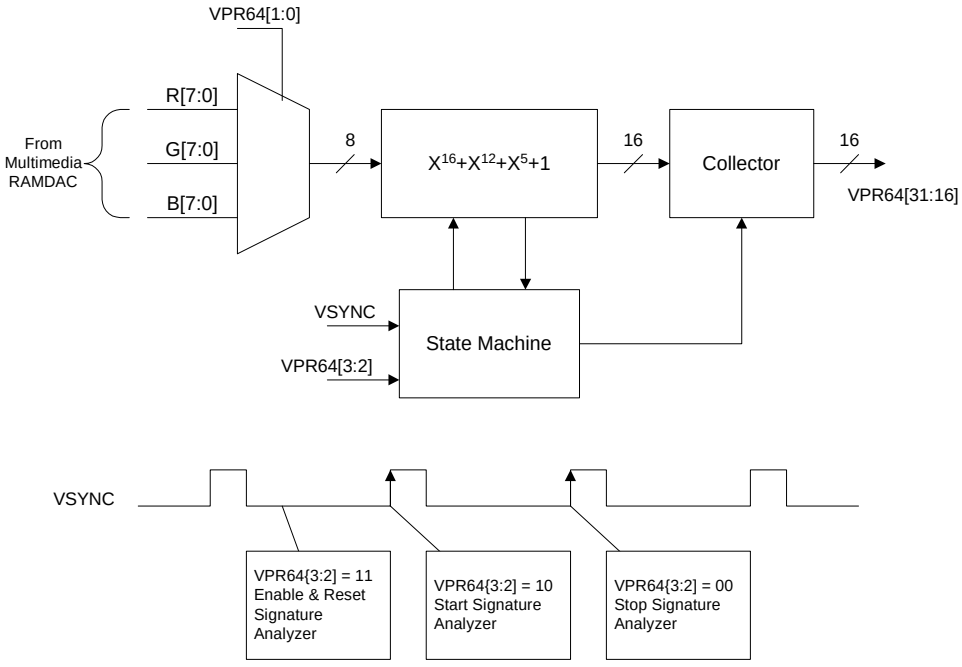


Figure 27: Signature Analyzer Block Diagram

Chapter 14: Power Management

LynxEM+ is designed to support ACPI requirements as defined in the PCI Bus Management Interface Specification 1.0 (PPMI v1.0) and Display device Class Power Management Specification v1.0a. LynxEM+ also supports a variety of adaptive power saving and clock management methods while in full operational mode. Finally, LynxEM+ supports traditional Standby and Suspend mode functionality for operating systems such as Windows 95 which do not have ACPI support built into the OS. A summary of these capabilities follows.

ACPI

LynxEM+ supports D0-D3 modes of operation via software programming of the Power Management Control/Status Register PMSCR[1:0]. As required by the PCI Bus Management Interface Specification, PCI Configuration Space Status Register (offset 06h) bit 4 is set to "1" to indicate new capabilities have been defined for LynxEM+. At offset 34h, the Cap_Ptr register stores the offset of the new capabilities (this register is hardwired to 40h). The first byte at offset 40h has a value of 01h, which indicates a Power Management capability (supports D1 and D2 states in addition to the required D0 and D3 power states). The second byte has a value of 00h indicating the no additional new capability features (Note: LynxEM+ does not offer support for optional ~PME capabilities as defined in PPMI v1.0).

Please refer to the PCI Bus Power Management Interface Specification 1.0 and Display Device Class Power Management Reference Specification v1.0a for additional details.

Display driver support for ACPI under Windows 98 and future versions of Windows NT will be provided by Silicon Motion in accordance with PC97 and PC98 requirements.

Adaptive Power Management

LynxEM+ provides intelligent power saving control during graphics/video operation. Two key methods through which power savings is achieved are Dynamic control of functional blocks, and dynamic clock control through Silicon Motion's Virtual Refresh architecture.

Dynamic Control of Functional Blocks

All major functional blocks within the device are laid out independently. There is no signal crossover between blocks. Special clock drivers are used to control each of the independent functional blocks. The clock drivers can be turned off by setting Power-Down Registers (PDR20 - PDR22), or by entering the internal auto-standby mode (PDR23 Bit 6). Functional blocks therefore can be turned on/off dynamically in response to how LynxEM+ is being utilized. Since the blocks shut down are unused functional blocks, this power saving feature is transparent to the end user.

Below are some programming recommendations for selected display configurations. These auto power saving features are implemented through video BIOS and system PMI. In addition to these display configuration recommendations, the drawing engine, ZV Port, video processor can be turned off through video driver control.

CRT is the only selected display

- Disable LCD frame buffer write operation (PDR21 bit 5 = 1)
- Disable LCD frame buffer read operation and DSTN dithering engine (PDR21 bit 4 = 1)

Color TFT is the only selected display with normal refresh

- Disable the 135 MHz DAC (PDR21 bit 7= 1)
- Disable LCD frame buffer write operation (PDR21 bit 5= 1)
- Disable LCD frame buffer read operation and DSTN dithering engine (PDR21 bit 4 = 1)

Color DSTN is the only selected display with Virtual Refresh

- Disable the 135 MHz DAC (PDR21 bit 7 = 1)
- Enable auto shut-down of display memory screen refresh cycle and LCD frame buffer write cycle (FPR31 bit 3 = 1)
- Set VCLK clock rate to 10 MHz (reduce clock rate to save power)

TV is the only selected display

- Set VCLK clock rate to 14.1 MHz and set interlaced mode (CRT30 bit 7 = 1)
- Disable LCD frame buffer write operation (PDR21 bit 5= 1)
- Disable LCD frame buffer read operation and DSTN dithering engine (PDR21 bit 4 = 1)

Dynamic Clock Control and Virtual Refresh

Dynamic clock control is made possible through Silicon Motion's Virtual Refresh architecture. Virtual Refresh is an intelligent architecture for dynamic clock control in LCD only mode, as well as independent display refresh control when multiple displays are enabled (e.g. CRT/LCD, TV/LCD). Virtual Refresh utilizes two independent clocks (VCLK, VRCLK): one clock, VRCLK drives the panel interface and maintains proper screen refresh. The second clock, VCLK is now independent of the panel and can be scaled according to user needs (e.g. scaled down for power savings, or scaled up to drive a higher refresh rate on CRT).

Virtual Refresh is enabled by setting FPR31 bit 7 to "1". When the LCD display is the only display viewed by the user, power saving can achieved via three key functions:

- Dynamically slows down the video clock (VCLK) to 25%~50% of the original clock rate
- Auto shut-down display memory screen refresh
- Auto shut-down the LCD write frame buffer

These functions can be automatically implemented when LynxEM+ detects the user has not performed any activity for selectable number of screen refresh cycles. Since a significant percentage of the logic is synchronized with VCLK, the average power consumption of the chip will drop dramatically. The LCD screen remains on with proper screen refresh, so the power savings is transparent to the end user.

Note: When multiple displays are used, Virtual Refresh architecture can also be used to simultaneously display CRT/TV and the LCD with different resolutions, and independent refresh rates.

Standard Power Management

Standby Mode

LynxEM+ supports Standby Mode in two ways: internal auto-standby and system standby from system PMI. The internal auto-standby is enabled and controlled by Activity Detection Register (PDR23). When the internal timer matches the selected condition (PDR23 bit [2:0]), LynxEM+ immediately enters standby mode Any CPU Memory or I/O access to

LynxEM+ will cause the device to exit standby mode, and reset as an internal counter timer. The system PMI can enable system standby mode by pulling LynxEM+'s "~PDOWN" signal low. (Note: To select standby mode, PDR20 bit 7 must be set to 0 before pulling ~PDOWN low) LynxEM+ will exit standby mode when "~PDOWN" goes high. When the system PMI standby is on, the internal auto-standby is ignored. Programming sequences for internal auto-standby and system standby follow.

Start Internal Auto-standby Mode

- PDR23 bit[7:6] = 11b
- PDR20 bit 7 = 0 to enter standby mode
- The internal timer count matches the setting from PDR23 bit[2:0]

Start System Standby Mode

- PDR20 bit 7 = 0 to enter standby mode
- "~PDOWN" input pin is driven low

Power Saving In Standby Mode

The standby mode is designed to provide an automatic power saving mechanism for the portable PC when the graphics display sub-system is idle for a short period of time. There is no need for BIOS or application software to program LynxEM+ registers. All power saving control are done by hardware. Both internal auto-standby and system PMI standby have the same power saving mechanisms listed below.

- Both memory clock and video clock switch to lower frequencies which are selected by bit [5:4] of PDR20 register
- LynxEM+ will continuously issue DRAM refresh cycles
- The following functional blocks are disabled (PDR21 bit 7, 5, 4, 3, 2, and 1)

  * DAC
  * LCD frame buffer write
  * LCD frame buffer read and DSTN dithering engine
  * Color Palette RAM
  * ZV Port
  * Drawing engine
  * Video processor

- LCD auto-power off sequence enabled
- VESA DPMS standby mode enabled

Sleep Mode

Sleep mode is the maximizes power-saving mode while maintaining display memory and register integrity. Sleep mode is selected when the whole system will be idle for a long period of time. All selected displays will be shutdown. PLLs can also be shutdown if the external 32 KHz refresh clock is selected (CCR69 bit 3 = 0) or memory self-refresh mode is selected. LCD panel on/off sequence will be done by simply programming the PDR22 register. The programming sequence for Sleep Mode follows.

Setting Before Entering Sleep Mode

- PDR20 bit 7 = 1 to enter sleep mode
- Set PDR20 bit 6 to select memory refresh type
- Set CCR69 bit 3 to select external or internal refresh clock

Enter Sleep Mode (Suspend)

- Power OFF the LCD panel if the LCD display is enabled. There are two ways to power OFF the LCD panel: hardware or software (selected by FPR34 bit 7). For software approach, the system PMI needs to program FPR34 bit 7 = 0 and PDR22 bit [3:0] to control FPEN, FPVDD, VBIAS,VBKLGT and panel interface pins. For hardware approach, one needs to program FPR34 bit 7 = 1 and panel ON/OFF timing select via FPR33 [3:2], then LynxEM+ will generate the proper panel sequencing.
- "~PDOWN" input pin is driven low. After ~PDOWN has been asserted for 2 vertical sync cycles, LynxEM+ will automatically shut-down the following blocks:

  * DAC
  * LCD frame buffer write
  * LCD frame buffer read and DSTN dithering engine
  * Color Palette RAM
  * ZV Port
  * 2D drawing engine
  * Video processor
  * Memory screen refresh
  * Start power-down memory refresh cycle

Exit Sleep Mode (Resume)

- Drive "~PDOWN" input high. (200 ms after PLLs are turned on)
- After 200 ms, Power ON the LCD panel by either hardware or software. For software panel sequencing, enable LCD display by programming the PDR22 register. The whole system will be back to original state. For hardware panel sequencing, set FPR34 bit 7 = 1.

Activity Detection

The activity detection function is used to monitor LynxEM+ I/O and memory activity. System designer can select a fixed time period by programming PDR23 bit [2:0]. An internal timer will count the idle period of memory or I/O operation. If the idle period matches the selected value, LynxEM+ will generate a "Low-High" or "High-Low" signal to system through ACTIVITY output pin. Any Memory or I/O operation can reset the ACTIVITY signal and the internal counter.

After receiving the ACTIVITY signal from LynxEM+, the system power management unit can start Standby mode or Sleep Mode by pulling "~PDOWN" signal low. The activity detection function can also be used to enable internal auto-standby mode by setting PDR23 bit [7:6]. This power saving feature is independent of software and transparent to the end users.

Power-down Sleep Mode States

Table 15: Interface Signals Sleep Mode States

Signal Name	Sleep Mode
Host Interface	
AD [31:0]	tri-state
C/ ~BE [3:0]	tri-state
PAR	tri-state
~FRAME	tri-state
~TRDY	tri-state

Signal Name	Sleep Mode
~IRDY	tri-state
~STOP	tri-state
~DEVSEL	tri-state
IDSEL	x
CLK	x
~RST	H
~REQ	tri-state
~GNT	x
~INTA	tri-state
Power Down Interface	
~PDOWN	L
~CLKRUN	open-collector
Clock Interface	
REFCLK/PALCLK	x
CKIN	x
LVDSCLK/MCKIN	tri-state
~EXCKEN	H
Memory Interface	
MA [9:0]	H
MD [63:0]	H or L (note 2)
~WE	H
~RAS	L
~CAS	L
~CS [1:0]	L
~DQM [7:0]	H
DSF	L
BA	H
SDCKEN	L (self-refresh), H (CAS-b-RAS)
SCK	depends on PLL
~ROMEN	H
Flat Panel Interface	
FDATA [23:0]	L
FPSCLK	L
FPEN	L
FPVDDEN	L
VBIASEN	L
LP/FHSYNC	L

Signal Name	Sleep Mode
FP/FVSYNC	L
CRT Interface	
R, G, B	0 V
CRTVSYNC	L
CRTHSYNC	L
Video Port Interface	
P [15:0]	x
PCLK	H
VREF	H
HREF	H
BLANK/TVCLK	H
General Purpose Registers/I^2C	
USR3	H
USR2	H
USR1/SDA	H
USR0/SCL	H
Test Mode Pins	
TEST [1:0]	L

Notes:

1. This entry specifies when PDR20 bit 6 = 1 (self-refresh). When PDR20 bit 6 = 0 (CAS before RAS), both ~RAS and ~CAS control are based on 32K Hz refresh clock
2. MD lines have internal pull-up, therefore, without external pulldown resistors, MD lines will be at HIGH. With external pulldown resistors, MD lines will be at LOW.

Chapter 15: PCI Configuration Space Registers

Table 16: PCI Configuration Registers Quick Reference

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CSR02: Device ID	15 - 2
CSR04: Command	15 - 2
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CSR08: Revision ID and Class Code	15 - 3
CSR0D: Latency Timer	15 - 4
CSR10: Memory Base Address Register	15 - 4
CSR2C: PCI Configuration Space Subsystem Vendor ID	15 - 5
CSR2E: PCI Configuration Space Subsystem ID	15 - 5
CSR30: Expansion ROM Base Address	15 - 5
CSR30: Expansion ROM Base Address	15 - 5
CSR34: Power Down Capability Pointer	15 - 6
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PCI Configuration Space Registers

The PCI specification defines the configuration space for auto-configuration (plug-and-play), device and memory relocation.

CSR00: Vendor ID

Read Only Address: 00h
Power-on Default: 126Fh

This register specifies the vendor ID

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR ID															

Bit 15:0 Vendor ID
This register is hardwired to 126Fh to identify as Silicon Motion, Inc.

CSR02: Device ID

Read Only Address: 02h
Power-on Default: 0712h

This register specifies the device ID.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE ID															

Bit 15:0 Device ID
This register is hardwired to 0712h to identify the device as a LynxEM+.

CSR04: Command

Read/Write Address: 04h Note: Reserved bits are read only
Power-on Default: 00h

This register controls which types of PCI command cycles are supported by LynxEM+.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										**PSE**	**MWR**	**R**	**PCI**	**MS**	**IO**

Bit 15:6 Reserved

Bit 5 Palette Snooping Enable (PSE)
0 = Disable
1 = Enable

Bit 4 Memory Write Invalidate Enable for PCI master (MWR)
0 = Disable
1 = Enable

Bit 3 Reserved (R)

Bit 2 PCI Master Enable (PCI)
0 = Disable
1 = Enable

Bit 1 Memory Space Access Enable (MS) (Note: This bit needs to be set to "1" in order to enable BIOS addressing decoding)
0 = Disable
1 = Enable

Bit 0 I/O Space Access Enable (IO)
0 = Disable
1 = Enable

CSR06: Status

Read Only Address: 06h
Power-on Default: 20h

This register controls device select timing status, detect parity status, and detects target abort status for LynxEM+. In order to clear any bit of this register, you must write a "1" to that particular bit.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DPE	**RESERVED**		**DTA**	**R**	**TS**		**RESERVED**								

Bit 15 Detect Parity Error (DPE)

Bit 14:13 Reserved (R)

Bit 12 Detect Target Abort for Master Mode (DTA)

Bit 11 Reserved (R)

Bit 10:9 ~DEVSEL Timing Select (TS)
01 = medium speed (hardwired)

Bit 8:0 Reserved

CSR08: Revision ID and Class Code

Read Only Address: 08h
Power-on Default: 030000A0h

This register specifies the silicon revision ID and the Class Code that the silicon supports.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE CLASS CODE								**SUBCLASS CODE**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG LEVEL PROGRAMMING INTERFACE								**REVISION ID**							

Bit 31:24 Base Class Code
03h = for Video Controller

Bit 23:16 Subclass Code
00h = VGA

Bit 15:8 Register Level Programming Interface
00h = hardwired setting

Bit 7:0 Revision ID
For example, A0h = revision A; B0h = revision B

CSR0D: Latency Timer

Read Only Address: 0Dh
Power-on Default: 00h

This register specifies the latency timer that LynxEM+ supports for burst master mode.

7	6	5	4	3	2	1	0
LATENCY TIMER							

Bit 7:0 Latency Timer for burst capable master

CSR10: Memory Base Address Register

Read/Write Address: 10h (Note: Reserved bits are read only)
Power-on Default: 00h

This register specifies the PCI configuration space for address relocation

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LINEAR ADDRESSING MEMORY BASE								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**MSI**

Bit 31:24 Linear Addressing Memory Base Address. Memory segment allocated within 16 MB boundary

Bit 23:1 Reserved

Bit 0 Memory Space Indicator (MSI) (Read only)
0 = memory base

CSR2C: PCI Configuration Space Subsystem Vendor ID

Read/Write Address: 2Ch
Power-on Default: 00h

This register specifies the Subsystem Vendor ID.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM VENDOR ID															

Bit 15:0 Subsystem Vendor ID

CSR2E: PCI Configuration Space Subsystem ID

Read/Write Address: 2Eh
Power-on Default: 712h

This register specifies the Subsystem ID. The default setting of MD[22:20] = 111b which configures the system BIOS to load subsystem ID information during POST.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSYSTEM ID															

Bit 15:0 Subsystem ID. This System ID is written by system BIOS during POST

CSR30: Expansion ROM Base Address

Read/Write Address: 30h
Power-on Default: 00h

This register specifies the expansion ROM base address. Note: Reserved bits are read only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM BASE ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															**BIOS**

Bit 31:16 ROM Base Address. Memory segment allocated for BIOS ROM in 64KB boundary [15:0]

Bit 15:1 Reserved

Bit 0 BIOS Address Decode Enable. This bit is valid only if memory space access is enabled. (CSR04 bit 1 = 1)
0 = Disable
1 = Enable

CSR34: Power Down Capability Pointer

Read Only Address: 34h
Power-on Default: 40h

This register contains the address where PCI power down management registers are located

7	6	5	4	3	2	1	0
CAPABILITY POINTER/PCI POWER DOWN MGMT							

Bit 7:0 Capability pointer contains the address where PCI Power Down Management Register are located.

CSR3C: Interrupt Line

Read/Write Address: 3Ch
Power-on Default: 00h

This register specifies the PCI Interrupt Line.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bit 7:0 Interrupt Line

CSR3D: Interrupt Pin

Read Only Address: 3Dh
Power-on Default: 01h

This register specifies the PCI Interrupt Pin.

7	6	5	4	3	2	1	0
RESERVED							IP

Bit 7:1 Reserved

Bit 0 Interrupt Pin (IP) (~INTA)

CSR40: Power Down Capability Register

Read Only Address: 40h
Power-on Default: 0601h

This register contains the address where PCI power down management Capabilities.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI POWER DOWN MANAGEMENT CAPABILITY (0601h)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI POWER DOWN MGMT CAPABILITY POINT LINK								**PCI POWER DOWN MGMT CAPABILITY (01h)**							

Bit 31:16 PCI Power Down Management Capability = 0601h
Offset 2

Bit 15:8 PCI Power Down Management Capability Point Link List = 00h
Offset 1

Bit 7:0 PCI Power Down Management Capability ID= 01h
Offset 0

CSR44: Power Down Capability Data

Read/Write Address: 44h
Power-on Default: 00h

This register contains the address where PCI power down management Control, Status and Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA								**RESERVED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI POWER DOWN MGMT CONTROL/STATUS															

Bit 31:24 Data
Read Only. Offset 7

Bit 23:16 Reserved =00
Offset 6

Bit 15:0 PCI Power Down Management Control/Status
Offset 4

LOCK: Extended Register Write Protect Control

Read/Write Address: 3C3h or 3C5h index 1Fh
Power-on Default: 00h

This register specifies write protect controls for the SMI extended registers. SMI extended registers are write-protected. In order to write to the SMI extended registers, one must write Bit [7:5] = 010b.

7	6	5	4	3	2	1	0
WPE			**RESERVED**				

Bit 7:5 Write Protect Enable (WPE)
101 = All SMI Extended registers are Write-Protected
010 = Enable writes to SMI Extended registers
Others = Maintain previous state

Bit 4:0 Reserved

Chapter 16: Standard VGA Registers

Table 17: Standard VGA Registers Quick Reference

Summary of Registers	Page
General Registers	
MISC: Miscellaneous Output Register	16 - 4
ISR0: Input Status Register 0	16 - 5
ISR1: Input Status Register 1	16 - 5
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Standard VGA Registers

This chapter describes standard VGA registers. In the following registers description, a '?' in an address stands for a hexadecimal value of either 'B' or 'D'. If Bit 0 of the Miscellaneous Output Register is set to 1, the address is based at 3Dxh for color emulation. If Bit 0 of the Miscellaneous Output Register is set to 0, the address is based at 3Bxh for monochrome emulation.

General Registers

MISC: Miscellaneous Output Register

Write Only Address: 3C2h
Read Only Address: 3CCh
Power-on Default: 00h

7	6	5	4	3	2	1	0
VSP	**HSP**	**OEM**	**R**	**VIDEO CLOCK**		**EVR**	**IO**

Bit 7 Vertical Sync Polarity Select (VSP)
0 = positive vertical sync polarity
1 = negative vertical sync polarity

Bit 6 Horizontal Sync Polarity Select (HSP)
0 = positive horizontal sync polarity
1 = negative horizontal sync polarity

Bit 5 Odd/Even Memory Page Select (OEM)
0 = Select lower 64K page of memory
1 = Select upper 64K page of memory

Bit 4 Reserved (R)

Bit 3:2 Video Clock Select
00 = Select 25.175MHz for 640 dots/line mode
01 = Select 28.322MHz for 720 dots/line mode
10 = Reserved (enable external clock source)
11 = Reserved (enable external clock source)

Bit 1 Enable Video RAM Access from CPU (EVR)
0 = Disable Video RAM access from CPU
1 = Enable Video RAM access from CPU

Bit 0 I/O Address Select (IO)
0 = Select monochrome mode. Address based at3Bxh.
1 = Select for color mode. Address based at 3Dxh

ISR0: Input Status Register 0

Read Only Address: 3C2h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
CRT	**RESERVED**		**MDS**	**RESERVED**			

Bit 7 CRT Vertical Retrace Interrupt (CRT)
0 = Vertical Retrace Interrupt is cleared
1 = Vertical Retrace Interrupt is pending.

Bit 6:5 Reserved

Bit 4 Monitor Detect Status (MDS)
0 = Monochrome display is detected
1 = Color display is detected

Bit 3:0 Reserved

ISR1: Input Status Register 1

Read Only Address: 3?Ah
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED		**COLOR PLANE**		**VRS**	**R**	**DISPLAY ENABLE**	

Bit 7:6 Reserved

Bit 5:4 Color Plane Diagnostics
These bits return two of the 8 video outputs VID0-VID7, as selected by Color Plane Enable Register [5:4]

Bit 3 Vertical Retrace Status (VRS)
0 = In display mode
1 = In vertical retrace mode

Bit 2:1 Reserved (R)

Bit 0 Display Enable
0 = In display mode
1 = Not in display mode. (it is either in horizontal or vertical retrace mode)

FCR: Feature Control Register

Write Only Address: 3?Ah

Read Only Address: 3CAh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**VSC**	**RESERVED**		

Bit 7:4 Reserved

Bit 3 Vertical Sync Control
0 = VSYNC output is enabled
1 = VSYNC output is logical 'OR' of VSYNC and Vertical Display Enable

Bit 2:0 Reserved

Sequencer Register

SEQX: Sequencer Index Register

Read/ Write Address: 3C4h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
RESERVED				**SEQUENCER ADDRESS/INDEX**			

Bit 7:4 Reserved

Bit 3:0 Sequencer Address/Index
The Sequencer address register is written with the index value of the sequencer register to be accessed.

SEQ00: Reset Register

Read/ Write Address: 3C5h, Index: 00h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED						**SR**	**AR**

Bit 7:2 Reserved

Bit 1 Synchronous Reset (SR)
0 = Sequencer is cleared and halted synchronously
1 = Normal operating mode

Bit 0 Asynchronous Reset (AR)
0 = Sequencer is cleared and halted asynchronously
1 = Normal operating mode

SEQ01: Clocking Mode Register

Read/ Write Address: 3C5h, Index: 01h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SO**	**VS**	**DCS**	**SL**	**R**	**DC**

Bit 7:6 Reserved

Bit 5 Screen Off (SO)
0 = Normal operating mode
1 = Screen is turned off but SYNC signals remain active

Bit 4 Video Serial Shift Select (VS)
0 = Load video serializer every or every other character or clock, depending on Bit2 of this register.
1 = Load video serializer every 4th character clock

Bit 3 Dot Clock Select (DCS)
0 = Normal dot clock select by VCLK input frequency
1 = Dot clock is divided by 2 (320/360 pixel mode)

Bit 2 Shift Load (SL)
0 = Load video serializer every character or clock
1 = Load video serializer every other character or clock

Bit 1 Reserved (R)

Bit 0 8/9 Dot Clock (DC)
0 = 9 dot wide character clock
1 = 8 dot wide character clock

SEQ02: Enable Write Plane Register

Read/ Write Address: 3C5h, Index: 02h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**ENABLE WRITING**			

Bit 7:4 Reserved

Bit 3:0 Enable Writing to Memory Maps 3 through 0 (respectively)
0 = Disable writing to corresponding plane
1 = Enable writing to corresponding plane

SEQ03: Character Map Select Register

Read/ Write Address: 3C5h, Index: 03h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SCM**	**SCMB**	**SCMA**	**SCMA**	**SCMB**	**SCMB**

Bit 7:6 Reserved

Bit 5,3,2 Select Character Map A (SCMA)

This value select the portion of plane 2 used to generate text character when bit 3 of this register = 0, according to the following table:

Bit 5,3,2	Font Table Location
000	First 8K of plane 2
100	Second 8K of plane 2
001	Third 8K of plane 2
101	Fourth 8K of plane 2
010	Fifth 8K of plane 2
110	Sixth 8K of plane 2
011	Seventh 8K of plane 2
111	Eighth 8K of plane 2

Bit 4,1,0 Select Character Map B (SCMB)

This value select the portion of plane 2 used to generate text character when bit 3 of this register = 1, according to the same table as character Map A

SEQ04: Memory Mode Register

Read/ Write Address: 3C5h, Index: 04h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED				**CM**	**SSA**	**EVM**	**R**

Bit 7:4 Reserved

Bit 3 Chained 4 Map (CM)
0 = Enable odd/even mode
1 = Enable Chain 4 mode. Uses the two lower bits of CPU address to select plane in video memory as follows:

MA1	MA0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Select Sequential Addressing Mode (SSA). This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enable the odd/even addressing mode. Even addresses access planes 0 and 2, and odd addresses access plane 1 and 3
1 = Enable system to use a sequential addressing mode

Bit 1 Extended Video Memory Enable (EVM)
0 = Memory access restricted to 16/32K
1 = Enable extended video memory access. Allows complete memory access to 256K

Bit 0 Reserved (R)

CRTC Controller Registers

The CRTC registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register (3?4h), then writing to the data register (3?5h). The I/O address is either 3Bxh or 3Dxh depending on bit 0 of the Miscellaneous Output Register at 3C2h.

CRTX: CRTC Controller Index Register

Read/Write Address: 3?4h
Power-on Default: 00h

This register is loaded with a binary value that indexes the CRTC controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED			**CRTC ADDRESS INDEX**				

Bit 7:5 Reserved

Bit 4:0 CRTC Address Index
These bits specify the CRTC register to be addressed. Its value is programmed in hexadecimal.

CRT00: Horizontal Total Register

Read/Write Address: 3?5h, Index 00h
Power-on Default: Undefined

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bit 7:0 Horizontal Total
This value = (number of character clocks per scan line) - 5.

CRT01: Horizontal Display End Register

Read/Write Address: 3?5h, Index 01h
Power-on Default: Undefined

This register defines the number of character clocks for one horizontal line active display. This register is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY ENABLE							

Bit 7:0 Horizontal Display End
This value = (number of character clocks during active display) - 1.

CRT02: Horizontal Blank Start Register

Read/Write Address: 3?5h, Index 02h
Power-on Default: Undefined

This register defines the number of character clocks at which horizontal ~Blank is asserted.

7	6	5	4	3	2	1	0
HORIZONTAL BLANK START							

Bit 7:0 Horizontal Blank Start
This value = character value at which ~Blank signal becomes active.

CRT03: Horizontal Blank End Register

Read/Write Address: 3?5h, Index 03h
Power-on Default: Undefined

This register defines the display enable skew and pulse width of ~Blank signal.

7	6	5	4	3	2	1	0
R	**DISPLAY ENABLE**		**HORIZONTAL BLANK END**				

Bit 7 Reserved

Bit 6:5 Display Enable Skew. These 2 bits define the display enable signal skew timing in relation to horizontal synchronization pulses.

DESKW1	DESKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Horizontal Blank End
Horizontal Blank End has a 6-bit value. This register contains the least significant 5-bits of this value. Bit 6 of this value is at CRTC index 05 bit 7.

CRT04: Horizontal Sync Pulse Start Register

Read/Write Address: 3?5h, Index 04h
Power-on Default: Undefined

This register is used to adjust screen position horizontally and to specify the position at which HSYNC is active.

7	6	5	4	3	2	1	0
HORIZONTAL SYNC PULSE START							

Bit 7:0 Horizontal Sync Pulse Start
This value = character clock count value at which HSYNC becomes active.

CRT05: End Horizontal Sync Pulse Register

Read/Write Address: 3?5h, Index 05h
Power-on Default: Undefined

This register defines the horizontal sync skew and pulse width of HSYNC signal.

7	6	5	4	3	2	1	0
HBE	**HSS**		**HORIZONTAL SYNC END**				

Bit 7 Horizontal Blank End Bit 5. This bit is End Horizontal Blank Bit 5. (HBE)

Bit 6:5 Horizontal Sync Skew. (HSS)
These 2-bits define the HSYNC signal skew timing in relation to horizontal synchronization pulses.

HSSKW1	HSSKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Horizontal Sync End
Horizontal Sync End has a 5-bit value. This value defines the character clock counter value at which HSYNC signal becomes inactive.

CRT06: Vertical Total Register

Read/Write Address: 3?5h, Index 06h
Power-on Default: Undefined

This register defines the number of scan lines from VSYNC going active to the next VSYNC going active. Vertical total has a 11-bit value. Bit 8 of this value is located at CRT07 bit 0. Bit 9 of this value is located at CRT07 bit 5. Bit 10 of this value is located at CRT30 bit 3.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bit 7:0 Vertical Total
Vertical Total has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines from VSYNC going active to the next VSYNC) - 2. Bit 8 is in CRT07 bit 0. Bit 9 is in CRT 07 bit 5. Bit 10 is in CRT30 bit 3.

CRT07: Overflow Vertical Register

Read/ Write Address: 3?5hIndex: 07h
Power-on Default: Undefined

This register specifies the CRTC vertical overflow registers.

7	6	5	4	3	2	1	0
VSS	**VDE**	**VT**	**LC**	**VBS**	**VSS**	**VDE**	**VT**

Bit 7 Vertical Sync Start Bit 9 (VSS)

Bit 6 Vertical Display Enable End Bit 9. This bit is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register. (VDE)

Bit 5 Vertical Total Bit 9 (VT)

Bit 4 Line Compare Bit 8 (LC)

Bit 3 Vertical Blank Start Bit 8 (VBS)

Bit 2 Vertical Sync Start Bit 8 (VSS)

Bit 1 Vertical Display Enable End Bit 8. This bit is locked when FPR33 (SC5h, index 33) bit 5 = 1. (VDE)

Bit 0 Vertical Total Bit 8 (VT)

CRT08: Preset Row Scan Register

Read/Write Address: 3?5h, Index 08h
Power-on Default: Undefined

This register is used for panning and text scrolling.

7	6	5	4	3	2	1	0
R	**BYTE PLANNING**		**PRESET ROW SCAN COUNT**				

Bit 7 Reserved (R)

Bit 6:5 Byte Panning Control. These 2-bits controls the number of bytes to pan.

BPC1	BPC0	Operation
0	0	Normal
0	1	1 Byte left shift
1	0	2 Bytes left shift
1	1	3 Bytes left shift

Bit 4:0 Preset Row Scan Count
These bits preset the vertical row scan counter once after each vertical retrace. This counter is automatically incremented by 1 after each horizontal sync period. Once the maximum row scan count is reached, this counter is cleared. This is useful for smoothing vertical text scrolling.

CRT09: Maximum Scan Line Register

Read/Write Address: 3?5h, Index 09h
Power-on Default: Undefined

This register defines the maximum number of scan lines per character row and provides one scanning control and two overflow bits

7	6	5	4	3	2	1	0
EDS	**LC**	**VB**	**MAXIMUM SCAN LINE**				

Bit 7 Enable Double Scan (EDS)
0 = Normal Operating

1 = Enable Double Scan. The row scan counter is clocked at half of the horizontal scan rate.

Bit 6 Line Compare Register Bit 9 (LC)

Bit 5 Vertical Blank Start Register Bit 9 (VB)

Bit 4:0 Maximum Scan Line
This value equals to the total number of scan lines per character row - 1

CRT0A: Cursor Start Scan Line Register

Read/Write Address: 3?5h, Index 0Ah
Power-on Default: Undefined

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
RESERVED		**EC**	**CURSOR START SCAN LINE**				

Bit 7:6 Reserved

Bit 5 Enable Cursor (EC)
0 = Cursor is on
1 = Cursor is off

Bit 4:0 Cursor Start Scan Line
This value equals to the starting cursor row within the character box. If this value is programmed with a value greater than the Cursor End Scan Line Register (3?5h, index 0Bh), no cursor will be displayed.

CRT0B: Cursor End Scan Line Register

Read/Write Address: 3?5h, Index 0Bh
Power-on Default: Undefined

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
R	**CURSOR SKEW**		**CURSOR END SCAN LINE**				

Bit 7 Reserved (R)

Bit 6:5 Cursor Skew. These 2 bits defines the cursor delay skew, which moves the cursor to the right, in character clock.

CSKW1	CSKW0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0 Cursor End Scan Line
This value equals to the ending cursor row within the character box. If this value is programmed with a value less than the Cursor Start Scan Line Register (3?5h, index 0Ah), no cursor will be displayed.

CRT0C: Display Start Address High Register

Read/Write Address: 3?5h, Index 0Ch
Power-on Default: Undefined

This register defines the high order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are located in CRT30 bit [6:4]. Bit [7:0] are located in CRT0D.

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS [15:8]							

Bit 7:0 Display Start Address [15:8]
This register is the high order byte of the address [15:8].

CRT0D: Display Start Address Low Register

Read/Write Address: 3?5h, Index 0Dh
Power-on Default: Undefined

This register defines the low order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are in CRT30 bit [6:4]. Bit [15:8] are in CRT0C.

7	6	5	4	3	2	1	0
START ADDRESS [7:0]							

Bit 7:0 Start Address [7:0]
This register is the low order byte of the address [7:0].

CRT0E: Cursor Location High Register

Read/Write Address: 3?5h, Index 0Eh
Power-on Default: Undefined

This register defines the high order cursor location address. This value is a 19-bit value along with CRT30 bit[6:4] are the high order bits of the address.

7	6	5	4	3	2	1	0
CURSOR LOCATION HIGH							

Bit 7:0 Cursor Location High
This register is the high order byte of the cursor location address.

CRT0F: Cursor Location Low Register

Read/Write Address: 3?5h, Index 0Fh
Power-on Default: Undefined

This register defines the low order cursor location address.

7	6	5	4	3	2	1	0
CURSOR LOCATION LOW							

Bit 7:0 Cursor Location Low
This register is the low order byte of the cursor location address.

CRT10: Vertical Sync Pulse Start Register

Read/Write Address: 3?5h, Index 10h
Power-on Default: Undefined

This register is used to adjust screen position vertically and to specify the position at which VSYNC is active. Bit 10 of this value is in CRT30 bit 0. Bit 9 of this value is in CRT07 bit 7. Bit 8 of this value is in CRT07 bit 2.

7	6	5	4	3	2	1	0
VERTICAL SYNC PULSE START							

Bit 7:0 Vertical Sync Pulse Start
Vertical Sync Start has a 11-bit value. This register contains the least significant 8 bits of this value. This value = number of scan lines at which VSYNC becomes active.

CRT11: Vertical Sync Pulse End Register

Read/Write Address: 3?5h, Index 11h
Power-on Default: 0xh.

This register is used to control vertical interrupt, vertical sync end CRT0-7 Write protect.

7	6	5	4	3	2	1	0
LW	**RCS**	**DVI**	**CVI**	**VERTICAL SYNC PULSE END**			

Bit 7 Lock writing to CRTC registers: CRT00-07. (LW)
0 = Enable writing to CRTC registers are
1 = Disable writing to CRTC registers, except CRT07 bit 4 (line compare)

Bit 6 Refresh Cycle Select (3/5) (RCS)
0 = 3 DRAM refresh cycles per horizontal scan line
1 = 5 DRAM refresh cycles per horizontal scan line

Bit 5 Disable Vertical Interrupt (DVI)
0 = vertical retrace interrupt enabled
1 = vertical retrace interrupt disabled

Bit 4 Clear Vertical Interrupt (CVI)
0 = vertical retrace interrupt is cleared
1 = vertical retrace interrupt. This allows an interrupt to be generated at the end of active vertical display.

Bit 3:0 Vertical Sync Pulse End
This value = number of scan lines at which VSYNC becomes inactive.

CRT12: Vertical Display End Register

Read/Write Address: 3?5h, Index 12h
Power-on Default: Undefined

This register defines the number of scan line where the display on the screen ends. Bit 10 of this value is in CRT30 bit 2. Bit 9 of this value is in CRT07 bit 6. Bit 8 of this value is in CRT07 bit 1. This register is locked when FPR33 (SC5h, index 33) bit 5 = 1. Please refer to FPR33 register.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7:0 Vertical Display End
Vertical Display End has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines during active display) - 1.

CRT13: Offset Register

Read/Write Address: 3?5h, Index 13h
Power-on Default: Undefined

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

This register defines the logical line width of the screen. The starting memory address for the next display row is larger than the current row by two (in byte mode), four (in word mode), or eight (in double word mode) times this offset.

Bit 7:0 Logical Screen Width
Logical Screen Width has a 10-bit value. This register contains the least significant 8-bits of this value. The addressing mode is specified by bit 6 of CRT14 and bit 3 of CRT17.

CRT14: Underline Location Register

Read/Write Address: 3?5h, Index 14h
Power-on Default: Undefined

This register defines the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
R	**DWS**	**CS**	**UNDER LINE LOCATION**				

Bit 7 Reserved (R)

Bit 6 Double Word Mode Select (DWS)
0 = the memory address are byte or word addresses
1 = the memory address are double word addresses

Bit 5 Count by 4 Select (CS)
0 = the memory address counter depends on bit 3 of CRT17
1 = the memory address counter is incremented every four character clocks

Bit 4:0 Under Line Location
Under Line Location has a 5-bit value. This value = (scan line count of a character row on which an underline occurs) - 1.

CRT15: Vertical Blank Start Register

Read/Write Address: 3?5h, Index 15h
Power-on Default: Undefined

This register defines the number of scan lines at which vertical blank is asserted. Bit 10 of this value is in CRT30 bit 1. Bit 9 of this value is in CRT09 bit 5. Bit 8 of this value is in CRT07 bit 3.

7	6	5	4	3	2	1	0
VERTICAL BLANK START							

Bit 7:0 Vertical Blank Start
Vertical Blank Start has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (scan line count at which vertical blank signal becomes active) - 1.

CRT16: Vertical Blank End Register

Read/Write Address: 3?5h, Index 16h
Power-on Default: Undefined

This register defines the number of scan lines at which vertical blank is de-asserted.

7	6	5	4	3	2	1	0
VERTICAL BLANK END							

Bit 7:0 Vertical Blank End
Vertical Blank End is a 8-bit value. This value = [(scan line count at which vertical blank signal becomes active) -1)] + (desired width of vertical blanking pulse in scan lines)

CRT17: CRT Mode Control Register

Read/Write Address: 3?5h, Index 17h
Power-on Default: Undefined

This register defines the controls for CRT mode.

7	6	5	4	3	2	1	0
HR	**BAS**	**AW**	**R**	**WS**	**HCS**	**EGA**	**CGA**

Bit 7 ~RST Hardware Reset for Horizontal and Vertical Sync (HR)
0 = horizontal and vertical sync outputs inactive
1 = horizontal and vertical sync outputs active

Bit 6 Byte Address Mode Select (BAS)
0 = word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB
1 = byte address mode

Bit 5 Address Wrap is useful in implementing CGA mode. (AW)
0 = In word address mode, memory address counter bit 13 appears on the memory address output signal of the CRT controller and the video memory address wraps around at 16KB.
1 = In word address mode, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRTC controller.

Bit 4 Reserved (R)

Bit 3 Word Mode Select (WS)
0 = byte mode addressing is selected and memory address counter is clocked by the character clock input
1 = word mode addressing is selected and memory address counter is clocked by the character clock divided by two.

Bit 2 Horizontal Retrace Clock Select (HCS)
0 = select horizontal retrace clock rate
1 = select horizontal retrace clock rate divided by two.

Bit 1 EGA Emulation (EGA)

0 = Row scan counter bit 1 is replaced by memory address bit 14 during active display time
1 = Memory address bit 14 appear son the memory address output bit 14 signal of the CRT controller.

Bit 0 CGA Emulation (CGA)
0 = Row scan counter bit 0 is replaced by memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller.

CRT18: Line Compare Register

Read/Write Address: 3?5h, Index 18h
Power-on Default: Undefined

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0.

7	6	5	4	3	2	1	0
LINE COMPARE REGISTER							

Bit 7:0 Line Compare Register
This value = number of scan lines at which the screen is split into screen 1 and screen 2.

CRT22: Graphics Controller Data Latches Readback Register

Read Only Address: 3?5h, Index 22h
Power-on Default: Undefined

This register is used to read the CPU latches in the graphics controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU DATA LATCHES							

Bit 7:0 Graphics Controller CPU Data Latches
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

CRT24: Attribute Controller Toggle Readback Register

Read Only Address: 3?5h, Index 24h
Power-on Default: Undefined

This register is used to provide access to the attribute controller toggle.

7	6	5	4	3	2	1	0
ACS	**RESERVED**						

Bit 7 Attribute Controller Index Select (ACS)
0 = the attribute controller reads or writes an index value on the next access

1 = the attribute controller reads or writes a data value on the next access

Bit 6:0 Reserved

CRT26: Attribute Controller Index Readback Register

Read Only Address: 3?5h, Index 26h
Power-on Default: Undefined

This register is used to provide access to the attribute controller index.

7	6	5	4	3	2	1	0
RESERVED		**VES**	**ATTRIBUTE CONTROLLER INDEX**				

Bit 7:6 Reserved

Bit 5 Video Enable Status (VES)
This bit provides status of the video display enable bit in Attribute Controller (3C0h) index bit 5.

Bit 4:0 Attribute Controller Index
This value is the attribute controller index data at 3C0h.

Graphics Controller Registers

The graphics controller registers are located at a two byte I/O address space. The registers are accessed by first writing an index to 3CEh and followed by writing a data to 3CFh.

GRXX: Graphics Controller Index Register

Read/Write Address: 3CEh
Power-on Default: Undefined

This register is loaded with a binary value that indexes the graphics controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED				**GRAPHICS CONTROLLER**			

Bit 7:4 Reserved

Bit 3:0 Graphics Controller Address Index
These bits specify the graphics controller register to be addressed. Its value is programmed in hexadecimal.

GRX00: Set/Reset Register

Read/Write Address: 3CFh, Index: 00h.
Power-on Default: Undefined

This register represents the value written to all 8-bits of the corresponding memory planes when CPU executes a memory write in write mode 0.

7	6	5	4	3	2	1	0
RESERVED				**SET/RESET PLANE**			

Bit 7:4 Reserved

Bit 3:0 Set/Reset Plane3:0
In write mode 0, the set/reset data can be enabled on the corresponding bit of the bit of the Enable Set/ Reset Data register. These bits become the color value for CPU memory write operations.

GRX01: Enable Set/Reset Register

Read/Write Address: 3CFh, Index: 01h.
Power-on Default: Undefined

This register enable the set/reset register in write mode 0.

7	6	5	4	3	2	1	0
RESERVED				**ENABLE SET/RESET PLANE**			

Bit 7:4 Reserved

Bit 3:0 Enable Set/Reset Plane3:0
In write mode 0, the enable set/reset bits allow writing to the corresponding planes with the data in set/ reset register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

GRX02: Color Compare Register

Read/Write Address: 3CFhIndex: 02h.
Power-on Default: Undefined

This register is to used to compare with the CPU memory read data. This register works in conjunction with the Color Don't Care Register.

7	6	5	4	3	2	1	0
RESERVED				**COLOR COMPARE PLANE**			

Bit 7:4 Reserved

Bit 3:0 Color Compare Plane [3:0]
These bits represent the reference color used to compare each pixel in corresponding plane. A logical 1 is returned in each plane bit position when color matches.

GRX03: Data Rotate/ROP Register

Read/Write Address: 3CFhIndex: 03h.
Power-on Default: Undefined

This register is to used to control rotation and raster operations.

7	6	5	4	3	2	1	0
RESERVED			**ROS**		**ROTATE COUNT**		

Bit 7:5 Reserved

Bit 4:3 Raster Operations Select (ROS)
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

Bit 2:0 Rotate Count
These bits specifies the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0. To write non-rotated data, the CPU must present a count with 0.

GRX04: Read Plane Select Register

Read/Write Address: 3CFhIndex: 04h.
Power-on Default: Undefined

This register is selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
RESERVED						**READ PLANE**	

Bit 7:2 Reserved

Bit 1:0 Read Plane Select is as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

GRX05: Graphics Mode Register

Read/Write Address: 3CFhIndex: 05h.
Power-on Default: Undefined

This register is selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
R	**CS**	**OES**	**OEA**	**ERC**	**R**	**WRITING MODE**	

Bit 7 Reserved (R)

Bit 6 256 Color Shift Mode Select (CS)
0 = Enable bit 5 of this register to control loading of the shift registers.
1 = The shift registers are loaded in a manner that support the 256 color mode.

Bit 5 Odd/Even Shift Mode Select (OES)
0 = Normal shift mode
1 = The video shift registers are directed to format the serial data stream with even numbered bits from both planes on the even numbered planes and odd numbered bits from both planes on the odd planes.

Bit 4 Odd/Even Addressing Select (OEA)
0 = Normal addressing
1 = CGA Odd/even addressing mode is selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3.

Bit 3 Enable Read Compare (ERC)
0 = System read data from memory planes selected by read map select register (3CFh index 04h). This is called read mode 0.
1 = System read the results of logical comparison between the data in 4 memory planes selected by the Color Don't Care Register and the Color Compare Register. The results is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1.

Bit 2 Reserved (R)

Bit 1:0 Write Mode Select

00 = Write mode 0. Each of four video planes is written with CPU data rotated by the number of counts in rotate register. If Set/Reset register is enabled for any of the four planes, the corresponding planes is written with the data stored in the Set/Reset register.
01 = Write mode 1. Each of four video planes is written with CPU data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, Set/Reset data, enable Set/Reset data and bit mask registers are ignored.
10 = Write mode 2. Video planes [3:0] are written with the value of CPU write data [3:0]. The 32-bit output from the four planes is then operated on by the Bit Mask register and the resulting data are written into the four planes. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored.
11 = Write mode 3. Each of the four video planes is written with 8-bit of the color value in the Set/Reset register for the corresponding plane. The bit-position-enable field is formed with the logical AND of the Bit Mask register and rotated CPU data. The Enable Set/Reset register is ignored.

GRX06: Graphics Miscellaneous Register

Read/Write Address: 3CFhIndex: 06h.

Power-on Default: Undefined

This register controls video memory addressing.

7	6	5	4	3	2	1	0
RESERVED				**MEMORY MAP**		**OES**	**GMS**

Bit 7:4 Reserved

Bit 3:2 Memory Map Mode. These bits control the address mapping of video memory into the CPU address space.
00 = A0000h to BFFFFh (128KB)
01 = A0000h to AFFFFh (64KB)
10 = B0000h to B7FFFh (32KB)
11 = B8000h to BFFFFh (32KB)

Bit 1 Odd/Even Mode Select (OES)
0 = CPU address bit A0 is the memory address bit MA0
1 = CPU address A0 is replaced by a higher order address bit. A0 is then used to select odd or even maps. A0=0, selects Map 2 or 0; A0 = 1, select Map 3 or 1.

Bit 0 Graphics Mode Select (GMS)
0 = Select Text mode
1 = Select Graphics mode

GRX07: Color Don't Care Plane Register

Read/Write Address: 3CFhIndex: 07h.
Power-on Default: Undefined

This register controls whether the corresponding bit of the Color Compare Register, GRX02, is to be ignored or used for color comparison. This register is used with GRX02 for Read Mode 1 accesses.

7	6	5	4	3	2	1	0
RESERVED				**COMPARE PLANE SELECT**			

Bit 7:4 Reserved

Bit 3:0 Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1.
1 = The corresponding color plane is used for color comparison with the data in the Color Compare Register, GRX02.

GRX08: Bit Mask Register

Read/Write Address: 3CFhIndex: 08h.
Power-on Default: Undefined

This register controls bit mask operations which applies simultaneously to all four maps. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bit 7:0 Bit Mask
0 = corresponding bit of each plane in memory is set to the corresponding bit in the processor latches.
1 = corresponding bit of each plane in memory is set as specified by other conditions.

Attribute Controller Registers

The attribute controller registers are located at the same byte I/O address for writing address and data. The Attribute Index Register has an internal flip-flop rather than an input bit to control the selection of the address and data registers. Reading the Input Status Register 1 at Port 3?Ah clears the flip-flop and selects the Address Register, which is read at address 3C1h and written at address 3C0h. Once the Address Register has been loaded with an index, the next write operation to 3C0h loads the Data Register. The flip-flop toggles between the Address and the Data Register after every write to address 3C0h, but does not toggle for reads from address 3C1h. Furthermore, the attribute controller index register is read at 3C0h, and the attribute controller data register is read at address 3C1h.

ATRX: Attribute Controller Index Register

Read/Write Address: 3C0h
Power-on Default: Undefined

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED		**PAS**	**ATTRIBUTE CONTROLLER ADDRESS**				

Bit 7:6 Reserved

Bit 5 Palette Address Source (PAS)
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers
1 = Enable internal color palette and normal video translation.

Bit 4:0 Attribute Controller Address
A binary value that points to the attribute controller register where data is to be written.

ATR00-0F: Palette Register

Read/Write Address: 3C1h/3C0hIndex 00h - 0Fh.
Power-on Default: Undefined

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
RESERVED		**PALETTE COLORS**					

Bit 7:6 Reserved

Bit 5:0 Palette Colors
0 = corresponding pixel color is de-selected
1 = corresponding pixel color is enabled

ATR10: Attribute Mode Control Register

Read/Write Address: 3C1h/3C0hIndex: 10h.
Power-on Default: 00h

This register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
VID	**CS**	**PPE**	**R**	**BIS**	**LGC**	**MCE**	**TGM**

Bit 7 VID5, VID4 Select (VID)
0 = VID5 and VID4 palette register outputs are selected
1 = Color Select Register Port 3C1h/3C0h, Index 14h, bit 1 and bit 0 are selected for outputs.

Bit 6 256 Color Select (CS)
0 = Disable 256 color mode pixel width. PCLK rate = internal dot clock rate.
1 = Enable 256 color mode pixel width. PCLK rate = internal dot clock rate / 2

Bit 5 Pixel Panning Enable (PPE)
0 = Line compare will have no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC is active

Bit 4 Reserved (R)

Bit 3 Blinking and Intensity Select (BIS)
0 = Select background intensity from the text attribute byte.
1 = Select blink attribute in text modes

Bit 2 Line Graphics Character Enable (LGC)
0 = Forces the ninth dot to be the same color as the background in line graphics character codes.
1 = Enable special line graphics character codes.

Bit 1 Mono/Color Emulation (MCE)
0 = Select color display text attributes
1 = Select monochrome display text attributes

Bit 0 Text /Graphics Mode Select (TGM)
0 = Select text attribute control mode
1 = Select graphics control mode

ATR11: Overscan Color Register

Read/Write Address: 3C1h/3C0hIndex: 11h.
Power-on Default: 00h

This register controls the overscan or border color. This register will be locked if CRT3C register (3?5h, index 3Ch) bit 5 is set to 1. Please refer to CRT3C register for details.

7	6	5	4	3	2	1	0
OVERSCAN COLOR REGISTER							

Bit 7:0 OverScan Color register determines the overscan or border color displayed on the CRT screen.

ATR12: Color Plane Enable Register

Read/Write Address: 3C1h/3C0hIndex: 12h.
Power-on Default: 00h

This register enables the respective video memory color plan 0-3 and selects the video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
RESERVED		**VIDEO SATUS**		**COLOR PLANE ENABLE**			

Bit 7:6 Reserved

Bit 5:4 Video Status Multiplexer. These bits select two out of the 8 color outputs which can be read by the Input Status Register 1 at port 3?Ah, bit 5 and bit 4.

Color Plane Register		**Input Status Register 1**	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID7

Bit 3:0 Color Plane Enable
0 = disable the corresponding color planes. Forces pixel bit to be 0 before it address palette.
1 = enables the corresponding color planes.

ATR13: Horizontal Pixel Panning Register

Read/Write Address: 3C1h/3C0hIndex: 13h.
Power-on Default: 00h

This register specifies the number of pixels to shift the display data horizontally to the left. Horizontal pixel panning is available in text and graphics modes.

7	6	5	4	3	2	1	0
RESERVED				**HORIZONTAL PIXEL PLANNING**			

Bit 7:4 Reserved

Bit 3:0 Horizontal Pixel Panning. These 4 bits determine the horizontal left shift of the video data in number of pixels. In the 9 pixel/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixel/character text mode and all graphics modes, except for 256 color mode, a maximum shift of 7 pixels is allowed. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

Bits 3:0	9 pixel/character	8 pixel/character	256 color modes
0000	1	0	0
0001	2	1	-
0010	3	2	1
0011	4	3	-
0100	5	4	2
0101	6	5	-
0110	7	6	3
0111	8	7	-
1000	0	-	-

ATR14: Color Select Register

Read/Write Address: 3C1h/3C0h, Index: 14h.
Power-on Default: 00h

This register specifies the high-order bits of video output when pixel padding is enable/disabled for 256 color modes.

7	6	5	4	3	2	1	0
RESERVED				**SC7/6**		**SC5/4**	

Bit 7:4 Reserved

Bit 3:2 Select Color 7 and Color 6 (SC7/6)

These are the two most significant bits of the 8 bits color value for video DAC. These are normally used in all modes except 256 color modes.

Bit 1:0 Select Color 5 and Color 4 (SC5/4)
These bits can be substituted for VID5 and VID4 from the palette registers to form the 8-bit color value for video DAC.

RAMDAC Registers

The section describes the RAMDAC registers. Special programming sequences are used to read or write data to and from the RAMDAC.

Writing data to DAC:

Write the color code to DAC Write Address Register at 3C8h.
Three bytes: Red, Green, Blue values are written into DAC Data Register at 3C9h.
Following the third write, the values are transferred to Color Lookup Table.

- The DAC Write Address Register is auto incremented by 1.

Reading data from DAC:

- Write the color code to DAC Read Address Register at 3C7h.
- Three bytes: Red, Green, Blue values are read from the DAC Data Register at 3C9h.

3C6: DAC Mask Register

Read/Write Address: 3C6h
Power-on Default: Undefined

This register is the pixel read mask register to select pixel video output.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bit 7:0 DAC Address Mask
This field is the pixel mask for palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry I the Color Lookup Table. This register is initialized to FFh by the BIOS during a video mode set.

3C7W: DAC Address Read Register

Write Only Address: 3C7h
Power-on Default: Undefined

This register contains the pointer to one of the 256 palette data registers and is used when reading the color palette. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bit 7:0 DAC Read Address
After a color code is written into this register, the chip will identifies that a DAC read sequence will occur. A read sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C7R: DAC Status Register

Read Only Address: 3C7h
Power-on Default: Undefined

This register specifies the DAC Status: read or write cycles.

7	6	5	4	3	2	1	0
RESERVED						**DAC STATUS**	

Bit 7:2 Reserved

Bit 1:0 DAC Status bits
00 = DAC write operation in progress
11 = DAC read operation in progress

3C8: DAC Address Write Register

Read/Write Address: 3C8h
Power-on Default: Undefined

This register contains the pointer to one of the 256 palette data registers and is during a palette load. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS							

Bit 7:0 DAC Write Address
After a color code is written into this register, the chip identifies that a DAC write sequence will occur. A write sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C9: DAC Data Register

Read/Write Address: 3C9h
Power-on Default: Undefined

This register is the data port to read or write the contents of the location in the Color Lookup Table pointed to by the DAC Read Address or the DAC Write Address registers. An access to this register will cause 01b to be driven to RAMDAC outputs.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bit 7:0 DAC Read/Write Data
These read/write register bits store the Pixel data for the Palette DAC.

Chapter 17: Extended SMI Registers

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Extended SMI Registers

This chapter describes the extended SMI registers including:

- System control registers
- Power down control register
- Flat panel registers
- Memory control registers
- Clock control registers
- General purpose registers
- Popup-Icon and hardware cursor registers
- Extended CRT registers
- Shadow VGA registers

All extended SMI registers are accessed through 3C3h, 3C5h, or 3?5h address. (? = B for monochrome mode and D for color mode). In order to access extended SMI registers, one must unlock the extended SMI register by writing 010xxxxxb to Lock register (3C3h).

The name of the register consists of the index which the register resides in. For example, SCR10 can be accessed through index 10h of 3C5h.

System Control Registers

All system control registers are controlled by PCI system clock, rather than memory clock (MCLK) or video clock (VCLK). During LynxEM+ power down (when MCLK and VCLK are shutdown), the system control registers can still be accessed through PCI bus.

SCR10: PCI Master Starting Address 7:0

Read/Write Address: 3C5h, Index: 10h
Power-on Default: Undefined

This register specifies the starting read/write address [7:1] in PCI master mode and Bi-Endian Mode Select.

7	6	5	4	3	2	1	0
STARTING ADDRESS [7:1] PCI MASTER MODE							**BES**

Bit 7:1 Starting Address [7:1] in PCI Master Mode

Bit 0 Bi-Endian Select (BES)
0 = Normal
1 = Select Bi-Endian mode

SCR11: PCI Master Starting Address 15:8

Read/Write Address: 3C5h, Index: 11h
Power-on Default: Undefined

This register specifies the starting read/write address [15:8] in PCI master mode.

7	6	5	4	3	2	1	0
STARTING ADDRESS [15:8] PCI MASTER MODE							

Bit 7:0 Starting Address [15:8] in PCI Master Mode

SCR12: PCI Master Starting Address 23:16

Read/Write Address: 3C5h, Index: 12h
Power-on Default: Undefined

This register specifies the starting read/write address [23:16] in PCI master mode.

7	6	5	4	3	2	1	0
STARTING ADDRESS [23:16] PCI MASTER MODE							

Bit 7:0 Starting Address [23:16] in PCI Master Mode

SCR13: PCI Master Starting Address 31:24

Read/Write Address: 3C5h, Index: 13h
Power-on Default: Undefined

This register specifies the starting read/write address [31:24] in PCI master mode.

7	6	5	4	3	2	1	0
STARTING ADDRESS [31:24] PCI MASTER MODE							

Bit 7:0 Starting Address [31:24] in PCI Master Mode

SCR15: PCI Miscellaneous Control Register

Read Only Address: 3C5h, Index: 15h
Power-on Default: 00h

This register defines the various PCI control registers.

7	6	5	4	3	2	1	0
BRE	**R**	**SDE**	**DEA**	**PCI**	**RESERVED**		**DS**

Bit 7 PCI Burst Read Enable (BRE)
0 = Disable
1 = Enable. SCR17 bit 5 needs to be set to 1 in order for this bit to take effect. For example, if SCR17 bit 5 = 0, even this bit is set to 1, PCI burst read will not be enabled.

Bit 6 Reserved (R)

Bit 5 Software Abort Drawing Engine Enable (SDE)
0 = Normal
1 = Enable. This bit has no effect unless bit 4 is set to 1.

Bit 4 Drawing Engine Abort Enable (DEA)
0 = Normal
1 = Enable

Bit 3 PCI Configuration Space: Subsystem ID Lock Enable (PCI)
0 = Disable
1 = Enable

Bit 2:1 Reserved

Bit 0 LynxEM+ device select (DS)
0 = SM810
1 = SM811

SCR16: Status for Drawing Engine and Video Processor

Read Only Address: 3C5h, Index: 16h
Power-on Default: Undefined

This register specifies status of LynxEM+ including Drawing Engine Status, Video Processor Status, and Drawing Engine FIFO Available.

7	6	5	4	3	2	1	0
GES	**VWI**	**VWII**	**FIFO**	**DEBS**	**DEFIFO**		

Bit 7 Graphics Engine Status (GES)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 6 Video Window I Status (VWI)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 5 Video Window II Status (VWII)
0 = Indicate current display frame is using the source starting address
1 = Indicate current display frame is not using the source starting address

Bit 4 Drawing Engine FIFO Empty Status (FIFO)
0 = Drawing Engine FIFO empty
1 = Drawing Engine FIFO not empty

Bit 3 2D Drawing Engine Busy Status (DEBS)
0 = Drawing Engine Idle
1 = Drawing Engine Busy

Bit 2:0 # of Drawing Engine FIFO entries available in 32-bit quantity (DEFIFO)
000 = 1 entry available
001 = 2 entry available
010 = 3 entry available
011 = 4 entry available
100 = 5 entry available
101 = 6 entry available
110 = 7 entry available
111 = FIFO empty (if bit 4=0) or FIFO full (if bit 4=1)

SCR17: General Graphics Command Register 1

Read/Write Address: 3C5h, Index: 17h
Power-on Default: 00h

This register specifies command controls for Memory Access Disable, PCI bus master status, PCI bus burst write and burst read enable, Big-Endian Swap mode Select, Memory mapped access enable and BIOS ROM size select.

7	6	5	4	3	2	1	0
MAD	**R**	**PCI**	**BESM**	**DIRECT3D**		**MMA**	**DLT**

Bit 7 Memory Access Disable when Drawing Engine Busy (MAD)
0 = Normal
1 = Disable memory access when Drawing Engine is busy

Bit 6 Reserved (R)

Bit 5 PCI burst read and write enable. (PCI)
0 = Disable
1 = Enable

Bit 4 Big Endian Swap Mode Select (BESM)

0 = Big Endian with byte swap

1 = Big Endian with word swap

	[31:24]	[23:16]	[15:8]	[7:0}
↓				
After	**[7:0]**	**[15:8]**	**[23:16]**	**[31:24]**

	[31:16]	[15:0]
↓		
After	**[15:0]**	**31:16]**

Bit 3:2 Direct3D Z-Buffer Data Select

00 = Normal (use all 32-bit data)

01 = Use low word [15:0]

10 = Use high word [31:16]

11 = Normal (use all 32-bit data)

Bit 1 Memory Mapped Aperture Select (MMA)
0 = Select Banking Aperture. No Memory Mapped registers access allowed.
1 = Select Memory Mapped Aperture

Bit 0 Disable Latency Timer (DLT)
0 = Normal
1 = Disable latency timer count

SCR18: General Graphics Command Register 2

Read/Write Address: 3C5h, Index: 18h
Power-on Default: 00h

This register specifies command control for aperture select, graphics modes select, 32/64 memory data path select and linear addressing mode enable.

7	6	5	4	3	2	1	0
SCLK	**ECLK**	**AS**	**GRAPHICS MODE**		**MDP**	**ERH**	**LMM**

Bit 7 Select ~CLKRUN or ACTIVITY (SCLK)
0 = Select ~CLKRUN as input for Pin 161
1 = Select ACITIVITY as output for Pin 161

Bit 6 Enable ~CLKRUN Function (ECLK)
0 = disable
1 = enable

Bit 5 Aperture Select. This bit is only valid in linear memory mode (bit 0 = 1) (AS)
0 = Select dual aperture. Allow 0A0000h-0AFFFFh and linear aperture to coexist.
1 = Select single aperture. Only linear aperture can be used.

Bit 4:3 Graphics Modes Select for Memory Access
00 = Standard VGA mode. The memory access only uses the lower 32-bit of the 64-bit internal memory bus. The memory address wraps after 256 KB.
01 = VESA Super VGA 16 color (4-bit) mode. The memory access only uses the low 32-bit of the 64-bit internal memory bus. The memory address does not wrap after 256 KB.
1x = Extended packed pixel graphics modes (8/16/24/32-bit). The memory access always use the internal 64-bit memory bus.

Bit 2 32/64 memory data path select. This bit is only valid in VGA or VESA Super VGA 16 color modes (bit 4 of this register = 0) (MDP)
0 = CPU access VGA memory. All host memory access goes through VGA aperture: 0A0000h - 0BFFFFh (controlled by 3CFh index 6 Bit [3:2]). The memory access only uses the low 32-bit of the 64-bit memory bus.
1 = CPU access graphics memory. All host memory access does not goes through VGA aperture. This bit is used to allow 64-bit memory access even in VGA or super VGA 16 color modes.

For example, when programming pop-up icon in VGA mode or VESA super VGA 16 color mode, one must set bit 2 = 1 and bit 4 = 0 of this register, in order to access full range of the display memory.

Bit 1 Enable Repeat Hardware Rotation BLT function (ERH)
0 = disable
1 = enable

Bit 0 Linear Memory Mode Enable (LMM)
0 = disable. Nonlinear addressing (banking) mode is selected, and MCR61 register will be used for memory bank select. Memory will be accessed according to 3CF index 6 Bit [3:2]:

3CF.6 Bit [3:2]	**Memory Range**
00	0A0000-0BFFFF
01	0A0000-0AFFFF
10	0B0000-0B7000
11	0B8000-0BFFFF

1 = enable. Linear memory mode is selected, and memory will be accessed according to the PCI base address register. *To enable MMIO the following must be set prior to setting SCR18 [0]: SCR17 [1] = 1*.

SCR19: Interrupt Enable and Mask I

Read/Write Address: 3C5h, Index: 19h
Power-on Default: 00h

This register specifies interrupt enables and interrupt masks for PCI master, Zoom Video Port, and Drawing Engine. Each interrupt mask will block out its particular interrupt when the interrupt mask is enabled. When the interrupt mask is disabled, the corresponding interrupt will be generated when its particular interrupt is enabled.

7	6	5	4	3	2	1	0
R	**IEPCI**	**IEZVP**	**IEDE**	**R**	**IMPCI**	**IMZVP**	**IMDE**

Bit 7 Reserved (R)

Bit 6 Interrupt Enable for PCI Master (IEPCI)
0 = Disable
1 = Enable

Bit 5 Interrupt Enable for Zoom Video Port (IEZVP)
0 = Disable
1 = Enable

Bit 4 Interrupt Enable for Drawing Engine (IEDE)
0 = Disable
1 = Enable

Bit 3 Reserved

Bit 2 Interrupt Mask for PCI Master (IMPCI)
0 = Disable
1 = Enable

Bit 1 Interrupt Mask for Zoom Video Port (IMZVP)
0 = Disable
1 = Enable

Bit 0 Interrupt Mask for Drawing Engine (IMDE)
0 = Disable
1 = Enable

SCR1A: Interrupt Status

Read Only Address: 3C5h, Index: 1Ah
Power-on Default: Undefined

This register specifies Interrupt Status of Drawing Engine, Video Port, PCI Master, and VGA. The interrupt enable and mask bits for these interrupts are located in SCR19 register, with the exception of VGA's enable and mask bits which reside within the VGA block.

7	6	5	4	3	2	1	0
RESERVED			**VGA**	**R**	**PCI**	**ZVP**	**DEI**

Bit 7:5 ReservedI

Bit 4 VGA Interrupt Status. VGA's interrupt enable and mask bits are in the VGA block. (VGA)
0 = No interrupt
1 = VGA Interrupt is detected

Bit 3 Reserved (R)

Bit 2 PCI Master Interrupt Status (PCI)
0 = No interrupt
1 = PCI Master Interrupt is generated

Bit 1 Zoom Video Port Interrupt Status (ZVP)
0 = No interrupt
1 = Zoom Video Port Interrupt is detected

Bit 0 Drawing Engine Interrupt Status (DEI)
0 = No interrupt
1 = Drawing Engine Interrupt is detected

SCR1C: Interrupt Status USR 0-3

Read Only Address: 3C5h, Index: 1Ch
Power-on Default: Undefined

This register specifies the Interrupt Status for USR 0-3

7	6	5	4	3	2	1	0
RESERVED				**USR3**	**USR2**	**USR1**	**USR0**

Bit 7:4 ReservedI

Bit 3 Interrupt Status for USR3

Bit 2 Interrupt Status for USR2

Bit 1 Interrupt Status for USR1

Bit 0 Interrupt Status for USR0

SCR1F: Interrupt Mask & Interrupt Status USR 0-3

Read Only Address: 3C5h, Index: 1Fh
Power-on Default: Undefined

This register specifies Interrupt Mask and Interrupt enable register for USR 0-3.

7	6	5	4	3	2	1	0
HUSR3	**HUSR2**	**HUSR1**	**HUSR0**	**MUSR3**	**MUSR2**	**MUSR1**	**MUSR0**

Bit 7 Enable hardware interrupt for USR3 (HUSR3)
0 = Disable
1 = Enable USR3 PIN as Interrupt input

Bit 6 Enable hardware interrupt for USR2 (HUSR 2)
0 = Disable
1 = Enable USR2 PIN as Interrupt input

Bit 5 Enable hardware interrupt for USR1 (HUSR1)

Bit 4 Enable hardware interrupt for USR0 (HUSR0)

Bit 3 Mask out interrupt for USR3 (MUSR3)

Bit 2 Mask out interrupt for USR2 (MUSR2)

Bit 1 Mask out interrupt for USR1 (MUSR1)

Bit 0 Mask out interrupt for USR0 (MUSR0)

Power Down Control Registers

The power down control registers are controlled by system clock only. The power down control registers can still be read or written by CPU even when internal PLL is off.

PDR20: Power Down Control for Memory, Flat Panel, PLL, and Video Port

Read/Write Address: 3C5h, Index: 20h
Power-on Default: 04h

This register defines the different power down control for Memory, Flat Panel Interface, PLL, and Video Port. This register can still be read or written by CPU even when PLL is off.

7	6	5	4	3	2	1	0
SPDM	**SMR**	**SICLK**		**LVDS**	**VPO**	**FPI**	**DMI**

Bit 7 Select Power Down Mode. External "~PDOWN" pin needs to be pulled "Low" to enable the selected power down mode. For more details on power down modes, please refer to the power down management chapter of this data book. (SPDM)
0 = Standby mode
1 = Sleep mode

Bit 6 Select Memory Refresh Type During Sleep Mode (Bit 7 of this register = 1). (SMR)
0 = Auto Refresh
1 = Self Refresh

Bit 5:4 Select internal VCLK and MCLK frequencies to control DRAM refresh during standby or sleep mode (CCR69 bit 3 = 1). This register setting will be ignored when the chip is in operation mode. (SICLK)
00 = No change.
01 = Both VCLK and MCLK are divided by 4 (standby and sleep mode)
10 = Both VCLK and MCLK are divided by 8 (standby and sleep mode)
11 = Both VCLK and MCLK are divided by 16 (sleep mode only)

Bit 3 Tri-state LVDSCLK output pin. When ~EXCKEN = 0, Pin 159 (MCKIN) becomes an input pin. When ~EXCKEN = 1, Pin 159 (LVDSCLK) becomes an output pin. This register is only valid when ~EXCKEN = 1. This bit is used to test the silicon. (LVDS)
0 = Enable LVDSCLK output pin
1 = Tri-state LVDSCLK output pin

Bit 2 Tri-state Video Port Output. When this bit = 0, 20-bit outputs (R[7:2], G[7:2], B[7:2], BLANK, and PCLK) will be driven out. When Video Capture is enabled (CPR00 [0] = 1), video port output will be tri-stated automatically, except for BLANK/TVCLK output pin. This bit is used to test the silicon. (VPO)
0 = Enable output pins
1 = Tri-state output pins (default)

Bit 1 Tri-state Flat Panel Interface Output Pins. This bit is used to test the silicon (FPI)
0 = Enable output pins
1 = Tri-state output pins

Bit 0 Tri-state Display Memory Interface output pins. This bit can also be used to isolate LynxEM+ from display memory. All display memory interface pins: control signals, output clock, data bus and address bus are tri-stated. This bit is used to test the silicon. (DMI)
0 = Enable display memory interface output pins

1 = Tri-state display memory interface output pins

PDR21: Functional Blocks Disable Control

Read/Write Address: 3C5h, Index: 21h
Power-on Default: 00h

This register is designed to achieve optimum power saving in operation mode. Special clock drivers are built-in to control major functional blocks independently. This power saving feature will not affect the graphics and video performance, or LCD display quality. This register could be read or written by CPU even when PLL is off.

7	6	5	4	3	2	1	0
MHZ	**PLLS**	**FBWO**	**FBRO**	**CPR**	**ZVP**	**DE**	**VP**

Bit 7 Disable 135 MHz DAC (MHZ)
0 = Enable DAC
1 = Disable DAC

Bit 6 Disable PLLs (PLLS)
0 = Enable PLLs
1 = Disable PLLs

Bit 5 Disable LCD Frame Buffer Write Operation. This bit is used to shut-down the 64 x 8 LCD write FIFO and remove the display memory bus request for LCD frame buffer write from arbitration control. (FBWO)

This bit needs to be set to "1" in Dual View Mode -- displaying different graphics data on CRT (or TV) and LCD.

This bit should be set to "1" when LCD display is not enabled or when TFT is selected in standard refresh mode in order to obtain optimum power saving.
0 = Enable LCD frame buffer write
1 = Disable LCD frame buffer write

Bit 4 Disable LCD Frame Buffer Read Operation and DSTN Dithering Engine. This bit is used to shut-down the 64 x 8 LCD read FIFO1 and LCD read FIFO2, turn off DSTN dithering engine and remove the display memory bus request from LCD Read FIFO1 and LCD read FIFO2. (FBRO)

This bit should be set to "1" when LCD display is not enabled, or when TFT is selected in standard refresh mode.
0 = Enable LCD frame buffer read and DSTN dithering engine
1 = Disable LCD frame buffer read and DSTN dithering engine

Bit 3 Disable 256 x 18 Color Palette RAM. Color Palette RAM will be automatically disabled by hardware in standby mode or sleep mode. (CPR)
0 = Enable Color Palette RAM
1 = Disable Color Palette RAM

Bit 2 Disable Zoom Video Port. This bit is used when there is no external video source which is connected to the LynxEM+. The LynxEM+ will block input data from external video port, turn off the clock driver of ZV Port, and remove the ZV Port display memory bus request from memory controller. (ZVP)
0 = Enable Zoom Video Port
1 = Disable Zoom Video Port

Bit 1 Disable 2D Drawing Engine. This bit is used to turn-off the 2D drawing engine block. For optimum power saving, this bit should be set to "1" in standard VGA mode since 2D drawing engine is not in use. (DE)
0 = Enable 2D drawing engine
1 = Disable 2D drawing engine

Bit 0 Disable Video Processor. This bit is used to turn-off the video processor block which includes graphics FIFO, V0FIFO, V1FIFO, horizontal/vertical color interpolation, YUV-to-RGB conversion, TV flicker reduction, HW pop-up icon, and related control logic. For optimum power saving, This bit could be set to "1" in standard VGA mode since video processor is not in use. (VP)
0 = Enable video processor
1 = Disable video processor

PDR22: LCD Panel Control Select

Read/Write Address: 3C5h, Index: 22h
Power-on Default: x0h

This register specifies the flat panel control and data: FPEN, VBIASEN, FPVDDEN. This register is not valid when panel S/W power ON/OFF sequence is selected during display switching - FPR34 bit 7 = 0. For panel power ON/OFF sequence, please refer to the flat panel interface chapter of this data book.

7	6	5	4	3	2	1	0
RESERVED		**DPMS CONTROL**		**FPEN**	**VOP**	**FP**	**FOP**

Bit 7:6 Reserved

Bit 5:4 DPMS Control

	DPMS State	**VSYNC**	**HSYNC**
00 =	Normal	Pulses	Pulses
01 =	Standby	Pulses	No Pulse
10 =	Suspend	No Pulse	Pulses
11 =	Off	No Pulse	No Pulse

Bit 3 Control FPEN output pin. This function is disabled when LCD H/W auto-power ON/OFF sequence is enabled (FPR34 bit 7 = 1). This pin can also be used to control LCD back light (VBKLGT) at the same time. FPEN is part of the VESA FDPI-1B specification. (FPEN)
0 = Driven low
1 = Driven high

Bit 2 Control VBIASEN output pin. This function is disabled when LCD H/W auto-power ON/OFF sequence is enabled (FPR34 bit 7 = 1). (VOP)

0 = Driven low
1 = Driven high

Bit 1 Disable Flat Panel control signals and data lines. All Control signals and data lines from output pins will be forced to logic "Low". (FP)
0 = Enable Flat Panel control signals and data
1 = Disable Flat Panel control signals and data

Bit 0 Control FPVDDEN output pin. This function is disabled when LCD H/W auto-power ON/OFF sequence is enabled (FPR34 bit 7 = 1). (FOP)
0 = Driven low
1 = Driven high

PDR23: Activity Detection Control Register

Read/Write Address: 3C5h, Index: 23h
Power-on Default: 00h

The activity detection function is used to monitor I/O write and memory write activities. System designer can select a fixed time period by programming bit [2:0] of this register. An internal timer will count the idle period of memory write or I/O write operation. If the idle period is equal or greater than the selected value, a "Low-High" or "High-Low" on the ACTIVITY output signal will generate to the system. Any Memory write or I/O write operation will reset the ACTIVITY output signal and the internal counter. Please note that the internal counter will not start unless video capture is disabled (VPR3C bit 0 = 0). The activity detection can also be used to enable internal auto-standby mode.

7	6	5	4	3	2	1	0
ECAD	**EIAS**	**SA**	**SELECT I/O**		**INTERNAL TIMER SELECT**		

Bit 7 Enable chip activity detection (ECAD)
0 = Disable
1 = Enable

Bit 6 Enable internal auto-standby mode. This bit has no effect if chip activity detection is disabled (PDR23 bit 7 = 0). This bit is used to enable internal auto-standby mode through activity detection function. Before enabling this function, the internal timer bit [2:0] of this register needs to be programmed first. (EIAS)0 = Disable
1 = Enable

Bit 5 Select active "LOW" or "HIGH" signal for the ACTIVITY output (SA)
0 = Select active "LOW"
1 = Select active "HIGH"

Bit 4:3 Select I/O Write Activity Detection or Host Memory Write Activity Detection
00 = No detection
01 = Enable Host Memory Write detect
10 = Enable I/O Write detect
11 = Enable both I/O Write and Host Memory Write detect

Bit 2:0 Internal Timer Select

000 = Select 0 minute
001 = Select 1 minute (4K vertical frames period in standard setting)
010 = Select 2 minutes
.....
110 = Select 32 minutes
111 = Select 64 minutes (256K vertical frames period)

PDR24: Power Down Register Select

Read/Write Address: 3C5h, Index: 24h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED							**PDMS**

Bit 7:1 Reserved

Bit 0 Power Down Mode Select (PDMS)
0 = VESA Compliance power down mode
1 = PCI power down Spec 1.0 compliance

Flat Panel Registers

FPR30: Flat Panel Type Select

Read/Write Address: 3C5h, Index: 30h
Power-on Default: This is a power-on configurable register (by RESET)

This register specifies different types of flat panel.

7	6	5	4	3	2	1	0
DSTN	**COLOR TFT**			**LCD DISPLAY**		**TFT**	**LCD**

Bit 7 Color DSTN interface type select. This bit is power-on configurable by MD15. (DSTN)
0 = 16-bit interface
1 = 24-bit interface

Bit 6:4 Color TFT interface type select. This is a power-on configurable bit by MD [14:12]. For detailed interconnection for different type of LCD panels, please refer to the Flat Panel Interface Chapter of this data book.
000 = 9-bit, 3-bit per R, G, B
001 = 12-bit, 4-bit per R, G, B
010 = 18-bit, 6-bit per R, G, B
011 = 24-bit, 8-bit per R, G, B
100 = 12+12-bit, or 24-bit (two pixels/clock)
101 = analog TFT interface
110 = 18+18-bit, or 36-bit (two pixels/clock)

others = reserved

Bit 3:2 LCD display size select for DSTN and TFT LCD. This is a power-on configurable bit by MD [11:10].
00 = 640 x 480
01 = 800 x 600
10 = 1024 x 768

Bit 1 TFT FPSCLK Clock Phase Select. To adjust TFT flat panel data timing, one may wish to change the TFT FPSCLK phase by inverting the TFT FPSCLK. This register is only valid for TFT panel in single pixel/clock mode and 2 pixels/clock mode. (TFT)
This is a power-on configurable bit by MD9.
0 = Normal
1 = Inverted clock

Bit 0 Color LCD type select. This is a power-on configurable bit by MD8. (LCD)
0 = color TFT
1 = color DSTN

FPR31: Virtual Refresh and Auto Shut Down Control

Read/Write Address: 3C5h, Index: 31h
Power-on Default: 00h

This register defines the control for display select, Virtual Refresh mode enable and auto shut-down.

7	6	5	4	3	2	1	0
VRE	**VRES**	**SELECT AUTO S/D**		**EASD**	**DISPLAY SELECT**		

Bit 7 Virtual Refresh Enable. This bit is independent of FPR31 bit [2:0]. (VRE)
0 = Disable
1 = Enable

Bit 6 Virtual Refresh Encode Select (VRES)
0 = Select 8-bit per pixel encode, RGB = 3:3:2
1 = Select 16-bit per pixel encode, RGB = 5:6:5

Bit 5:4 Select Auto Shut-Down Period. Define a period to start auto shut-down of display memory screen refresh cycle and LCD frame buffer write cycle. Auto shut-down mode can only be used when the display is in LCD mode only and Virtual Refresh is enabled. This function is only valid when auto shut-down of memory screen refresh and LCD frame buffer write cycles are enabled (bit 3 of this register = 1).
00 = 8 frames
01 = 16 frames
10 = 32 frames
11 = 64 frames

Bit 3 Enable auto shut-down of display memory screen refresh cycle and LCD frame buffer write cycle in Virtual Refresh mode. This bit is only valid when Virtual Refresh mode is enabled (FPR31 bit 7 = "1"). If the display memory write operation is idle for more than the selected period specified by FPR31 bit

[5:4], the display memory screen refresh cycle and LCD frame buffer write cycle will be automatically shut-down when auto shut-down is enabled. The graphics FIFO and video FIFO are also shut-down. Any Host memory write operation to LynxEM+ will turn on the display memory screen refresh and LCD frame buffer write cycle at the end of a vertical sync signal. (EASD)
0 = Disable auto shut-down
1 = Enable auto shut-down

Bit 2:0 Display Select. (Note: TV and CRT can not be enabled at the same time.)
000 = Disable all displays (default value)
001 = Enable LCD display
010 = Enable CRT display
011 = Enable both CRT and LCD display
100 = Enable TV display
101 = Enable both TV and LCD display
others = Reserved

FPR32: Dithering Engine Select, Polarity, and Expansion Control

Read/Write Address: 3C5h, Index: 32h
Power-on Default: 00h

This register defines the TFT and DSTN dithering engines select, LCD signal polarities, and screen auto-centering or vertical expansion select.

7	6	5	4	3	2	1	0
TFT DITHERING		**STN**	**LCDV**	**LCDH**	**ACE**	**VLEE**	**HPEE**

Bit 7:6 TFT Dithering Engine Select
00 = No dithering
01 = 4-gray level dithering patterns (for 9-bit, 12-bit, and 18-bit TFT only)
10 = 8-gray level dithering patterns (for 9-bit and 12-bit TFT only)
11 = Reserved

	FPR30 [6:4]			
	= 000	= 001 or 100	= 010 or 110	= 011
Bit [7:6]	**9-bit**	**12-bit**	**18-bit**	**24-bit**
00	512 colors	4K colors	256K colors	16M colors
01	24,389 colors	226,981 colors	16M colors	16M colors
10	185,193 colors	1,771,561 colors	16M colors	16M colors

Bit 5 STN Dithering Engine Select (STN)
0 = Select 64 gray levels for each R, G, and B
1 = Select 256 gray levels for each R, G, and B

Bit 4 LCD VSYNC/FP Polarity Select (LCDV)
0 = Select active "LOW"
1 = Select active "HIGH"

Bit 3 LCD HSYNC/LP polarity Select (LCDH)
0 = Select active "LOW"
1 = Select active "HIGH"

Bit 2 Auto Centering Enable. This register is used to control screen centering for VGA modes. (ACE)
0 = Disable
1 = Enable. This bit needs to be set to "1" and CRT shadow registers need to be reprogrammed to allow screen centering.

Bit 1 Vertical Line Expansion Enable for VGA modes (VLEE)
0 = Disable
1 = Enable

Bit 0 Horizontal Pixel Expansion Enable for VGA modes (HPEE)
0 = Disable
1 = Enable. Character clock is forced to 10-dot timing.

FPR33: Panel Power Sequence and LCD Character/Cursor Blink Control

Read/Write Address: 3C5h, Index: 33h
Power-on Default: 05h

This register defines the control for LCD power ON/OFF sequence timing, lock VGACRT horizontal and vertical display enable, and blinking rate for LCD character/cursor.

7	6	5	4	3	2	1	0
RESERVED		**VDE**	**R**	**PANEL ON/OFF**		**SELECT LCD**	

Bit 7:6 Reserved

Bit 5 Lock VGA CRT Vertical and Horizontal Display Enable registers used in Virtual Refresh mode (FPR31 bit 7 = 1) to lock the control signals to LCD BKEND. When this bit is set to 1, it will lock the following registers: CRT01 (3?5h, index1) [Horizontal Display Enable], CRT07 (3?5h, index 07) bit 6 [Vertical Display Enable bit 9] and bit 1[Vertical Display Enable bit 8], CRT12 (3?5h, index12) [Vertical Display Enable]. (VDE)
This register is also used to lock Shadow VGA CRT Horizontal Display Enable and Vertical Display Enable Registers.
0 = unlock (default)
1 = lock

Bit 4 Reserved (R)

Bit 3:2 Panel ON/OFF timing select. These two bits are used to control the time period from FPEN to VBIASEN, from VBIASEN to LCD control signals, and from LCD control signals to FPVDDEN. These two bits are only valid when LCD H/W auto-power ON/OFF sequence is selected (FPR34 bit 7 =1).
00 = 1 vertical frame
01 = 2 vertical frames

10 = 4 vertical frames
11 = 8 vertical frames

Bit 1:0 Select LCD character/cursor blink rate

Bit [1:0]	Cursor	Character
00	16 frames	32 frames
01	32 frames	64 frames
10	64 frames	128 frames

FPR34: LCD Panel ON/OFF Sequence Select and DSTN LCD Control

Read/Write Address: 3C5h, Index: 34h
Power-on Default: 80h

This register defines LCD panel ON/OFF sequence select during display switching and color DSTN panel control, such as: LP pulse width, additional line pulse in odd and even frame.

7	6	5	4	3	2	1	0
SHS	**SLP**	**SELPO**		**SELECT EXTRA LP EVEN FRAME**			

Bit 7 Select Hardware or Software LCD auto-power ON/OFF sequence during display switching in operation or power down modes. This bit can be used to select two different ways to turn ON/OFF LCD panel. For special programming sequences, please refer to the Power Down Management chapter of this data book. (SHS)
0 = Select software LCD power sequencing
1 = Select hardware LCD power sequencing

Bit 6 Select LP (DSTN) Pulse Width in Pixel Clocks (SLP)
0 = 16 pixel clocks
1 = 32 pixel clocks

Bit 5:4 Select Extra LP in Odd Frame for DSTN LCD in Standard Refresh Mode (SELPO)
00 = 0 extra line pulses
01 = 1 extra line pulses
10 = 2 extra line pulses
11 = 3 extra line pulses

Bit 3:0 Select Extra LP in Even Frame for DSTN LCD in Standard Refresh Mode, or Extra LP in Every Frame for DSTN LCD in Virtual Refresh Mode.
0000 = 0 extra line pulses
0001 = 1 extra line pulses
0010 = 2 extra line pulses
.....
1111 = 15 extra line pulses

FPR3E: DSTN LCD Panel Height - High

Read/Write Address: 3C5h, Index: 3Eh
Power-on Default: 00h

This register defines bit 9 and bit 8 of DSTN LCD panel height register. This 10-bit register needs to be programmed as "DSTN LCD panel height ÷ 2". This 10-bit register also has to be an even number. For example, DSTN LCD panel height register equals to "12Ch" for a 800x600 DSTN.

7	6	5	4	3	2	1	0
DES	**R**	**GFIFO**	**VFIFO**	**FPD**	**LP**	**DSTN LCD PANEL**	

Bit 7 M-Signal or Display Enable Select (DES)
0 = Select Display Enable as output for Pin 81
1 = Select M-Signal as output for Pin 81

Bit 6 Reserved (R)

Bit 5 Graphic FIFO flipping - Software sets this bit and continues to sample until = 0 (GFIFO)

Bit 4 Video FIFO flipping - Software sets this bit and continues to sample until = 0 (VFIFO)

Bit 3 Frame pulse detection - Software sets this bit and continues to sample until = 0 (FPD)

Bit 2 Free running LP enable for DSTN (LP)
0 = Disable
1 = Enable

Bit 1:0 Bit 9 and bit 8 of the 10-bit DSTN LCD Panel Height Register.

FPR3F: DSTN LCD Panel Height- Low

Read/Write Address: 3C5h, Index: 3Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
BIT [7:0] OF THE 10-BIT DSTN LCD PANEL HEIGHT REGISTER							

This register defines lower 8-bit of DSTN LCD panel height register. This 10-bit register needs to be programmed as "DSTN LCD panel height ÷ 2". This 10-bit register also has to be an even number. For example, DSTN LCD panel height register equals to "180h" for a 1024x768 DSTN LCD.

Bit 7:0 Bit [7:0] of the 10-bit DSTN LCD Panel Height Register.

FPR40: Read FIFO1 Start Address Low for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 40h

Power-on Default: Undefined

This register defines the lower 8-bit of the read FIFO1 start address for LCD frame buffer. This Read FIFO1 start address is used for DSTN LCD in standard refresh mode or TFT LCD in Virtual Refresh mode. When DSTN LCD is selected and in Virtual Refresh mode, this register defines the lower 8-bit of the read FIFO1 start address for upper panel of the DSTN LCD.

7	6	5	4	3	2	1	0
BIT [7:0] OF DISPLAY MEMORY READ FIFO1							

Bit 7:0 Select bit [7:0] of display memory read FIFO1 address bus for the LCD frame buffer of DSTN LCD in standard refresh mode or for TFT LCD in Virtual Refresh mode. When Virtual Refresh is enabled (FPR31 bit 7 = 1) and when DSTN LCD is selected (FPR30 [1:0] = 01b), this register selects bit [7:0] of the display memory read FIFO1 address for the upper panel of DSTN LCD.

FPR41: Read FIFO1 Start Address High for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 41h
Power-on Default: Undefined

This register defines the higher 8-bit of the read FIFO1 start address for LCD frame buffer. This Read FIFO1 start address is used for DSTN LCD in standard refresh mode or TFT LCD in Virtual Refresh mode. When DSTN LCD is selected and in Virtual Refresh mode, this register defines the higher 8-bit of the read FIFO1 start address for upper panel of the DSTN LCD.

7	6	5	4	3	2	1	0
BIT [15:8] OF DISPLAY MEMORY READ FIFO1							

Bit 7:0 Select bit [15:8] of display memory read FIFO1 address bus for the LCD frame buffer of DSTN LCD in standard refresh mode or for TFT LCD in Virtual Refresh mode. When Virtual Refresh is enabled (FPR31 bit 7 = 1) and when DSTN LCD is selected (FPR30 [1:0] = 01b), this register selects bit [15:8] of the display memory read FIFO1 address for the upper panel of DSTN LCD.

FPR42: Read FIFO2 Start Address Low for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 42h
Power-on Default: Undefined

This register defines the lower 8-bit of the read FIFO2 start address for LCD frame buffer. This register is only valid when DSTN LCD is selected (FPR30 [1:0] = 01b) and Virtual Refresh is enabled (FPR31 bit 7 = 1).

7	6	5	4	3	2	1	0
BIT [7:0] OF DISPLAY MEMORY READ FIFO2							

Bit 7:0 Select bit [7:0] of display memory read FIFO2 address bus for lower panel of DSTN LCD.

FPR43: Read FIFO2 Start Address High for LCD Frame Buffer

Read/Write Address: 3C5h, Index: 43h
Power-on Default: Undefined

This register defines the higher 8-bit of the read FIFO2 start address for LCD frame buffer. This register is valid only when DSTN LCD is selected (FPR30 [1:0] = 01b) and Virtual Refresh is enabled (FPR31 bit 7 = 1).

7	6	5	4	3	2	1	0
BIT [15:8] OF DISPLAY MEMORY READ FIFO2							

Bit 7:0 Select bit [15:8] of display memory read FIFO2 address bus for lower panel of DSTN LCD.

FPR44: Read FIFO1 Offset Value of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 44h
Power-on Default: Undefined

This register defines the read FIFO1 offset value of LCD Frame buffer. This offset value is used to calculate the read start address of the next line of LCD Frame buffer from the current line. The offset register is a 10-bit register. Bit [9:8] of Read Offset Value Register are in FPR45 register.

7	6	5	4	3	2	1	0
BIT [7:0] OF READ FIFO1							

Bit 7:0 Bit [7:0] of read FIFO1 offset value for LCD frame buffer. This offset value is a direct mapping from bit [10:3] of display memory read address bus.

FPR45: Read FIFO1 Address Offset for LCD Frame Buffer Overflow

Read/Write Address: 3C5h, Index: 45h
Power-on Default: Undefined

This register defines the MSB of the read FIFO1 start address. In additional, this register specifies the MSB of the LCD frame buffer read offset value.

7	6	5	4	3	2	1	0
RFIFO1		**DMFIFO1**			**DISPLAY MEM READ FIFO2**		

Bit 7:6 Bit [9:8] of Read FIFO1 offset value register of LCD Frame buffer. These two bits are mapped to bit [12:11] of display memory address bus. The lower 8 bits are in FPR44 register. (RFIFO1)

Bit 5:3 Bit [18:6] of display memory read FIFO1 address bus. The lower [15:0] of display memory read FIFO1 address is located in FPR41 and FPR40 registers. (DMFIFO1)

When TFT LCD is in Virtual Refresh mode, or DSTN LCD is in standard refresh mode, this register specifies bit [18:16] of display memory read address. This register is used for upper panel of DSTN LCD when Virtual Refresh is enabled (FPR 31 bit 7 = 1) and DSTN LCD (FPR30 [1:0] = 01b) is selected.

Bit 2:0 Bit [18:16] of display memory read FIFO2 address bus for lower panel of DSTN LCD. The lower [15:0] of display memory read FIFO1 address is located in FPR43 and FPR42 registers. This register is valid only when DSTN LCD is selected (FPR30 [1:0] = 01b) and Virtual Refresh is enabled (FPR31 bit 7 = 1).

FPR46: Write Start Address Low of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 46h
Power-on Default: Undefined

This register defines the lower 8-bit of the start address for LCD Write Frame Buffer.

7	6	5	4	3	2	1	0
BIT [7:0] OF START ADDRESS LCD							

Bit 7:0 Bit [7:0] of start address for LCD write frame buffer. This register is a direct mapping from bit [10:3] of display memory write address bus.

FPR47: Write Start Address High of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 47h
Power-on Default: Undefined

This register defines the high byte start address of LCD Write Frame Buffer.

7	6	5	4	3	2	1	0
BIT [7:0] OF START ADDRESS LCD WRITE FRAME BUFFER							

Bit 7:0 Bit [15:8] of start address for LCD write frame buffer. This register is a direct mapping from bit [18:11] of display memory write address bus.

FPR48: Write Offset Value of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 48h
Power-on Default: Undefined

This register defines the offset value of LCD Write Frame Buffer. This offset value is used to calculate the start address of the next line of LCD Write Frame Buffer from the current line. The offset register is a 10-bit register. Bit [9:8] of the write offset value is in FPR49 register.

7	6	5	4	3	2	1	0
BIT [7:0] OF OFFSET VALUE LCD WRITE FRAME BUFFER							

Bit 7:0 Bit [7:0] of offset value for LCD write frame buffer. This offset value is a direct mapping from bit [10:3] of display memory write address bus.

FPR49: LCD Frame Buffer Write Overflow

Read/Write Address: 3C5h, Index: 49h
Power-on Default: Undefined

This register specifies the MSB of the LCD frame buffer write offset address. The lower 8-bit of the LCD frame buffer write offset address is in FPR48.

7	6	5	4	3	2	1	0
RESERVED			**START ADDRESS LCD**			**OVR**	

Bit 7:5 Reserved

Bit 5:2 Bit [18:16] of start address for LCD Write Frame Buffer. This register is a direct mapping from bit [21:19] of display memory write address bus.

Bit 1:0 Bit [9:8] of offset value register of LCD Write Frame Buffer. These two bits are mapped to bit 12 and 11 of display memory write address bus. The lower 8 bits are in FPR48. (OVR)

FPR4A: LCD Read and Write FIFOs Request Level Control

Read/Write Address: 3C5h, Index: 4Ah
Power-on Default: 44h

This register controls the LCD Read and Write FIFOs Request Level. These bits can be used to maximize the available memory bandwidth.

7	6	5	4	3	2	1	0
LCD READ FIFO2		**LCD READ FIFO1**		**RESERVED**		**LCD WRITE FIFO**	

Bit 7:6 LCD Read FIFO2 Request Level. When the LCD Read FIFO2 empty level reaches the level specified by this register, a LCD Read FIFO2 Request will be generated.
00 = RFIFO2 has 4 or more entries empty
01 = RFIFO2 has 8 or more entries empty
1x = RFIFO2 has 12 or more entries empty

Bit 5:4 LCD Read FIFO1 Request Level. When the LCD Read FIFO1 empty level reaches the level specified by this register, a LCD Read FIFO1 Request will be generated.
00 = RFIFO1 has 4 or more entries empty
01 = RFIFO1 has 8 or more entries empty
1x = RFIFO1 has 12 or more entries empty

Bit 3:2 Reserved

Bit 1:0 LCD Write FIFO Request Level. When the LCD Write FIFO filled level reaches the level specified by this register, a LCD Write Request will be generated.
00 = WFIFO has 4 or more entries filled
01 = WFIFO has 8 or more entries filled
1x = WFIFO has 12 or more entries filled

FPR4B: Read FIFO2 Offset Value of LCD Frame Buffer

Read/Write Address: 3C5h, Index: 4Bh
Power-on Default: Undefined

This register defines the read FIFO2 offset value of LCD Frame buffer. This offset value is used to calculate the read start address of the next line of LCD Frame buffer from the current line. The offset register is a 10-bit register.

7	6	5	4	3	2	1	0
BIT [7:0] OF READ FIFO2 OFFSET VALUE							

Bit 7:0 Bit [7:0] of read FIFO2 offset value for LCD frame buffer. This offset value is a direct mapping from bit [10:3] of display memory read address bus. The upper two bits are in FPR4C register.

FPR4C: Read FIFO Offset Value of LCD Frame Buffer Overflow

Read/Write Address: 3C5h, Index: 4Ch
Power-on Default: Undefined

This register defines the read FIFO offset value of LCD Frame buffer. This offset value is used to calculate the read start address of the next line of LCD Frame buffer from the current line.

7	6	5	4	3	2	1	0
READ FIFO2		**RESERVED**					

Bit 7:6 Bit [9:8] of Read FIFO2 offset value register of LCD Frame buffer. These two bits are mapped to bit [12:11] of display memory address bus. The lower 8 bits are in FPR4B register.

Bit 5:0 Reserved

FPR50: LCD Overflow Register 1 for Virtual Refresh

Read/Write Address: 3C5h, Index: 50h
Power-on Default: Undefined

This register defines the high order MSB bits of LCD Horizontal Sync Start (FPR54), and LCD Vertical Total (FPR55) registers which are used to control Virtual Refresh timing.

7	6	5	4	3	2	1	0
RESERVED				**[10:8] FPR55**			**FPR54**

Bit 7:4 Reserved

Bit 3:1 Bit [10:8] of FPR55, Vertical Total of LCD in Virtual Refresh mode

Bit 0 Bit 8 of FPR54, Horizontal Sync Start of LCD in Virtual Refresh mode (FPR54)

FPR51: LCD Overflow Register 2 for Virtual Refresh

Read/Write Address: 3C5h, Index: 51h
Power-on Default: Undefined

This register defines the overflow bits of FPR52, FPR53, FPR56, and FPR57 registers which are used to control Virtual Refresh timing.

7	6	5	4	3	2	1	0
[10:8] FPR57			**[10:8] FPR 56**			**FPR53**	**FPR4\52**

Bit 7:5 Bit [10:8] of FPR57, Vertical Sync Start of LCD in Virtual Refresh mode

Bit 4:2 Bit [10:8] of FPR56, Vertical Display End of LCD in Virtual Refresh mode

Bit 1 Bit 8 of FPR53, Horizontal Display End of LCD in Virtual Refresh mode (FPR53)

Bit 0 Bit 8 of FPR52, Horizontal Total of LCD in Virtual Refresh mode (FPR52)

FPR52: LCD Horizontal Total for Virtual Refresh

Read/Write Address: 3C5h, Index: 52h
Power-on Default: Undefined

This register defines the bit [7:0] of LCD Horizontal Total. This register is used in Virtual Refresh mode only. It represents one line in TFT LCD and two lines in DSTN LCD. The LSB bit represents a 8-pixel period. The equation to calculate the LCD horizontal total in Virtual Refresh mode is as follows:

For TFT: LCDHT = (LCD panel width + horizontal blanking pixels) ÷ 8 - 1
For DSTN: LCDHT = (LCD panel width * 2 + horizontal blanking pixels) ÷ 8 - 1

7	6	5	4	3	2	1	0
LCD HORIZONTAL TOTAL							

Bit 7:0 LCD Horizontal Total [7:0] in Virtual Refresh mode. Bit 8 of LCD horizontal total is in FPR51 register.

FPR53: LCD Horizontal Display Enable for Virtual Refresh

Read/Write Address: 3C5h, Index: 53h
Power-on Default: Undefined

This register defines the active horizontal display period of LCD in Virtual Refresh mode. It represents one line in TFT LCD and two lines in DSTN LCD. The equation to calculate the LCD horizontal display enable in Virtual Refresh mode:

For TFT: LCDHDE = (LCD panel width pixels) ÷ 8 - 1
For DSTN: LCDHDE = (LCD panel width * 2) ÷ 8 - 1

7	6	5	4	3	2	1	0
LCD HORIZONTAL DISPLAY ENABLE PERIOD							

Bit 7:0 LCD Horizontal display enable period [7:0] in Virtual Refresh mode. Bit 8 of LCD horizontal display enable is in FPR51 register.

FPR54: LCD Horizontal Sync Start for Virtual Refresh

Read/Write Address: 3C5h, Index: 54h
Power-on Default: Undefined

This register defines the LCD horizontal sync start in Virtual Refresh mode. This register is used to generate the start timing of HYSNC for TFT LCD, or the start timing of LP for DSTN LCD. The value in LCDHSS needs to be larger than the value in LCDHDE. The horizontal sync pulse width is 8 pixels or 16 pixels wide, which is dependent on FPR34 bit 6.

7	6	5	4	3	2	1	0
LCD HORIZONTAL SYNC START PERIOD							

Bit 7:0 LCD Horizontal sync start period [7:0] in Virtual Refresh mode. Bit 8 of LCD horizontal sync start is in FPR50 register.

FPR55: LCD Vertical Total for Virtual Refresh

Read/Write Address: 3C5h, Index: 55h
Power-on Default: Undefined

This register defines the bit [7:0] of LCD Vertical Total. This register is used in Virtual Refresh mode only. The calculation equation of LCD vertical total in Virtual Refresh mode is as follows:

For TFT: LCDVT = (LCD panel height + vertical blank lines) - 1

For DSTN: LCDVT = ((LCD panel height ÷ 2) + vertical blank lines) - 1

7	6	5	4	3	2	1	0
LCD VERTICAL TOTAL							

Bit 7:0 LCD Vertical Total [7:0] in Virtual Refresh mode. Bit [10:8] of LCD vertical total are in FPR50 register.

FPR56: LCD Vertical Display Enable for Virtual Refresh

Read/Write Address: 3C5h, Index: 56h
Power-on Default: Undefined

This register defines the LCD active vertical display period in Virtual Refresh mode. The calculation equation of LCD vertical display enable in Virtual Refresh mode is as follows:

For TFT: LCDVDE = (LCD panel height) - 1

For DSTN: LCDVDE = (LCD panel height ÷ 2) - 1

7	6	5	4	3	2	1	0
LCD VERTICAL DISPLAY ENABLE PERIOD							

Bit 7:0 LCD vertical display enable period [7:0] in Virtual Refresh mode. Bit [10:8] of LCD vertical display enable are in FPR51 register.

FPR57: LCD Vertical Sync Start for Virtual Refresh

Read/Write Address: 3C5h, Index: 57h
Power-on Default: Undefined

This register defines the LCD vertical sync start in Virtual Refresh mode. This register is used to generate the start timing VSYNC for TFT LCD, or the start timing of FP for DSTN LCD. The value in LCDVSS needs to be larger than the value in LDVDE. The vertical sync pulse width is equal to one horizontal scan line.

7	6	5	4	3	2	1	0
LCD VERTICAL SYNC START PERIOD							

Bit 7:0 LCD Vertical sync start period [7:0] in Virtual Refresh mode. Bit [10:8] of LCD vertical sync start are in FPR51 register.

FPR58: EMI Control Register

Read/Write Address: 3C5h, Index: 58h
Power-on Default: 00h

This register defines the EMI control register for LCD flat panels, including LCD Panel I/O pad drive strength, FSPCLK clock delay control.

7	6	5	4	3	2	1	0
RESERVED				**EMIRC**	**LCD**	**FPSCLK**	

Bit 7:4 Reserved

Bit 3 EMI reduction control (EMIRC)
0 = disable
1 = enable

Bit 2 LCD Panel I/O pad drive strength select (LCD)
0 = 8 mA
1 = 6 mA

Bit 1:0 FPSCLK Clock Control. Each unit of clock is approximately 1.2ns best case or 2.0ns best case.
00 = normal
01 = FPSCLK delays by 1 unit of clock
10 = FPSCLK delays by 2 unit of clock
11 = FPSCLK delays by 3 unit of clock

FPR59: Panel M-Signal Control Register

Read/Write Address: 3C5h, Index: 59h
Power-on Default: 00h

This register defines the panel M-signal control such as modulation clock and modulation count.

7	6	5	4	3	2	1	0
MCS	**MODULATION COUNT**						

Bit 7 Modulation Clock Select (MCS)
0 = Select Frame Clock
1 = Select Line Clock

Bit 6:0 Modulation Count. The modulation is generated at a rate that is specified by the modulation count and modulation clock.

FPR5A: SYNC Pulse-widths Adjustment

Read/Write Address: 3C5h, Index: 5Ah
Power-on Default: 00h

This register allows adjust to the HSYNC and VSYNC Pulsewidths.

7	6	5	4	3	2	1	0
HSYNC					**VSYNC**		

Bit 7:3 Additional HSYNC pulse width in # of character clocks

Bit 2:0 Additional VSYNC pulse width in # of HSYNCs

FPRA0: Panel HW Video Control

Read/Write Address: 3C5h, Index: A0h
Power-on Default: 00h

This register defines the panel video display logic during Virtual Refresh mode. The video display logic will only be activated during Virtual Refresh mode with TFT panel.

7	6	5	4	3	2	1	0
EPV	**EHPD**	**ECK**	**RGB**	**EFS**	**EIC**	**RESERVED**	

Bit 7 Enable Panel Video (EPV)
0 = Disable
1 = Enable

Bit 6 Enable Horizontal Pixel Duplication (EHPD)
0 = Disable
1 = Enable

Bit 5 Enable Color Key (ECK)
0 = Disable
1 = Enable

Bit 4 RGB Format (RGB)
0 = YUV Format
1 = RGB Format

Bit 3 Enable Full screen video (EFS)
0 = Disable
1 = Enable

Bit 2 Enable 8-bit index color mode (only works in Virtual Refresh mode) (EIC)
0 = Disable
1 = Enable

Bit 1:0 Reserved

FPRA1: Panel Video Color Key

Read/Write Address: 3C5h, Index: A1h
Power-on Default: 00h

This register defines the panel video color key [7:0]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY [7:0]							

Bit 7:0 Panel Video Color Key[7:0]

FPRA2: Panel Video Color Key

Read/Write Address: 3C5h, Index: A2h
Power-on Default: 00h

This register defines the panel video color key [15:8]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY [15:8]							

Bit 7:0 Panel Video Color Key[15:8]

FPRA3: Panel Video Color Key Mask

Read/Write Address: 3C5h, Index: A3h
Power-on Default: 00h

This register defines the panel video color key mask [7:0]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY MASK [7:0]							

Bit 7:0 Panel Video Color Key Mask[7:0]

FPRA4: Panel Video Color Key Mask 15:8

Read/Write Address: 3C5h, Index: A4h
Power-on Default: 00h

This register defines the panel video color key mask [15:8]

7	6	5	4	3	2	1	0
PANEL VIDEO COLOR KEY MASK [15:8]							

Bit 7:0 Panel Video Color Key Mask[15:8]

FPRA5: Panel Video Red Constant

Read/Write Address: 3C5h, Index: A5h
Power-on Default: EDh

This register defines the panel video Red Constant

7	6	5	4	3	2	1	0
PANEL VIDEO RED CONSTANT [7:0]							

Bit 7:0 Panel Video Red Constant [7:0]

FPRA6: Panel Video Green Constant

Read/Write Address: 3C5h, Index: A6h
Power-on Default: EDh

This register defines the panel video green constant

7	6	5	4	3	2	1	0
PANEL VIDEO GREEN CONSTANT [7:0]							

Bit 7:0 Panel Video Green Constant [7:0]

FPRA7: Panel Video Blue Constant

Read/Write Address: 3C5h, Index: A7h
Power-on Default: EDh

This register defines the panel video Blue Constant

7	6	5	4	3	2	1	0
PANEL VIDEO BLUE CONSTANT [7:0]							

Bit 7:0 Panel Video Blue Constant [7:0]

FPRA8: Panel Video Top Boundary

Read/Write Address: 3C5h, Index: A8h
Power-on Default: 00h

This register defines the panel video top boundary

7	6	5	4	3	2	1	0
PANEL VIDEO TOP BOUNDARY [7:0]							

Bit 7:0 Panel Video Top Boundary [7:0]

FPRA9: Panel Video Left Boundary

Read/Write Address: 3C5h, Index: A9h

Power-on Default: 00h

This register defines the panel video left boundary

7	6	5	4	3	2	1	0
PANEL VIDEO LEFT BOUNDARY [7:0]							

Bit 7:0 Panel Video Left Boundary [7:0]

FPRAA: Panel Video Bottom Boundary

Read/Write Address: 3C5h, Index: AAh
Power-on Default: 00h

This register defines the panel video bottom boundary

7	6	5	4	3	2	1	0
PANEL VIDEO BOTTOM BOUNDARY [7:0]							

Bit 7:0 Panel Video Bottom Boundary [7:0]

FPRAB: Panel Video Right Boundary

Read/Write Address: 3C5h, Index: ABh
Power-on Default: 00h

This register defines the panel video Right boundary

7	6	5	4	3	2	1	0
PANEL VIDEO RIGHT BOUNDARY [7:0]							

Bit 7:0 Panel Video Right Boundary [7:0]

FPRAC: Panel Video Top and Left Boundary Overflow

Read/Write Address: 3C5h, Index: ACh
Power-on Default: 00h

This register defines the panel video top and left boundary overflow

7	6	5	4	3	2	1	0
PVLB			**RESERVED**			**PVTB**	

Bit 7:5 Panel Video Left Boundary [10:8] (PVLB)

Bit 4:3 Reserved

Bit 2:0 Panel Video Top Boundary [10:8] (PVTB)

FPRAD: Panel Video Bottom and Right Boundary Overflow

Read/Write Address: 3C5h, Index: ADh
Power-on Default: 00h

This register defines the panel video bottom and right boundary overflow

7	6	5	4	3	2	1	0
PVRB			**RESERVED**		**PVBB**		

Bit 7:5 Panel Video Right Boundary [10:8] (PVRB)

Bit 4:3 Reserved

Bit 2:0 Panel Video Bottom Boundary [10:8] (PVBB)

FPRAE: Panel Video Vertical Stretch Factor

Read/Write Address: 3C5h, Index: AEh
Power-on Default: 00h

This register defines the panel video vertical stretch factor.

7	6	5	4	3	2	1	0
PANEL VIDEO VERTICAL STRETCH FACTOR [7:0]							

Bit 7:0 Panel Video Vertical Stretch Factor [7:0]. The stretch factor equals to:
S/D * 256.
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch.

FPRAF: Panel Video Horizontal Stretch Factor

Read/Write Address: 3C5h, Index: AFh
Power-on Default: 00h

This register defines the panel video horizontal stretch factor

7	6	5	4	3	2	1	0
PANEL VIDEO HORIZONTAL STRETCH FACTOR [7:0]							

Bit 7:0 Panel Video Horizontal Stretch Factor [7:0] The stretch factor equals to:
S/D * 256. Note: when stretch factor is set to 0, it becomes a 1-to-1 stretch.

Memory Control Registers

MCR60: Memory Control

Read/Write Address: 3C5h, Index: 60h
Power-on Default: 00h

This register specifies memory control for Memory Address Wrap Around, DRAM refresh, VGA to memory burst write, and synchronization. This register also includes RAMDAC Write/Read Command Pulse Width select.

7	6	5	4	3	2	1	0
RESERVED		**RAM**	**DVGA**	**VGAF**	**R**	**DDRR**	**DRC**

Bit 7:6 **Reserved**

Bit 5 RAMDAC Write/Read Command Pulse Width Select (RAM)
0 = Command Pulse is 4 MCLK high and 12 MCLK low
1 = Command Pulse is 8 MCLK high and 24 MCLK low

Bit 4 Disable VGA to memory burst write (DVGA)
0 = Enable
1 = Disable

Bit 3 VGA FIFO Empty Level Request Select. VGA FIFO is 8 level deep. (VGAF)
0 = VGA FIFO request if VGA FIFO is two level empty
1 = VGA FIFO request if VGA FIFO is four level empty

Bit 2 Reserved (R)

Bit 1 Disable DRAM Refresh Request (DDRR)
0 = Enable
1 = Disable

Bit 0 DRAM Refresh Control (DRC)
0 = Normal DRAM refresh
1 = Force to 1 DRAM refresh per scan line

MCR61: Memory Bank Address High

Read/Write Address: 3C5h, Index: 61h
Power-on Default: 00h

This register specifies the high order memory bank address for non-linear addressing (or banking) mode (SCR18 bit 0 = 0).

7	6	5	4	3	2	1	0
MEMORY BANK ADDRESS HIGH							

Bit 7:0 Memory Bank Address High

Specifies the high-order address for memory access in non-linear addressing (or banking) mode. The host will take these bits append with address [15:0] to form a 22 bits address (4Mbyte).

MCR62: Memory Type and Timing Control

Read/Write Address: 3C5h, Index: 62h
Power-on Default: This is a power-on configurable register (by RESET)

LynxEM+ supports both internal and external memory. This register specifies the memory type and memory timing control. This register is power-on configurable by MD [7:0] of memory data bus.

7	6	5	4	3	2	1	0
IL	**EMD**	**MD[5:4]**		**MD3**	**ME**	**MD1**	**MD0**

Bit 7 Internal Logic (IL)
0 = Internal logic will be running 1/2X MCLK
1 = Internal logic will be running 1X MCLK

Bit 6 Enable Memory Data Bus (EMD)
0 = Enable 32-bit memory data bus
1 = Enable 64-bit memory data bus

Bit 5:4 External Memory Column Address Control Select. Power-on configurable by MD [5:4]. (MD[5:4])
10 = 8 column address
11 = 9 column address
0x = 10 column address

Bit 3 Reserved

Bit 2 External Memory Enable (ME)
0 = Enable external 32-bit memory
1 = Disable external 32-bit memory

Bit 1 External SDRAM/SGRAM Memory Active to Precharge delay Control. Power-on configurable by MD1. (MD1)
0 = 7 MCLK
1 = 6 MCLK

Bit 0 External SDRAM/SGRAM Memory refresh to command delay. Power-on configurable bit by MD0. (MD0)
0 = 10 MCLK
1 = 9 MCLK

CCR65: TV Encoder Control Register

Read/Write Address: 3C5h, Index: 65h
Power-on Default: 00h

This register specifies the various TV controls.

7	6	5	4	3	2	1	0
RESERVED				**SRAM**	**TVSC**	**TVSS**	**CHOS**

Bit 7:4 **Reserved**

Bit 3 Select which SRAM to read from index color modes. (SRAM)
0 = Read from CRT SRAM
1 = Read from LCD SRAM

Bit 2 TV Sub-carrier Select. (TVSC)
0 = Set ALT per field clock
1 = Set free running clock

Bit 1 TVCLK Source Select (TVSS)
0 = TVCLK source is from “CKIN” input pin. Normally “CLKIN” input is connected with 14.31818 MHZ clock for NTSC TV. TVCLK for NTSC is derived from 14.31818 MHz divided by 4.
1 = TVCLK source is from “REFCLK” input pin. If “REFCLK” input is connected with 17.734480 MHz clock for PAL TV. TVCLK for PAL is derived from 17.734480 MHz divided by 4.

Bit 0 CRT HSYNC output select (CHOS)
0 = CRTHYSNC output to CRTHSYNC pin
1 = CRT composite SYNC to CRTHSYNC pin

CCR66: RAM LUT On/Off Control

Read/Write Address: 3C5h, Index 66h
Power-on Default: 00h

RAM control and function ON/OFF register.

Bit 7:6 RAM operation control bits
00 = Both RAM on
10 = LCD RAM off
01 = CRT RAM off
11 = Both RAM off

Bit 5:4 RAM write control bits
00 = Write both RAM (CRT/LCD)
10 = Write CRT RAM only

01 = Write LCD RAM only
11 = Reserved

Bit 3:2 CRT RAM 8/6 bits and gamma control
00 = 6 bits RAM
10 = 8 bits RAM
x1 = Gamma correction on
01 = 8 bits RAM

CCR67: Reserved

This register is reserved for simulation purposes.

CCR68: Clock Control 1

Read/Write Address: 3C5h, Index: 68h
Power-on Default: C0h

This register is used to select clock frequencies and pulse-width control.

7	6	5	4	3	2	1	0
VCLKF		**ISO**	**CLK**	**SELECT VCLK**		**SELECT MCLK**	

Bit 7:6 Select VCLK frequency based on the following table (VCLKF)

Bit [7:6]	~EXCKEN	VCLK frequency
00	1	VCLK is selected from VGA 3C2h register
01	1	VCLK is selected from programmable VCLK registers: CCR6C and CCR6D
10	1	VCLK is selected from 17.734 MHz (Reserve)
11	1	VCLK is selected from 14.131818 MHz
xx	0	VCLK is selected from CKIN input

Bit 5 Enable ISO standard at VGA modes. This bit is designed to increase the CRT screen refresh rate to ISO standard at VGA modes. This bit is used only when CCR68 bit [7:6] = 00b. (ISO)
0 = Standard VGA frequency which controlled by 3C2h bit [3:2]
1 = ISO frequency which selected by 3C2h bit [3:2]

CCR68 Bit 5	3C2h Bit [3:2]	VCLK frequency
0	00	25.180 MHz
0	01	28.325 MHz
1	00	31.500 MHz
1	01	35.484 MHz

Bit 4 Select 8-dot character clock and disable dot clock divided by 2 function. This bit is used when LCD or TV is selected (determined by FPR31 [2:0]). When this bit set to "1", the bit 3 and bit 0 setting of VGA Clocking Mode Register will be ignored. (CLK)
0 = Character clock and dot clock are controlled by VGA clocking mode register
1 = Select 8-dot character clock and non-divided by 2 dot clock

Bit 3:2 Select VCLK high/low pulse width
00 = default value
01 = reduce 1 ns low time
10 = increase 1 ns low time
11 = increase 2 ns low time

Bit 1:0 Select MCLK high/low pulse width
00 = default value
01 = reduce 1 ns low time
10 = increase 1 ns low time
11 = increase 2 ns low time

CCR69: Clock Control 2

Read/Write Address: 3C5h, Index: 69h
Power-on Default: 80h

This register is used to select Virtual Refresh clock frequency, DRAM refresh clock frequency during sleep mode and standby mode, and HSYNC & VSYNC control during sleep mode.

7	6	5	4	3	2	1	0
TVCLK	**TDSS**	**LVDSCLK**		**DRAM**	**SHVSM**	**SELECT VRCLK**	

Bit 7 TVCLK or BLANK Select (TVCLK)
0 = Select BLANK output
1 = Select TVCLK to external analog NTSC/PAL TV encoder. TVCLK is equal to ¼ of VCLK, where VCLK is programmable by CCR6C and CCR6D registers.

Bit 6 Test Data Source Select. This bit is used for LSI testing only. (TDSS)
0 = Select index color data for test data
1 = Select direct color data for test data

Bit 5:4 Select LVDSCLK output clock source when ~EXCKIN = 1. LVDSCLK can be used to drive National's FPD Link transmitter for color DSTN panel LCD. For more detailed information on how to interface with the FPD Link transmitter, please refer to the Flat Panel Interface chapter of this data book. (LVDSCLK)
00 = Select VRCLK (VRCLK is defined by bit [1:0] of this register)
01 = Select inverted VRCLK
10 = Select ½ VRCLK
11 = Select inverted ½ VRCLK

Bit 3 Select refresh clock source to control DRAM refresh during sleep mode and standby mode. It is recommended to select external 32 KHz refresh clock to achieve highest power saving. (DRAM)

0 = Select external 32 KHz refresh clock
1 = Select internal PLL. During standby or sleep mode, the VCLK and MCLK frequency are selected by PDR20 [5:4]. MCLK is used to replace external 32 KHz refresh clock to control DRAM refresh.

Bit 2 Select HSYNC and VSYNC during Sleep Mode. (PDR20 bit 7 = 1) This bit is used to support VESA DPMS during Sleep Mode. LynxEM+ will automatically support VESA DPMS Standby Mode during its internal Standby Mode. (SHVSM)

Bit 2	DPMS STATE	HSYNC	VSYNC
0	Suspend	Pulses	No Pulses
1	Off	No Pulses	No Pulses

Bit 1:0 Select Virtual Refresh clock (VRCLK). The VRCLK is used to generate the timing sequence of LCD interface signals and control logic during Virtual Refresh mode.

Bit [1:0]	VRCLK Frequency
00	VCLK2
01	½ MCLK
10	MCLK
11	programmable Video Clock[1]

Notes:

1. In TV display mode, VCLK is set up as 14.31818 MHz clock from CKIN input (CCR68 [7:6] = 11b) to control TV timing. VRCLK could be chosen from programmable Video Clock which is selected by CCR6C and CCR6D registers by programming CCR69 [1:0] = 11b.

2. In non-Virtual Refresh mode (FPR31 bit 7 = 0), VRCLK is the same as VCLK.

CCR6A: MCLK Numerator Register

Read/Write Address: 3C5h, Index: 6Ah
Power-on Default: 5Ah

This register specifies the 8-bit numerator value of MCLK frequency (MNR). The MNR value is used to calculate the programmable MCLK frequency as follows:

$$\text{MCLK} = 14.31818\ \text{MHz} * \frac{\text{MNR}}{\text{MDR}}$$

7	6	5	4	3	2	1	0
CALCULATE MCLK FREQUENCY [8]							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected MCLK frequency. The power-on default of this register is 5Ah. Along with CCR6B, the default frequency is set to 40.27 MHz.

CCR6B: MCLK Denominator Register

Read/Write Address: 3C5h, Index: 6Bh
Power-on Default: 20h

This register specifies the 6-bit denominator value of MCLK frequency (MDR). The MDR value is used to calculate the programmable MCLK frequency as follows:

$$MCLK = 14.31818\ MHz * \frac{MNR}{MDR}$$

7	6	5	4	3	2	1	0
RESERVED		**CALCULATE MCLK FREQUENCY [6]**					

Bit 7:6 Reserved

Bit 5:0 Specify the 6-bit denominator value to calculate the selected MCLK frequency. The power-on default of this register is 20h. Along with CCR6A, the default frequency is set to 40.27 MHz.

CCR6C: VCLK Numerator Register

Read/Write Address: 3C5h, Index: 6Ch
Power-on Default: 5Bh

This register specifies the numerator value of VCLK frequency (VNR). The VNR value is used to calculate the programmable VCLK frequency as follows:

$$VCLK = 14.31818\ MHz * \frac{VNR}{VDR} * \frac{1}{(1+PS)}$$

7	6	5	4	3	2	1	0
CALCULATE VCLK FREQUENCY							

Bit 7:0 Specify the numerator value to calculate the selected VCLK frequency. The power-on default setting of this register is 5Bh. Along with CCR6D, the default frequency is set to 28.325 MHz.

CCR6D: VCLK Denominator Register

Read/Write Address: 3C5h, Index: 6Dh
Power-on Default: 2Eh

This register specifies the 6-bit denominator (VDR) value of and 1 bit post scalar (PS) value of VCLK frequency. The VDR value is used to calculate the programmable VCLK frequency. The post scalar is used to support VCLK frequencies which originally need high and even VDR value. With PS enabled, the revised VDR value should be set half of the original VDR value in order to reduce potential jitters.

CCR68_[7] or CCR68[6]	CCR6D_[6]	CCR6D_[7]	VCLK Frequency
x	0	0	VCLK
x	0	1	1/2 VCLK
1	1	0	1/4 VCLK
1	1	1	1/8 VCLK

$$VCLK = 14.31818\ MHz * \frac{VNR}{VDR} * \frac{1}{(1+PS)}$$

7	6	5	4	3	2	1	0
POST SCALAR		**VCLK FREQUENCY [6]**					

Bit 7:6 Enable Post Scalar.

0 0 Post Scalar not enable, vclk = programmed vclk
1 0 Post Scalar enable, vclk = 1/2 programmed vclk
0 1 Post Scalar enable, vclk = 1/4 programmed vclk
1 1 Post Scalar enable, vclk = 1/8 programmed vclk

Bit 5:0 Specify the 6-bit denominator value to calculate the selected VCLK frequency. The power-on default setting of this register is 2Eh. Along with CCR6C, the default frequency is set to 28.325 MHz.

CCR6E: VCLK2 Numerator Register

Read/Write Address: 3C5h, Index: 6Eh
Power-on Default: 5Ah

This register specifies the 8-bit numerator value of VCLK2 frequency (VCKL2NR). The VCLK2NR value is used to calculate the programmable VCLK2 frequency as follows:

$$VCLK2 = 14.31818\ MHz * \frac{VCLK2NR}{VCLK2DR}$$

7	6	5	4	3	2	1	0
VCLK2 FREQUENCY [8]							

Bit 7:0 Specify the 8-bit numerator value to calculate the selected VCLK2 frequency. Along with CCR6F, the default frequency is set to 40.27 MHz.

CCR6F: VCLK2 Denominator Register

Read/Write Address: 3C5h, Index: 6Fh
Power-on Default: 20h

This register specifies the 6-bit denominator value of VCLK2 frequency (VCLK2DR). The VCLK2DR value is used to calculate the programmable VCLK2 frequency as follows:

$$VCLK2 = 14.31818\ MHz * \frac{VCLK2NR}{VCLK2DR}$$

7	6	5	4	3	2	1	0
RESERVED		**CALCULATE VCLK2 FREQUENCY [6]**					

Bit 7:6 Reserved

Bit 5:0 Specify the 6-bit denominator value to calculate the selected VCLK2 frequency. Along with CCR6E, the default frequency is set to 40.27 MHz.

General Purpose Registers

GPR70: Scratch Pad Register 1

Read/Write Address: 3C5h, Index: 70h
Power-on Default: Undefined except for bit [3:0] which are power-on configurable (by RESET)

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD REG BITS				**SCRATCH PAD REG BITS MD [19:16]**			

Bit 7:4 Scratch pad register bits. This register can be used as general purpose bits.

Bit 3:0 Scratch pad register bits. These lower 4 bits are also connected to MD [19:16] of memory data bus. The external pull-down on MD lines will generate a logic "0", and internal pull-up will generate a logic "1" during power-on reset period. For power-on configuration, please refer to Initialization chapter of this data book.

GPR71: Scratch Pad Register 2

Read/Write Address: 3C5h, Index: 71h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 2 REGISTER							

Bit 7:0 Scratch Pad 2 register. This register can be used as general purpose scratch bits.

GPR72: User Defined Register 1 for DDC2/ I²C

Read/Write Address: 3C5h, Index: 72h
Power-on Default: 00h

This register is used for user defined registers: USR1/SDA and USR0/SCL. The SDA and SCL can be used for VESA DDC2 / I²C serial communication port.

7	6	5	4	3	2	1	0
RESERVED		**EUSR1**	**EUSR0**	**USR1S**	**USR0S**	**USR1W**	**USR0W**

Bit 7:6 Reserved

Bit 5 Enable USR1/SDA Port (EUSR1)
0 = Disable use of bit 1 of this register
1 = Enable use of bit 1 of this register

Bit 4 Enable USR0/SCL Port (EUSR0)
0 = Disable use of bit 0 of this register
1 = Enable use of bit 0 of this register

Bit 3 USR1/SDA Status (Read only). This bit can be used for DDC2/I²C Data. (USR1S)
0 = pin USR1/SDA is low
1 = pin USR1/SDA is tri-stated

Bit 2 USR0/SCL Status (Read only). This bit can be used for DDC2/I²C Clock. (USR0S)
0 = pin USR0/SCL is low
1 = pin USR0/SCL is tri-stated

Bit 1 USR1/SDA Write. Pin 131 can be used for DDC2/I²C Data. When pin USR1/SDA is tri-stated, other devices may drive this line. The actual state of the pin USR1/SDA is read via bit 3 of this register. (USR1W)
0 = pin USR1/SDA is driven low
1 = pin USR1/SDA is tri-stated

Bit 0 USR0/SCL Write. Pin 132 can be used for DDC2/I²C Clock. When pin USR0/SCL is tri-stated, other devices may drive this line. The actual state of the pin USR0/SCL is read via bit 2 of this register. (USR0W)0 = pin USR0/SCL is driven low
1 = pin USR0/SCL is tri-stated

GPR73: User Defined Register 2

Read/Write Address: 3C5h, Index: 73h
Power-on Default: 00h

This register can be used to control user programmable outputs: USR2 and USR3 pins.

7	6	5	4	3	2	1	0
RESERVED		**USR3P**	**USR2P**	**USER3**	**USER2**	**USR3W**	**USR2W**

Bit 7:6 Reserved

Bit 5 Enable USR3 Port (USR3P)
0 = Disable use of bit 1 of this register
1 = Enable use of bit 1 of this register

Bit 4 Enable USR2 Port (USR2P)
0 = Disable use of bit 0 of this register
1 = Enable use of bit 0 of this register

Bit 3 USER3 Status (Read only) (USER3)
0 = pin USR3 is low
1 = pin USR3 is tri-stated

Bit 2 USER2 Status (Read only) (USER2)
0 = pin USR2 is low
1 = pin USR2 is tri-stated

Bit 1 USR3 Write. When pin USR3 is tri-stated, other devices may drive this line. The actual state of the pin USR3 is read via bit 3 of this register. (USR3W)
0 = pin USR3 is driven low
1 = pin USR3 is tri-stated

Bit 0 USR2 Write. When pin USR2 is tri-stated, other devices may drive this line. The actual state of the pin USR2 is read via bit 2 of this register. (USR2W)
0 = pin USR2 is driven low
1 = pin USR2 is tri-stated

GPR74: Scratch Pad Register 3

Read/Write Address: 3C5h, Index: 74h
Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 3 REGISTER							

Bit 7:0 Scratch Pad 3 register. This register can be used as general purpose scratch bits.

GPR75: Scratch Pad register 4

Read/Write Address: 3C5h, Index: 75h

Power-on Default: Undefined

This register can be used as general purpose scratch bits.

7	6	5	4	3	2	1	0
SCRATCH PAD 4 REGISTER							

Bit 7:0 Scratch Pad 4 register. This register can be used as general purpose scratch bits.

Pop-up Icon and Hardware Cursor Registers

PHR80: Pop-up Icon and Hardware Cursor Pattern Location Low

Read/Write Address: 3C5h, Index: 80h
Power-on Default: Undefined

This register specifies the low 8 bits of the address for pop-up icon and Hardware Cursor Pattern Location, which is a 11-bit register. The high order 3 bits are specified in the PHR81 [2:0] register.

7	6	5	4	3	2	1	0
POP-UP ICON AND HARDWARE CURSOR PATTERN							

Bit 7:0 Pop-up Icon and Hardware Cursor Pattern Location Low. The PHR80 and PHR81 [2:0] registers allocate 2KB off-screen memory within the maximum 4MB of physical memory. The lower 1KB is used to store Pop-up Icon image. The upper 1KB is used to store Hardware Cursor image

PHR81: Hardware Cursor Enable & PI/HWC Pattern Location High

Read/Write Address: 3C5h, Index: 81h
Power-on Default: 0xh

This register specifies the hardware cursor enable and the high-order 3 bits of the address for pop-up icon and Hardware Cursor Pattern Location, which is a 11-bit register. The low order 8 bits are specified in the PHR80 register.

7	6	5	4	3	2	1	0
HCE	**RESERVED**				**POP-UP ICON**		

Bit 7 Hardware Cursor Enable (HCE)
0 = Disable (default)
1 = Enable

Bit 6:3 Reserved

Bit 2:0 Pop-up Icon and Hardware Cursor Pattern Location High. The PHR80 and PHR81 [2:0] registers allocate 2KB off-screen memory within the maximum 4MB of physical memory. The lower 1KB is used to store Pop-up Icon image. The upper 1KB is used to store Hardware Cursor image.

Pop-up Icon Registers

POP82: Pop-up Icon Control

Read/Write Address: 3C5h, Index: 82h
Power-on Default: 00h

This register specifies the control for pop-up icon.

7	6	5	4	3	2	1	0
PUIE	**PUIZE**	**RESERVED**					

Bit 7 Pop-up Icon Enable (PUIE)
0 = Disable
1 = Enable

Bit 6 Pop-up Icon Zoom Enable (PUIZE)
0 = Normal. (Pop-up Icon size is 64x64x2)
1 = zoom up the Pop-up Icon size by 2. (Pop-up Icon size is 128x128x2)

Bit 5:0 Reserved

POP83: Reserved

Read/Write Address: 3C5h, Index: 83h
Power-on Default: Undefined

This register is reserved.

7	6	5	4	3	2	1	0
RESERVED							

Bit 7:0 Reserved

POP84: Pop-up Icon Color 1

Read/Write Address: 3C5h, Index: 84h
Power-on Default: Undefined

This register specifies the color1 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR1							

Bit 7:0 Pop-up icon color1.

POP85: Pop-up Icon Color 2

Read/Write Address: 3C5h, Index: 85h
Power-on Default: Undefined

This register specifies the color2 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR2							

Bit 7:0 Pop-up icon color2.

POP86: Pop-up Icon Color 3

Read/Write Address: 3C5h, Index: 86h
Power-on Default: Undefined

This register specifies the color3 for pop-up icon.

7	6	5	4	3	2	1	0
POP-UP ICON COLOR3							

Bit 7:0 Pop-up icon color3.

POP90: Pop-up Icon Start X - Low

Read/Write Address: 3C5h, Index: 90h
Power-on Default: Undefined

This register specifies Pop-up icon location X start [7:0]

7	6	5	4	3	2	1	0
POP-UP ICON X START [7:0]							

Bit 7:0 Pop-up icon X start [7:0]

POP91: Pop-up Icon Start X - High

Read/Write Address: 3C5h, Index: 91h
Power-on Default: Undefined

This register specifies Pop-up icon location X start [11:8]

7	6	5	4	3	2	1	0
RESERVED					**POP-UP ICON X START**		

Bit 7:3 Reserved

Bit 2:0 Pop-up icon X start [10:8]

POP92: Pop-up Icon Start Y - Low

Read/Write Address: 3C5h, Index: 92h
Power-on Default: Undefined

This register specifies Pop-up icon location Y start [7:0]

7	6	5	4	3	2	1	0
POP-UP ICON Y START							

Bit 7:0 Pop-up icon Y start [7:0]

POP93: Pop-up Icon Start Y - High

Read/Write Address: 3C5h, Index: 93h
Power-on Default: Undefined

This register specifies Pop-up icon location Y start [11:8]

7	6	5	4	3	2	1	0
RESERVED					**POP-UP ICON Y START**		

Bit 7:3 Reserved

Bit 2:0 Pop-up icon Y start [10:8]

Hardware Cursor Registers

HCR88: Hardware Cursor Upper Left X Position - Low

Read/Write Address: 3C5h, Index: 88h
Power-on Default: 00h

This register specifies the lower 8-bit upper left X position for hardware cursor.

7	6	5	4	3	2	1	0
HARDWARE CURSOR X POSITION LOW ORDER							

Bit 7:0 Hardware Cursor X position low order 8 bits. The high order 3 bits are in HCR89[2:0].

HCR89: Hardware Cursor Upper Left X Position- High

Read/Write Address: 3C5h, Index: 89h
Power-on Default: 00h

This register specifies the upper left X position for hardware cursor.

7	6	5	4	3	2	1	0
RESERVED				**HCUL**	**HCXP**		

Bit 7:4 Reserved

Bit 3 Hardware Cursor Upper Left X Position Boundary Select (HCUL)
0 = hardware cursor is within the screen left side boundary. {HCR89[2:0], HCR88[7:0]} specify the X position of the hardware cursor from the left side boundary.
1 = hardware cursor is partially or totally outside of the left side screen boundary. HCR88 [4:0] specify how many pixels of the hardware cursor are outside the left side screen boundary.

Bit 2:0 Hardware Cursor X position high-order 3 bits. The low order 8 bits are specified in the HCR88 register. (HCXP)

HCR8A: Hardware Cursor Upper Left Y Position - Low

Read/Write Address: 3C5h, Index: 8Ah
Power-on Default: 00h

This register specifies the upper left Y position for hardware cursor.

7	6	5	4	3	2	1	0
HARDWARE CURSOR Y POSITION LOW ORDER							

Bit 7:0 Hardware Cursor Y position low order 8 bits. The high order 3 bits are in HCR8B [2:0].

HCR8B: Hardware Cursor Upper Left Y Position - High

Read/Write Address: 3C5h, Index: 8Bh
Power-on Default: 00h

This register specifies the upper left Y position for hardware cursor.

7	6	5	4	3	2	1	0
RESERVED				**HCUL**	**HCYP**		

Bit 7:4 Reserved

Bit 3 Hardware Cursor Upper Left Y Boundary Select (HCUL)

0 = hardware cursor is within the screen top side boundary. {HCR8B[2:0], HCR8A[7:0]} specify the Y position of the hardware cursor from the top side boundary.
1 = hardware cursor is partially or totally outside of the top side screen boundary. HCR8A [4:0] specify how many pixels of the hardware cursor are outside the top side screen boundary.

Bit 2:0 Hardware Cursor Y position high-order 3 bits. The low order 8 bits are specified in the HCR8A register. (HCYP)

HCR8C: Hardware Cursor Foreground Color

Read/Write Address: 3C5h, Index: 8Ch
Power-on Default: 00h

This register specifies the foreground color for hardware cursor. Hardware Cursor is always in 24-bit color. The 24-bit color is the expansion of 3:3:2 RGB into 8:8:8 RGB color.

7	6	5	4	3	2	1	0
HARDWARE CURSOR FOREGROUND COLOR							

Bit 7:0 Hardware Cursor foreground color
This register defines 3:3:2 8-bit RGB of the Hardware Cursor foreground color.

HCR8D: Hardware Cursor Background Color

Read/Write Address: 3C5h, Index: 8Dh
Power-on Default: 00h

This register specifies the background color for hardware cursor. Hardware Cursor is always in 24-bit color. The 24-bit color is the expansion of 3:3:2 RGB into 8:8:8 RGB color.

7	6	5	4	3	2	1	0
HARDWARE CURSOR BACKGROUND COLOR							

Bit 7:0 Hardware Cursor background color
This register defines 3:3:2 8-bit RGB of the Hardware Cursor background color.

Extended CRT Control Registers

CRT30: CRTC Overflow and Interlace Mode Enable

Read/Write Address: 3?5h, Index: 30h
Power-on Default: 00h

This register specifies the CRTC overflow registers and Interlace Mode Enable.

7	6	5	4	3	2	1	0
IME	**CRT DISPLAY**			**CVTR**	**CVDER**	**CVBS**	**CVRS**

Bit 7 Interlace Mode Enable (IME)
0 = Disable
1 = Enable

Bit 6:4 Bit [18:16] of the CRT display starting address. The lower order 16-bit are located in CRTC register index 0Ch and 0Dh.

Bit 3 Bit 10 of the CRT vertical total register. The lower bit [9:0] are defined in CRTC register index 07h and 06h. (CVTR)

Bit 2 Bit 10 of the CRT vertical display end register. The lower bit [9:0] are defined in CRTC register index 12h and 07h. (CVDER)

Bit 1 Bit 10 of the CRT vertical blank start. The lower bit [9:0] are defined in CRTC register index 15h, 09h, and 07h. (CVBS)

Bit 0 Bit 10 of the CRT vertical retrace start. The lower bit [9:0] are defined in CRTC register index 10h and 07h. (CVRS)

CRT31: Interlace Retrace

Read/Write Address: 3?5h, Index: 31h
Power-on Default: 00h

This register specifies when vertical retrace begins. This register is only valid if interlace mode is enabled (CRT30 Bit 7 = 1).

7	6	5	4	3	2	1	0
SPECIFIC # CHARACTER UNITS IN HORIZONTAL TIMING							

Bit 7:0 Specify the number of character units in horizontal timing when vertical retrace begins.

CRT32: TV Vertical Display Enable Start

Read/Write Address: 3?5h, Index: 32h
Power-on Default: 00h

This register specifies the vertical display enable start for TV timing.

7	6	5	4	3	2	1	0
TV VERTICAL DISPLAY ENABLE							

Bit 7:0 When CRT vertical count = CRT32 [7:0], TV vertical display enable become active.

CRT33: TV Vertical Display Enable End - High

Read/Write Address: 3?5h, Index: 33h
Power-on Default: 00h

This register specifies the vertical display enable end for TV timing. This register is a 11-bit register. The lower 8-bit of this register resides in CRT34.

7	6	5	4	3	2	1	0
ITE	**HBE**			**VBE**	**CRT VERTICAL COUNT**		

Bit 7 Interlace Timing Enable for double scan modes (i.e.: mode 13, etc.) (ITE)
0 = Disable
1 = Enable

Bit 6:5 Bit [7:6] of Horizontal Blank End. Bit 5 is located in bit 7 of CRTC register, 3?5h, index 5. Bit [4:0] is located in CRTC register, 3?5h, index 3. (HBE)

Bit 4:3 Bit [9:8] of Vertical Blank End. Bit [7:0] of Vertical Blank End is located in CRTC register, 3?5h, index 16. (VBE)

Bit 2:0 When CRT vertical count = {CRT33 [2:0],CRT34 [7:0]}, TV vertical display enable becomes inactive.

CRT34: TV Vertical Display Enable End - Low

Read/Write Address: 3?5h, Index: 34h
Power-on Default: 00h

This register specifies the vertical display enable end for TV timing.

7	6	5	4	3	2	1	0
CRT VERTICAL COUNT							

Bit 7:0 When CRT vertical count = {CRT33 [2:0],CRT34 [7:0]} TV vertical display enable becomes inactive.

CRT35: Vertical Screen Expansion DDA Control Constant - Low

Read/Write Address: 3?5h, Index: 35h
Power-on Default: 00h

This register specifies bit [7:0] the DDA control constant (DDACC) which is used for vertical screen expansion in VGA modes. Bit [9:8] of the DDACC is located in CRT36.

To enable vertical screen expansion in VGA graphics modes, one needs to program the DDA control constant (DDACC) equal to:

$$DDACC = \frac{1024 * \text{actual vertical size}}{\text{expanded vertical size}}$$

To enable vertical expansion in VGA text mode, one must program DDACC [2:0] = # of times the last character row should be repeated.

7	6	5	4	3	2	1	0
VERTICAL SCREEN EXPANSION							

Bit 7:0 This register defines the lower 8 bits of the vertical screen expansion DDA control constant. The upper 2 bits of the DDACC register is located in CRT36. For VGA text modes, only the lower [2:0] are valid.

CRT36: Vertical Screen Expansion DDA Control Constant - High

Read/Write Address: 3?5h, Index: 36h
Power-on Default: 00h

This register the vertical screen expansion DDA control constant lower 8 bits.

7	6	5	4	3	2	1	0
RESERVED						**VSE**	

Bit 7:2 Reserved

Bit 1:0 This register defines bit [9:8] of the vertical screen expansion DDA control constant. The lower 8-bit are located in CRT35. (VSE)

CRT38: TV Equalization Pulse Control For External TV Encoder

Read/Write Address: 3?5h, Index: 38h
Power-on Default: 00h

7	6	5	4	3	2	1	0
CSS	**R**	**EQUALIZATION PULSE WIDTH**					

Bit 7 Composite Sync Select (CSS)
0 = CSYNC is generated by SYNCs (HSYNC NOR VSYNC)
1 = CSYNC is generated by equalizer state machine

Bit 6 Reserved (R)

Bit 5:0 Equalization pulse width in units of four VCLK

CRT39: TV Serration Pulse Control For External TV Encoder

Read/Write Address: 3?5h, Index: 39h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**SERRATION PULSE WIDTH**					

Bit 7:6 Reserved

Bit 5:0 Serration pulse width in units of four VCLK

CRT3A: HSync and Character Clock Fine Turn Control Register

Read/Write Address: 3?4, Index: 3Ah
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**PIXEL CLOCK DELAY**			**CHARACTER DOT**		

Bit 7:6 Reserved

Bit 5:3 Pixel clock delay selection
00 = Normal
01 = Hsync delayed by one pixel clock
02 = Hsync delayed by two pixel clocks
03 = Hsync delayed by three pixel clocks
04 = Hsync delayed by four pixel clocks
05 = Hsync delayed by five pixel clocks

Bit 2:0 Character clock dot selection
07 = one character clock contains 7 dot clocks
06 = one character clock contains 6 dot clocks
05 = one character clock contains 5 dot clocks
04 = one character clock contains 4 dot clocks
03 = one character clock contains 3 dot clocks
02 = one character clock contains 2 dot clocks

Example: to program the 910 pixel horizontal total for 4FC NTSC TV mode: Program CRT horizontal total register to be 109 character clock. Program 3?4, Index 3A, bit [2:0] = 06. The actual total number of character per horizontal line is 109+5=114. The horizontal total in pixel clock is : 113x8+6=910.

CRT3B: Hardware Testing Register 2

Read/Write Address: 3?5h, Index: 3Bh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED							

Bit 7:0 Reserved for VGA hardware testing

CRT3C: Hardware Testing Register 3

Read/Write Address: 3?4h, Index: 3Ch
Power-on Default: 00h

7	6	5	4	3	2	1	0
VGA DEBUG		**BSS**	**LCB**	**VGA DEBUG AND TESTING**			

Bit 7:6 VGA debug test bus selection

Bit 5 Blanking signal selection (BSS)
0 = The blanking signal sent to RAMDAC is reversed active display. Outside of active display the blanking is active (black color). The border color register has no effect.
1 = The blank signal sent to RAMDAC is the normal blank signal from CRT. When both the blank and dispen are inactive the border color is displayed.

Bit 4 Line compare bit selection (LCB)
0 = No effect
1 = Line compare bit [9:8] (CRT09 - [6], CRT07 - [4]) has no effect to line compare logic

Bit 3:0 VGA debug and testing

CRT3D: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Dh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT3E: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Eh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT3F: Scratch Register Bits

Read/Write Address: 3?4h, Index: 3Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
SCRATCH REGISTER BITS							

Bit 7:0 Scratch Register Bits

CRT9E: Expansion/Centering Control Register 2

Read/Write Address: 3?4h, Index: 9Eh
Power-on Default: 00h

7	6	5	4	3	2	1	0
FE	**HSCRT**	**HSRW**	**VE**	**VC**	**VEE**	**VCE**	**HCE**

Bit 7 Font expansion control bit (FE)
This bit is effective if the following is true: CRT9E_[4] = 0 and the text mode plus the vertical expansion is on and CRT09_[4:0] < H0F
0 = The font vertical expansion will repeat the last character row
1 = The font vertical expansion will insert lines (with screen background color) between the last scan line of the current character row and the first scan of the next character row.

Bit 6 Horizontal shadow register selection for CRT timing control (HSCRT)
0 = There are two sets of horizontal shadow registers (primary and secondary). The selection switch is at the beginning of the vsync. If CR9F_[0] or CR9F [1] or FPR32_[0] is equal to 1 the second set is selected. If these registers are not equal to 1 then the primary set is selected.
1 = To force the selection of the second set of horizontal shadow register

Bit 5 Horizontal shadow register read/write selection (HSRW)

The following register update are effected
SVR40_[7:0] - Horizontal total shadow
SVR41_[7:0] - Horizontal blank start shadow
SVR42_[4:0] - Horizontal blank end shadow
SVR44_[7] - Horizontal blank end bit 5 shadow
CRT33_[6:5] - Horizontal blank end bit 7 & 6
SVR43_[7:0] - Horizontal sync start shadow
SVR44_[4:0] - Horizontal sync end
CRT9F_[0] - 10 dots expansion
CRT9F_[1] - 12 dots expansion

These registers have two sets - primary and secondary.

Bit 5=0: The primary registers are selected for W/R and control crt
Bit 5=1: The secondary registers are selected for W/R and control crt

Bit 4 Vertical expansion DDA value selection (VE)
0 = Vertical expansion will select the DDA value from the DDA look up table (3?4.35&36). This bit has no effect if bit 2 of this register = 0.
1 = Vertical expansion will select the DDA value from the DDA look up table (3?4.90-91B).

Bit 3 Vertical centering offset value selection (VC)
0 = Select vertical centering offset value from vertical center offset register (3?4, Index A6). This bit has no effect if bit 1 of this register = 0
1 = Select vertical centering offset value from a look-up table (look up by vdispend)

Bit 2 Vertical expansion enable selection (VEE)
0 = Vertical expansion disable
1 = Vertical expansion enable

Bit 1 Vertical centering enable selection (VCE)
0 = Vertical centering disable
1 = Vertical centering enable

Bit 0 Horizontal centering enable selection (HCE)
0 = Horizontal centering disable
1 = Horizontal centering enable

CRT9F: Expansion/Center Control Register 1

Read/Write Address: 3?4h, Index: 9Fh
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED						**CC12**	**CC10**

Bit 7:2 Reserved

Bit 1 12 dot expansion (CC12)
0 = 12 dots expansion disabled
1 = Character clock expand to 12 dots regardless of bit 0 of this register

Bit 0 10 dot expansion (CC10)
0 = 10 dots expansion
1 = Character clock expand to 10 dots

CRT90-9B Vertical DDA Look Up Table & CRTA0-A5: Vertical Centering Offset Look Up Table

Read/Write Address: 3?4, Index A0h-A5h
Power-on Default: 00h

3?4.90								3?4.91								3?4.A0					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	5	4	3	2	1	0
FIELD 3								**FIELD 2**								**FIELD 1**					

Field 3: This field compared with Vdisp_end (3?4.12 bit_[7:2])

Field 2: This field is selected DDA value if field 3 compares

Field 1: This field is selected vertical centering offset value if field 3 compares. The actual offset value = 3?4.A0_[5:0] x 4

The vertical expansion/centering using look up table is enabled only if the following conditions are true: CR9E_[3:1] = 111; if the compare fails to match with any entry, the value from 3?4.A6 will be used for vertical centering and the 3?4.35&36 will be used for DDA.

The following register groups behave the same:

3?4.92; 3?4.93; 3?4.A1
3?4.94; 3?4.95; 3?4.A2
3?4.96; 3?4.97; 3?4.A3
3?4.98; 3?4.99; 3?4.A4
3?4.9A; 3?4.9B; 3?4.A5

CRTA0-A5: Vertical Centering Offset Look Up Table

Read/Write Address: 3?4, Index A0h-A5h
Power-on Default: 00h

3?4.90								3?4.91								3?4.A0					
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	5	4	3	2	1	0
FIELD 3								**FIELD 2**								**FIELD 1**					

Field 3: This field compared with Vdisp_end (3?4.12 bit_[7:2])

Field 2: This field is selected DDA value if field 3 compares

Field 1: This field is selected vertical centering offset value if field 3 compares. The actual offset value = 3?4.A0_[5:0] x 4

The vertical expansion/centering using look up table is enabled only if the following conditions are true: CR9E_[3:1] = 111; if the compare fails to match with any entry, the value from 3?4.A6 will be used for vertical centering and the 3?4.35&36 will be used for DDA.

The following register groups behave the same:

3?4.92; 3?4.93; 3?4.A1

3?4.94; 3?4.95; 3?4.A2
3?4.96; 3?4.97; 3?4.A3
3?4.98; 3?4.99; 3?4.A4
3?4.9A; 3?4.9B; 3?4.A5

CRTA6: Vertical Centering Offset Register

Read/Write Address: 3?4, Index: A6h
Power-on Default: 00h

7	6	5	4	3	2	1	0
RESERVED		**LINE SHIFT DOWN**					

Bit 7:6 Reserved

Bit 5:0 Specifies how many lines the screen image will shift down. This register will have no effect if 3?4.9E bit_[1]=1

CRTA7: Horizontal Centering Offset Register

Read/Write Address: 3?4h, Index: A7h
Power-on Default: 00h

7	6	5	4	3	2	1	0
R	**CHARACTER UNIT SHIFT RIGHT**						

Bit 7 Reserved (R)

Bit 6:0 Specifies how many character units the screen image will shift to the right. This register has no effect if 3?4.9E BIT_[0] = 0

Shadow VGA Registers

The Shadow VGA Registers are designed to control CRT, LCD and TV timing, and maintain VGA compatibility. LynxEM+ shadows 12 VGA CRT registers. When these shadow registers are unlocked, the CPU I/O write operation can write into both standard CRT registers and shadow registers through standard VGA CRTC I/O location. When these shadow registers are locked, the CPU I/O write can only write into the standard CRT registers through CRTC I/O location. These 12 shadow registers also have specific I/O location which is not controlled by Shadow Lock/Unlock Register.

SVR40 - Horizontal Total	SVR45 - Vertical Total	SVR4A - Overflow (bit 7, 6,5, 3, 2, 1,and 0)
SVR41 - Start Horizontal Blanking	SVR46 - Start Vertical Blank	SVR4B - Maximum Scan Line (bit 5 only)
SVR42 - End Horizontal Blanking	SVR47 - End Vertical Blank	SVR4C - Horizontal Display End
SVR43 - Start Horizontal Retrace	SVR48 - Vertical Retrace Start	SVR4D - Vertical Display End
SVR44 - End Horizontal Retrace	SVR49 - Vertical Retrace End	

Automatic Lock/Unlock Scheme for Shadow Registers

There are two ways to access shadow registers. One is through standard VGA CRTC I/O location when CRT is the only selected display. These VGA CRT I/O write operations will write to both standard VGA CRT registers and shadow registers. The other way to access shadow registers is through their dedicated I/O locations. The shadow registers can only be read through their dedicated I/O locations.

When LCD or TV display is selected, the shadow registers will be automatically locked. The VGA CRT I/O write operation will write only to the standard VGA CRT registers. The shadow registers have to be accessed from their dedicated I/O location. This approach will reduce programming difficulty and maintain VGA compatibility.

SVR40: Shadow VGA Horizontal Total

Read/Write Address: 3?5h, Index: 40h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Total register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL TOTAL							

Bit 7:0 Defines the total character count minus 5 characters per horizontal scan line. This register only depends on the resolution of LCD, not the type of LCD.

SVR41: Shadow VGA Horizontal Blank Start

Read/Write Address: 3?5h, Index: 41h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Blank Start register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL BLANK							

Bit 7:0 When the horizontal character = SVR41 [7:0], shadow VGA horizontal blank become active.

SVR42: Shadow VGA Horizontal Blank End

Read/Write Address: 3?5h, Index: 42h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Blank End register.

7	6	5	4	3	2	1	0
R	**SDES**		**SHADOW VGA HORIZONTAL BLANK INACTIVE**				

Bit 7 Reserved (R)

Bit 6:5 Shadows display enable skew control (SDES)

Bit 4:0 When the horizontal character = {SVR44 [7],SVR42 [4:0]}, shadow VGA horizontal blank become inactive.

SVR43: Shadow VGA Horizontal Retrace Start

Read/Write Address: 3?5h, Index: 43h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Retrace Start register.

7	6	5	4	3	2	1	0
SHADOW VGA HORIZONTAL RETRACE INACTIVE							

Bit 7:0 When the horizontal character = SVR43 [7:0], shadow VGA horizontal retrace become active.

SVR44: Shadow VGA Horizontal Retrace End

Read/Write Address: 3?5h, Index: 44h
Power-on Default: 00h

This register shadows VGA CRT Horizontal Retrace End register.

7	6	5	4	3	2	1	0
SVHB	**SHRD**		**SHADOW VGA HORIZONTAL RETRACE INACTIVE**				

Bit 7 When the horizontal character = {SVR44 [7], SVR41 [4:0]}, shadow VGA horizontal blank become inactive. (SVHB)

Bit 6:5 Shadows horizontal retrace delay (SHRD)

Bit 4:0 When the horizontal character = SVR44 [4:0], shadow VGA horizontal retrace become inactive.

SVR45: Shadow VGA Vertical Total

Read/Write Address: 3?5h, Index: 45h
Power-on Default: 00h

This register shadows VGA CRT Vertical Total register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL TOTAL							

Bit 7:0 Shadows the least significant 8 bits of 11 bits count of raster scan lines for display frame.

SVR46: Shadow VGA Vertical Blank Start

Read/Write Address: 3?5h, Index: 46h
Power-on Default: 00h

This register shadows VGA CRT Vertical Blank Start register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL BLANK START							

Bit 7:0 Shadows the least significant 8-bit of the 11-bit VGA CRT vertical blank start register.

SVR47: Shadow VGA Vertical Blank End

Read/Write Address: 3?5h, Index: 47h
Power-on Default: 00h

This register shadows VGA CRT Vertical Blank End register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL BLANK END							

Bit 7:0 Shadows the least significant 8-bit VGA CRT vertical blank end register.

SVR48: Shadow VGA Vertical Retrace Start

Read/Write Address: 3?5h, Index: 48h
Power-on Default: 00h

This register shadows VGA CRT Vertical Retrace Start register.

7	6	5	4	3	2	1	0
SHADOW VGA VERTICAL RETRACE START							

Bit 7:0 Shadows the least significant 8-bit of the 11-bit vertical retrace start register.

SVR49: Shadow VGA Vertical Retrace End

Read/Write Address: 3?5h, Index: 49h
Power-on Default: 00h

This register shadows VGA CRT Vertical Retrace End register.

7	6	5	4	3	2	1	0
RESERVED				**SHADOW VGA/CRT VERTICAL RETRACE**			

Bit 7:4 Reserved

Bit 3:0 Shadows bit [3:0] of VGA CRT vertical retrace end register.

SVR4A: Shadow VGA Vertical Overflow

Read/Write Address: 3?5h, Index: 4Ah
Power-on Default: 00h

This register shadows VGA CRT Vertical Overflow register.

7	6	5	4	3	2	1	0
SVRS9	**SVDE9**	**SVTB9**	**R**	**SVBS**	**SVRS8**	**SVDE8**	**SVTB8**

Bit 7 Shadows vertical retrace start bit 9 (SVRS9)

Bit 6 Shadow vertical display enable bit 9 (3?5h, index 7 [6]). When FPR33[5] = 1, can only access this bit through 3?5h, index 4Ah. (SVDE9)

Bit 5 Shadows vertical total bit 9 (SVTB9)

Bit 4 Reserved (R)

Bit 3 Shadows vertical blank start bit 8 (SVBS)

Bit 2 Shadows vertical retrace start bit 8 (SVRS8)

Bit 1 Shadow vertical display enable bit 8 (3?5h, index 7 [1]). When FPR33[5] = 1, can only access this bit through 3?5h, index 4Ah. (SVDE8)

Bit 0 Shadows vertical total bit 8 (SVTB8)

SVR4B: Shadow VGA Maximum Scan Line

Read/Write Address: 3?5h, Index: 4Bh
Power-on Default: 00h

This register shadows VGA CRT Maximum Scan Line register.

7	6	5	4	3	2	1	0
SSP		**SVBS**	**RESERVED**				

Bit 7:6 Shadow 3C2 bit_[7:6] for sync polarity (SSP)

Bit 5 Shadows vertical blank start bit 9 (SVBS)

Bit 4:0 Reserved

SVR4C: Shadow VGA Horizontal Display End

Read/Write Address: 3?5h, Index: 4Ch
Power-on Default: 00h

This register shadows VGA CRT Horizontal Display end.

7	6	5	4	3	2	1	0
SHADOW HORIZONTAL DISPLAY END							

Bit 7:0 Shadows Horizontal Display End register (3?5h, index 01). When FPR33[5] = 1, it locks access to this register only through 3?5h, index 4Ch.

SVR4D: Shadow VGA Vertical Display End

Read/Write Address: 3?5h, Index: 4Dh
Power-on Default: 00h

This register shadows VGA CRT Vertical Display end.

7	6	5	4	3	2	1	0
SHADOW VERTICAL DISPLAY END							

Bit 7:0 Shadows Vertical Display End register [7:0] (3?5h, index 12) When FPR33[5] = 1, it locks access to this register only through 3?5h, index 4Dh.

Chapter 18: Memory Mapped Registers

Table 19: Memory Mapped Registers Quick Reference

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The drawing processor and video processor registers are all memory mapped. The following diagram illustrates the memory mapped register address assignment.

1. Drawing Processor Data Register
   The drawing processor data port for HOSTBLT is a memory-mapped and is located at DP_Port = PCI graphics base address + 4MB + 0KB.

2. Drawing Processor Control Registers
   Drawing Processor Control Registers are memory-mapped. The drawing processor control registers address start at DP_Base = PCI graphics base address + 4MB+32K.

3. Video Processor Control Registers
   Video Processor Control Registers are memory-mapped. The video processor control registers address start at VP_Base = PCI VGA graphics base address + 4MB + 48K.

4. Capture Processor Control Registers
   Capture Processor Control Registers are memory-mapped. The capture processor control registers address start at CP_Base = PCI VGA graphics base address + 4MB + 56K.

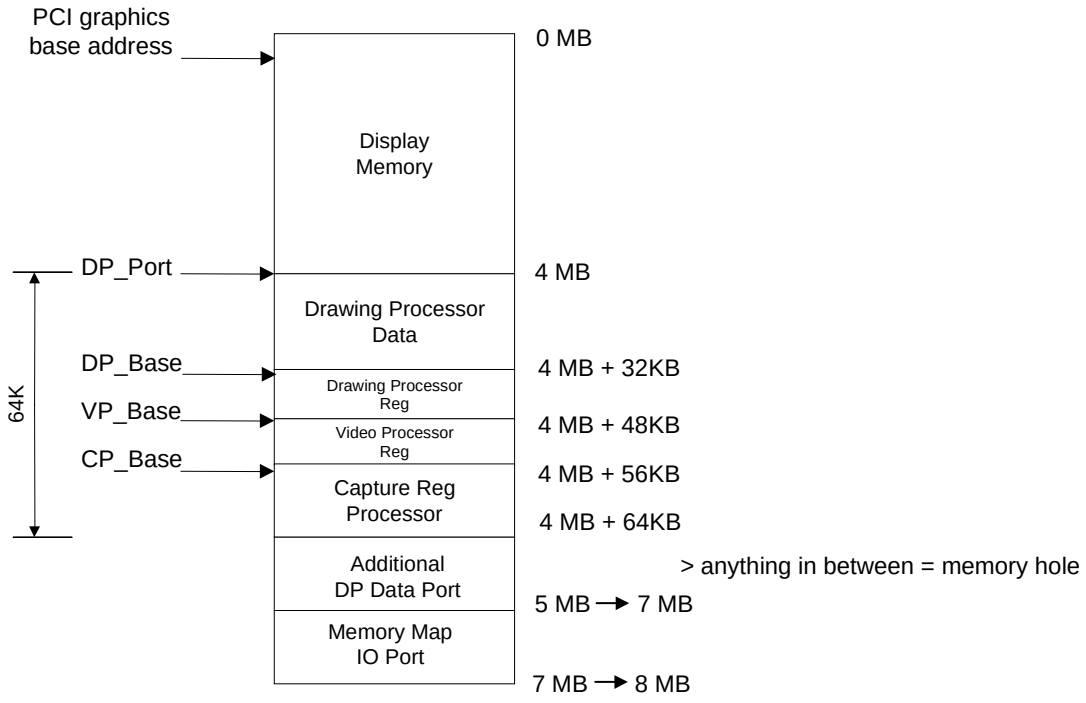


Figure 28: Memory Mapped Address Diagram

Drawing Engine Control Registers

The Drawing Engine supports various drawing functions, including Bresenham line draw (8-bit and 16-bit only), short stroke line draw, BITBLT, rectangle fill (8-bit and 16-bit only), HOSTBLT, Rotation Blit, and others. Hardware clipping is supported by 4 registers, DPR2C-DPR32, which defines a rectangular clipping area.

The drawing engine supports two types of format for its source and destination locations. One can specify location format in X-Y coordinate, where the upper left corner of the screen is defined to be (0,0); this method is referred as X-Y addressing. Also, one can specify the location format based on its position in the display memory sequentially from the first pixel of the visible data; this method is referred as DE linear addressing. To select DE linear addressing, one must set DPR1E bit [3:0] = 11xx.

All Drawing Engine control registers can be accessed via memory-mapped. The address is at DP_Base + XXXh; where DP_Base is at PCI graphics base address + 4MB + 32K.

DPR00: Source Y or K2

Read/Write Address: DP_Base+00h
Power-on Default: Undefined

This register specifies the 12-bit Source Y position in x-y addressing mode, or low-order source address in DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify the 14-bit for K2 constant of Bresenham line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE Y FOR X-Y ADDRESSING**											

Bit 15:12 Reserved

Bit 11:0 Source Y for X-Y addressing. In 24-bit packed modes, Source Y needs to be multiplied by 3.
OR
High-order source address SA[23:12] for DE linear addressing. Low-order 12-bit are in DPR02.

Bresenham Line (DPR0E bit [3:0] = 0111b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**AXIAL DIAGONAL CONSTANT (K2)**													

Bit 15:14 Reserved

Bit 13:0 Axial Diagonal Constant (K2) = 2 * (min(|dx|,|dy|) - max(|dx|,|dy|))

DPR02: Source X or K1

Read/Write Address: DP_Base+02h
Power-on Default: Undefined

This register specifies the 12-bit Source X position in x-y addressing mode, or low-order source address in linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify the 14-bit for K1 constant of

Bresenham line when DPR0E bit [3:0] = 0111b to select Bresenham line command function. For HOSTBLT write command function (when DPR0E bit [3:0] = 1000b), this register is also used to specify the 3-bit HOST mono source for alignment.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE X FOR X-Y ADDRESSING**											

Bit 15:12 Reserved

Bit 11:0 Source X for X-Y addressing mode. In 24-bit packed modes, Source X needs to be multiplied by 3.
OR
Low-order source address SA [11:0] for DE linear addressing mode. Higher order 12-bit are in DPR00.

Note: For 24-bit color pattern, Xs = (PatXs * 3) LOGIC_OR (Yd[2:0] *3, shift 3 bits to left)
For 32-bit color pattern, Xs = (PatXs) LOGIC_OR (Yd[2:0], shift 3 bits to left)

Bresenham Line (DPR0E bit [3:0] = 0111b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**AXIAL STEP CONSTANT K1**													

Bit 15:14 Reserved

Bit 13:0 Axial Step Constant (K1) = 2 * min (|dx|, |dy|)

HOSTBLT Write (DPR0E bit [3:0] = 1000b)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**HMSA**		

Bit 15:3 Reserved

Bit 2:0 Host mono source alignment for 8, 16, or 32-bit color modes. For 24-bit color mode, software needs to adjust for alignment. (HMSA)

DPR04: Destination Y or Start Y

Read/Write Address: DP_Base+04h
Power-on Default: Undefined

This register specifies the 12-bit Destination Y position in x-y addressing mode or higher-order destination address for DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify Vector Y start address for Bresenham Line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DESTINATION Y OR START Y**											

Bit 15:12 Reserved

	Bresenham Line (DPR0E bit [3:0] = 0111b
Bit 13:0 Destination Y for X-Y addressing. In 24-bit packed modes, Destination Y needs to be multiplied by 3. OR High-order 12 bits destination address DA[23:12] for DE linear addressing.	Vector Y start address

DPR06: Destination X or Start X

Read/Write Address: DP_Base+06h
Power-on Default: Undefined

This register specifies 12-bit Destination X position in x-y addressing mode or low-order 12-bit destination address in DE linear addressing mode (when DPR1E bit [3:0] = 11xxb). This register is also used to specify Vector X start address for Bresenham Line when DPR0E bit [3:0] = 0111b to select Bresenham line command function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DESTINATION X OR START X**											

Bit 15:12 Reserved

	Bresenham Line (DPR0E bit [3:0] = 0111b
Bit 11:0 Destination X for X-Y addressing. In 24-bit packed modes, Destination X needs to be multiplied by 3. OR Low-order 12 bits destination address DA[11:0] for DE linear addressing.	Vector X start address

DPR08: Dimension Y or Error Term

Read/Write Address: DP_Base+08h
Power-on Default: Undefined

This register specifies the rectangle height or Dimension Y in pixels. When Bresenham line command function is selected (DPR0E bit [3:0] = 0111b), this register specifies the Vector Error Term. When Short Stroke Line command function is selected (DPR0E bit [3:0] = 0110b), this register specifies the short stroke line length for non-horizontal short stroke line

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DIMENSION Y OR ERROR TERM**											

		Short Stroke (DPR0E bit [3:0] = 0110b)	**Bresenham Line (DPR0E bit [3:0] = 0111b)**
Bit 15:14	Reserved	Reserved	Reserved
Bit 13:12	Reserved	Reserved	Vector Error Term

		Short Stroke (DPR0E bit [3:0] = 0110b)	Bresenham Line (DPR0E bit [3:0] = 0111b)
Bit 11:0	Dimension Y	Short Stroke Length if not a horizontal line (≠ 0° or ≠ 180°)	(ET)*

* Vector Error Term is determined based on the following logic:
ET = 2 * min (|dx|,|dy|) - max (|dx|,|dy|) if starting X > ending X
ET = 2 * min (|dx|,|dy|) - max (|dx|,|dy|) -1 if starting X <= ending X

DPR0A: Dimension X or Vector Length

Read/Write Address: DP_Base+0Ah
Power-on Default: Undefined

This register specifies the rectangle width or Dimension X in pixels. When Bresenham line command function is selected (DPR0E bit [3:0] = 0111b), this register specifies the Vector Length. When Short Stroke Line command function is selected (DPR0E bit [3:0] = 0110b), this register specifies the short stroke line length for horizontal short stroke line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DIMENSION X OR VECTOR LENGTH**											

Bit 15:12 Reserved

	.	Bresenham Line (DPR0E bit [3:0] = 0111b)	Short Stroke (DPR0E bit [3:0] = 0110b)
Bit 11:0	Dimension X. In 24-bit packed mode, Dimension X needs to be multiplied by 3. (note: Dimension Y does not need to be multiplied by 3)	Vector Length = D_{max} + 1.Where D_{max} is the dimension of Vector length which is on the major axis. Major axis is determined to be the axis which has longer length.	Short Stroke Length for horizontal short stroke line. (= 0° or = 180°)

DPR0C: ROP and Miscellaneous Control

Read/Write Address: DP_Base+0Ch
Power-on Default: Undefined

This register specifies the ROP2/ROP3 select, ROP2 source select, mono data format, pixel control, and 3 ROP operands.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROP	**ROPS**	**MDS**		**ERR**	**MPC**	**PCTS**	**TE**	**ROP3 RESERVED**				**ROP CODE**			

Bit 15 ROP2 or ROP3 select (ROP)
0 = select ROP3
1 = select ROP2

Bit 14 ROP2 source select. This bit is only valid when bit 15 of this register is set to "1". (ROPS)
0 = ROP2 source is not pattern

1 = ROP2 source is pattern

Bit 13:12 Mono Data Select. Mono data format is used to optimize font performance. Driver selects particular mono data format for particular font sizes. (MDS)
00 = No packed mono data
01 = Mono data packed at 8-bit
10 = Mono data packed at 16-bit
11 = Mono data packed at 32-bit

Bit 11 Enable Repeat Rotation BLT. This bit is only valid when DPR0E[3:0] = 1011b. (ERR)
0 = disable
1 = enable

Bit 10 Matching Pixel Control. This bit is only valid when transparency is enabled (bit 8 of this register = 1) (MPC)
0 = Matching pixel is opaque
1 = Matching pixel is transparent

Bit 9 Pixel Control Transparency Select (PCTS)
0 = Source controls transparency
1 = Destination controls transparency

Bit 8 Transparency Enable (TE)
0 = disable
1 = enable

Bit 7:4 ROP3 code[1] Reserved

Bit 3:0 ROP3 code[1] ROP2 code[2]

Notes:
[1] 3 Operands 256 operations ROP codes table reference listed below. For details on ROP codes, please refer to the Microsoft's device driver adaptation guide.

ROP3 Code	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pattern	1	1	1	1	0	0	0	0
Source	1	1	0	0	1	1	0	0
Destination	1	0	1	0	1	0	1	0

[2] 2 Operands 16 operations ROP codes table listed below:

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
Zero	0	0	0	0
~(D+ S)	0	0	0	1
D * ~S	0	0	1	0

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
D * S	1	0	0	0
~(D ⊕ S)	1	0	0	1
D	1	0	1	0

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
~ S	0	0	1	1
S * ~D	0	1	0	0
~D	0	1	0	1
D ⊕ S	0	1	1	0
~(D * S)	0	1	1	1

ROP2 Code	Bit 3	Bit 2	Bit 1	Bit 0
D + ~S	1	0	1	1
S	1	1	0	0
S + ~D	1	1	0	1
D + S	1	1	1	0
One	1	1	1	1

DPR0E: Drawing Engine Commands and Control

Read/Write Address: DP_Base+0Eh
Power-on Default: Undefined (except for Bit 15 and Bit 12 = 0)

This register specifies the drawing engine command and control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEA	**PS**	**DUE**	**DEQS**	**SSL**	**BMA**	**XYS**		**GSE**	**HBSC**	**PSB**	**DECE**	**COMMAND FUNCTIONS**			

Bit 15 Drawing Engine Activate (DEA)
0 = Idle (Power-on default = 0)
1 = Start Activate Drawing Engine

Bit 14 Pattern Select (PS)
0 = mono pattern
1 = color pattern

Bit 13 Destination X Update Enable (DUE)

0 = Do not update destination X on completion of a drawing engine function
1 = Update destination X on completion of a drawing engine function

Bit 12 Drawing Engine Quick Start Enable. If this bit is set, drawing engine will be activated right after dimension X is provided. One does not need to activate the drawing engine by setting bit 15 = 1 if quick start is already enabled. (DEQS)
0 = disable (Power-on default = 0)
1 = enable

Bit 11 Direction for Short Stroke Line and BITBLT For diagonal and vertical line, this bit needs to be set to "0". (SSL)

Bit 11	Short Stroke Line Direction	BITBLT Direction
0	not horizontal	Left to Right
1	horizontal	Right to Left

Bit 10 Bresenham Major Axis (Y) (BMA)
0= major axis is X

1= major axis is Y. For vertical line, this bit needs to be set.

Bit 9:8 X-Step and Y-Step (XYS)
01 = Counter Clock Wise Rotate 90 degree (CCW90)
10 = Clock Wise Rotate 90 degree (CW90)
00 = Right_Top and Left_Bottom as axis flip
11 = Left_Top and Right_Bottom as axis flip

Bit 7 Graphics Stretch Enable (only for Y direction) (GSE)
0 = disable
1 = enable

Bit 6 HOST BITBLT Source Color Select (HBSC)
0 = Source is color
1 = Source is monochrome

Bit 5 Last Pixel Select for Bresenham line (PSB)
0 = Vector not draw last pixel
1 = Vector draw last pixel

Bit 4 Drawing Engine Capture Enable (DECE)
0 = Normal Operation. No HOSTBLT capture operation.
1 = Enable HOSTBLT Read capture operation

Bit 3:0 Command Functions
0000 = BITBLT
0001 = Rectangle Fill
0010 = Reserved
0011 = Trapezoid Pattern Fill
0100 = Reserved
0101 = Run Length Encoding (RLE) Strip Draw
0110 = Short Stroke
0111 = Bresenham Line Draw
1000 = Host BLT Write
1001 = Host BLT Read
1010 = Host BLT Write from Left_Bottom
1011 = Rotation BLT
others = Reserved

DPR10: Source Row Pitch

Read/Write Address: DP_Base+10h
Power-on Default: Undefined

This register specifies the source row offset in pixel unit for 8/16/32-bit color modes. In 24-bit color mode, source row offset needs to be multiplied by 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE ROW OFFSET**											

Bit 15:12 Reserved

Bit 11:0 Source Row Offset. In 24-bit color mode, source row offset needs to be multiplied by 3.

DPR12: Destination Row Pitch

Read/Write Address: DP_Base+12h
Power-on Default: Undefined

This register specifies the destination row offset in pixel unit for 8/16/32-bit color modes. In 24-bit color mode, destination row offset needs to be multiplied by 3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**DESTINATION ROW OFFSET**											

Bit 15:12 Reserved

Bit 11:0 Destination Row Offset. In 24-bit color mode, destination row offset needs to be multiplied by 3.

DPR14: Foreground Colors

Read/Write Address: DP_Base+14h
Power-on Default: Undefined

The register specifies the foreground graphics color for 8-bit color (DPR1E bit [5:4] = 00b), 16-bit color (DPR1E bit [5:4] = 01b), and 24-bit color (DPR1E bit [5:4] = 11b) modes.

8-bit color mode

31	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**FOREGROUND COLOR**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR HIGH BYTE								**FOREGROUND COLOR LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**FOREGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR GREEN								**FOREGROUND COLOR BLUE**							

Bit 31:24 Reserved

	8-bit color mode	16-bit color mode	24-bit color mode
Bit 23:16	Reserved	Reserved	Foreground Color Red
Bit 15:8	Reserved	Foreground Color High Byte	Foreground Color Green
Bit 7:0	Foreground Color 8-bit index	Foreground Color Low Byte	Foreground Color Blue

DPR18: Background Colors

Read/Write Address: DP_Base+18h
Power-on Default: Undefined

The register specifies the background graphics color for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.

Note: in monochrome transparency mode (font operation), the background color needs to be programmed to equal to the invert of foreground color in DPR14.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BACKGROUND COLOR**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR HIGH BYTE								**BACKGROUND COLOR GREEN**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**BACKGROUND COLOR RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR GREEN								**BACKGROUND COLOR BLUE**							

Bit 31:24 Reserved

	8-bit color mode	16-bit color mode	24-bit color mode
Bit 23:16	Reserved	Reserved	Background Color Red

Bit 15:8	Reserved	Background Color High Byte	Background Color Green
Bit 7:0	Background Color 8-bit index	Background Color Low Byte	Background Color Blue

DPR1C: Stretch Source Height Y

Read/Write Address: DP_Base+1Ch
Power-on Default: Undefined

This register specifies the height of source block for stretch BITBLT.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE Y DIMENSION FOR STRETCH BLT**											

Bit 15:12 Reserved

Bit 11:0 Source Y dimension for stretch BLT. (only for Y direction)

DPR1E: Drawing Engine Data Format and Location Format Select

Read/Write Address: DP_Base+1Eh
Power-on Default: Undefined

The register specifies drawing engine source & destination locations select and data format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**XY**	**PATTERN START Y**			**PATTERN START X**			**RESERVED**		**DEDF**		**DRAWING ENG LOCATION**			

Bit 15 Reserved (R)

Bit 14 Pattern XY Overwrite Select (XY)
0 = Normal. Drawing Engine uses Bit [13:8] as pattern address only when it is in linear addressing mode (Bit [3:0] = 1111b]
1 = Overwrite. Drawing Engine uses Bit [13:8] as pattern address no matter what addressing mode it is in.

Bit 13:11 Pattern Start Y Address (Yd [2:0]). This address is only valid if Bit 14 = 1 or Bit [3:0] = 11xxb (linear addressing).

Bit 10:8 Pattern Start X Address (Xd [2:0]). This address is only valid if Bit 14 = 1 or Bit [3:0] = 11xxb (linear addressing). It is based on the top left corner of screen as (0,0) coordinate address. Rotation is needed for pattern source if Xd is non-zero.

Bit 7:6 Reserved

Bit 5:4 Drawing Engine Data Format (DEDF)
00 = 8-bit per pixel

01 = 16-bit per pixel
10 = 32-bit per pixel
11 = 24-bit per pixel (24-bit packed)

Bit 3:0 Drawing Engine Locations (Source and Destination) Format Select. The drawing engine supports two types of format for its source and destination locations. One can specifies location format in X-Y coordinate, where the upper left corner of the screen is defined to be (0,0); this method is referred as X-Y addressing. Also, one can specifies the location format based on its position in the display memory sequentially from the first pixel of the visible data; this method is referred as DE linear addressing. This register selects the pixel width for X-Y addressing and DE linear addressing.
1111 = DE linear addressing
else = XY screen width depends on DPR3C register

DPR20: Color Compare

Read/Write Address: DP_Base+20h
Power-on Default: Undefined

The register specifies the color compare for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.
Note, in monochrome transparency mode for font operations, the color compare needs to be programmed to equal to the foreground color in DPR14.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**COLOR COMPARE 8-BIT INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE HIGH BYTE								**COLOR COMPARE LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**COLOR COMPARE RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE GREEN								**COLOR COMPARE BLUE**							

	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 31:24	Reserved	Reserved	Reserved
Bit 23:16	Reserved	Reserved	Color Compare Red
Bit 15:8	Reserved	Color Compare High Byte	Color Compare Green

Bit 7:0	Color Compare 8-bit index	Color Compare Low Byte	Color Compare Blue

DPR24: Color Compare Masks

Read/Write Address: DP_Base+24h
Power-on Default: Undefined

The register specifies the color compare mask for 8-bit color (DPR1E bit [5:4] = 00), 16-bit color (DPR1E bit [5:4] = 01), and 24-bit color (DPR1E bit [5:4] = 11) modes.

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**COLOR COMPARE 8-BIT INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE MASK HIGH BYTE								**COLOR COMPARE MASK LOW BYTE**							

24-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**COLOR COMPARE MASK RED**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLOR COMPARE MASK GREEN								**COLOR COMPARE MASK BLUE**							

	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 31:24	Reserved	Reserved	Reserved
Bit 23:16	Reserved	Reserved	Color Compare Mask Red
	8-bit color mode	**16-bit color mode**	**24-bit color mode**
Bit 15:8	Reserved	Color Compare Mask High Byte	Color Compare Mask Green
Bit 7:0	Color Compare Mask 8-bit index	Color Compare Mask Low Byte	Color Compare Mask Blue

DPR28: Bit Mask

Read/Write Address: DP_Base+28h
Power-on Default: Undefined

The register specifies the Bit Mask for 8-bit color (DPR1E bit [5:4] = 00) and 16-bit color (DPR1E bit [5:4] = 01) modes.

8-bit color mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BIT MASK 8-BIT INDEX**							

16-bit color mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT MASK HIGH BYTE								**BIT MASK LOW BYTE**							

	8-bit color mode	**16-bit color mode**
Bit 15:8	Reserved	Bit Mask High Byte
Bit 7:0	Bit Mask 8-bit index	Bit Mask Low Byte

DPR2A: Byte Mask Enable

Read/Write Address: DP_Base+2Ah
Power-on Default: Undefined

The register specifies the byte mask enable register for 64-bit datapath.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**BYTE MASK FOR 64-BIT DATAPATH**							

Bit 15:8 Reserved

Bit 7:0 Byte Mask for 64-bit datapath. Each bit enables the corresponding byte data.
0 = disable write
1 = enable write

DPR2C: Scissors Left and Control

Read/Write Address: DP_Base+2Ch
Power-on Default: Undefined

The register specifies the Scissors left boundary and control registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		**SE**	**SBS**	**SCISSORS BOUNDARY LEFT**											

Bit 15:14 Reserved

Bit 13 Scissors Enable (SE)

0 = disable
1 = enable

Bit 12 Scissors Boundary Select (SBS)
0 = Write disable outside the Scissors boundary
1 = Write disable inside the Scissors boundary

Bit 11:0 Scissors Boundary Left. In 24-bit color mode, the scissors boundary left position needs to be multiplied by 3.

DPR2E: Scissors Top

Read/Write Address: DP_Base+2Eh
Power-on Default: Undefined

The register specifies the scissors top boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SCISSORS BOUNDARY TOP**											

Bit 15:12 Reserved

Bit 11:0 Scissors Boundary Top. In 24-bit color mode, the scissors boundary top position needs to be multiplied by 3.

DPR30: Scissors Right

Read/Write Address: DP_Base+30h
Power-on Default: Undefined

The register specifies the right boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SCISSORS BOUNDARY RIGHT**											

Bit 15:12 Reserved

Bit 11:0 Scissors Boundary Right. In 24-bit color mode, the scissors boundary right position needs to be multiplied by 3.

DPR32: Scissors Bottom

Read/Write Address: DP_Base+32h
Power-on Default: Undefined

The register specifies the bottom boundary.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SCISSORS BOUNDARY BOTTOM**											

Bit 15:12 Reserved

Bit 11:0 Scissors Boundary Bottom. In 24-bit color mode, the scissors boundary bottom position = scissors boundary top position DPR2E [11:0] + height of the clipping window.

DPR34: Mono Pattern Low

Read/Write Address: DP_Base+34h
Power-on Default: Undefined

The register specifies the monochrome pattern lower double word. It is 32-bit access only. The higher 32-bit are in DPR38.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MONO PATTERN TOP 4 LINES															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONO PATTERN TOP 4 LINES															

Bit 31:0 Mono pattern top 4 lines. Line 3 data is located in the most significant byte where as line 0 data is located in the least significant bye.

DPR38: Mono Pattern High

Read/Write Address: DP_Base+38h
Power-on Default: Undefined

The register specifies the monochrome pattern higher double word. It is 32-bit access only. The lower 32-bit are in DPR34.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MONO PATTERN LAST 4 LINES															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MONO PATTERN LAST 4 LINES															

Bit 31:0 Mono pattern last 4 lines. Line 7 data is located in the most significant byte where as line 4 data is located in the least significant byte.

DPR3C: XY Addressing Destination & Source Window Widths

Read/Write Address: DP_Base+3Ch
Power-on Default: Undefined

The register specifies the XY width for source and destination window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**DESTINATION WINDOW WIDTH IN PIXEL**											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				**SOURCE WINDOW WIDTH IN PIXEL**											

Bit 31:28 Reserved

Bit 27:16 Destination Window width in pixel for XY addressing mode (max. = 4096 pixel)

Bit 15:12 Reserved

Bit 11:0 Source Window width in pixel for XY addressing mode (max. = 4096 pixel)

DPR40: Source Base Address

Read/Write Address: DP_Base+40h
Power-on Default: Undefined

The register specifies the Source base address in 64-bit unit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SOURCE BASE ADDRESS**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOURCE BASE ADDRESS															

Bit 31:20 Reserved

Bit 19:0 Source Base address

DPR44: Destination Base Address

Read/Write Address: DP_Base+44h
Power-on Default: Undefined

The register specifies the destination base address in 64-bit unit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**DESTINATION BASE ADDRESS**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESTINATION BASE ADDRESS															

Bit 31:20 Reserved

Bit 19:0 Destination Base address

Video Processor Control Registers

LynxEM+ integrates a concurrent video processor. It can support 2 independent video windows using hardware scaling for any size of video windows at any location of the screen display. The Video Processor Control Registers specify the control registers for Video Processor. The Video Processor Control Registers can only be accessed through memory-mapped. The video processor control registers address start at VP_Base = PCI VGA graphics base address + 4MB + 48K.

VPR00: Miscellaneous Graphics and Video Control

Read/Write Address: VP_Base+00h
Power-on Default: 00h

This register specifies the controls for graphics and video window I/II. (where x = don't care)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				**CKEII**	**ESD**	**FR**	**VVWI**	**FVIE**	**FRIM**	**VIE**	**CKEI**	**TVWS**	**GDF**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**EVWII**	**EVWHII HR**	**VWIIAE**	**VWIIE**	**VWFII**			**R**	**EVWI**	**EVWIH**	**VWIAE**	**VWIE**	**VWIF**		

Bit 31:28 Reserved

Bit 27 Color Key Enable for Video Window II (CKEII)
0 = Disable
1 = Enable

Bit 26 Enable separate data (graphics or video) to DAC/TV. This bit is used to implement "Dual View" in index color mode. This bit needs to also be set when enabling flicker reduction for TV display in VGA index-color mode. (ESD)
0 = Disable
1 = Enable

Bit 25 Enable V0FIFO to fetch 8-bit index color data to LCD BKEND in non-VGA mode. Normally, the 8-bit index color data is fetched by graphics FIFO in non-VGA mode. This bit is designed to enable flicker reduction on TV display in non-VGA, 8-bit index color mode. (FR)
0 = Disable
1 = Enable

Bit 24 Select video window I source start address same as video capture buffer start address. This bit is used to automatically display captured data on video window I without programming video window I source start address register (SVWI).
0 = Normal. Video window I source start address is from VPR1C register.
1 = Video window I source start address is equal to capture port buffer I source start address (VPR48) or capture port buffer II source start address (VPR4C). If single buffer is selected for video capture, video window I source start address is equal to capture port buffer I source address. If double buffer is selected for video capture and capture port buffer I is busy, video window I source start address is equal to capture port buffer II source address.

Bit 23 Fixed Vertical Interpolation Enable. Scale factor is fixed to 80. (FVIE)
0 = Disable
1 = Enable

Bit 22 Flicker Reduction in Interlace Modes for TV display. V1FIFO will be used together with the graphics FIFO for flicker reduction. Therefore, only one video Window is allowed for this feature to be enabled. (FRIM)
0 = Disable
1 = Enable

Bit 21 Vertical Interpolation Enable. This bit can only be set when single window is enabled. (VIE)
0 = Disable (line duplication)
1 = Enable

Bit 20 Color Key Enable for Video Window I (CKEI)
0 = Disable
1 = Enable

Bit 19 Top Video Window Select (TVWS)
0 = video window I is on top
1 = video window II is on top

Bit 18:16 Graphics Data Format (GDF)
000 = 8-bit index
001 = 15 -bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
11x = Reserved

Bit 15 Reserved (R)

Bit 14 Enable Video Window II data doubling. This bit is in 8-bit index color mode when the VCLK is larger than 85 MHz. The V1FIFO will shift out data every 2 VCLK. (EVWII)
0 = Disable
1 = Enable

Bit 13 Enable Video Window II Horizontal Replication (EVWII HR)
0 = Disable (horizontal interpolation)
1 = Enable (pixel duplication)

Bit 12 Video Window II YUV Averaging Enable. 2 YUV pixels will be averaged and the result will become single pixel. (VWII AE)
0 = Disable
1 = Enable

Bit 11 Video Window II Enable (VWIIE)
0 = Disable
1 = Enable

Bit 10:8 Video Window II Format (VWFII)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
11x = YUV 4:2:2

Bit 7 Reserved (R)

Bit 6 Enable Video Window I data doubling. This bit is used in 8-bit index color mode when the VCLK is larger than 85 MHz. The V0FIFO will shift out data every 2 VCLK. (EVWI)
0 = Disable
1 = Enable

Bit 5 Enable Video Window I Horizontal Replication (EVWIH)
0 = Disable (horizontal interpolation)
1 = Enable (pixel duplication)

Bit 4 Video Window I YUV Averaging Enable. 2 YUV pixels will be averaged and the result will become single pixel. (VWIAE)
0 = Disable
1 = Enable

Bit 3 Video Window I Enable (VWIE)
0 = Disable
1 = Enable

Bit 2:0 Video Window I Format (VWIF)
000 = 8-bit index
001 = 15-bit 5-5-5 RGB
010 = 16-bit 5-6-5 RGB
011 = 32-bit x-8-8-8 RGB
100 = 24-bit 8-8-8 RGB (packed)
101 = 8-bit 3-3-2 RGB
11x = YUV 4:2:2

VPR04: Color Keys

Read/Write Address: VP_Base+04h
Power-on Default: Undefined

This register specifies color keys for the two video windows

8-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**VIDEO WINDOW II COLOR KEY INDEX**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								**VIDEO WINDOW I COLOR KEY INDEX**							

16-bit color mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY [15:8]								**VIDEO WINDOW II COLOR KEY [7:0]**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY [15:8]								**VIDEO WINDOW I COLOR KEY [7:0]**							

	8-bit color mode	**16-bit color mode**[1]
Bit 31:24	Reserved	Video Window II Color Key [15:8]
Bit 23:16	Video Window II Color Key Index	Video Window II Color Key [7:0]
Bit 15:8	Reserved	Video Window I Color Key [15:8]
Bit 7:0	Video Window I Color Key Index	Video Window I Color Key [7:0]

Note[1]: for 24-bit or 32-bit color mode, software will need to repack the color key data into RGB - 5:6:5 (16-bit) format.

VPR08: Color Key Masks

Read/Write Address: VP_Base+08h
Power-on Default: Undefined

This register specifies color key masks for the two video window.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II COLOR KEY MASK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I COLOR KEY MASK															

Bit 31:16 Video Window II Color Key Mask
0 = Disable color mask
1 = Enable color mask

Bit 15:0 Video Window I Color Key Mask
0 = Disable color mask
1 = Enable color mask

VPR0C: Data Source Start Address for Extended Graphics Modes

Read/Write Address: VP_Base+0Ch
Power-on Default: Undefined

This register specifies data source start address for extended graphics modes

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SB**	**GDSSA**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GDSSA															

Bit 31:20 Reserved

Bit 19 Status bit. This bit is used for software to read back the status of the current frame. Software needs to program this bit to 1 when programming the graphics data source start address. The hardware will reset this status bit to 0 when the current frame is using the data source starting address. (SB)
0 = Idle or video processor is processing graphics data source start address
1 = Waiting for video processor to use graphics data source start address

Bit 18:0 Graphics Data Source Starting Address, in 64-bit segment (GDSSA)

VPR10: Data Source Width and Offset for Extended Graphics Modes

Read/Write Address: VP_Base+10h
Power-on Default: Undefined

This register specifies data source data line width and offset address for extended graphics modes.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**GRAPHICS DATA SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**GRAPHICS DATA START ADDRESS OFFSET**									

Bit 31:26 Reserved

Bit 25:16 Graphics Data Source data line width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Graphics Data Start Address Offset, in 64-bit segment

VPR14: Video Window I Left and Top Boundaries

Read/Write Address: VP_Base+14h
Power-on Default: Undefined

This register specifies left and top boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, top boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, left boundary

VPR18: Video Window I Right and Bottom Boundaries

Read/Write Address: VP_Base+18h
Power-on Default: Undefined

This register specifies right and bottom boundary for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW I BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW I RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video window I, bottom boundary

Bit 15:11 Reserved

Bit 10:0 Video window I, right boundary

VPR1C: Video Window I Source Start Address

Read/Write Address: VP_Base+1Ch
Power-on Default: Undefined

This register specifies video start address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SB**	**VWISS**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWISS															

Bit 31:20 Reserved

Bit 19 Status bit. This bit is used for software to read back the status of the current frame. Software needs to program this bit to 1 when programming the graphics data source start address. The hardware will reset this status bit to 0 when the current frame is using the data source starting address. (SB)
0 = Idle or video processor is processing W1 data source start address
1 = Waiting for video processor to use W1 data source start address

Bit 18:0 Video Window I source start address for, in 64-bit segment. (VWISS)

VPR20: Video Window I Source Width and Offset

Read/Write Address: VP_Base+20h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW I SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW I SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window I Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window I Source Address Offset, in 64-bit segment

VPR24: Video Window I Stretch Factor:

Read/Write Address: VP_Base+24h
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window I. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1. The two high bytes of this register can be used to enable the “Bob” function.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW I INITAL ODD FIELD								**VIDEO WINDOW I INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I HORIZONTAL STRETCH								**VIDEO WINDOW I VERTICAL STRETCH**							

Bit 31:24 Video Window I Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window I Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window 1 Horizontal Stretch Factor (W1HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window 1 Vertical Stretch Factor (W1VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W1VSF = \left(1- \frac{Source}{Destination} \right) * 256$$

VPR28: Video Window II Left and Top Boundaries

Read/Write Address: VP_Base+28h
Power-on Default: Undefined

This register specifies left and top boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II TOP BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II LEFT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Top Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Left Boundary

VPR2C: Video Window II Right and Bottom Boundaries

Read/Write Address: VP_Base+2Ch
Power-on Default: Undefined

This register specifies right and bottom boundary for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO WINDOW II BOTTOM BOUNDARY**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO WINDOW II RIGHT BOUNDARY**										

Bit 31:27 Reserved

Bit 26:16 Video Window II, Bottom Boundary

Bit 15:11 Reserved

Bit 10:0 Video Window II, Right Boundary

VPR30: Video Window II Source Start Address

Read/Write Address: VP_Base+30h
Power-on Default: Undefined

This register specifies video start address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												**SB**	**(VWIIDS)**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VWIIDS															

Bit 31:20 Reserved

Bit 19 Status bit. This bit is used for software to read back the status of the current frame. Software needs to program this bit to 1 when programming the video window II source start address. The hardware will reset this status bit to 0 when the current frame is using the data source starting address. (SB)
0 = Idle or video processor is processing W1 data source start address
1 = Waiting for video processor to use W1 data source start address

Bit 18:0 Video Window II Source Starting Address in 64-bit segment (VWIIDS)

VPR34: Video Window II Source Width and Offset

Read/Write Address: VP_Base+34h
Power-on Default: Undefined

This register specifies video source data line width and offset address for video window II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO WINDOW II SOURCE DATA LINE**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO WINDOW II SOURCE ADDRESS**									

Bit 31:26 Reserved

Bit 25:16 Video Window II Source Data Line Width, in 64-bit segment

Bit 15:10 Reserved

Bit 9:0 Video Window II Source Address Offset, in 64-bit segment

VPR38: Video Window II Stretch Factor

Read/Write Address: VP_Base+38h
Power-on Default: 00000000h

This register specifies video horizontal and Vertical stretch factor for video window II. For optimal display quality, we recommend destination to source ratio to be maximum of 4:1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD								**VIDEO WINDOW II INITIAL EVEN FIELD**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II HORIZONTAL STRETCH								**VIDEO WINDOW II VERTICAL STRETCH**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window II Horizontal Stretch Factor (W2HSF)

note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2HSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Video Window II Vertical Stretch Factor (W2VSF)
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch

$$W2VSF = \left(1- \frac{Source}{Destination} \right) * 256$$

VPR3C: Graphics and Video Control II

Read/Write: Address: VP_Base+3Ch
Power-on Default: 000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**EGHS 2-1**	**R**	**EGVS**	**EGVSF**	**EGHR**	**EGVI**	**RESERVED**								

Bit 31:15 Reserved (R)

Bit 14 Enable Graphic 2-to-1 Horizontal Shrink (EGHS 2-1)

Bit 13 Reserved (R)

Bit 12 Enable Graphic Vertical Shrink (EGVS)

Bit 11 Enable Graphic Vertical Scale Factor to 80H (EGVSF)

Bit 10 Enable Graphic Horizontal Replication (EGHR)

Bit 9 Enable Graphic Vertical Interpolation (EGVI)

Bit 8:0 Reserved

VPR40: Graphic Scale Factor

Read/Write Address: VP_Base+40h
Power-on Default: 00000000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GRAPHIC INITIAL ODD FIELD VERTICAL								**GRAPHIC INITAL EVEN FIELD VERTICAL**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRAPHIC HORIZONTAL SCALE FACTOR								**GRAPHIC VERTICAL SCALE FACTOR**							

Bit 31:24 Graphic Initial Odd Field Vertical Scale Factor

Bit 23:16 Graphic Initial Even Field Vertical Scale Factor

Bit 15:8 Graphic Horizontal Scale Factor (GHSF)

$$GHSF = \frac{Source}{Destination} * 256$$

Bit 7:0 Graphic Vertical Scale Factor (GVSF)

$$GVSF = \left(1 - \frac{Source}{Destination}\right) * 256$$

VPR54: FIFO Priority Control

Read/Write Address: VP_Base+54h
Power-on Default: 07216543h

This register specifies FIFO priority controls for graphics, Flat Panel Read Frame Buffer FIFO1, Video Window I, Video Window II, Flat Panel Write Frame Buffer, Capture Window and Flat Panel Read Frame Buffer FIFO2. Graphics FIFO has the highest priority and Flat Panel Read FIFO2 has the lowest priority as default.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**FPR FIFO2**			**R**	**CWFIFO**			**R**	**FPW FIFO**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	**VWII FIFO**			**R**	**VWI FIFO**			**R**	**FPR FIFO1**			**R**	**GFIFO**		

Bit 31:27 Reserved

Bit 26:24 Flat Panel Read FIFO2 priority select (FPR FIFO2
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last) (default)

Bit 23 Reserved (R)

Bit 22:20 Capture Window FIFO priority select (CWFIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd) (default)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 19 Reserved (R)

Bit 18:16 Flat Panel Write FIFO priority select (FPW FIFO)
000 = request is off
001 = highest priority (1st) (default)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)

111 = lowest priority (last)

Bit 15 Reserved (R)

Bit14:12 Video Window II FIFO priority select (VWII FIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th) (default)
111 = lowest priority (last)

Bit 11 Reserved (R)

Bit 10:8 Video Window I FIFO priority select (VWI FIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th)
101 = next priority (5th) (default)
110 = next priority (6th)
111 = lowest priority (last)

Bit 7 Reserved (R)

Bit 6:4 Flat Panel Read FIFO1 priority select (FPR FIFO1)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd)
100 = next priority (4th) (default)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

Bit 3 Reserved

Bit 2:0 Graphics FIFO priority select (GFIFO)
000 = request is off
001 = highest priority (1st)
010 = next priority (2nd)
011 = next priority (3rd) (default)
100 = next priority (4th)
101 = next priority (5th)
110 = next priority (6th)
111 = lowest priority (last)

VPR58: FIFO Empty Request level Control

Read/Write Address: VP_Base+58h
Power-on Default: 00000444h

This register specifies FIFO empty request level for graphics FIFO, Video Window I, and Video Window II. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty. For LCD Read FIFO1/FIFO2 and LCD Write FIFO request level controls, they are located in FPR4A register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VWII FIFO**			**R**	**VWI FIFO**			**R**	**GFIFO**		

Bit 31:11 Reserved

Bit 10:8 Video Window II FIFO Empty request level Select (VWII FIFO)
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 7 Reserved (R)

Bit 6:4 Video Window I FIFO Empty request level Select (VWI FIFO)
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty
111 = 12 or more empty

Bit 3 Reserved (R)

Bit 2:0 Graphics FIFO Empty request level Select (GFIFO)
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty (default)
101 = 8 or more empty
110 = 10 or more empty

111 = 12 or more empty

VPR5C: YUV to RGB Conversion Constant

Read/Write Address: VP_Base+5Ch
Power-on Default: EDEDEDh
This register specifies the YUV to RGB conversion constant.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								**RED CONVERSION CONSTANT**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GREEN CONVERSION CONSTANT								**BLUE CONVERSION CONSTANT**							

Bit 31:24 Reserved

Bit 23:16 Red Conversion Constant

Bit 15:8 Green Conversion Constant

Bit 7:0 Blue Conversion Constant

VPR60: Current Scan Line Position

Read Only Address: VP_Base+60h
Power-on Default: Undefined

This register specifies the current scan line position.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**CURRENT SCAN LINE**										

Bit 31:11 Reserved

Bit 10:0 Current Scan Line. This register returns the number for current scan line.

VPR64: Signature Analyzer Control and Status

Read/Write Address: VP_Base+64h
Power-on Default: Undefined

This register specifies controls and status for signature analyzer as well as the analyzer signature.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ANALYZER SIGNATURE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												**SAE**	**SAR**	**SASS**	

Bit 31:16 Analyzer Signature. These bits are Ready Only.

Bit 15:4 Reserved

Bit 3 Signature Analyzer Enable/Stop. Software needs to set this bit = 1 as a "ENABLE" control bit in order to enable signature analyzer. Once the analysis is completed, the hardware will reset this bit = 0 as a "STOP" status bit. (SAE)
0 = Stop (analysis is completed)
1 = Enable (analysis is in progress)

Bit 2 Signature Analyzer Reset/Normal. Software needs to set this bit = 1 as a (SAR)
"RESET" control bit to reset signature shift register to "0" before turning on signature analyzer. In the next vertical sync pulse after bit 3 and bit 2 have been set to "11", bit 2 will be automatically reset to "0" as a "NORMAL" status bit.
0 = Normal (disable reset to signature analyzer)
1 = Reset (enable reset to signature analyzer)

Bit 1:0 Signature Analyzer Source Select. These bits selects the input source for the signature analyzer. (SASS)
00 = Source is Red output from Multimedia RAMDAC
01 = Source is Green output from Multimedia RAMDAC
1x = Source is Blue output from Multimedia RAMDAC

VPR68: Video Window I Stretch Factor:

Read/Write Address: VP_Base+24h
Power-on Default: 00000000h

This register specifies additional precision to the video horizontal and Vertical stretch factor for video window I. Combined with VPR24 it will give a 16 bit precision to the stretch factor

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD LSB								**VIDEO WINDOW II INITIAL EVEN FIELD LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW I HORIZONTAL STRETCH LSB								**VIDEO WINDOW I VERTICAL STRETCH LSB**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window 1 Horizontal Stretch Factor
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch W1HSF = $\text{LSB}\left(\frac{\text{Source}}{\text{Destination}}\right) * 65536$

Bit 7:0 Video Window 1 Vertical Stretch Factor
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch W1VSF = $\text{LSB}\left(1 - \frac{\text{Source}}{\text{Destination}}\right) * 65536$

VPR6C: Video Window II Stretch Factor

Read/Write Address: VP_Base+38h
Power-on Default: 00000000h

This register specifies additional precision to video horizontal and vertical stretch factor for video window II. Combined with VPR38 provides 16 bit precision to the stretch factor

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VIDEO WINDOW II INITAL ODD FIELD LSB								**VIDEO WINDOW II INITIAL EVEN FIELD LSB**							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO WINDOW II HORIZONTAL STRETCH LSB								**VIDEO WINDOW II VERTICAL STRETCH LSB**							

Bit 31:24 Video Window II Initial Odd Field Vertical Scale Factor

Bit 23:16 Video Window II Initial Even Field Vertical Scale Factor

Bit 15:8 Video Window II Hortizontal Stretch Factor
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch W2HSF = $\text{LSB}\left(\frac{\text{Source}}{\text{Destination}}\right) * 65536$

Bit 7:0 Video Window II Vertical Stretch Factor
note: when stretch factor is set to 0, it becomes a 1-to-1 stretch W2VSF = $\text{LSB}\left(1 - \frac{\text{Source}}{\text{Destination}}\right) * 65536$

Capture Processor Control Registers

The Capture Processor Control Registers specify the control registers for Capture Processor. The Capture Processor Control Registers can only be accessed through memory-mapped. The capture processor control registers address start at CP_Base = PCI VGA graphics base address + 4MB + 56K.

CPR00: Capture Port Control

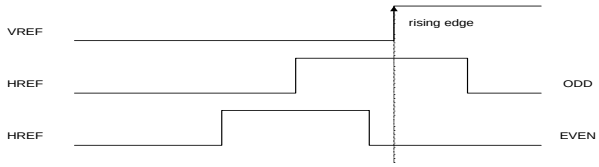
Read/Write Address: CP_Base+00h
Power-on Default: 00h
This register specifies the capture port which can be used for video capture and video playback.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**EMO**	**FDMS**	**VREF**	**HREF**	**EHF**		**EVR**		**EHR**	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDI		**FSE**			**IDCE**	**DBE**	**CC**	**FIS**	**IS**	**CBS**	**CFO**	**VIS**	**BUF2**	**BUF1**	**VCE**

Bit 31:26 Reserved

Bit 25 External Memory Only Select (Read Only). This register bit definition is opposite from the MD[23] definition in the Table 3: Power on Configuration. (EMO)
0 = Normal. Allow both internal and external memory access depends on MD[2]/MCR62[2] setting.
1 = External Memory Access Only

Bit 24 Field Detect Method Select (FDMS)
0 = Falling edge of VSYNC
1 = Rising edge of VSYNCt



Bit 23 VREF Polarity (VREF)
0 = "High" active
1 = "Low" active

Bit 22 HREF Polarity (HREF)
0 = "High" active
1 = "Low" active

Bit 21:20 Enable Horizontal Filtering (EHF)
00 = no filtering
01 = 2-tap filtering
10 = 3-tap filtering
11 = 4-tap filtering

Bit 19:18 Enable Vertical Reduction (EVR)
00 = no reduction
01 = 2 to 1 reduction
10 = 4 to 1 reduction
11 = reserved

Bit 17:16 Enable Horizontal Reduction (EHR)
00 = no reduction
01 = 2 to 1 reduction
10 = 4 to 1 reduction
11 = reserved

Bit 15:14 Video Capture Input Data Format (VDI)
00 = YUV 4:2:2
01 = YUV 4:2:2 (with byte swapping)
10 = RGB 5:5:5
11 = RGB 5:6:5

Bit 13:11 Frame Skip Enable (FSE)
000 = no skip
001 = skip every other frame
010 = skip even frame
011 = skip odd frame
100 = capture 2 and skip 1 frame
101 = capture 3 and skip 1 frame
110 = capture 1 and skip 2 frame
111 = capture 1 and skip 3 frame

Bit 10 Interlace Data Capture Enable (IDCE)
0 = Disable (non-interlace)
1 = Enable (interlace data. even field will be captured into buffer1 and odd field will be captured into buffer2) When this bit is set to 1, double buffer mode needs to be also enabled (bit 9 =1).

Bit 9 Double Buffer Enable (DBE)
0 = Disable. Use buffer1 addressed by VPR48.
1 = Enable. Use buffer1 and buffer2 addressed by VPR48 and VPR4C.

Bit 8 Capture Control (CC)
0 = Continuous Capture
1 = Conditional Capture. Capture is controlled by bit 1 or bit 2 of this register.

Bit 7 Field Input Status (Read Only) (FIS)
0 = even field
1 = odd field

Bit 6 Interlace Status (Read Only) (IS)
0 = non-interlace
1 = interlace

Bit 5 Current Buffer Status (Read Only) (CBS)
0 = Buffer 1 is the current buffer used
1 = Buffer 2 is the current buffer used

Bit 4 Current Frame Capture Status (Read Only) (CFO)
0 = Skip the current frame
1 = Capture the current frame

Bit 3 VSYNC Input Status (Read Only) (VIS)
0 = VSYNC pulse is inactive
1 = VSYNC pulse is active

Bit 2 Buffer 2 Status/Control Bit. This bit is used for software to read back the status of the current frame. Software needs to preset this bit to 1 when programming the Buffer 2 starting address in VPR4C. This bit can be set by drawing engine, and it can also be reset by video capture unit. If continuous capture is selected (bit 8 =0), this bit will be ignored. (BUF2)
0 = Idle or Capture has completed
1 = Capture in progress

Bit 1 Buffer 1 Status/Control Bit. This bit is used for software to read back the status of the current frame. Software needs to preset this bit to 1 when programming the Buffer 1 starting address in VPR48. This bit can be set by drawing engine, and it can also be reset by video capture unit. If continuous capture is selected (bit 8 =0), this bit will be ignored. (BUF1)
0 = Idle or Capture has completed
1 = Capture in progress

Bit 0 Video Capture Enable. When Video Capture is enabled, all video port I/O pins except for "BLANK" pin will become input pins only. (VCE)
0 = Disable
1 = Enable

CPR04: Video Source Clipping Control

Read/Write Address: CP_Base+04h
Power-on Default: Undefined

This register specifies top and left clipping of video source.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						**VIDEO SOURCE TOP CLIPPING**									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**VIDEO SOURCE LEFT CLIPPING**									

Bit 31:26 Reserved

Bit 25:16 Video Source Top Clipping, # of line to drop

Bit 15:10 Reserved

Bit 9:0 Video Source Left Clipping, # of pixel to drop

CPR08: Video Source Capture Size Control

Read/Write Address: CP_Base+08h
Power-on Default: Undefined

This register specifies video source capture size.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					**VIDEO SOURCE HEIGHT**										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					**VIDEO SOURCE WIDTH**										

Bit 31:27 Reserved

Bit 26:16 Video Source Height

Bit 15:11 Reserved

Bit 10:0 Video Source Width

CPR0C: Capture Port Buffer I Source Start Address

Read/Write Address: CP_Base+0Ch
Power-on Default: Undefined

This register specifies video source start address for Buffer I of Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													**CAPTURE PORT I**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE PORT I															

Bit 31:19 Reserved

Bit 18:0 Capture Port Buffer I source start address, in 64-bit segment

CPR10: Capture Port Buffer II Source Start Address

Read/Write Address: CP_Base+10h
Power-on Default: Undefined

This register specifies video source start address for Buffer II of Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													**CAPTURE PORT II**		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPTURE PORT II															

Bit 31:19 Reserved

Bit 18:0 Capture Port Buffer II source start address, in 64-bit segment.

CPR14: Capture Port Source Offset Address

Read/Write Address: CP_Base+14h
Power-on Default: Undefined

This register specifies video source offset address for Capture Port.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						**CAPTURE PORT SOURCE**									

Bit 31:10 Reserved

Bit 9:0 Capture Port Source Address Offset, in 64-bit segment

CPR18: Capture FIFO Empty Request level Control

Read/Write Address: CP_Base+18h
Power-on Default: 00000006h

This register specifies Capture FIFO empty request level. At the specified empty FIFO level, FIFO request will be generated. Default FIFO empty levels are all 6 or more empty.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													**CAPTURE WINDOW**		

Bit 31:3 Reserved

Bit 2:0 Capture Window FIFO Empty request level Select
000 = 2 or more empty
001 = 3 or more empty
010 = 4 or more empty
011 = 5 or more empty
100 = 6 or more empty
101 = 8 or more empty
110 = 10 or more empty (default)
111 = 12 or more empty

Chapter 19: Electrical Specifications

Absolute Maximum Ratings

Table 20: Absolute Maximum Ratings

Specification	Maximum rating
Ambient temperature (TA)	0º C to 75º C
Extended temperature*	-40º C to 80º C
Storage temperature	-40º C to 125º C
Voltage on I/O pins with respect to VSS	- 0.5V to VDD + 5%
Operating power dissipation	1.079 W
Core DC Power supply voltage	3.3V ± 5%

Note: * SMI712GE

DC Specifications

- Maximum VCLK = 80 MHz
- Maximum MCLK = 129 MHz (86 MHz for the 4MByte version)
- Maximum VRCLK = 80 MHz

Table 21: Digital DC Specification

Name	Parameter	Min	Typical	Max	Unit	Notes
V_{IL}	Input Low Voltage	-		0.8	V	
V_{IH}	Input High Voltage	2.0		3.5	V	
V_{OL}	Output Low Voltage	-		0.4	V	
V_{OH}	Output High Voltage	2.4		VDD+0.5	V	
I_{OZL}	Output Tri-state Current	-		10	µA	
I_{OZH}	Output Tri-state Current	-		10	µA	
I_{OZL} (Pull up pins)	Output Tri-state Current	-150		-10	µA	
I_{OZH} (Pull up pins)	Output Tri-state Current	-		10	µA	
I_{OZL} (Pull down pins)	Output Tri-state Current	-		10	µA	
I_{OZH} (Pull down pins)	Output Tri-state Current	10		150	µA	
C_{IN}	Input Capacitance			TBD	pF	
C_{OUT}	Output Capacitance			TBD	pF	
I_{CC}	Power Supply Current (Active)			255*	mA	
I_{CC}	Power Supply Current (Sleep)			2.5	mA	

Note: * LCD only

Table 22: RAMDAC Characteristics

Parameter	Min	Typical	Max	Unit
Resolution Each DAC	-	8		Bits
LSB Size	-	54.7		µA
Output Full Scale Current	-	14.0		mA
Integral Linearity Error	0	-	1.5	LSB
Differential Linearity Error	0	-	1.5	LSB
DAC to DAC Mismatch	0	-	5%	
Power Supply Rejection Ratio	0	-	0.5	% /% AVDD
Output Compliance	0	-	1.2	V
Output Capacitance	-	-	10	pF
Glitch Energy	-	30	-	pV-Sec

Table 23: RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
AVDD	DAC Supply Voltage	3.17	3.3	3.47	V
CVDD	PLL Supply Voltage	3.17	3.3	3.47	V
VREF	Internal DAC voltage reference	1.1	1.235	1.35	V

AC Specifications

Table 24: RAMDAC AC Specifications

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	3		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Setting Time	15		ns	
DAC-to-DAC Output Skew	2	15	ns	3

Notes:
1. Measured from the 50% of VCLK to the 50% point of full scale transaction
2. Measured from 10% to 90% full scale
3. With DAC outputs equally loaded

Parameter	I_{OUT} (mA)	VOUT (V)	BLANK	Input Data
White	**14.0**	**0.7**	**1**	**FFh**
Data	**Data**	**Data**	**1**	**Data**
Black	**0**	**0**	**1**	**00h**
~BLANK	**0**	**0**	**0**	**Don't Care**

Notes:
- Condition for V_{OUT} is a 50 Ohm terminated load, use of the internal VREF and RFSC = 1.2 K Ohms.

AC Timing Specifications

Power On Reset

Table 25: Power-on Reset and Configuration Reset Timing

Symbol	Parameter	Min	Max	Unit
t1	Reset active from VCC stable	5	-	ms
t2	Reset active from external oscillator stable	0	-	
t3	Reset active from ~PWRDN signal stable	2	-	ms
t4	Internal Power On ~RESET from VCC stable	-	200	ns
t5	External ~RESET to internal Power On ~RESET inactive	-	20	ms
t6	External ~RESET Pulse Width		-	ns
t7	Configuration cycle setup time	20	-	ns
t8	Configuration cycle hold time	5		

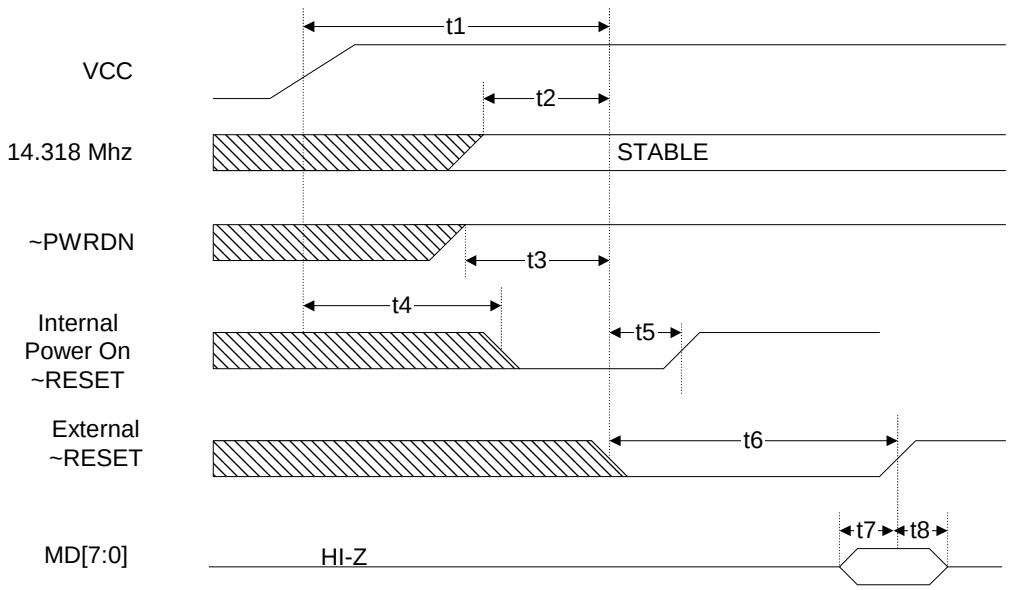


Figure 29: Power-on Reset and Reset Configuration Timing

PCI Bus Cycles

Table 26: PCI Bus Timing

Symbol	Parameter	Min	Max	Unit
t1	~FRAME setup to CLK	7	-	ns
t2	AD[31:0] (address) setup to CLK	7	-	ns
t3	AD[31:0] (address) hold from CLK	0	-	ns
t4	AD[31:0] (Read Data) valid from CLK	2	11	ns
t5	AD[31:0] (Read Data) hold from CLK	0	-	ns
t6	AD[31:0] (Write Data) setup to CLK	7	-	ns
t7	AD[31:0] (Write Data) hold from CLK	0	-	ns
t8	C/~BE[3:0] (Command) setup to CLK	7	-	ns
t9	C/~BE[3:0] (Command) hold from CLK	0	-	ns
t10	C/~BE[3:0] (Byte Enable) hold from CLK	0	-	ns
t11	~TRDY High-Z to High from CLK	2	-	ns
t12	~TRDY active from CLK	2	11	ns
t13	~TRDY inactive from CLK	2	11	ns
t14	~TRDY High before High-Z	1T	-	CLK
t15	~IRDY setup to CLK	7	-	ns
t16	~IRDY hold from CLK	0	-	ns
t17	~DEVSEL active from CLK	2	11	ns
t18	~DEVSEL inactive from CLK	2	11	ns
t19	~DEVSEL High before High-Z	1T	-	CLK

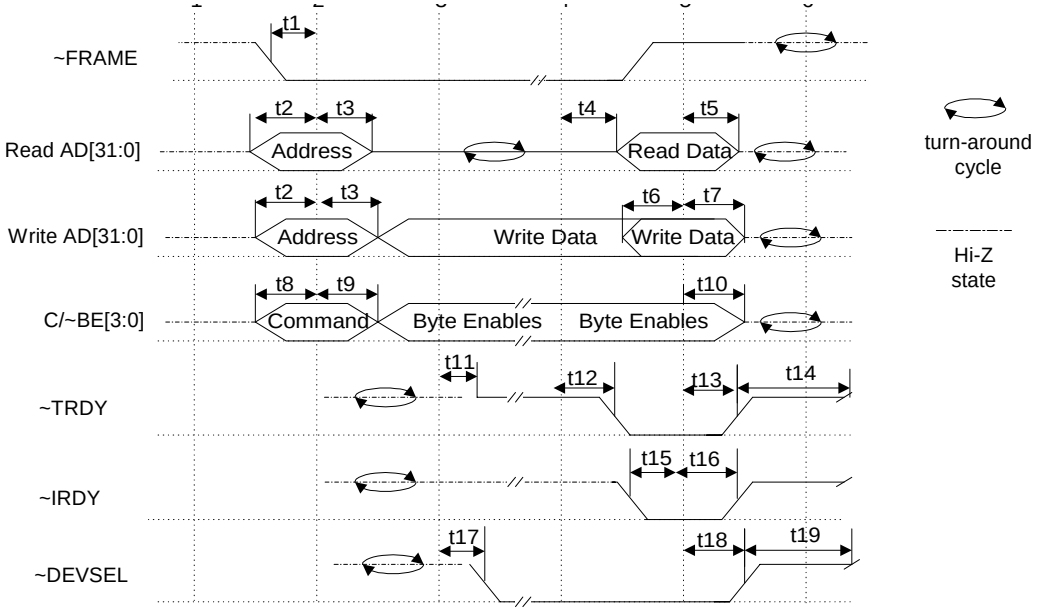


Figure 30: PCI Bus Timing Diagram

Flat Panel Interface Cycle Timing

Table 27: Color TFT Interface Timing

Symbol	Parameter	Min	Max	Unit
t1	TFT FPSCLK Cycle Time	12		ns
t2f	FDATA setup to FPSCLK falling edge	0.5T-2		ns
t3f	FDATA hold from FPSCLK falling edge	0.5T-2		ns
t4f	DE setup to FPSCLK falling edge	0.5T-4		ns
t5f	DE hold from FPSCLK falling edge	0.5T-4		ns
t2r	FDATA setup to FPSCLK rising edge	0.5T-5.5		ns
t3r	FDATA hold from FPSCLK rising edge	0.5T-2		ns
t4r	DE VSYNC setup to FPSCLK rising edge	0.5T-4		ns
t5r	DE VSYNC hold from FPSCLK rising edge	0.5T-4		ns
t6	FHSYNC Pulse Width	8	16	T
t7	FVSYNC Pulse Width	1		FHSYNC

Note: T = pixel clock rate on LCD

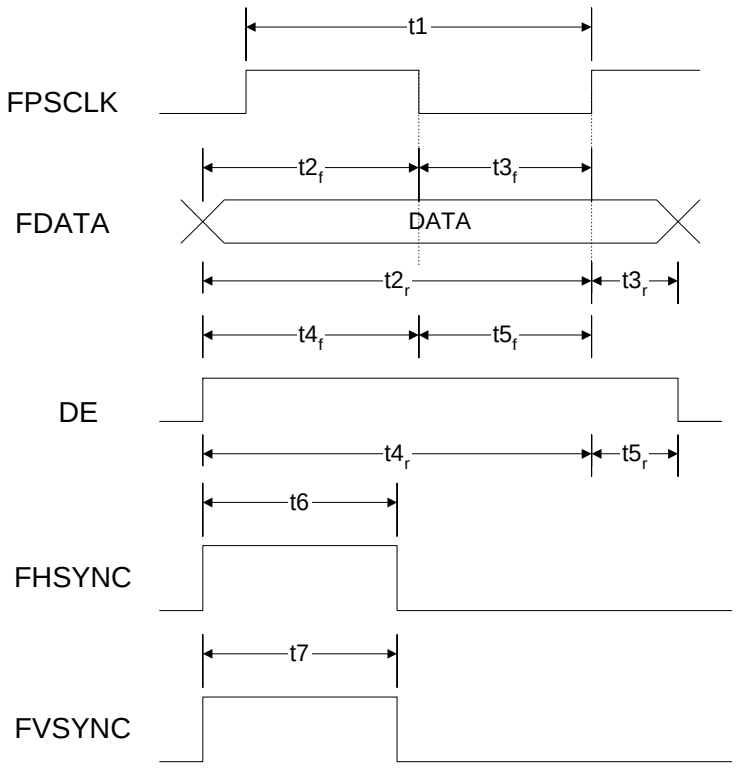


Figure 31: TFT Interface Timing

Table 28: Color DSTN Interface Timing

		16-Bit		24-BIt		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Unit**
t1	DSTN FPSCLK High Time	2.5T-3	3T+3			ns
t2	DSTN FPSCLK Low Time	2.5T-3	3t+3			ns
t3	FDATA setup to FPSCLK falling edge	2.5T-5				ns
t4	FDATA hold from FPSCLK falling edge	2.5T-5				ns
t5	LP Pulse Width	16T	32T			ns
t6	FP setup to LP falling edge	20T				ns
t7	FP hold from LP falling edge	4T				ns
t8	DSTN FPSCLK active from LP falling edge	16T				ns
t9	DSTN FPSCLK inactive to LP rising edge	8T				ns

Note: T = pixel clock rate on LCD

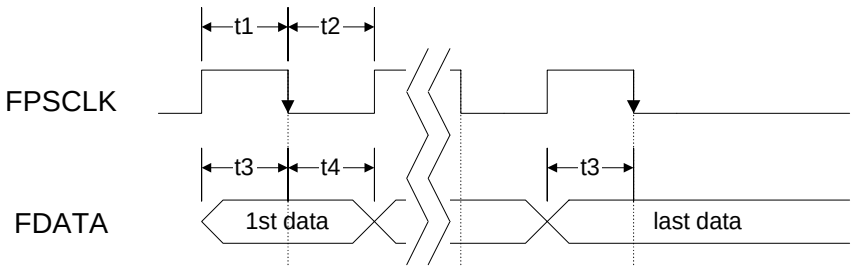


Figure 32: DSTN Interface (Clock and Data) Timing

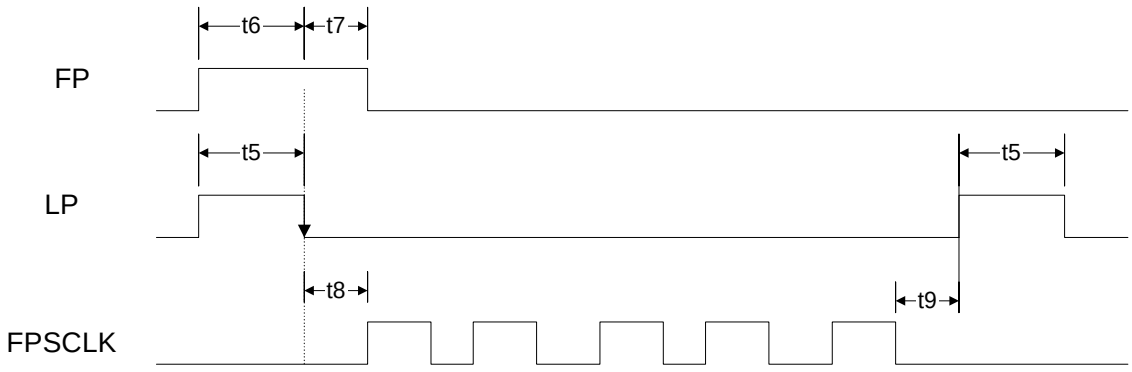


Figure 33: DSTN Interface (Control and Clock) Timing

Chapter 20: Mechanical Dimensions

Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.20	2.33	2.50	0.087	0.092	0.098
A1	—	0.60	—	—	0.024	—
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	—	0.75	—	—	0.030	—
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	—	24.13	—	—	0.950	—
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	17.95	18.00	18.05	0.707	0.709	0.711
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	—	24.13	—	—	0.950	—
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	17.95	18.00	18.05	0.707	0.709	0.711
e	—	1.27	—	—	0.050	—
ddd	—	—	0.15	—	—	0.006
θ	30° TYP			30° TYP		

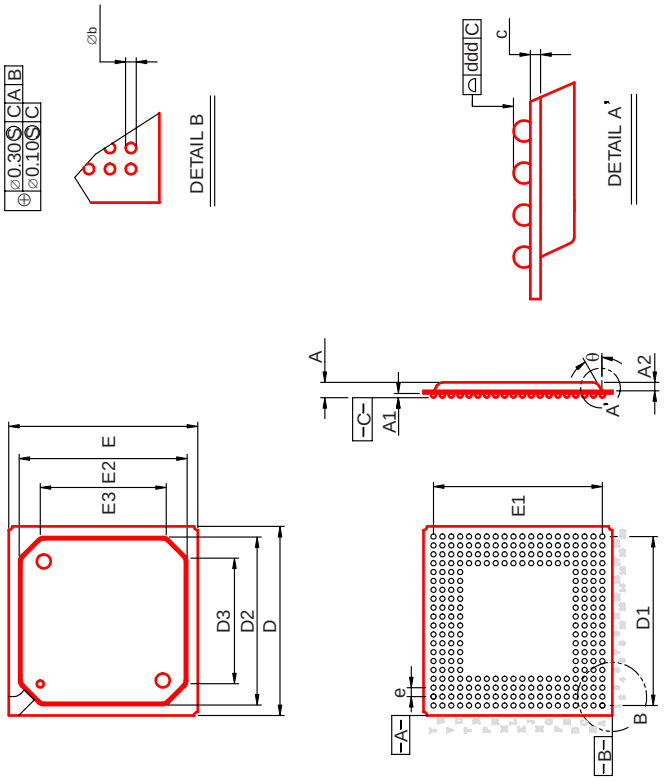


Figure 34: 256 BGA Mechanical Dimensions

Table 29: Ordering Information

Order Number	Description	Detailed Information
SM712GX020000-AA	SM712G AA	LynxEM+ 256 BGA Rev. AA
SM712GX02LF00-AA	SM712GF AA	LynxEM+ 256 BGA Rev. AA (lead free)
SM712GE020000-AA	SM712GE AA	LynxEM+ 256 BGA Rev. AA (ext. temp)
SM712GE02LF00-AA	SM712GEF AA	LynxEM+ 256 BGA Rev. AA (ext. temp/lead free)
SM712GX040000-AA	SM712G4 AA	LynxEM4+ 256 BGA Rev. AA
SM712GX04LF00-AA	SM712GF4 AA	LynxEM4+ 256 BGA Rev. AA (lead free)
SM712GE040000-AA	SM712GE4 AA	LynxEM4+ 256 BGA Rev. AA (ext. temp)
SM712GE04LF00-AA	SM712GEF4 AA	LynxEM4+ 256 BGA Rev. AA (ext. temp/lead free)

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