Low Noise Amplifier
20 - 55 GHz

MAAL-011186
Rev. V4

Features

- Wideband Performance
- Low Noise Figure: 2.5 dB
- Gain: 22 dB
- P1dB: 14 dB
- Bias Voltage: V_{DD} = 3.5 V
- Bias Current: I_{DSQ} = 130 mA
- 50 Ω Matched Input and Output
- Positive Voltage Only
- Lead-Free 5 mm 12-lead SMT Package
- RoHS* Compliant

Applications

- Test and Measurement
- EW
- ECM
- Radar

Description

The MAAL-011186 is an easy to use wideband low noise amplifier. It operates from 20 - 55 GHz and provides 2.5 dB noise figure, 22 dB gain and 14 dBm P1dB. The input and output are fully matched to 50 Ω with typical return loss of better than -10 dB.

This product is fabricated using a GaAs pHEMT process which features full passivation for enhanced reliability.

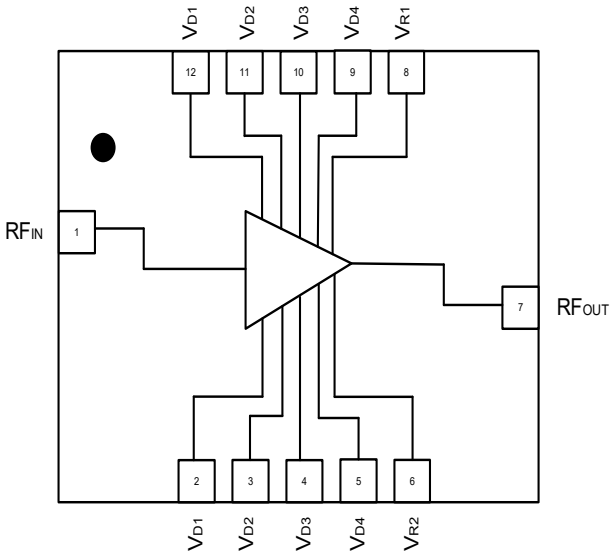
The MAAL-011186 can be used as a low noise amplifier stage or as a driver stage in higher power applications. This device is ideally suited for Test and Measurement, 5G communications, EW, ECM, and Radar applications.

Ordering Information[1,2]

Part Number	Package
MAAL-011186-TR0500	500 piece reel
MAAL-011186-SB1	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration[3]

Pin #	Function	Description
1	RF_{IN}	RF Input
2	V_{D1}	Lower Drain Bias One
3	V_{D2}	Lower Drain Bias Two
4	V_{D3}	Lower Drain Bias Three
5	V_{D4}	Lower Drain Bias Four
6	V_{R2}	Current Mirror Ref Voltage
7	RF_{OUT}	RF Output
8	V_{R1}	Current Mirror Ref Voltage
9	V_{D4}	Upper Drain Bias One
10	V_{D3}	Upper Drain Bias Two
11	V_{D2}	Upper Drain Bias Three
12	V_{D1}	Upper Drain Bias Four
PAD	PAD	Exposed Pad[3]

3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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Electrical Specifications:
Freq. = 20 - 55 GHz, T_A = +25°C, V_{CC} = 3.5 V, I_{DQ} = 130 mA, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Small Signal Gain	20 GHz 40 GHz 50 GHz	dB	20.0 16.5 15.0	22.0 18.0 16.5	—
Small Signal Gain Variation over Temperature	—	dB/°C	—	0.06	—
Gain Flatness	—	dB	—	±5	—
Noise Figure	20 GHz 25 - 40 GHz 40 - 50 GHz	dB	—	4.0 2.5 3.2	6.0 — —
Input Return Loss	—	dB	—	10	—
Output Return Loss	—	dB	—	10	—
Output Power 1dB Compression	—	dBm	—	14	—
Saturated Output Power (P_{SAT})	—	dBm	—	17	—
Output 3rd Order Intercept	—	dBm	—	24	—

Operational Maximum Ratings

Parameter	Absolute Maximum
Pin	+2 dBm
V_{DD}	4.0 V
Junction Temperature[4,5]	+150°C
Operating Temperature	-40°C to +85°C

4. Operating at nominal conditions with $T_J \leq$ +150°C will ensure MTTF > 1 x 10^6 hours.
5. Junction Temperature (T_J) = T_C + Θjc * (V * I)
   Typical thermal resistance (Θjc) = 22 °C/W.
   a) For T_C = +25°C,
   T_J = 36.4 °C @ 4 V, 130 mA
   b) For T_C = +85°C,
   T_J = 96.4 °C @ 4 V, 130 mA

Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Pin	+5 dBm
V_{DD}	4.5 V
Junction Temperature	+175°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

Recommended Operating Conditions

It is recommended to operate at a typical drain voltage of +3.5 V ± 5 %. The maximum recommended operating drain current (set by the voltage on V_R) is fundamentally defined by the combination of the maximum operating junction temperature and the power dissipated. This can be calculated as shown in note 5.

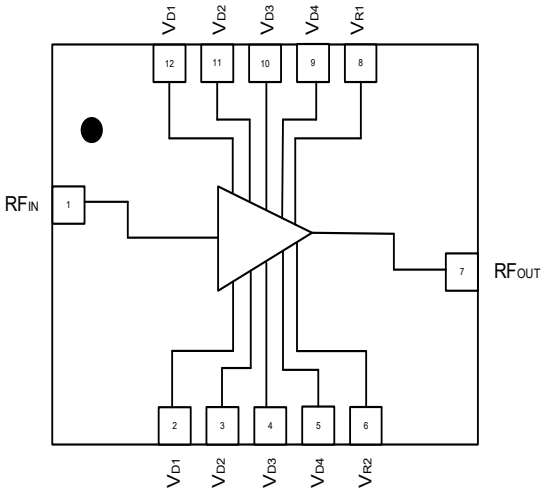
Electrostatic Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 1B HBM and class C3 CDM devices.

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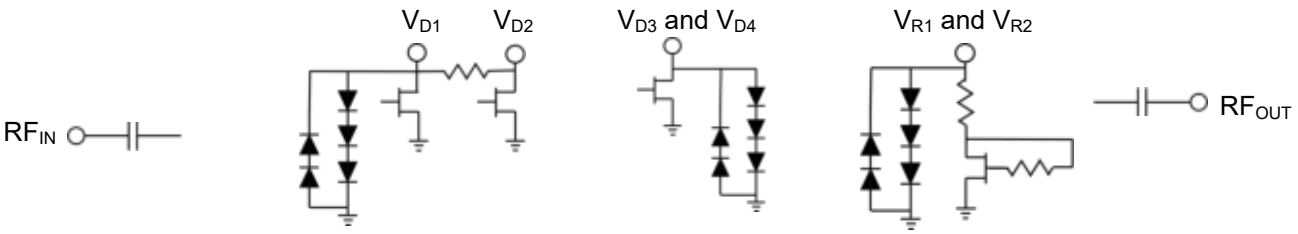
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Pin Configuration and Functional Descriptions



Pin #	Pin Name	Description
1	RF_{IN}	RF Signal Input. This pad is matched to 50 Ω and is AC coupled.
2,3,4,5	V_{D1},V_{D2}, V_{D3},V_{D4}	Drain biases for the lower half of the amplifier. External bypass capacitors are required as described in the applications schematic. There is no internal connection between these pads and pads 9,10,11,12 which are the drain biases for the upper half of the amplifier.
6	V_{R2}	Reference voltage for the lower half of the amplifier. This is used to set the drain current of the device. A voltage can be applied using a suitably sized series resistor to V_D, or can be applied using an active bias circuit for more precise control of the drain current. There is no internal connection to pin 8. See applications section for usage of this pin.
7	RF_{OUT}	RF Signal Output. This pad is matched to 50 Ω and is AC coupled.
8	V_{R1}	Reference voltage for the upper half of the amplifier. This is used to set the drain current of the device. A voltage can be applied using series resistor to V_D, or can be applied using an active bias circuit for more precise control of the drain current. There is no internal connection to pin 6. See applications section for correct usage of this pin.
9,10,11,12	V_{D4},V_{D3}, V_{D2},V_{D1}	Drain biases for the upper half of the amplifier. External bypass capacitors are required as described in the applications schematic. There is no internal connection between these pads and pads 2,3,4,5 which are the drain biases for the lower half of the amplifier.
	PAD	The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

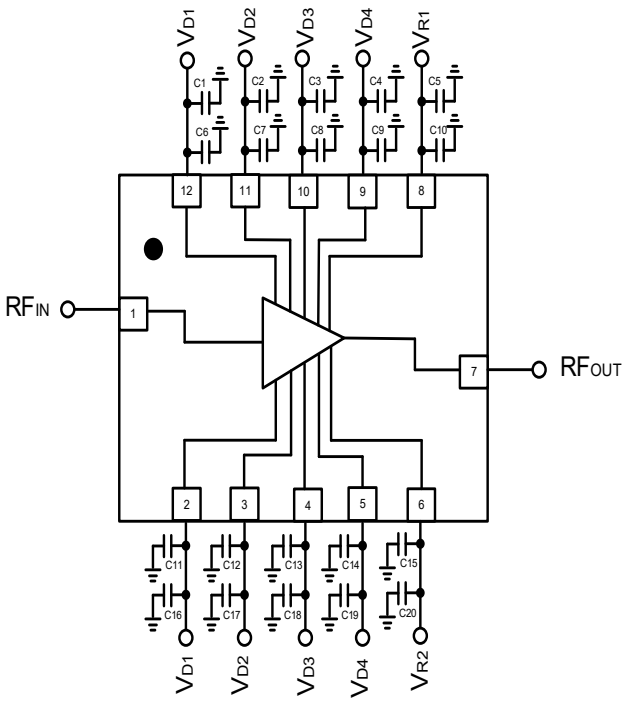
Interface Schematics



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Application Schematic



Parts List

Part	Value	Case Style
C6 - C15	100 pF	0402
C1 - C5, C16 - C20	0.1 µF	0402

Operating the MAAL-011186

Turn-on

1. Increase V_{D1}, V_{D2}, V_{D3}, V_{D4} to 3.5 V.
2. Set I_{DQ} by adjusting V_{R1} and V_{R2} or selecting a suitable resistor size. For a drain voltage of 3.5 V, a voltage of 1.4 V on V_{R1} and V_{R2} will result in a drain current of 130 mA. This corresponds to a 650 Ω resistor between the drain supply on each V_R pin.
3. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_{D1}, V_{D2}, V_{D3}, V_{D4} to 0 V.

Application Circuit and Operation

The basic application circuit is shown below. Place C6 - C15 capacitors as close to the package as physically possible. The position of the C1 - C5 and C16 - C20 capacitors are not as critical but should also be placed as closely as practically possible. All drain connections can be connected together so long as the recommended capacitors are placed as advised.

To set the drain current, a reference voltage (V_R) is applied to pins 6 and 8. If single positive supply operation is desired, a resistor can be connected in series between the drain supply and pin 6, and pin 8. A resistor value of 650 Ω between a drain supply of 3.5 V and each V_R pin, will result in a typical I_{DQ} of 130 mA. Alternatively, V_{R1} and V_{R2} can be supplied by a second voltage source, adjusted to achieve the desired drain current.

If using a fixed voltage on V_{R1} and V_{R2} to set the drain current it should be expected that there will be an amount of drain current variation over temperature and also between individual devices and manufacturing lots. If more precise control over the drain current is required, a simple, low cost active bias circuit can be used.

A suitable active bias circuit for use with the MAAL-011186 is detailed in MACOM applications note AN-0004357 which gives a full schematic, BOM, theory of operation and design guide. Here V_R should be considered to be the gate of the device as described in AN-0004357.

For all approaches to setting I_{DQ}, each V_R pin will sink between approximately 3 mA to 5 mA depending on the voltage applied: this should be accounted for when designing the circuit interfacing with the V_R pins.

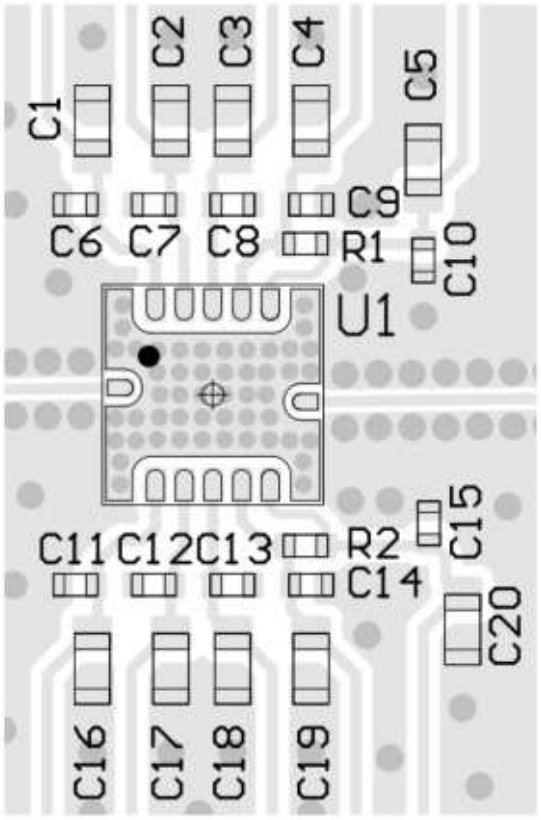
The number of electrical and thermal ground vias beneath the exposed ground paddle should be maximized in order to decrease the ground inductance and thermal impedance as far as possible within the confines of the application PCB. On the evaluation PCB described on the following page, XX vias have been used.

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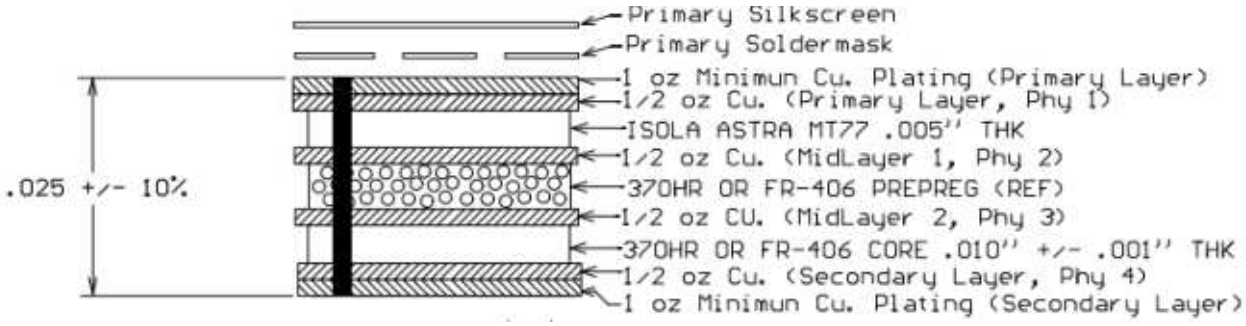
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Evaluation Board

If V_R and V_D are supplied separately, then R3 and R4 are not needed. To get agreement to the capacitor labels in the schematic on the previous page, subtract 20 from the labels below (C21 - 20 = C1).



Board Material



PCB Stackup

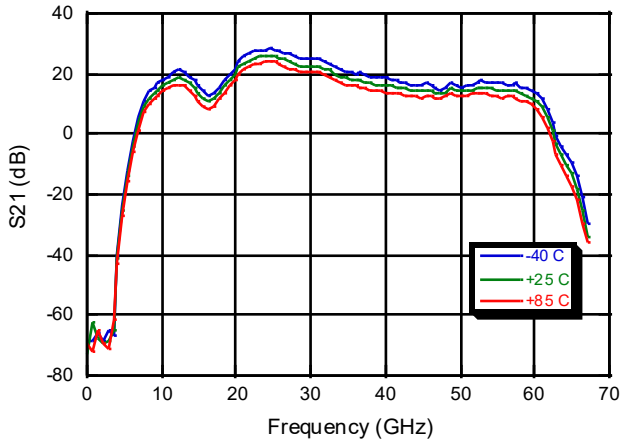
The PCB is a multi-layer board. The top layer (Isola Astra) is the microwave dielectric and the 0.5 oz. copper beneath it is the microwave ground (midlayer 1). The FR4 beneath this provides mechanical support and also DC trace routing.

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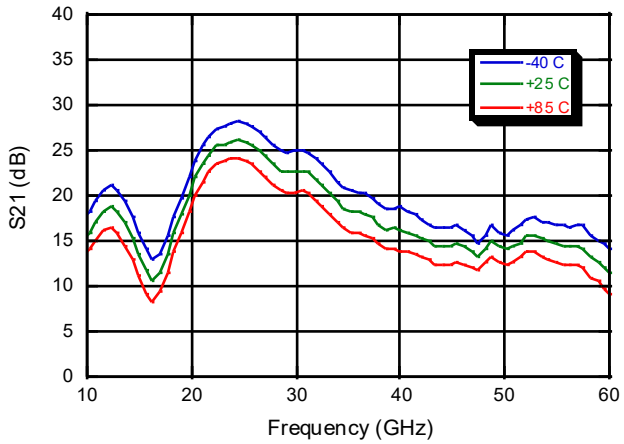
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Typical Performance Curves @ V_D = 3.5 V, I_D = 130 mA, Z_0 = 50 Ω

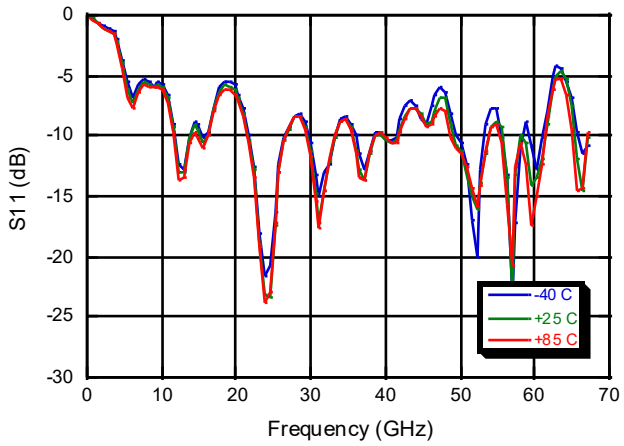
Gain



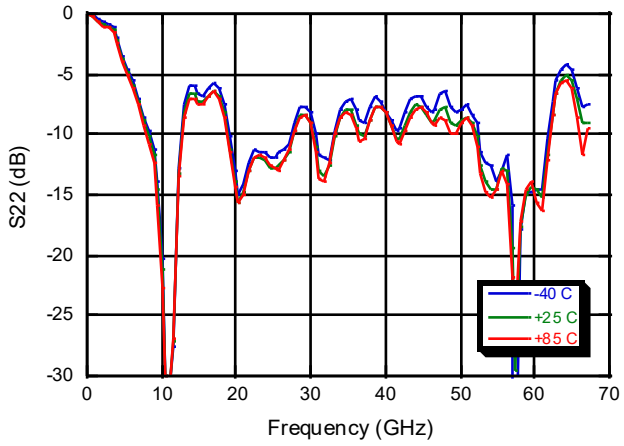
Gain 10 - 60 GHz



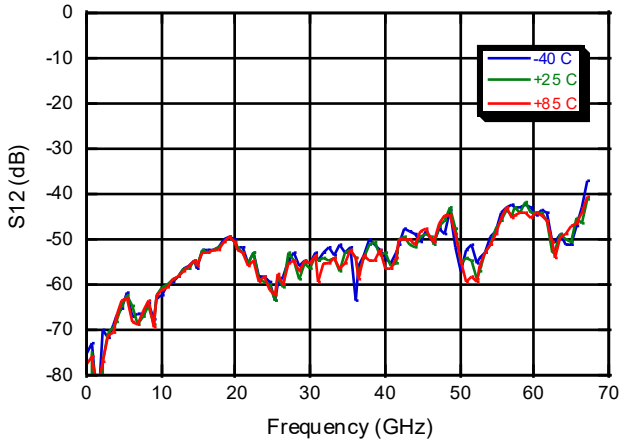
Input Return Loss



Output Return Loss



Reverse Isolation

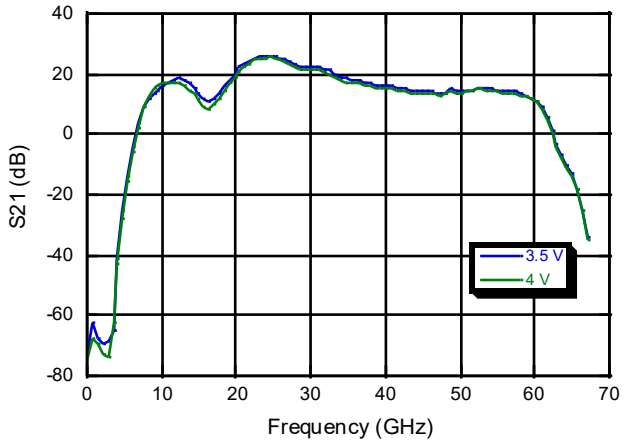


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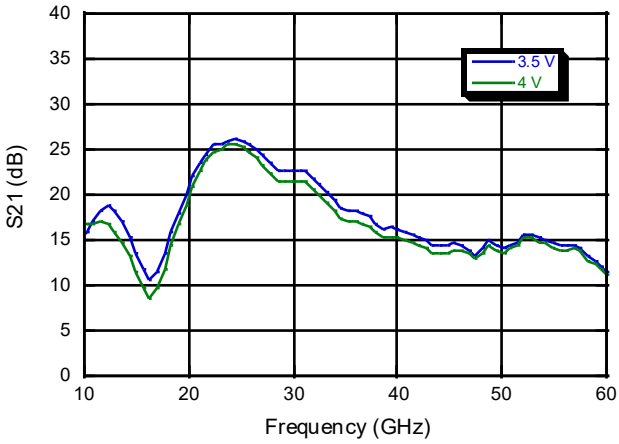
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Typical Performance Curves @ I_D = 130 mA, T_A = 25°C, Z_0 = 50 Ω

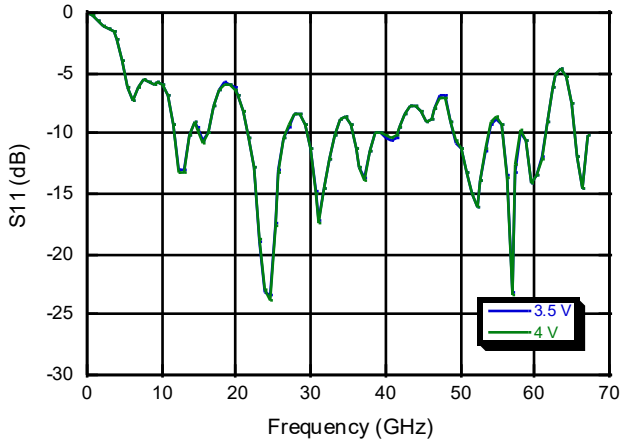
Gain



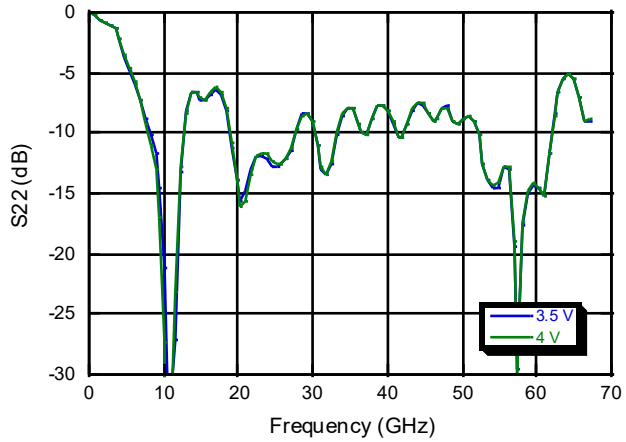
Gain 10 - 60 GHz



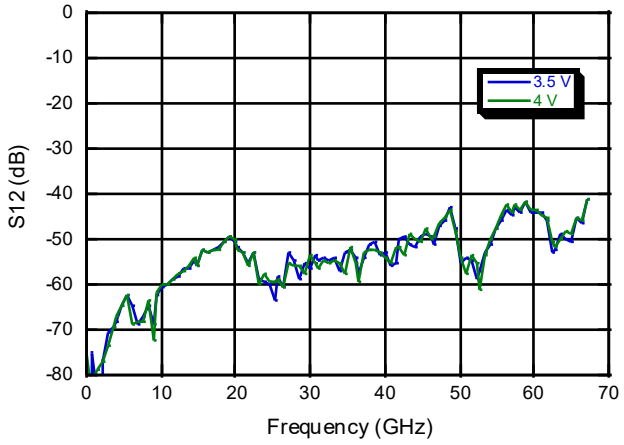
Input Return Loss



Output Return Loss



Reverse Isolation

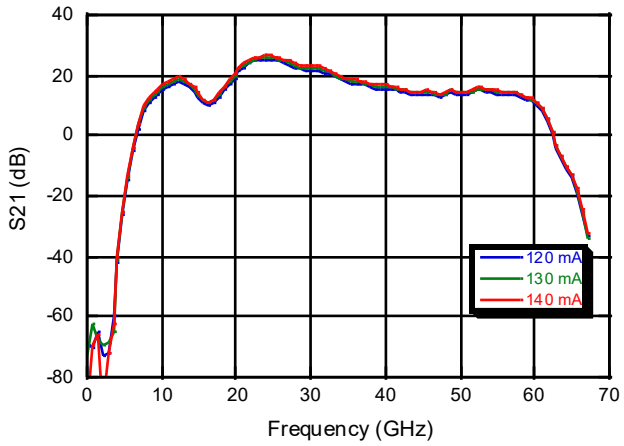


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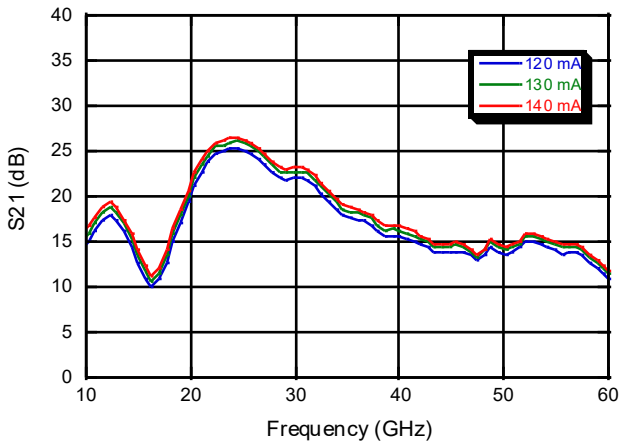
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Typical Performance Curves @ V_D = 3.5 V, T_A = 25°C, Z_0 = 50 Ω

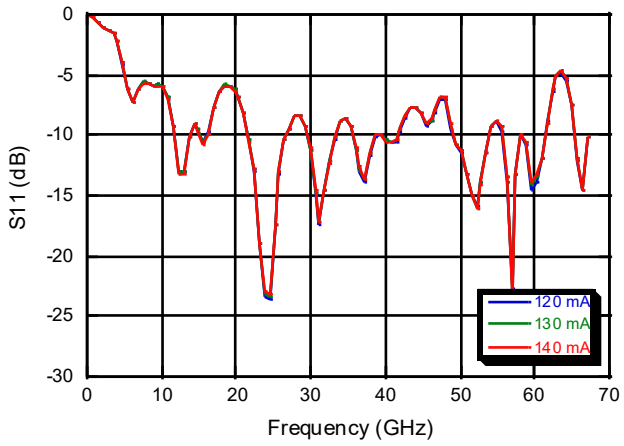
Gain



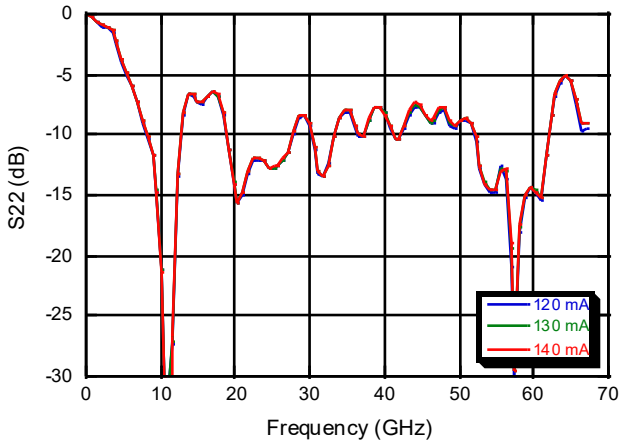
Gain 10 - 60 GHz



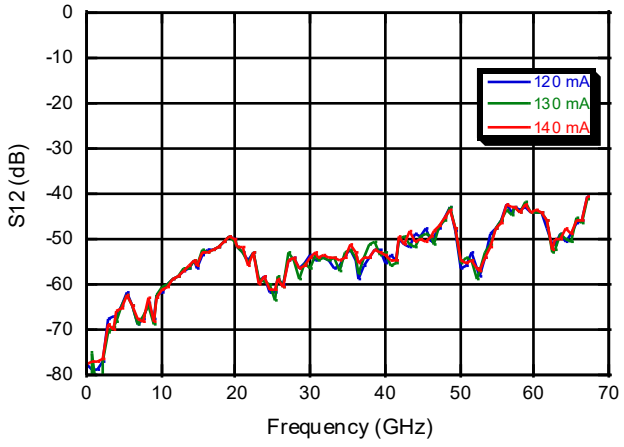
Input Return Loss



Output Return Loss



Reverse Isolation

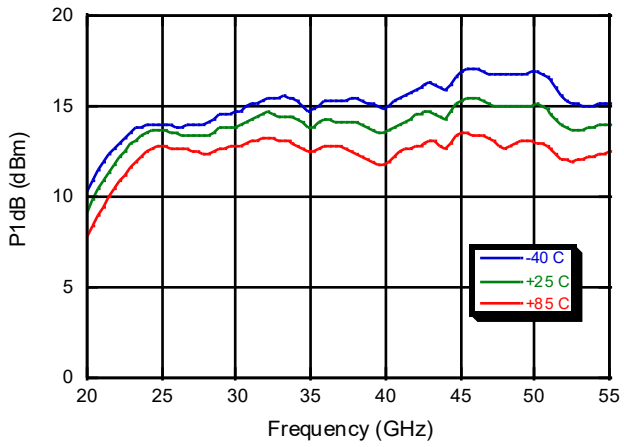


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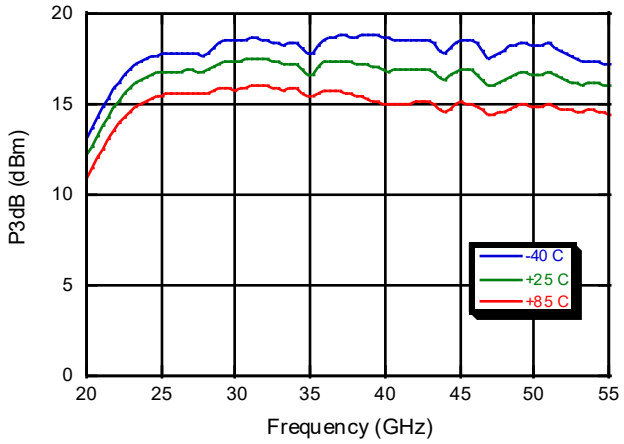
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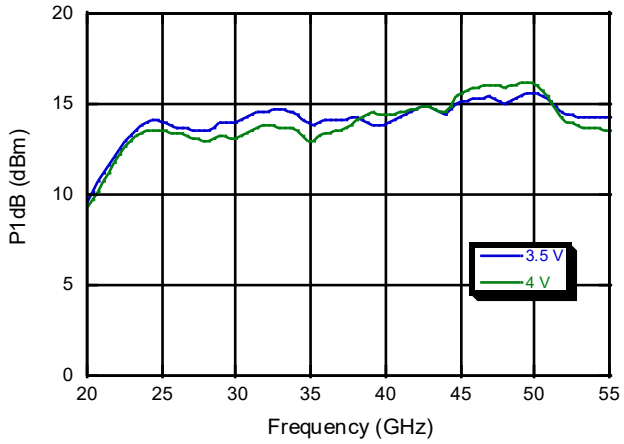
P1dB



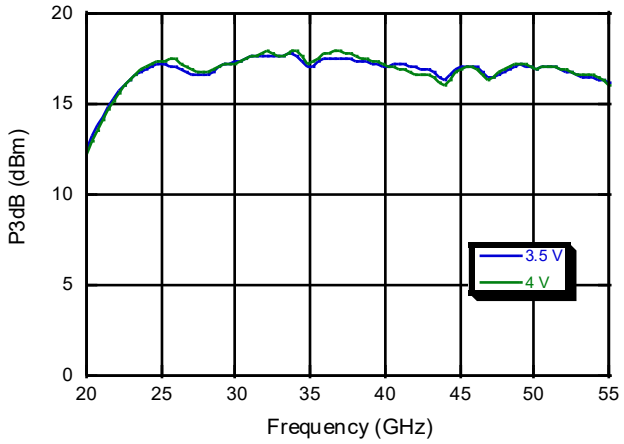
P3dB



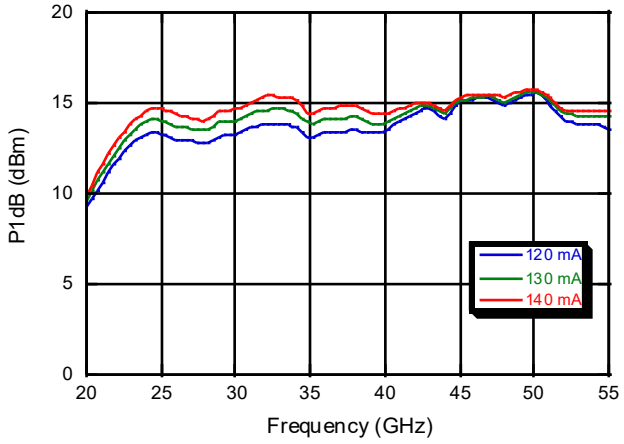
P1dB



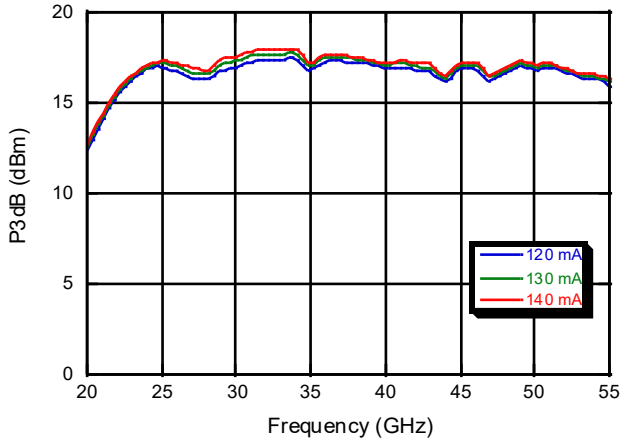
P3dB



P1dB



P3dB

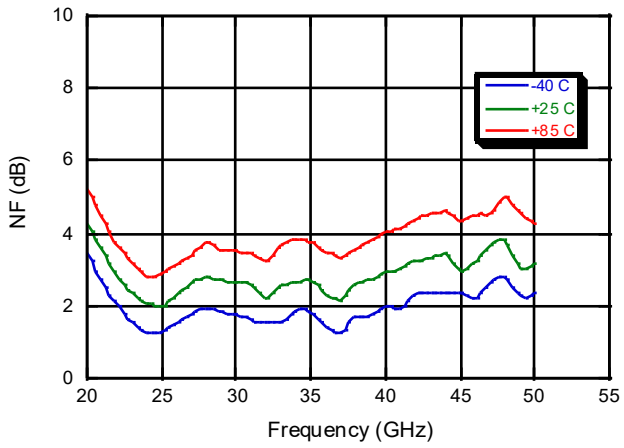


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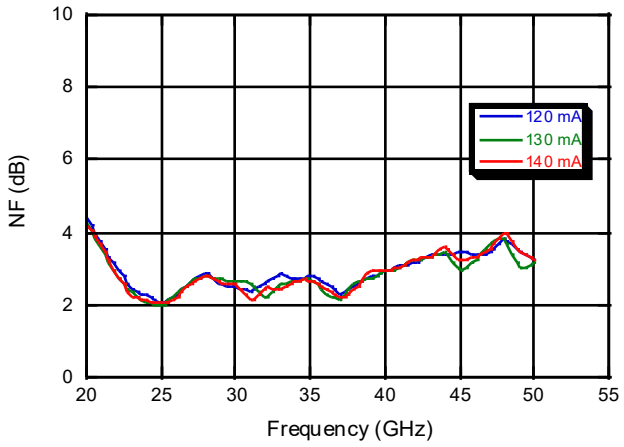
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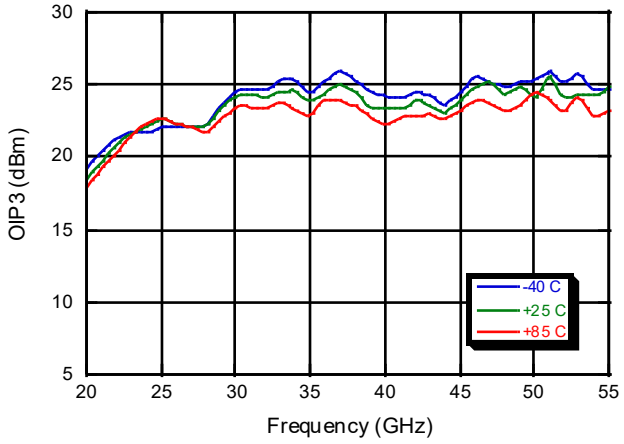
Noise Figure



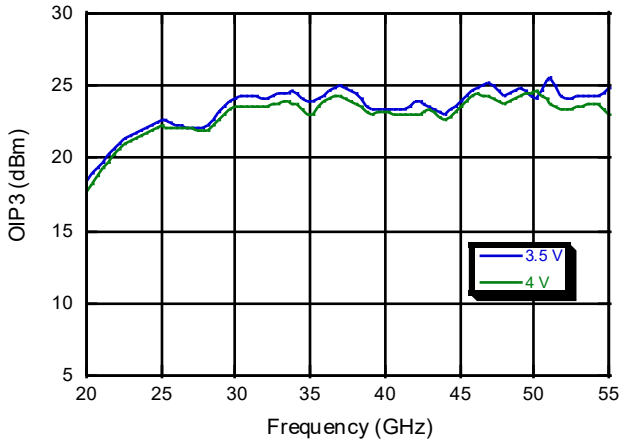
Noise Figure



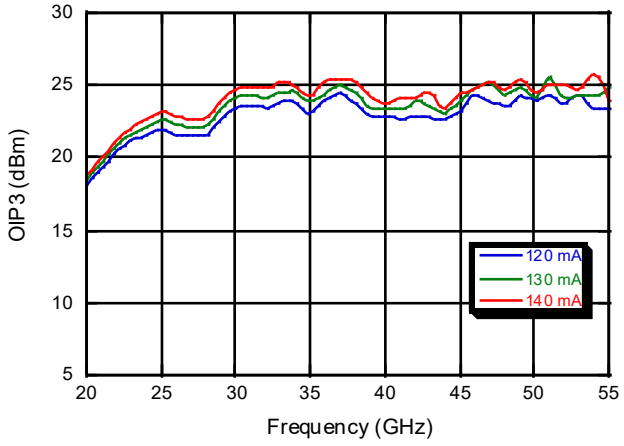
OIP3



OIP3



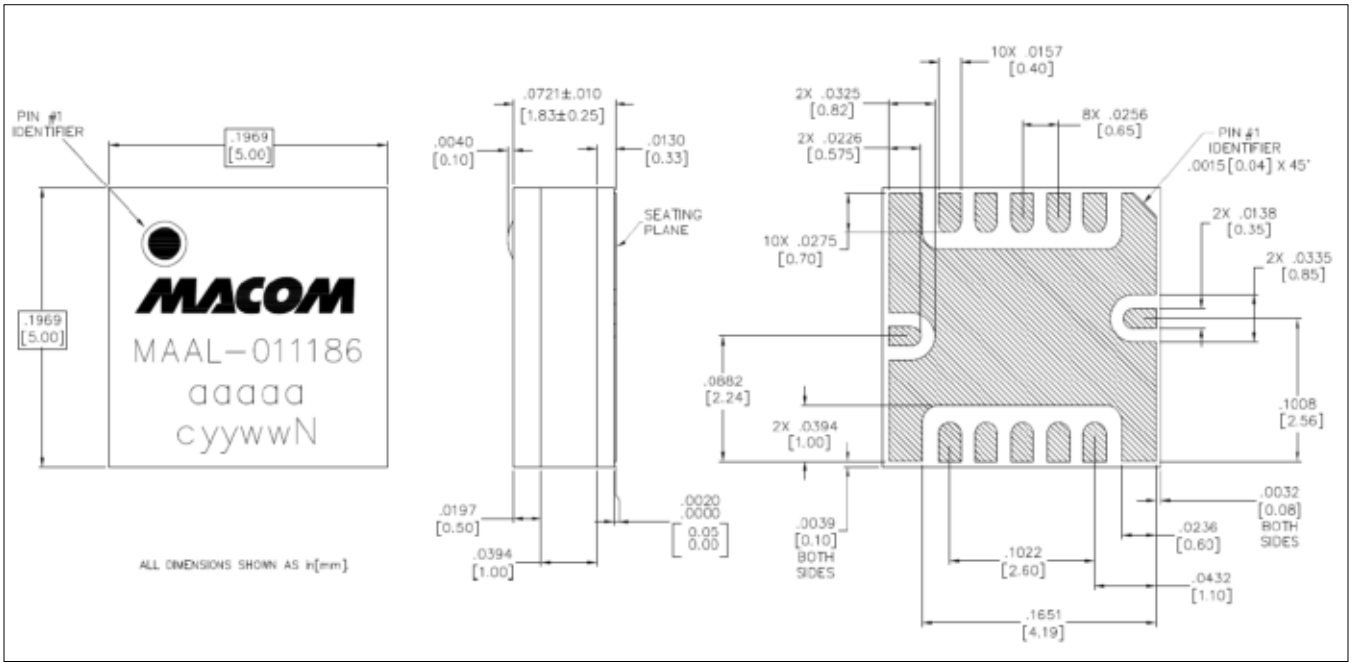
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Lead-Free 5 mm 12-Lead SMT[9,10,11,12,13]



9. All units in in [mm], unless otherwise noted, with a tolerance of .xxxx = ±.0005 in and .xxx = ±.005 in.
10. Lead finish: NiPdAu plating
11. Marking: line 2 part number; line 3 wafer lot number; line 4 c = country of origin (T = Thailand), yyww = date code, N = Nickel/Palladium/ Gold plating
12. Reference Application Note S2083 for lead-free solder reflow recommendations.
13. Meets JEDEC moisture sensitivity level 3 requirements.

Revision History

Rev	Date	Change Description
V4	Jan 2025	Update page 5 with new evaluation board drawing
V3	June 2025	Update page 3 reflect pin # for VR1 and VR2
V2	Oct 2023	Update evaluation board drawing on page 5 reflect correct sample board drawing.
V1	June 2022	Initial Release

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