maxim integrated™

MAX11209/MAX11211

18-Bit, Single-Channel, Ultra-Low-Power, Delta-Sigma ADCs with Programmable Gain and GPIO

General Description

The MAX11209/MAX11211 are ultra-low-power (< 300µA active current), high-resolution, serial-output ADCs. These devices provide the highest resolution per unit power in the industry, and are optimized for applications that require very high dynamic range with low power, such as sensors on a 4mA to 20mA industrial control loop. Optional input buffers provide isolation of the signal inputs from the switched capacitor sampling network allowing these converters to be used with high-impedance sources without compromising available dynamic range or linearity. The devices provide a high-accuracy internal oscillator that requires no external components. When used with the specified data rates, the internal digital filter provides more than 100dB rejection of 50Hz or 60Hz line noise. The devices are configurable using the SPI™ interface and include four GPIOs that can be used for external mux control. The MAX11209 includes digital programmable gain of 1 to 128.

The MAX11209/MAX11211 operate over the -40°C to +85°C temperature range, and are available in a 16-pin QSOP package.

Applications

Sensor Measurement (Temperature and Pressure)

Portable Instrumentation

Battery Applications

Weigh Scales

SPI and QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **18-Bit Noise-Free Resolution**
- **570nV$_{RMS}$ Noise at 10sps, ±3.6V$_{FS}$ Input**
- **3ppm INL (typ), 15ppm (max)**
- **No Missing Codes**
- **Ultra-Low Power Dissipation**
  Operating-Mode Current Drain < 300µA (max)
  Sleep-Mode Current Drain < 0.4µA
- **Programmable Gain (1 to 128) (MAX11209)**
- **Four SPI-Controlled GPIOs for External Mux Control**
- **2.7V to 3.6V Analog Supply Voltage Range**
- **1.7V to 3.6V Digital and I/O Supply Voltage Range**
- **Fully Differential Signal and Reference Inputs**
- **High-Impedance Inputs**
  Optional Input Buffers on Both Signal and Reference Inputs
- **> 100dB (min) 50Hz/60Hz Rejection**
- **SPI-, QSPI™-, MICROWIRE™-Compatible Serial Interface**
- **On-Demand Offset and Gain Self-Calibration and System Calibration**
- **User-Programmable Offset and Gain Registers**
- **-40°C to +85°C Operating Temperature Range**
- **±2kV ESD Protection**
- **Lead(Pb)-Free and RoHS-Compliant QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11209EEE+	-40°C to +85°C	16 QSOP
MAX11211EEE+	-40°C to +85°C	16 QSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Selector Guide

RESOLUTION (BITS)	4-WIRE SPI, 16-PIN QSOP, PROGRAMMABLE GAIN	4-WIRE SPI, 16-PIN QSOP	2-WIRE SERIAL, 10-PIN µMAX
24	MAX11210	MAX11200	MAX11201 (with buffers) MAX11202 (without buffers)
20	MAX11206	MAX11207	MAX11208
18	MAX11209	MAX11211	MAX11212
16	MAX11213	MAX11203	MAX11205

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5473; Rev 0; 8/10

ABSOLUTE MAXIMUM RATINGS

Any Pin to GND .....-0.3V to +3.9V
AVDD to GND.....-0.3V to +3.9V
DVDD to GND .....-0.3V to +3.9V
Analog Inputs (AINP, AINN, REFP, REFN)
to GND ..... -0.3V to (V_{AVDD} + 0.3V)
Digital Inputs and Digital Outputs
to GND ..... -0.3V to (V_{DVDD} + 0.3V)
ESD_{HB} (AVDD, AINP, AINN, REFP, REFN, DVDD, CLK, $\overline{CS}$, SCLK, DIN, $\overline{RDY}$/DOUT, GND, GPIO_) ..... ±2kV (Note 1)
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Human Body Model to specification MIL-STD-883 Method 3015.7.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = +3.6V, V_{DVDD} = +1.7V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, single-cycle mode (SCYCLE = 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Noise-Free Resolution (Notes 2, 3)	NFR	120sps		18		Bits
		10sps		18		
Noise (Notes 2, 3)	V_N	120sps		2.1		μV_{RMS}
		10sps		0.55		
Integral Nonlinearity	INL	At 10sps (Note 4)	-15		+15	ppmFSR
Zero Error		After self and system calibration, V_{REFP} - V_{REFN} = 2.5V	-15		+15	ppmFSR
Zero Drift				50		nV/°C
Full-Scale Error		After self and system calibration, V_{REFP} - V_{REFN} = 2.5V (Note 5)	-20		+20	ppmFSR
Full-Scale Error Drift				0.05		ppmFSR/°C
Power-Supply Rejection		AVDD DC rejection	70	80		dB
		DVDD DC rejection	90	100		
ANALOG INPUTS/REFERENCE INPUTS						
Common-Mode Rejection	CMR	DC rejection	90	123		dB
		50Hz/60Hz rejection at 120sps	90			
		50Hz/60Hz rejection at 1sps to 15sps	144			
Normal-Mode 50Hz Rejection	NMR_{50}	LINEF = 1, for 1sps to 15sps (Notes 6, 7)	100	144		dB
Normal-Mode 60Hz Rejection	NMR_{60}	LINEF = 0, for 1sps to 15sps (Notes 6, 7)	100	144		dB
Common-Mode Voltage Range		AIN buffers disabled	V_{GND}		V_{AVDD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +3.6V, V_{DVDD} = +1.7V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, single-cycle mode (SCYCLE = 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Absolute Input Voltage		Low input voltage	Buffers disabled		V_{GND} - 30mV		V
			Buffers enabled		V_{GND} + 100mV		
		High input voltage	Buffers disabled		V_{AVDD} + 30mV		
			Buffers enabled		V_{AVDD} - 100mV		
DC Input Leakage		Sleep mode			±1		µA
AIN Dynamic Input Current		Buffer disabled			±1.4		µA/V
		Buffer enabled			±20		nA
REF Dynamic Input Current		Buffer disabled			±2.1		µA/V
		Buffer enabled			±30		nA
AIN Input Capacitance		Buffer disabled			5		pF
REF Input Capacitance		Buffer disabled			7.5		pF
AIN Voltage Range		Unipolar		0		V_{REF}	V
		Bipolar		$-V_{REF}$		$+V_{REF}$	
Input Sampling Rate	f_S	LINEF = 0			246		kHz
		LINEF = 1			204.8		
REF Voltage Range		Buffers disabled		0		V_{AVDD}	V
		Buffers enabled		0.1		V_{AVDD} - 0.1	
REF Sampling Rate		LINEF = 0			246		kHz
		LINEF = 1			204.8		
LOGIC INPUTS (SCLK, CLK, DIN, GPIO1–GPIO4)							
Input Current		Input leakage current			±1		µA
Input Low Voltage	V_{IL}					0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}			0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}				200		mV
External Clock		60Hz line frequency			2.4576		MHz
		55Hz line frequency			2.25275		
		50Hz line frequency			2.048		
LOGIC OUTPUTS ($\overline{RDY}$/DOUT, GPIO1–GPIO4)							
Output Low Level	V_{OL}	I_{OL} = 1mA; also tested for V_{DVDD} = 3.6V				0.4	V
Output High Level	V_{OH}	I_{OH} = 1mA; also tested for V_{DVDD} = 3.6V		0.9 x V_{DVDD}			V
Leakage Current		High-impedance state			±500		nA
Output Capacitance		High-impedance state			9		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +3.6V, V_{DVDD} = +1.7V, V_{REFP} - V_{REFN} = V_{AVDD}; internal clock, single-cycle mode (SCYCLE = 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

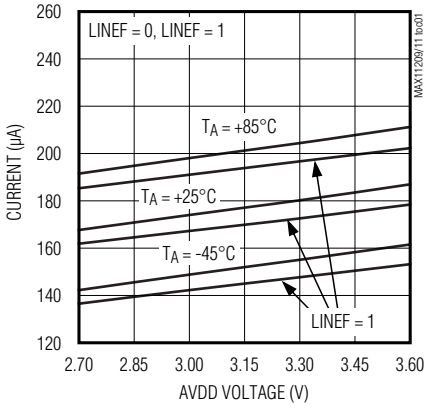
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Analog Supply	V_{AVDD}			2.7		3.6	V
Digital Supply	V_{DVDD}			1.7		3.6	V
Total Operating Current		AVDD + DVDD	Buffers disabled		235	300	µA
			Buffers enabled		255		
AVDD Sleep Current					0.15	2	µA
AVDD Operating Current		Buffers disabled			185	235	µA
		Buffers enabled			205		
DVDD Sleep Current					0.25	2	µA
DVDD Operating Current					50	65	µA
SPI TIMING CHARACTERISTICS							
SCLK Frequency	f_{SCLK}					5	MHz
SCLK Clock Period	t_{CP}			200			ns
SCLK Pulse-Width High	t_{CH}			80			ns
SCLK Pulse-Width Low	t_{CL}	60% duty cycle at 5MHz		80			ns
$\overline{CS}$ Low to 1st SCLK Rise Setup	t_{CSS0}			40			ns
$\overline{CS}$ High to 17th SCLK Setup	t_{CSS1}			40			ns
$\overline{CS}$ High After 16th SCLK Falling Edge Hold	t_{CSH1}			3			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}			40			ns
DIN to SCLK Setup	t_{DS}			40			ns
DIN Hold After SCLK	t_{DH}			0			ns
$\overline{RDY}$/DOUT Transition Valid After SCLK Fall	t_{DOT}	Output transition time, data changes on falling edge of SCLK				40	ns
$\overline{RDY}$/DOUT Remains Valid After SCLK Fall	t_{DOH}	Output hold time allows for negative edge data read		3			ns
$\overline{RDY}$/DOUT Valid Before SCLK Rise	t_{DOL}	t_{DOL} = t_{CL} - t_{DOT}		40			ns
$\overline{CS}$ Rise to $\overline{RDY}$/DOUT Disable	t_{DOD}	C_{LOAD} = 20pF				25	ns
$\overline{CS}$ Fall to $\overline{RDY}$/DOUT Valid	t_{DOE}	Default value of $\overline{RDY}$ is 1 for minimum specification; maximum specification for valid 0 on $\overline{RDY}$/DOUT		0		40	ns
DATA Fetch	t_{DF}	Maximum time after $\overline{RDY}$ asserts to read DATA register; t_{CNV} is the time for one conversion		0		t_{CNV} - 60 x t_{CP}	

Note 2: These specifications are not fully tested and are guaranteed by design and/or characterization.
Note 3: V_{AINP} = V_{AINN}.
Note 4: ppmFSR is parts per million of full scale.
Note 5: Positive full-scale error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges.
Note 6: For data rates (1, 2.5, 5, 10, 15)sps and (0.83, 2.08, 4.17, 8.33, 12.5)sps.
Note 7: Normal-mode rejection of power line frequencies of 60Hz/50Hz apply only for single-cycle data rates at 15sps/10sps and lower or continuous data rate of 60sps/50sps.

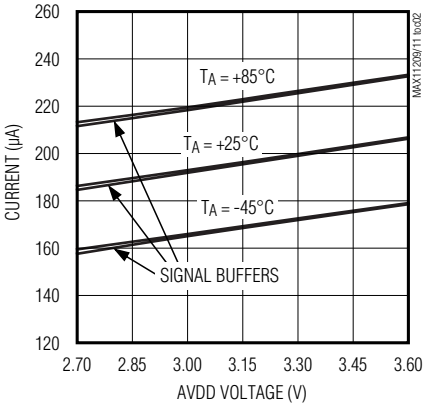
Typical Operating Characteristics

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = 2.5V; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

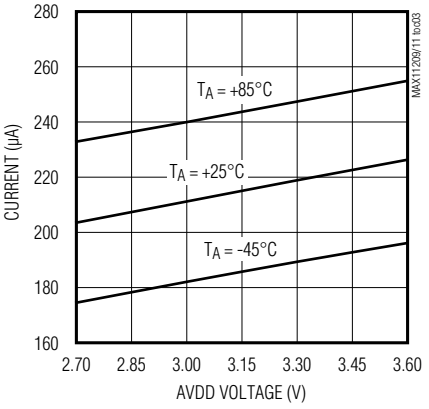
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (NO BUFFERS ENABLED)



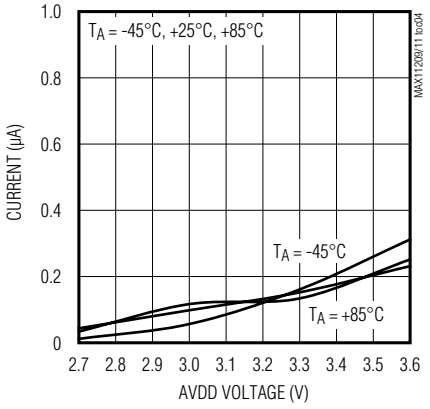
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (SIGNAL OR REFERENCE BUFFERS ENABLED)



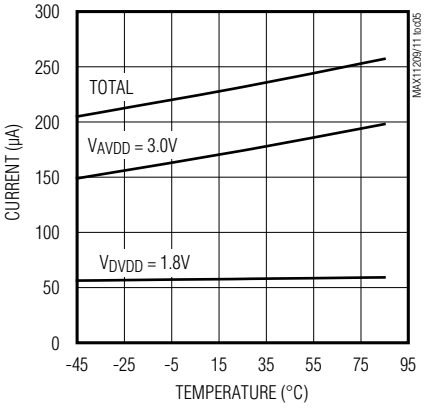
ANALOG ACTIVE CURRENT vs. AVDD VOLTAGE (SIGNAL AND REFERENCE BUFFERS ENABLED)



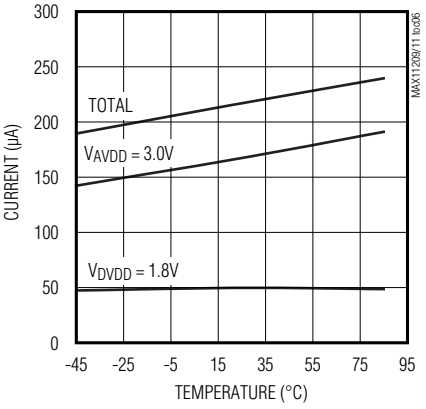
ANALOG SLEEP CURRENT vs. AVDD VOLTAGE



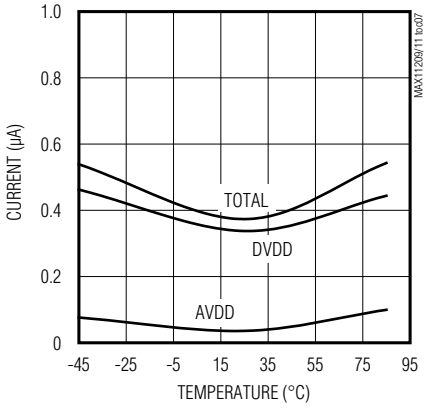
ACTIVE SUPPLY CURRENT vs. TEMPERATURE (LINEF = 0)



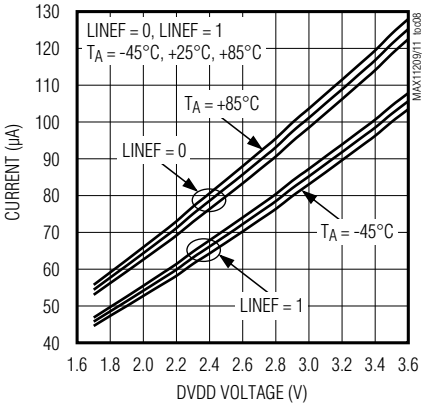
ACTIVE SUPPLY CURRENT vs. TEMPERATURE (LINEF = 1)



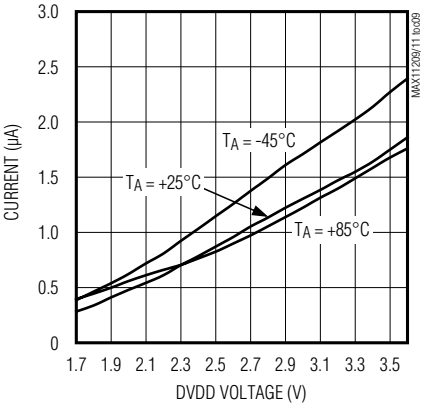
SLEEP CURRENT vs. TEMPERATURE



DIGITAL ACTIVE CURRENT vs. DVDD VOLTAGE



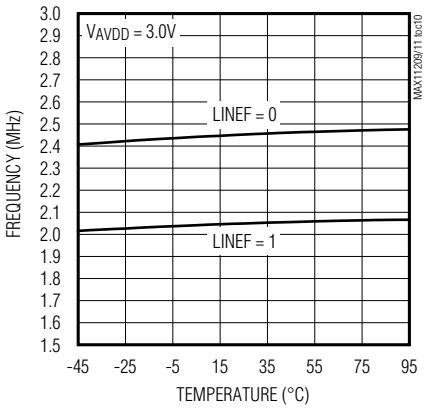
DIGITAL SLEEP CURRENT vs. DVDD VOLTAGE



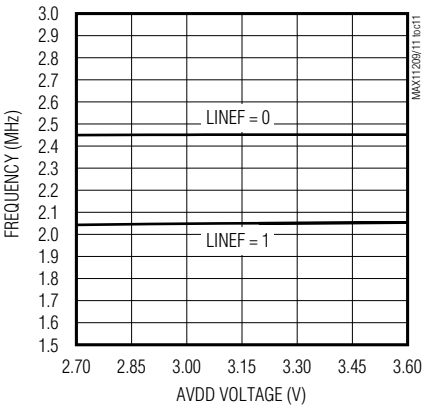
Typical Operating Characteristics (continued)

(V_{AVDD} = 3.6V, V_{DVDD} = 1.8V, V_{REFP} - V_{REFN} = 2.5V; internal clock; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

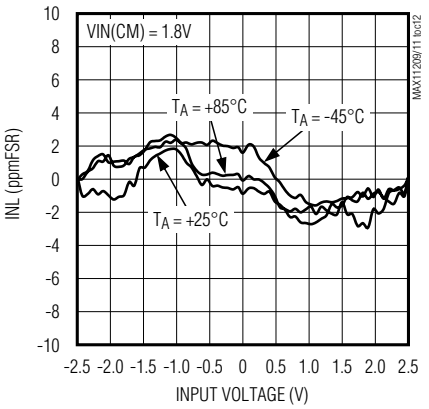
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



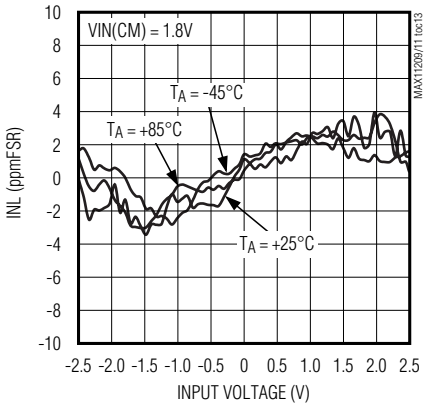
INTERNAL OSCILLATOR FREQUENCY vs. AVDD VOLTAGE



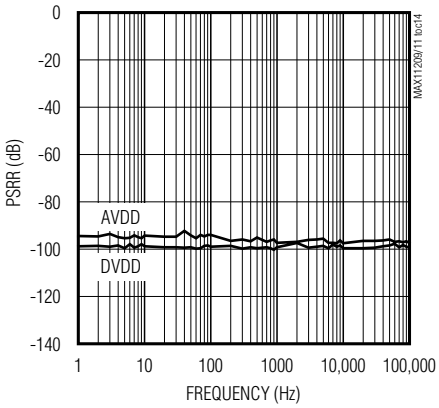
INTEGRAL NONLINEARITY vs. INPUT VOLTAGE



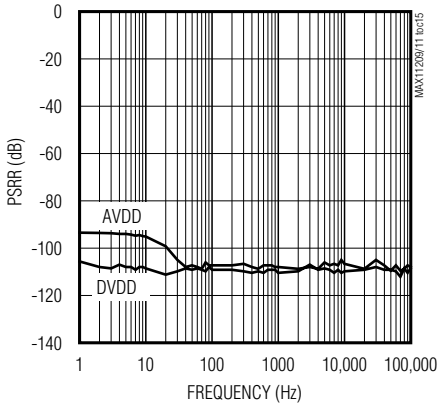
TUE vs. INPUT VOLTAGE



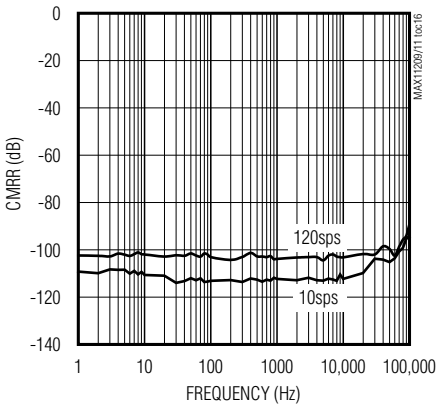
PSRR vs. FREQUENCY (DATA RATE 120sps)



PSRR vs. FREQUENCY (DATA RATE 10sps)

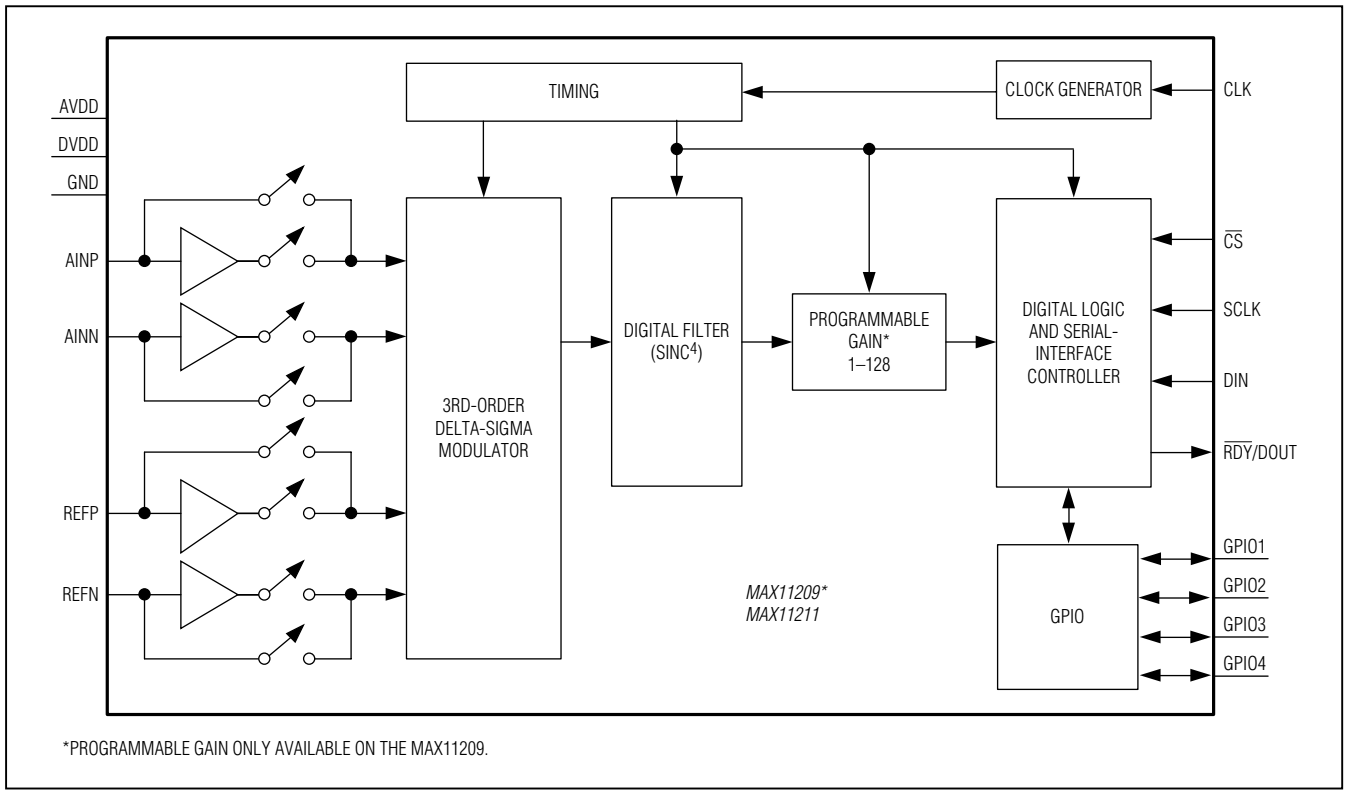


CMRR vs. FREQUENCY

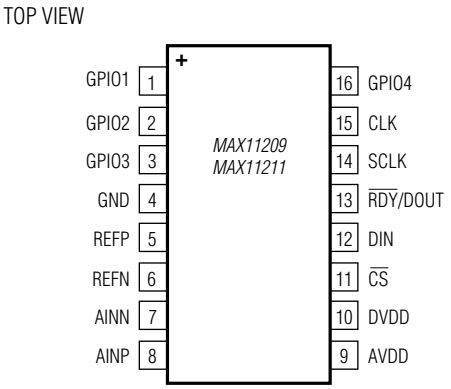


18-Bit, Single-Channel, Ultra-Low-Power, Delta-Sigma ADCs with Programmable Gain and GPIO

Functional Diagram



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	GPIO1	General-Purpose I/O 1. Register controllable using SPI.
2	GPIO2	General-Purpose I/O 2. Register controllable using SPI.
3	GPIO3	General-Purpose I/O 3. Register controllable using SPI.
4	GND	Ground. Ground reference for analog and digital circuitry.
5	REFP	Differential Reference Positive Input. REFP must be more positive than REFN. Connect REFP to a voltage between AVDD and GND.
6	REFN	Differential Reference Negative Input. REFN must be more negative than REFP. Connect REFN to a voltage between AVDD and GND.
7	AINN	Negative Fully Differential Analog Input
8	AINP	Positive Fully Differential Analog Input
9	AVDD	Analog Supply Voltage. Connect a supply voltage between +2.7V and +3.6V with respect to GND.
10	DVDD	Digital Supply Voltage. Connect a digital supply voltage between +1.7V and +3.6V with respect to GND.
11	$\overline{CS}$	Active-Low, Chip-Select Logic Input
12	DIN	Serial-Data Input. Data present at DIN is shifted to the device's internal registers at the rising edge of the serial clock at SCLK, when the device is accessed for an internal register write or for a command operation.
13	$\overline{RDY}$/DOUT	Data Ready Output/Serial-Data Output. This output serves a dual function. In addition to the serial-data output function, the $\overline{RDY}$/DOUT also indicates that the data is ready when the $\overline{RDY}$ is logic-low. $\overline{RDY}$/DOUT changes on the falling edge of SCLK.
14	SCLK	Serial-Clock Input. Apply an external serial clock to SCLK.
15	CLK	External Clock Signal Input. When external clock mode is selected (EXTCLK = 1), provide a 2.4576MHz or 2.048MHz clock signal at CLK. Other frequencies can be used, but the data rate and digital filter notch frequencies scale accordingly.
16	GPIO4	General-Purpose I/O 4. Register controllable using SPI.

Detailed Description

The MAX11209/MAX11211 are ultra-low-power (< 300µA active), high-resolution, low-speed, serial-output ADCs. These ADCs provide the highest resolution per unit power in the industry, and are optimized for applications that require very high dynamic range with low power such as sensors on a 4mA to 20mA industrial control loop. Optional input buffers provide isolation of the signal inputs from the switched capacitor sampling network, allowing the devices to be used with very high impedance sources without compromising available dynamic range. The devices provide a high-accuracy internal oscillator, which requires no external components. When used with the specified data rates, the internal digital filter provides more than 144dB rejection of 50Hz or 60Hz line noise. The devices are highly configurable using the SPI interface and include four GPIOs for external mux control.

Analog Inputs

The devices accept two analog inputs (AINP, AINN) in buffered or unbuffered mode. The input buffer isolates the inputs from the capacitive load presented by the modulator, allowing for high source-impedance analog transducers. The value of the SIGBUF bit in the CTRL1 register determines whether the input buffer is enabled or disabled. See Table 12.

Input Voltage Range

The modulator input range is programmable for bipolar ($-V_{REF}$ to $+V_{REF}$) or unipolar (0 to V_{REF}) ranges. The $U/\overline{B}$ bit in the CTRL1 register configures the MAX11209/MAX11211 for unipolar or bipolar transfer functions. See Table 12.

System Clock

The devices incorporate a highly stable internal oscillator that provides the system clock. The system clock runs the internal state machine and is trimmed to 2.4576MHz or 2.048MHz. The internal oscillator clock is divided down to run the digital and analog timing. The LINEF bit in the CTRL1 register determines the internal oscillator frequency. See Tables 10 and 12. Set LINEF = 0 to select the 2.4576MHz oscillator and LINEF = 1 to select the

Table 1. Continuous Conversion with SCYCLE Bit = 0

RATE[2:0]	DATA RATE* (sps)		BIPOLAR NFR (BITS)	BIPOLAR ENOB (BITS)	UNIPOLAR NFR (BITS)	UNIPOLAR ENOB (BITS)	OUTPUT NOISE (μV_{RMS})
	LINEF = 0	LINEF = 1					
100	60	50	18.0	18.0	18.0	18.0	0.74
101	120	100	18.0	18.0	18.0	18.0	1.03
110	240	200	18.0	18.0	18.0	18.0	1.45
111	480	400	18.0	18.0	18.0	18.0	2.21

**LINEF = 0 sets the clock frequency to 2.4576MHz and the input sampling frequency to 245.76kHz. LINEF bit = 1 sets the clock frequency to 2.048MHz and the input sampling frequency to 204.8kHz.*

Table 2. Single-Cycle Conversion with SCYCLE Bit = 1

RATE[2:0]	SINGLE-CYCLE DATA RATE* (sps)		BIPOLAR NFR (BITS)	BIPOLAR ENOB (BITS)	UNIPOLAR NFR (BITS)	UNIPOLAR ENOB (BITS)	OUTPUT NOISE (μV_{RMS})
	LINEF = 0	LINEF = 1					
000	1	0.833	18.0	18.0	18.0	18.0	0.21
001	2.5	2.08	18.0	18.0	18.0	18.0	0.27
010	5	4.17	18.0	18.0	18.0	18.0	0.39
011	10	8.33	18.0	18.0	18.0	18.0	0.55
100	15	12.5	18.0	18.0	18.0	18.0	0.74
101	30	25	18.0	18.0	18.0	18.0	1.03
110	60	50	18.0	18.0	18.0	18.0	1.45
111	120	100	18.0	18.0	18.0	18.0	2.21

**LINEF = 0 sets the clock frequency to 2.4576MHz and the input sampling frequency to 245.76kHz. LINEF bit = 1 sets the clock frequency to 2.048MHz and the input sampling frequency to 204.8kHz.*

2.048MHz oscillator. The 2.4576MHz oscillator provides maximum 60Hz rejection, and the 2.048MHz oscillator provides maximum 50Hz rejection. See Figures 1 and 2. For optimal simultaneous 50Hz and 60Hz rejection, apply a 2.25275MHz external clock at CLK.

Reference

The devices provide differential inputs REFP and REFN for an external reference voltage. Connect the external reference directly across the REFP and REFN to obtain the differential reference voltage. The common-mode voltage range for V_{REFP} and V_{REFN} is between 0 and V_{AVDD}.

The devices accept reference inputs in buffered or unbuffered mode. The value of the REFBUF bit in the CTRL1 register determines whether the reference buffer is enabled or disabled. See Table 12.

Buffers

The devices include reference and signal input buffers capable of reducing the average input current from 2.1µA/V on the reference inputs and from 1.4µA/V on the analog inputs to a constant 30nA current on the reference inputs and 20nA current on the analog inputs. The reference and signal input buffers can be selected individually by programming the CTRL1 register bits REFBUF and SIGBUF. When enabled, the reference and input signal buffers require an additional 20µA from the AVDD supply pin.

Power-On Reset (POR)

The devices utilize power-on reset (POR) supply-monitoring circuitry on both the digital supply (DVDD) and the analog supply (AVDD). The POR circuitry ensures proper device default conditions after either a digital or analog power sequencing event. The digital POR trigger threshold is approximately 1.2V and has 100mV of hysteresis. The analog POR trigger threshold is approximately 1.25V and has 100mV of hysteresis. Both POR circuits have lowpass filters that prevent high-frequency supply glitches from triggering the POR.

Calibration

The devices provide two sets of calibration registers which offer the user several options for calibrating their system. The calibration register value defaults are all zero, which require a user to either perform a calibration or program the register through the SPI interface to use them. The on-chip calibration registers are enabled or disabled by programming the NOSYSG, NOSYSO, NOSCG, and NOSCO bits in the CTRL3 register. The default values for these calibration control bits are 1, which disables the use of the internal calibration registers.

The devices power up with the internal calibration registers disabled, and therefore a full-scale input produces a result of 60% of the full-scale digital range. To use the full-scale digital range a calibration must be performed.

The first level of calibration is the self-calibration where the part performs the required connections to zero and full-scale internally. This level of calibration is typically sufficient for 1µV of offset accuracy and 2ppm of full-scale accuracy. The self-calibration routine does not include the source resistance effects from the signal source driving the input pins, which can change the offset and gain of the system.

A second level of calibration is available where the user can calibrate a system zero scale and system full scale by presenting a zero-scale signal or a full-scale signal to the input pins and initiating a system zero scale or system gain calibration command.

A third level of calibration allows for the user to write to the internal calibration registers through the SPI interface to achieve any digital offset or scaling the user requires with the following restrictions. The range of digital offset correction is $\pm V_{REF}/4$. The range of digital gain correction is from 0.5 to 1.5. The resolution of offset correction is 0.5 LSB.

The calibration operations are controlled with the CAL1 and CAL0 bits in the command byte. The user requests a self-calibration by setting the CAL1 bit to 0 and CAL0 bit to 1. A self-calibration requires 200ms to complete, and both the SCOC and SCGC registers contain the values that correct the chip output for zero scale and full scale. The user requests a system zero-scale calibration by setting the CAL1 bit to 1 and the CAL0 bit to 0 and presents a system zero-level signal to the input pins. The SOC register contains the values that correct the chip zero scale. The system zero calibration requires 100ms to complete, and the SOC register contains values that correct the chip zero scale. The user requests a system full-scale calibration by setting the CAL1 bit to 1 and the CAL0 bit to 1 and presents a system full-scale signal level to the input pins. The system full-scale calibration requires 100ms to complete, and the SGC register contains values that correct for the chip full-scale value. See Tables 3a and 3b for an example of a self-calibration sequence and a system calibration sequence.

Table 3a. Example of Self-Calibration

STEP	DESCRIPTION	REGISTER				BIT			
		SCOC	SCGC	SOC	SGC	NOSYSG	NOSYSO	NOSCG	NOSCO
1	Initial power-up	0x000000	0x000000	0x000000	0x000000	1	1	1	1
2	Enable self-calibration registers	0x000000	0x000000	0x000000	0x000000	1	1	0	0
3	Self-calibration, DIN = 10010000	0x00007E	0xBFD345	0x000000	0x000000	1	1	0	0

Table 3b. Example of System Calibration

STEP	DESCRIPTION	REGISTER				BIT			
		SCOC	SCGC	SOC	SGC	NOSYSG	NOSYSO	NOSCG	NOSCO
1	Initial power-up	0x000000	0x000000	0x000000	0x000000	1	1	1	1
2	Enable self-calibration registers	0x000000	0x000000	0x000000	0x000000	1	1	0	0
3	Self-calibration, DIN = 10010000	0x00007E	0xBFD345	0x000000	0x000000	1	1	0	0
4	Enable system offset register	0x00007E	0xBFD345	0x000000	0x000000	1	0	0	0
5	System-calibration offset, DIN = 1010000	0x00007E	0xBFD345	0xFFEE1D	0x000000	1	0	0	0
6	Enable system gain register	0x00007E	0xBFD345	0xFFEE1D	0x000000	0	0	0	0
7	System-calibration gain, DIN = 1011000	0x00007E	0xBFD345	0xFFEE1D	0x81CB5B	0	0	0	0

Noise vs. Data Rate

The devices offer software-selectable internal oscillator frequencies as well as software-selectable output data rates. The LINEF bit in the CTRL1 register (Table 12) determines the internal oscillator frequency. The RATE bits in the command byte (Table 8) determine the ADC's output data rate. The devices also offer the option of running in zero latency single-cycle conversion mode (Table 2) or continuous conversion mode (Table 1). Set SCYCLE = 0 in the CTRL1 register (Table 12) to run in continuous conversion mode and SCYCLE = 1 for single-cycle conversion mode.

Single-cycle conversion mode gives an output result with no data latency. The devices output data up to 100sps (2.048MHz internal oscillator) or 120sps (2.4576MHz internal oscillator) with no data latency. In continuous conversion mode, the output data rate is four times the single-cycle conversion mode, for sample rates up to 400sps or 480sps. In continuous conversion mode, the output data requires three additional 24-bit cycles to settle from an input step.

Digital Filter

The devices include a $SINC^4$ digital filter that produces spectral nulls at the multiples of the data rate. For all data rates less than 30sps, a spectral null occurs at the line frequency of 60Hz and is guaranteed to attenuate 60Hz normal-mode components by more than 100dB. Simultaneous 50Hz and 60Hz attenuation can be accomplished by using an external clock with a frequency of 2.25275MHz. This guarantees a minimum of 80dB rejection at 50Hz and 85dB rejection at 60Hz. The $SINC^4$ filter has a -3dB frequency equal to 24% of the data rate. See Figures 1 and 2.

GPIOs

The devices provide four GPIO ports. When set as outputs, these digital I/Os can be used to drive the digital inputs to a multiplexer or multichannel switch. Figure 3 details an example where four single-ended signals are multiplexed in a break-before-make switching sequence, using the MAX313, a quad SPST analog switch.

The devices' GPIO ports are configurable through the CTRL2 register. See Table 13. To select AIN1, write the command to CTRL2 according to Table 4a. This selects all GPIOs as outputs, as well as setting all logic signals to 0 except the selected channel AIN1.

To select channel AIN3 next, it is a good idea to set all switches to a high-impedance state first (see Table 4b).

Then select channel AIN3 by driving IN3 high (see Table 4c).

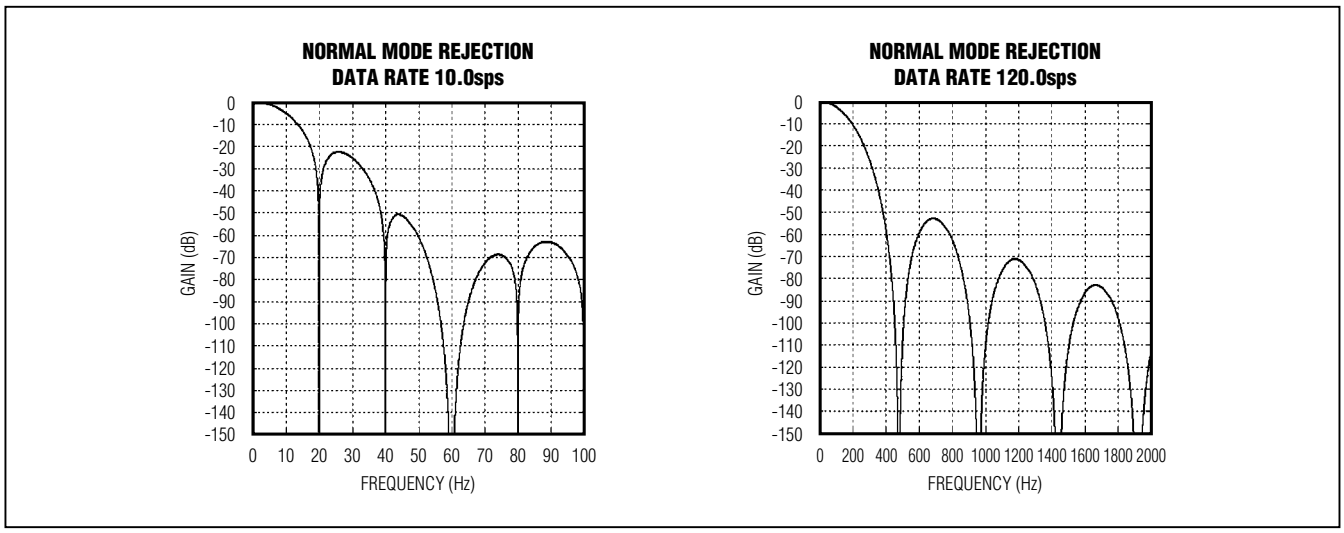


Figure 1. Normal-Mode Frequency Response (2.4576MHz Oscillator, LINEF = 0)

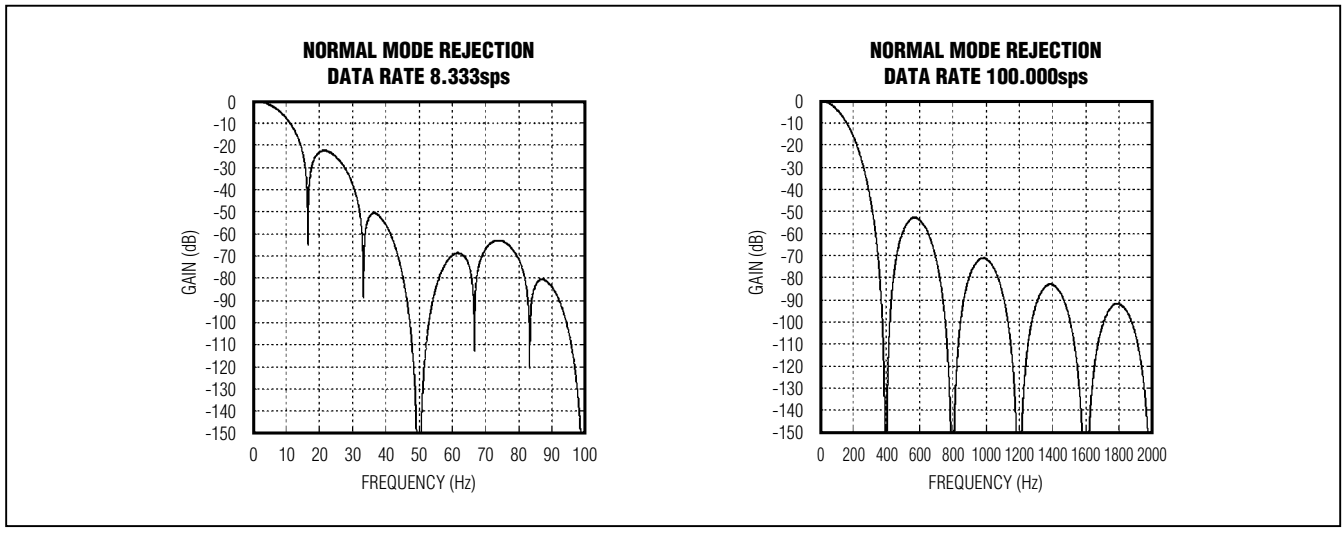


Figure 2. Normal-Mode Frequency Response (2.048MHz Oscillator, LINEF = 1)

Table 4a. Data Command to Select Channel AIN1 in Figure 3

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	DIR4	DIR3	DIR2	DIR1	DIO4	DIO3	DIO2	DIO1
VALUE	1	1	1	1	0	0	0	1

Table 4b. Set All Channels High Impedance in Figure 3

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	DIR4	DIR3	DIR2	DIR1	DIO4	DIO3	DIO2	DIO1
VALUE	1	1	1	1	0	0	0	0

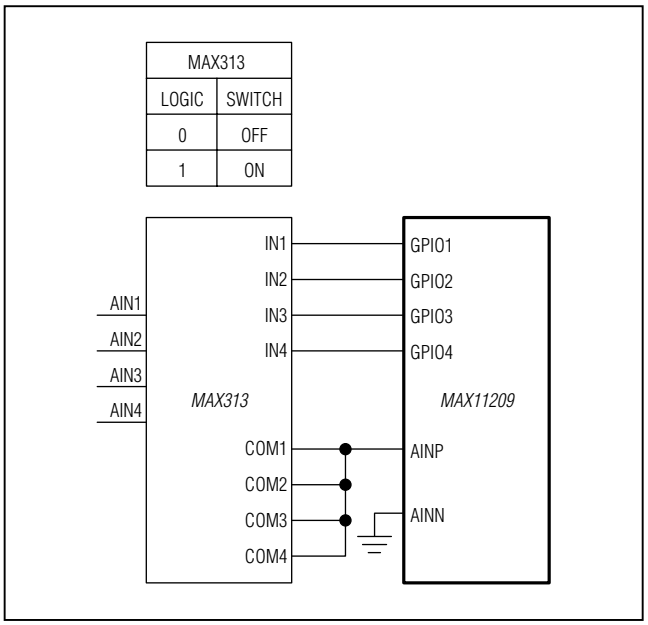


Figure 3. MAX11209 GPIOs Drive an External 4-Channel Switch (MAX313)

It is not always necessary to transition to a high-impedance state between channel selections, but depends on the source analog signals as well as the control structure of the multiplexed switches.

Digital Programmable Gain (MAX11209)

The MAX11209 offers programmable gain settings that can be digitally set to 1, 2, 4, 8, 16, 32, 64, or 128. The DGAIN_ bits in the CTRL3 register (see Table 14) configure the digital gain setting and control the input referred gain. The MAX11209's input range is 0V to V_{REF}/gain (unipolar) or ±V_{REF}/gain (bipolar). The MAX11209 always outputs 18 bits of data. But as this is a digital programmable gain, the noise floor remains constant, depending on the output rate setting. At an output rate of 10sps, as shown in Figure 4, the noise floor is such that all gain settings from 1 to 32 provide 18 bits of noise-free resolution. A gain setting of 128 at 10sps means the LSB is below the noise floor. The MAX11209 digital gain is beneficial for low-voltage applications that only require a small portion of the 0V to V_{REF} or ±V_{REF} ranges.

Table 4c. Data Command to Select Channel AIN3 in Figure 3

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	DIR4	DIR3	DIR2	DIR1	DIO4	DIO3	DIO2	DIO1
VALUE	1	1	1	1	0	1	0	0

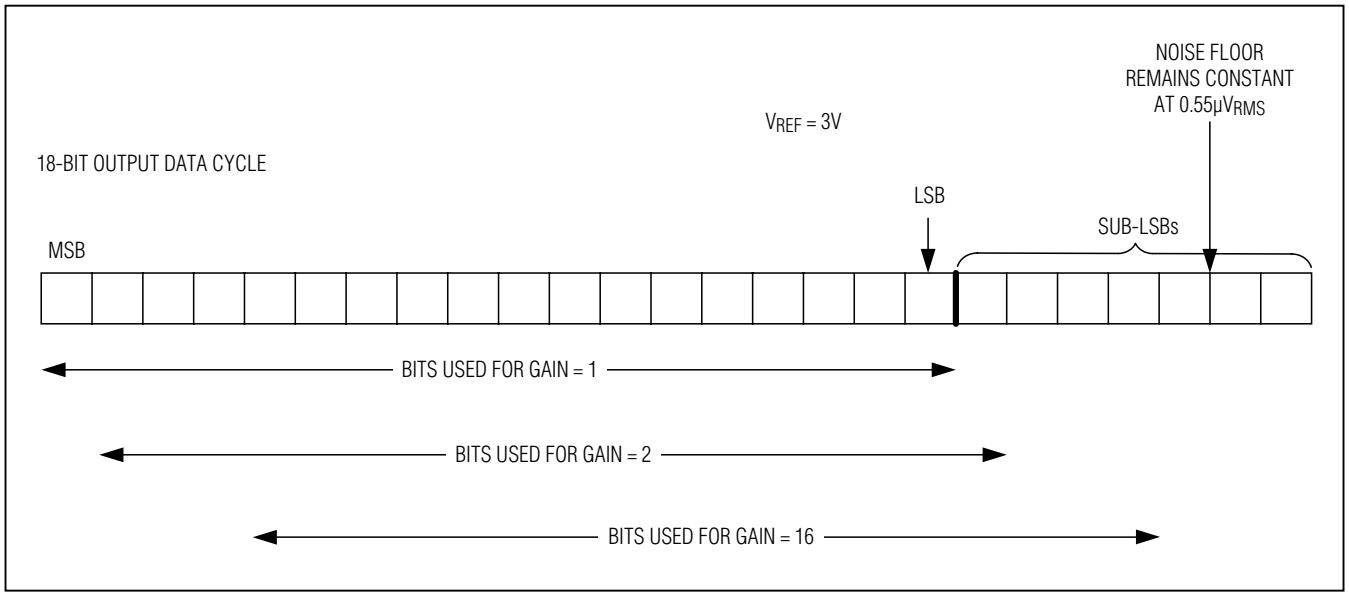


Figure 4. MAX11209 Digital Programmable Gain Example (10sps Output Rate)

Serial-Digital Interface

The MAX11209/MAX11211 interface is fully compatible with SPI-, QSPI-, and MICROWIRE-standard serial interfaces. The SPI interface provides access to nine on-chip registers that are 8 or 24 bits wide.

Drive $\overline{CS}$ low to transfer data in and out of the devices. Clock in data at DIN on the rising edge of SCLK. The $\overline{RDY}$/DOUT output serves two functions: conversion status and data read. To find the conversion status, assert $\overline{CS}$ low and read the $\overline{RDY}$/DOUT output; the conversion is in progress if the $\overline{RDY}$/DOUT output reads logic-high and the conversion is complete if the $\overline{RDY}$/DOUT output reads logic-low. Data at $\overline{RDY}$/DOUT changes on the falling edge of SCLK and is valid on the rising edge of SCLK. DIN and DOUT are transferred MSB first. Drive $\overline{CS}$ high to force DOUT high impedance and cause the devices to ignore any signals on SCLK and DIN. Connect $\overline{CS}$ low for 3-wire operation. Figures 5, 6, and 7 show the SPI timing diagrams.

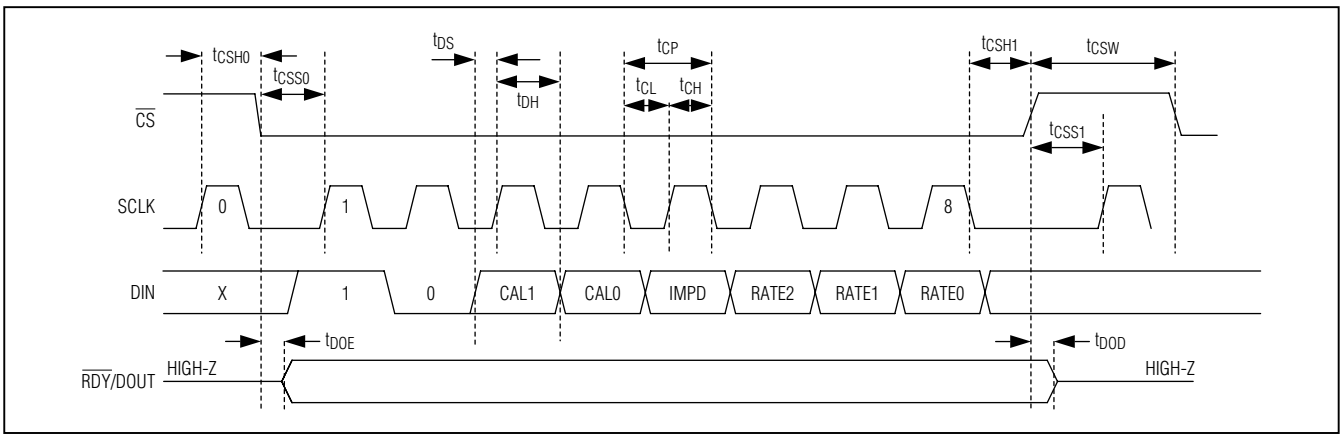


Figure 5. SPI Command Byte

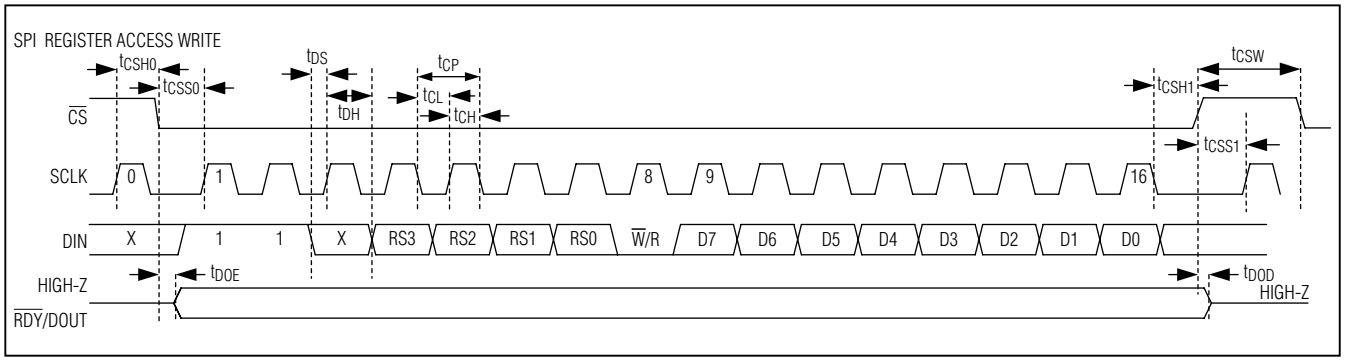


Figure 6. SPI Register Access Write

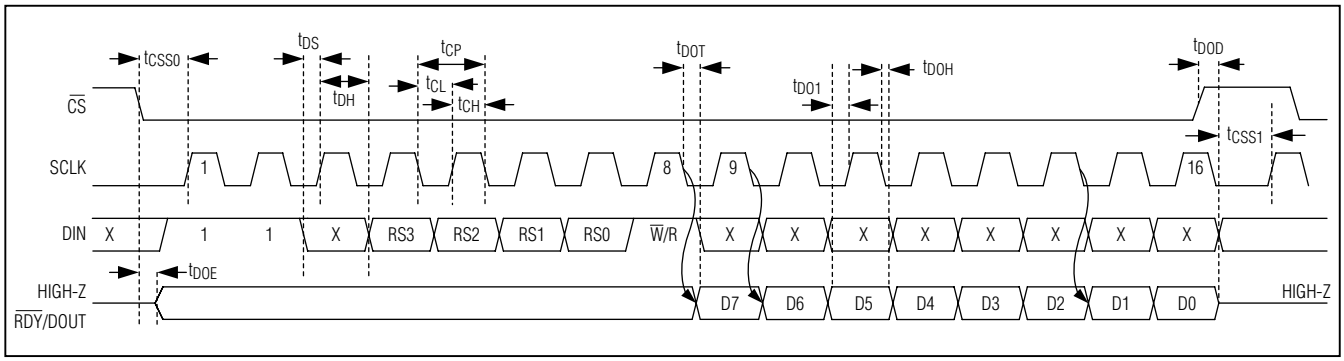


Figure 7. SPI Register Access Read

Command Byte

Communication between the user and the device is conducted through SPI using a command byte. The command byte consists of two modes differentiated as command modes and data modes. Command modes and data modes are further differentiated by decoding the remaining bits in the command byte. The mode selected is determined by the MODE bit. If the MODE bit is 0, then the user is requesting either a conversion, calibration, or power-down; see Table 5. If the MODE bit is 1, then the user is selecting a data command and can either read from or write to a register; see Table 6.

The Status register (STAT1) is a read-only register and provides general chip operational status to the user. If the user attempts to calibrate the system and overranges the internal signal scaling, then a gain overrange condition is flagged with the SYSOR bit. The last data rate programmed for the ADC is available in the RATE bits. If the input signal has exceeded positive or negative full scale, this condition is flagged with the OR and UR bits. If the modulator is busy converting, then the MSTAT bit is set. If a conversion result is ready for readout, the RDY bit is set; see Table 11.

The Control 1 register (CTRL1) is a read/write register, and the bits determine the internal oscillator frequency, unipolar or bipolar input range, selection of an internal or external clock, enabling or disabling the reference and input signal buffers, the output data format (offset binary or two's complement), and single-cycle or continuous conversion mode. See Table 12.

The Control 2 register (CTRL2) is a read/write register, and the bits configure the GPIOs as inputs or outputs and their values. See Table 13.

The Control 3 register (CTRL3) is a read/write register, and the bits determine the MAX11209 programmable gain setting and the calibration register settings for both the MAX11209 and MAX11211. See Table 14.

The Data register (DATA) is a read-only register. Data is output from RDY/DOUT on the next 24 SCLK cycles once CS is forced low. The data bits transition on the falling edge of SCLK. Data is output MSB first, and is offset binary or two's complement, depending on the setting of the FORMAT bit in the CTRL1 register. See Table 15.

The System Offset Calibration register (SOC) is a read/write register, and the bits contain the digital value that corrects the data for system zero scale. See Table 17.

The System Gain Calibration register (SGC) is a read/write register, and the bits contain the digital value that corrects the data for system full scale. See Table 18.

The Self-Cal Offset Calibration register (SCOC) is a read/write register, and the bits contain the value that corrects the data for chip zero scale. See Table 19.

The Self-Cal Gain Calibration register (SCGC) is a read/write register, and the bits contain the value that corrects the data for chip full scale. See Table 20.

Table 5. Command Byte (MODE = 0)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	START = 1	MODE = 0	CAL1	CAL0	IMPD	RATE2	RATE1	RATE0

Table 6. Command Byte (MODE = 1)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	START = 1	MODE = 1	0	RS3	RS2	RS1	RS0	W/R

Note: *The START bit is used to synchronize the data from the host device. The START bit is always 1.*

Table 7. Operating Mode (MODE Bit)

MODE BIT SETTING	OPERATING MODE
0	The command byte initiates a conversion or an immediate power-down. See Tables 5 and 8.
1	The device interprets the command byte as a register access byte, which is decoded as per Tables 6 and 9.

Table 8. Command Byte (MODE = 0, LINEF = 0)

COMMAND	START	MODE	CAL1	CAL0	IMPD	RATE2	RATE1	RATE0
Self-calibration cycle	1	0	0	1	0	0	0	0
System offset calibration cycle	1	0	1	0	0	0	0	0
System gain calibration	1	0	1	1	0	0	0	0
Immediate power-down	1	0	0	0	1	0	0	0
Convert 1sps	1	0	0	0	0	0	0	0
Convert 2.5sps	1	0	0	0	0	0	0	1
Convert 5sps	1	0	0	0	0	0	1	0
Convert 10sps	1	0	0	0	0	0	1	1
Convert 15sps	1	0	0	0	0	1	0	0
Convert 30sps	1	0	0	0	0	1	0	1
Convert 60sps	1	0	0	0	0	1	1	0
Convert 120sps	1	0	0	0	0	1	1	1

Table 9. Register Selection (MODE = 1)

RS3	RS2	RS1	RS0	REGISTER ACCESS	POWER-ON RESET STATUS	REGISTER SIZE (BITS)
0	0	0	0	STAT1	0x00	8
0	0	0	1	CTRL1	0x02	8
0	0	1	0	CTRL2	0x0F	8
0	0	1	1	CTRL3	0x1E	8
0	1	0	0	DATA	0x000000	24
0	1	0	1	SOC	0x000000	24
0	1	1	0	SGC	0x000000	24
0	1	1	1	SCOC	0x000000	24
1	0	0	0	SCGC	0x000000	24

Table 10. Register Address Map

REGISTER NAME	R/$\overline{W}$	ADDRESS SEL (RS[3:0])	B7	B6	B5	B4	B3	B2	B1	B0
STAT1	R	0x0	SYSOR	RATE2	RATE1	RATE0	OR	UR	MSTAT	RDY
CTRL1	R/$\overline{W}$	0x1	LINEF	U/$\overline{B}$	EXTCLK	REFBUF	SIGBUF	FORMAT	SCYCLE	RESERVED
CTRL2	R/$\overline{W}$	0x2	DIR4	DIR3	DIR2	DIR1	DIO4	DIO3	DIO2	DIO1
CTRL3	R/$\overline{W}$	0x3	DGAIN2*	DGAIN1*	DGAIN0*	NOSYSG	NOSYSO	NOSCG	NOSCO	RESERVED
DATA	R	0x4	D[17:16]							
			D[15:8]							
			D[7:0]							
SOC	R/$\overline{W}$	0x5	B[23:16]							
			B[15:8]							
			B[7:0]							
SGC	R/$\overline{W}$	0x6	B[23:16]							
			B[15:8]							
			B[7:0]							
SCOC	R/$\overline{W}$	0x7	B[23:16]							
			B[15:8]							
			B[7:0]							
SCGC	R/$\overline{W}$	0x8	B[23:16]							
			B[15:8]							
			B[7:0]							

**These DGAIN_ bits set the digital gain for the MAX11209 These bits are don't-care bits for the MAX11211.*

STAT1: Status Register

Table 11. STAT1 Register (Read Only)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	SYSOR	RATE2	RATE1	RATE0	OR	UR	MSTAT	RDY
DEFAULT	0	0	0	0	0	0	0	0

SYSOR: The system gain overrange bit, when set to 1, indicates that a system gain calibration was over range. The SCGC calibration coefficient is maximum value of 1.9999999. This bit, when set to 1, indicates that the full-scale value out of the converter is likely not available.

RATE[2:0]: The data rate bits indicate the conversion rate that corresponds to the result in the DATA register or the rate that was used for calibration coefficient calculation. If the previous conversions were done at a different rate, the RATE[2:0] bits indicate a rate different than the rate of the conversion in progress.

OR: The overrange bit, OR, is set to 1 to indicate the conversion result has exceeded the maximum value of the converter and that the result has been clipped or limited to the maximum value. The OR bit is set to 0 to indicate the conversion result is within the full-scale range of the device.

UR: The underrange bit, UR, is set to 1 to indicate the conversion result has exceeded the minimum value of the converter and that the result has been clipped or limited to the minimum value. The UR bit is set to 0 to indicate the conversion result is within the full-scale range of the device.

MSTAT: The measurement status bit, MSTAT is set to 1 when a signal measurement is in progress. When MSTAT = 1, a conversion, self-calibration, or system calibration is in progress and indicates that the modulator is busy. When the modulator is not converting, the MSTAT bit is set to 0.

RDY: The RDY ready bit is set to 1 to indicate that a conversion result is available. Reading the DATA register resets the RDY bit to 0 only after another conversion has been initiated. If the DATA has not been read before another conversion is initiated, the RDY bit remains 1; if the DATA is read before another conversion is initiated, the RDY bit resets to 0. If the DATA for the previous conversion is read during a following conversion, the RDY bit is reset immediately after the DATA read operation has completed.

CTRL1: Control 1 Register

The byte-wide CTRL1 register is a bidirectional read/write register. The byte written to the CTRL1 register indicates if the part converts continuously or single cycle, if an external or internal clock is used, if the reference and signal buffers are activated, the format of the data when in bipolar mode, and if the analog signal input range is unipolar or bipolar.

Table 12. CTRL1 Register (Read/Write)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	LINEF	U/$\overline{B}$	EXTCLK	REFBUF	SIGBUF	FORMAT	SCYCLE	UNUSED
DEFAULT	0	0	0	0	0	0	1	0

LINEF: Use the line frequency bit, LINEF, to select if the data rate is centered for 50Hz power mains or 60Hz power mains. To select data rates for 50Hz power mains, write 1 to LINEF and to select data rates for 60Hz power mains, write 0 to LINEF.

U/$\overline{B}$: The unipolar/bipolar bit, U/$\overline{B}$, selects if the input range is unipolar or bipolar. A 1 in this bit location selects a unipolar input range and a 0 selects a bipolar input range.

EXTCLK: The external clock bit, EXTCLK, controls the selection of the system clock. A 1 enables an external clock as system clock, whereas as a 0 enables the internal clock.

REFBUF: The reference buffer bit, REFBUF, enables/disables the reference buffers. A 1 enables the reference buffers. A 0 powers down the reference buffers and the reference inputs bypass the reference buffers when driving the ADC.

SIGBUF: The signal buffer, SIGBUF, enables/disables the signal buffers. A 1 enables the signal buffer. A 0 powers down the signal buffers and the analog signal inputs bypass the signal buffers when driving the ADC.

FORMAT: The format bit, FORMAT, controls the digital format of the data. Unipolar data is always in offset binary format. The bipolar format is two's complement if the FORMAT bit is set to 0 or offset binary if the FORMAT bit is set to 1.

SCYCLE: The single-cycle bit, SCYCLE, determines if the device runs in "no-latency" single-conversion mode (SCYCLE = 1) or if the device runs in "latent" continuous-conversion mode (SCYCLE = 0). When in single-cycle conversion mode, the device completes one no-latency conversion and then powers down into a leakage-only state. When in continuous-conversion mode, the part is continuously converting and the first three data from the part are incorrect due to the $SINC^4$ filter latency.

Important Note: When operating in continuous-conversion mode (SCYCLE = 0), it is recommended to keep $\overline{CS}$ low to properly detect the end of conversion. The end of conversion is signaled by $\overline{RDY}$/DOUT changing from 0 to 1. The transition of $\overline{RDY}$/DOUT from 0 to 1 must be used to synchronize the DATA register read back. If the $\overline{RDY}$/DOUT output is not used to synchronize the DATA read back, a timing hazard exists where the DATA register is updated internally after a conversion has completed simultaneously with the DATA register being read out, causing an incorrect read of DATA.

CTRL2: Control 2 Register

The byte-wide CTRL2 register is a bidirectional read/write register. The byte written to the CTRL2 register controls the direction and values of the digital I/O ports.

Table 13. CTRL2 Register (Read/Write)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	DIR4	DIR3	DIR2	DIR1	DIO4	DIO3	DIO2	DIO1
DEFAULT	0	0	0	0	1	1	1	1

DIR[4:1]: The direction bits configure the direction of the DIO bit. When a DIR bit is set to 0, the associated DIO bit is configured as an input and the value returned by a read of the DIO bit is the value being driven on the associated GPIO. When a DIR bit is set to 1, the associated DIO bit is configured as an output and the GPIO port is driven to a logic value of the associated DIO bit.

DIO[4:1]: The data input/output bits are bits associated with the GPIO ports. When a DIO is configured as an input, the value read from the DIO bit is the logic value being driven at the GPIO port. When the direction is configured as an output, the GPIO port is driven to a logic value associated with the DIO bit.

CTRL3: Control 3 Register

The byte-wide CTRL3 register is a bidirectional read/write register. The CTRL3 register controls the operation and calibration of the device.

Table 14. CTRL3 Register (Read/Write)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
BIT NAME	DGAIN2*	DGAIN1*	DGAIN0*	NOSYSG	NOSYSO	NOSCG	NOSCO	RESERVED
DEFAULT	0	0	0	1	1	1	1	0

**These DGAIN_ bits are don't-care bits for the MAX11209.*

DGAIN[2:0] (MAX11209 only): The digital gain bits control the input referred gain. With a gain of 1, the input range is 0 to V_{REF} (unipolar) or $\pm V_{REF}$ (bipolar). As the gain in increased by 2x, the input range is reduced to 0 to V_{REF}/gain or $\pm V_{REF}$/gain. Digital gain is applied to the final offset and gain-calibrated digital data. The DGAIN[2:0] bits decode to digital gains as follows:

000 = 1 100 = 16
001 = 2 101 = 32
010 = 4 110 = 64
011 = 8 111 = 128

NOSYSG: The no-system gain bit, NOSYSG, controls the system gain calibration coefficient. A 1 in this bit location disables the use of the system gain value when computing the final offset and gain corrected data value. A 0 in this location enables the use of the system gain value when computing the final offset and gain corrected data value.

NOSYSO: The no system offset bit, NOSYSO, controls the system offset calibration coefficient. A 1 in this location disables the use of the system offset value when computing the final offset and gain corrected data value. A 0 in this location enables the use of the system offset value when computing the final offset and gain corrected data value.

NOSCG: The no self-calibration gain bit, NOSCG, controls the self-calibration gain calibration coefficient. A 1 in this location disables the use of the self-calibration gain value when computing the final offset and gain corrected data value. A 0 in this location enables the use of the self-calibration gain value when computing the final offset and gain corrected data value.

NOSCO: The no self-calibration offset bit, NOSCO, controls the use of the self-calibration offset calibration coefficient. A 1 in this location disables the use of the self-calibration offset value when computing the final offset and gain corrected data value. A 0 in this location enables the use of the self-calibration offset value when computing the final offset and gain corrected data value.

DATA: Data Register

The data register is a 24-bit read-only register. Any attempt to write data to the data register has no effect. The data read from this register is clocked out MSB first. The data register holds the conversion result. D17 is the MSB, and D0 is the LSB. The result is stored in a format according to the FORMAT bit in the CTRL1 register.

The data format while in unipolar mode is always straight binary. In straight binary format, the most negative value is 0x00000 (V_{AINP} - V_{AINN} = 0V), the midscale value is 0x20000 (V_{AINP} - V_{AINN} = V_{REF}/2), and the most positive value is 0x3FFFF (V_{AINP} - V_{AINN} = V_{REF}).

In bipolar mode, if the FORMAT bit = 1, then the data format is offset binary. If the FORMAT bit = 0, then the data format is two's complement. In two's complement the negative full-scale value is 0x20000 (V_{AINP} - V_{AINN} = -V_{REF}), the midscale is 0x00000 (V_{AINP} - V_{AINN} = 0V), and the positive full scale is 0x1FFFF (V_{AINP} - V_{AINN} = V_{REF}). Any input exceeding the available input range is limited to the minimum or maximum data value.

Table 15. DATA Register (Read Only)

BIT	D17	D16	D15	D14	D13	D12	D11	D10
DEFAULT	0	0	0	0	0	0	0	0

BIT	D9	D8	D7	D6	D5	D4	D3	D2
DEFAULT	0	0	0	0	0	0	0	0

BIT	D1	D0	0	0	0	0	0	0
DEFAULT	0	0	0	0	0	0	0	0

Table 16a. Output Data Format for the Unipolar Input Range

INPUT VOLTAGE V_{AINP} - V_{AINN}	DIGITAL OUTPUT CODE FOR UNIPOLAR RANGE STRAIGHT BINARY FORMAT
$\geq V_{REF}$	0x3FFFF
$V_{REF} \times \left(1 - \frac{1}{2^{18}-1}\right)$	0x3FFFF
$\frac{V_{REF}}{2^{18}-1}$	0x00001
0	0x00000

Table 16b. Output Data Formats for the Bipolar Input Range

INPUT VOLTAGE V_{AINP} - V_{AINN}	DIGITAL OUTPUT CODE FOR BIPOLAR RANGES	
	OFFSET BINARY FORMAT	TWO'S COMPLEMENT FORMAT
$\geq V_{REF}$	0x3FFFF	0x1FFFF
$V_{REF} \times \left(1 - \frac{1}{2^{17}-1}\right)$	0x3FFFE	0x1FFFE
$\frac{V_{REF}}{2^{17}-1}$	0x2000	0x00001
0	0x20000	0x00000
$\frac{-V_{REF}}{2^{17}-1}$	0x1FFFF	0x3FFFF
$-V_{REF} \times \left(1 - \frac{1}{2^{17}-1}\right)$	0x00001	0x20001
$\leq -V_{REF}$	0x00000	0x20000

SOC: System Offset Calibration Register

The system offset calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB (most significant bit) first. This register holds the system offset calibration value. The format is always in two's complement binary format. A write to the system-calibration register is allowed. The value written remains valid until it is either rewritten or until an on-demand system-calibration operation is performed, which overwrites the user-supplied value.

The system offset calibration value is subtracted from each conversion result provided the NOSYSO bit in the CTRL3 register is set to 0. The system offset calibration value is subtracted from the conversion result after self-calibration but before system gain correction. The system offset calibration value is also applied prior to the 1x or 2x scale factor associated with bipolar and unipolar modes.

Table 17. SOC Register (Read/Write)

BIT	B23	B22	B21	B20	B19	B18	B17	B16
DEFAULT	0	0	0	0	0	0	0	0

BIT	B15	B14	B13	B12	B11	B10	B9	B8
DEFAULT	0	0	0	0	0	0	0	0

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0	0	0	0	0	0	0	0

SGC: System Gain Calibration Register

The system gain calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the system gain calibration value. The format is always in two's complement binary format. A write to the system-calibration register is allowed. The written value remains valid until it is either rewritten or until an on-demand system-calibration operation is performed, which overwrites the user-supplied value.

The system gain calibration value is used to scale the offset corrected conversion result, provided the NOSYSG bit in the CTRL3 register is set to 0. The system gain calibration value scales the offset-corrected result by up to 2x or corrects a gain error of approximately -50%. The amount of positive gain error that can be corrected is determined by modulator overload characteristics, which can be as much as +25%. The gain is corrected to within 2 LSB.

Table 18. SGC Register (Read/Write)

BIT	B23	B22	B21	B20	B19	B18	B17	B16
DEFAULT	0	0	0	0	0	0	0	0

BIT	B15	B14	B13	B12	B11	B10	B9	B8
DEFAULT	0	0	0	0	0	0	0	0

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0	0	0	0	0	0	0	0

SCOC: Self-Calibration Offset Register

The self-calibration offset register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the self-calibration offset value. The format is always in two's complement binary format. A write to the self-calibration offset register is allowed. The written value remains valid until it is either rewritten or until an on-demand self-calibration operation is performed, which overwrites the user-supplied value.

The self-calibration offset value is subtracted from each conversion result provided the NOSCO bit in the CTRL3 register is set to 0. The self-calibration offset value is subtracted from the conversion result before the self-calibration gain correction and before the system offset and gain correction. The self-calibration offset value is also applied prior to the 2x scale factor associated with unipolar mode.

Table 19. SCOC Register (Read/Write)

BIT	B23	B22	B21	B20	B19	B18	B17	B16
DEFAULT	0	0	0	0	0	0	0	0

BIT	B15	B14	B13	B12	B11	B10	B9	B8
DEFAULT	0	0	0	0	0	0	0	0

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0	0	0	0	0	0	0	0

SCGC: Self-Calibration Gain Register

The self-calibration gain register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the self-calibration gain calibration value. The format is always in two's complement binary format. A write to the self-calibration register is allowed. The written value remains valid until it is either rewritten or until an on-demand self-calibration operation is performed, which overwrites the user-supplied value. Any attempt to write to this register during an active calibration operation is ignored.

The self-calibration gain value is used to scale the self-calibration offset corrected conversion result before the system offset and gain calibration values have been applied, provided the NOSCG bit in the CTRL3 register is set to 0. The self-calibration gain value scales the self-calibration offset corrected conversion result by up to 2x or can correct a gain error of approximately -50%. The gain is corrected to within 2 LSB.

Table 20. SCGC Register (Read/Write)

BIT	B23	B22	B21	B20	B19	B18	B17	B16
DEFAULT	0	0	0	0	0	0	0	0

BIT	B15	B14	B13	B12	B11	B10	B9	B8
DEFAULT	0	0	0	0	0	0	0	0

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DEFAULT	0	0	0	0	0	0	0	0

Table 21. Data Rates for All Combinations of RATE[2:0] (LINEF = 0)

RATE[2:0]	SINGLE-CYCLE DATA RATE (sps)	CONTINUOUS DATA RATE (sps)
000	1	—
001	2.5	—
010	5	—
011	10	—
100	15	60
101	30	120
110	60	240
111	120	480

Table 22. Data Rates for All Combinations of RATE[2:0] (LINEF = 1)

RATE[2:0]	SINGLE-CYCLE DATA RATE (sps)	CONTINUOUS DATA RATE (sps)
000	0.833	—
001	2.08	—
010	4.17	—
011	8.33	—
100	12.5	50
101	25	100
110	50	200
111	100	400

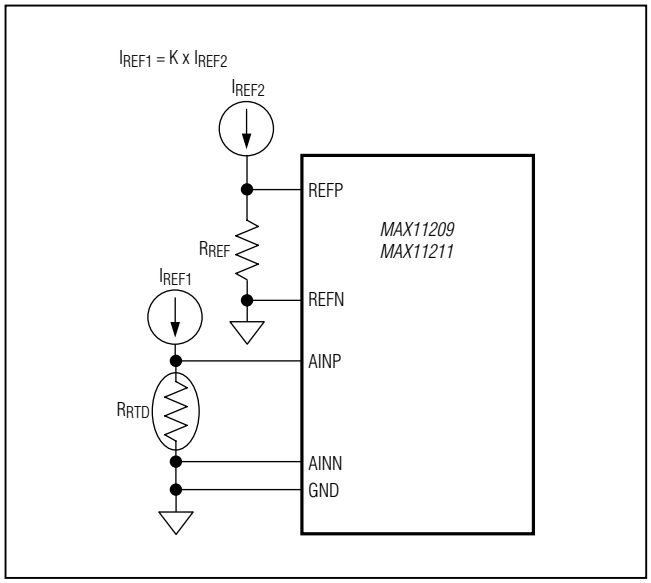


Figure 8. RTD Temperature Measurement Circuit

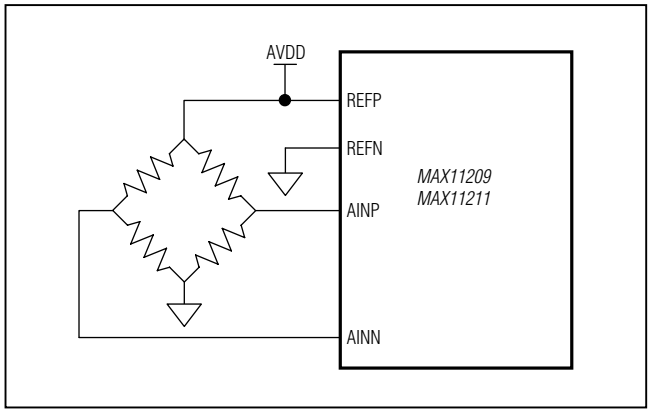


Figure 9. Resistive Bridge Measurement Circuit

Applications Information

See Figure 8 for the RTD temperature measurement circuit and Figure 9 for a resistive bridge measurement circuit.

Adding more active circuitry to the analog input signal path is not always the best solution to a small-signal problem. Sometimes, increasing the dynamic range of an active device can lead to a simpler solution that also helps power consumption and linearity.

Often, circuit designers immediately look for an external op amp or programmable gain amplifier (PGA) when confronted with coupling low-amplitude signals to sampled digital systems. In many cases, choosing an ADC with more dynamic range and better low-noise performance yields a solution that works better, simpler, and with less power.

One such example is measurements from a strain gauge in a Wheatstone bridge configuration. Assuming a differential output signal from the bridge in Figure 10, the bridge's output voltage varies from 5mV to 105mV, while the noise of the bridge itself limits the sensitivity to approximately 1µV. This gives approximately 100,000 discrete levels that are available for quantization, a feat accomplished quite well with any ADC having 17 bits or more of usable resolution. However, as it is not likely that a 19-bit ADC will have an input range of 105mV, a gain stage is needed to boost the signal to span the input range of the ADC (typically between 3V and 5V).

This solution requires finding an amplifier and associated passives that meet the overall system noise and linearity needs. Also, the power consumed in the gain stage may equal or surpass that of the ADC itself, a fact that is significant in systems where power consumption is severely constrained, such as portable sensors or 4–20mA loops.

The low-noise floor of the MAX11209 family of 16-/18-/20-bit devices gives the designer the ability to use simple binary shifting (digital gain) of the data word to align the sample range with the available code space. Digital gain is internally available in the MAX11209.

18-Bit, Single-Channel, Ultra-Low-Power, Delta-Sigma ADCs with Programmable Gain and GPIO

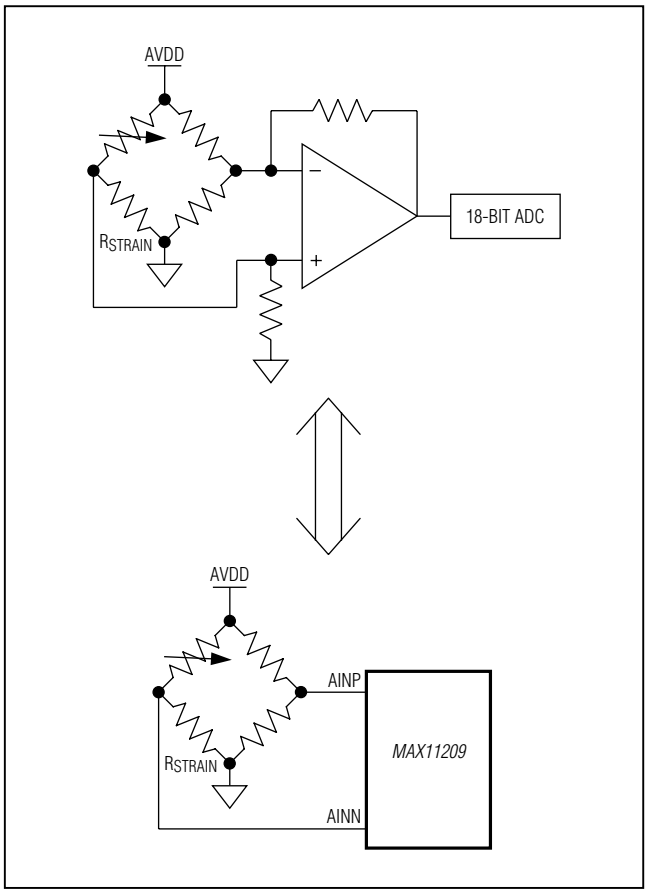


Figure 10. The MAX11209 ADC Eliminates an External Gain Stage.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/10	Initial release	—

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